Establishing Effective Accelerated Testing Conditions and Criteria for Confirming Reliability for High Density Interconnect Circuits

Bill Birch
PWB Interconnect Solutions Inc.

Abstract
The electronics industry applies a single criterion/standard for determining the acceptance and rejection of traditional and high density interconnect (HDI) structures during accelerated reliability testing. The criterion specifies that if a plated feature (plated through hole, microvia, etc.) exceeds a 10% increase in resistance, it is deemed failed. In practice, the determination of the effective resistance increase is an important factor for evaluating the risks associated with various failure modes that demonstrate a wear-out or fatigue driven failure condition. In situations where a failure is related to an interfacial interconnect (e.g.: microvia to target pad), the magnitude of localized resistance change must overwhelm the bulk resistance on the "non-failing" circuits to be considered failed. This paper will demonstrate why different electrical acceptance and rejection criteria must be applied to these failures, based on a direct relationship to their electrical sensitivity to change. Test vehicle design, measurement accuracy, testing protocols, methodologies and isolation of defect location will be discussed to understand how each individual situation is pertinent for establishing confidence in HDI electronics reliability.

Introduction
The concerns related to both maintaining and applying the existing reliability performance standard are the increased risk that defective products can be deemed acceptable because the test vehicle did not reach the traditional rejection criteria, resulting in false positive results. Obviously, this situation must be corrected to prevent any implantable devices (life critical) or high reliability products from failing in their end use environment. To achieve this goal, it is necessary to consider all aspects of the reliability testing methodology and make the appropriate changes based on present and future interconnect technology being designed into HDI products. Test vehicle designs must represent all aspects of the product's interconnect structures and be configured intelligently to achieve optimum electrical sensitivity. Continuous resistance monitoring is a critical requirement that must utilize state of the art measurement and data collect systems that are designed in parallel with temperature cycling, that fully represent the combinations of stresses associated to product assembly, possible rework and the anticipated life cycle of the end use environment.

The key factors that must be in place to establish an effective test methodology for reliability assessment of HDI electronics require the combination of intelligent design, measurement accuracy/speed of data transfer, sufficient thermal energy to detect or precipitate latent defects and determination of the rejection criteria that correlates between a measured electrical activity and an unacceptable level of physical change. This strategy can be enhanced if further consideration is given to the quantification of material degradation in combination with interconnect structure reliability. Electronics are now required to comply with the restriction of hazardous substances (RoHS) initiatives, which require lead free finishes and potentially halogen free materials. It is now necessary to quantify that both the structures and materials used to construct the printed wiring board (PWB) are sufficiently robust enough to withstand the multiple exposures to elevated assembly and possible rework thermal excursions.

The measurement of resistance change in the plated connections and the capacitance change between individual dielectric layers must be combined to achieve an effective methodology for identifying interconnect failures and material degradation/damage. This logic must be applied throughout the test vehicle design phase, test equipment design and establishment of the testing protocols; if completed correctly it will deliver a broader understanding of total product reliability.

History of accelerated reliability testing methodology and acceptance criteria
All segments of the electronics industry presently apply an interconnect reliability acceptance and rejection standard that dates back to the early 1960's. The industry standard organizations (IPC, Mil Std, Telecordia, etc.) adopted a single 10% resistance increase rejection criterion to be applied to all accelerated reliability testing, specifically thermal cycling where continuous resistance monitoring was utilized. The basis for setting the original criteria at this level was a compromise between identifying a level of electrical degradation that confirmed irreversible change (structural damage) and the level of damage accumulation that could be easily confirmed when completing conventional failure analysis. The consortiums activities took several years to complete multiple studies on thermal oven cycling using only plated through hole (PTH) structures. A correlation was confirmed between electrical degradation and identified physical damage; the standard was premised on fatigue as the only failure mode that generated circumferential cracking within the copper plating located around the central zone of a PTH barrel.

The industry standards organizations have not revisited this specification since its release. The same criteria is applied to today's interconnect structures despite the reality that products containing HDI devices have driven via structure types, feature sizes, geometries, sequential interconnections and methods of formation to a level which was not anticipated when the standard was established. An example would be an implantable defibrillator which is commonly constructed with multiple layers of thin polyimide based (Kapton or equivalent) materials, sub-laminated incrementally from a central core, with multiple levels of ablated microvia structures; PTH structures are generally not included. The traditional failure mode of barrel cracking has been superseded by interfacial separations as the dominant HDI failure mechanism. The question to be answered is; should the industry continue to apply the existing standard which has negligible relevance to the anticipated product design rules and the anticipated failure modes associated to the products interconnect technology? This paper is intended to offer an alternative perspective and standard for confirming the reliability of HDI structures in electronics.

The documented 10% criteria does not specify the test vehicle design, the via type, or number of via structures. The specification does not consider whether the resistance change is localized or globally generated. In many cases it is not even required to expose the test vehicle to multiple assembly level temperature excursions prior to accelerated reliability testing.

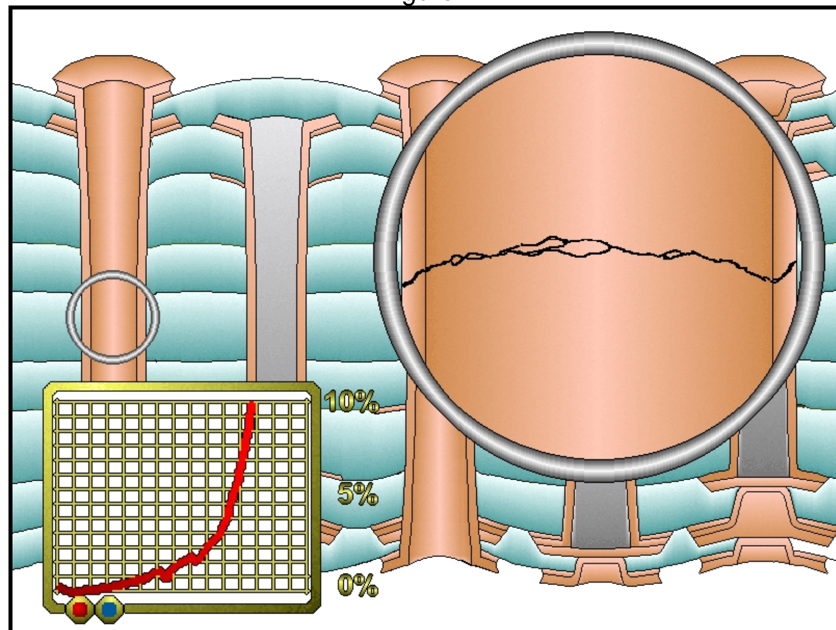
Physics of Interconnect Failure
High temperature thermal excursions experienced during the product's exposure to product assembly/rework and low-level thermal gradients in the end use environment apply either high or low levels of stress to the interconnect structures and materials. The magnitude of strain created by thermal gradients is determined by whether the temperatures experienced in the product are above or below the materials glass transition temperature (Tg). The Tg is a phase change where the material transitions from a rigid to plastic state. Tg is usually measured to be between 150^0C and 180^0C for epoxy/phenolic (FR4) based materials and between 200^0C and 260^0C for polyimide materials. Thermal analysis of the constructed materials measures for both the Tg and the coefficient of thermal expansion (CTE). The CTE is the overall change in thickness of the dielectric composite. The CTE of dielectric materials used in PWB products are measured in parts per million per degree centigrade (ppm/C). Below and above Tg the rate of CTE in the z axis increases by a factor of approximately 5x to 10x. The rate of change is dependent on the properties of the resin system and the glass to resin ratio. A typical z axis CTE value for a multilayer PWB is between 30 to 50 ppm/C below Tg, this increases to 250 to 400 ppm/C above Tg.

The most common failure mode for a PTH is barrel cracking of the plated copper, usually within the central zone, or at the knee/corner. The second most common failure mode is a separation between the barrel and the internal copper interconnections, usually at the outermost inner-layer connections, where the rotational stress (bending moment) is generated. In microvia structures the dominant failure mode is a separation between the base of the ablated via and its attachment to the underlying target pad. In the case of the PTH, copper plating quality/thickness are dominant influences. For microvia structures, the strength of adhesive bond between different layers/types of copper ultimately determines interconnect reliability.

When the product experiences assembly/rework temperatures, usually for one to four minutes (per assembly cycle) above Tg, the amount of stress exerted on the interconnect structures and materials is significant. The resulting strain creates physical distortions in the material which the plated structures must withstand. The stress applied to a PTH barrel is very different to the stress applied to a microvia. The stress applied to a PTH barrel is created by a combination of x, y and z axis stresses. The z axis CTE of the material forces the barrel into expansion; the x, y stress is primarily directed toward the centre of construction. The copper plating in the central zone is forced inwards causing the copper crystals to withstand a flexural movement. The ability of the copper plating to withstand this movement is determined by the quality, thickness and uniformity of the copper plating. The quality of the copper plating requires regular measurement to confirm the ductility and tensile strength. The strain created during each thermal excursion are caused by the inherent expansion characteristics of the resin system, but the strain is applied or transferred to the PTH structure through the resin impregnated glass fabric. Most PTH barrel cracks are found within the centre zone of the barrels, they are initiated and propagated at the location of a glass bundles around the sidewall of the drilled hole. Once the crack has initiated, any additional cyclic exposure will cause the crack to work around or through the copper crystals, forming micro-cracks. This is considered the point of irreversible change, from an electrical perspective. Continued thermal cycling increases the crack propagation and damage accumulation causing the micro-cracks to coalesce into semi-cylindrical cracks around the cylindrical structures. As the crack formation advances the damage accumulation accelerates, causing the structures to become electrically unstable and intermittent activity is experienced.

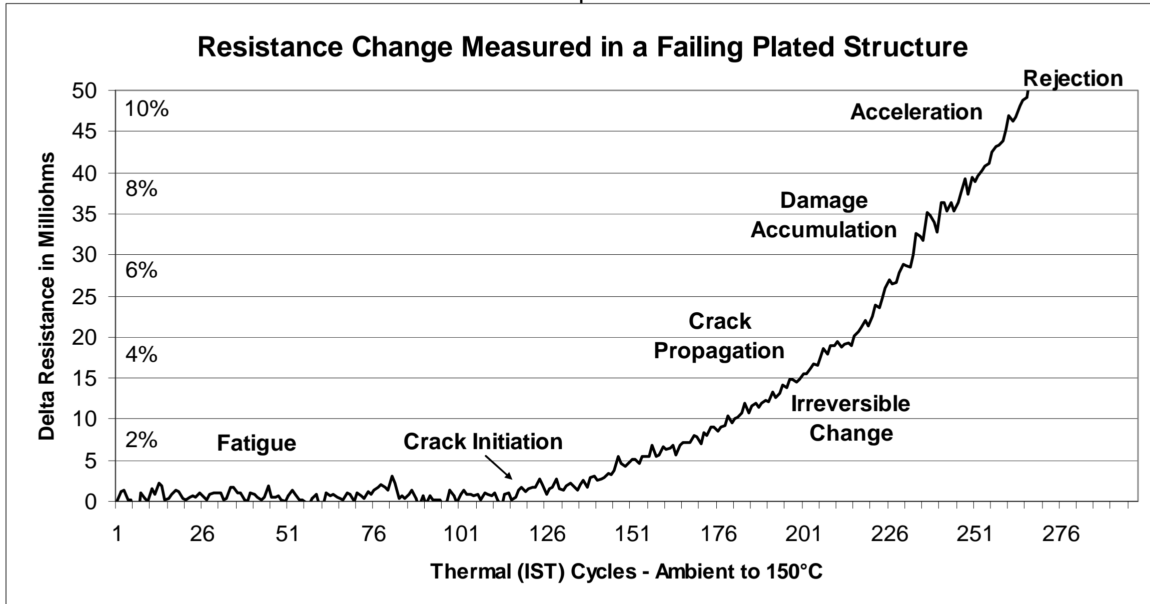
Figure 1 contains an animation that represents the progressive crack propagation described above relative to the measured resistance degradation. The traditional requirement to reach a 10% resistance increase was based on the need find a completely cylindrical barrel crack.

Figure 1



Graph 1 illustrates the measured electrical activity of a failing PTH structure. The top of the y axis denotes a bulk resistance increase of 10%. The present standard determines that this magnitude of change is required before a confirmation of failure can be established. This is despite the fact that failure initiated half way through the thermal cycling test and the test vehicles' continued to be exposed to these unnecessary additional cycles. This situation will create collateral damage that can make root cause analysis more difficult to confirm.

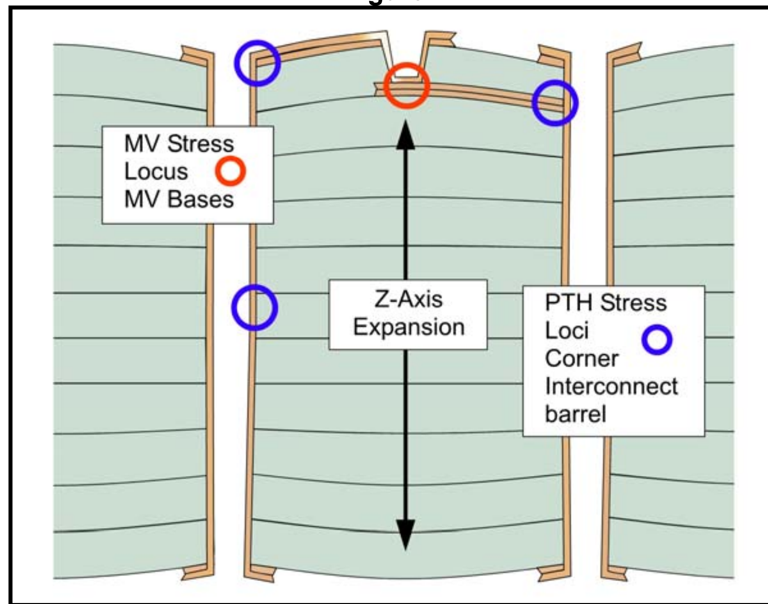
Graph 1



Laser ablated microvias are a standard form of interconnection used in HDI products. Their use is generally combined with traditional structures (PTH, buried via or blind via), although they can also be the only means of interconnection designed into the product, especially dense flexible substrates. Strain distribution and failure modes for microvia structures are very different compared to a PTH, however, the same methodology and criteria is used to determine acceptance.

Because the microvia dielectrics are very thin (0.05mm/.002" to 0.15mm/.006"), the amount of thermal stress applied to the microvia structure is relatively low, compared to the barrel of a PTH. Figure 2 illustrates the most common location where strain is applied to products that combines PTH and microvia structures. Assuming that the PWB is processed correctly, the hierarchy of influence for strain distributions and the associated fatigue should precipitate wear-out failures in a predictable order. Firstly, the central zone of the PTH barrel, followed by corner/knee cracking, copper foil in the internal interconnects and lastly, the microvia structure. It is only when the microvia formation compromises uniform copper plating into the via, or when an adhesive bond is not achieved that the hierarchy of influenced is reversed.

Figure 2

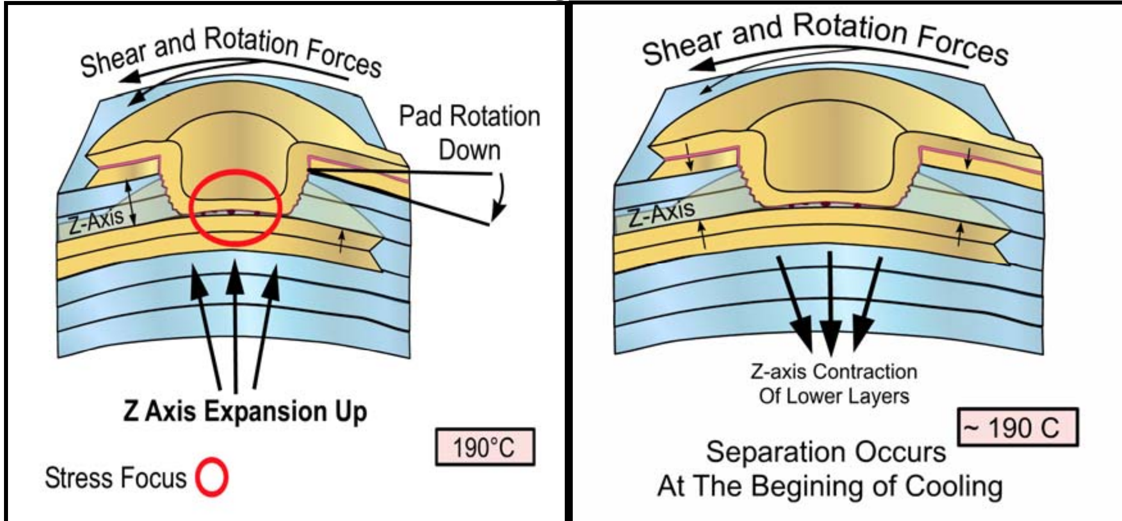


The CTE of the dielectric around the microvia is generally the same or higher than the CTE of the dielectric below the microvia structure, assuming the same material types are used. Because there is increased resin content in the dielectric surrounding the microvia there is a higher amount of strain created at the location of the attachment between the microvia and target pad. The main cause of strain on the microvia during thermal excursions is from the Z-axis expansion of the dielectric between the top of the microvia (outer layer) and the target pad. The amount of stress on the structure is a function of dielectric thickness, surface area, shear forces and the visco-elastic properties of the dielectric material.

In many typical HDI board constructions microvia structures are frequently found only on the outer layers of the board, although this situation is changing rapidly to multilevel structures. For single level microvias, the surface layers are not inhibited and move in unison with the z axis expansion, creating a bending moment, literally moving freely without constraint. Figure 3 illustrates the localized stress/strain characteristics of a microvia in both the heating and cooling phase.

During product heating the z axis expansion enables the target pad to move with the microvia structure making intimate contact with the base. This situation explains why microvia failures do not generally occur during a heating (or ambient) phase. It is immediately when the cooling phase begins that the material below the microvia contracts (very briefly) away from the base, this is where many electrical intermittent (unstable) measurements in microvia structures are found.

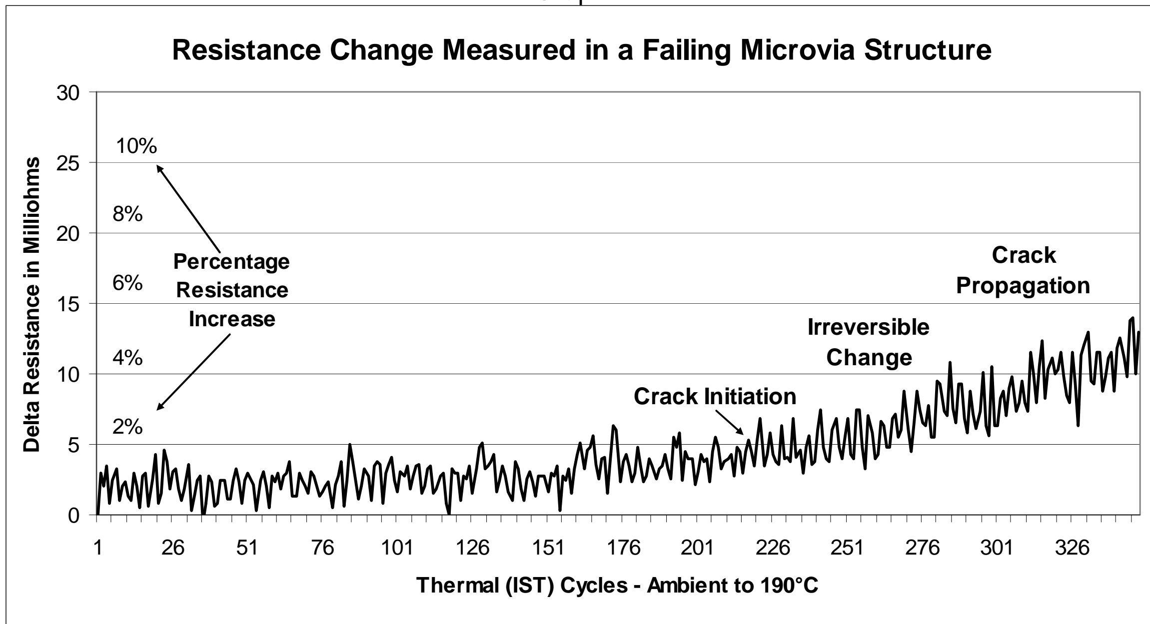
Figure 3



The ability to measure or "watch" a microvia failing is only possible if the correct test vehicle design conditions and measurement capability are put into place, Graph 2 demonstrates the measured resistance change associated to a failing microvia structure that is exhibiting fatigue as the expected failure mode. The rate of change (electrical degradation) is much slower compared to the PTH barrel. This should be expected based on the relative small physical geometries and electrical sensitivity involved with the contact area at the base of a microvia.

Graph 2 shows the coupon's resistance only reached a 4% increase at the end of test; if additional cycles were completed, the trend would be further small increases until an immediate high resistance (spike) value was measured. This high resistance change signifies the point where the failing microvia fully separated from the target pad, effectively long after damage initiation had occurred. The important element of any reliability test is the ability to understand why a test vehicle failed to meet the criterion. In the example shown in graph 2, physical damage will be present at the level of 4% resistance increase.

Graph 2



If failure analysis is completed at the point of 4% change effective root cause analysis is not only possible but more likely to explain the cause and effect of the failure mechanism. Photo 1 shows the "beginning" of a microvia to target pad separation which was stopped at a 4% bulk resistance increase; fatigue cracks are visibly migrating from the outer edges and propagating cylindrically toward the centre. A projected resistance degradation scale has been added to the image to illustrate the ability to relate resistance change with physical damage. This capability is only possible in failure modes that exhibit a fatigue type wear out, assuming an electrically sensitive test vehicle design is being measured. Further thermal cycling would result in additional separation, but this would only inhibit the ability to diagnose the nature of the failure mechanism.

Photo1

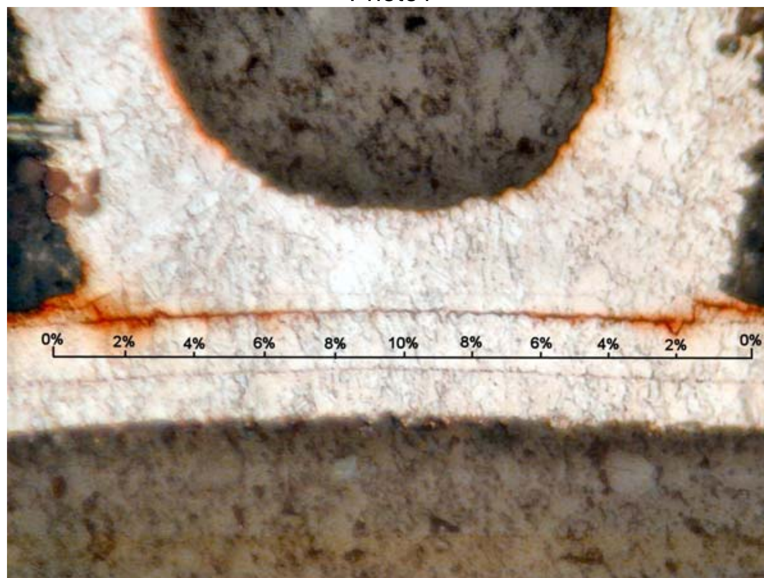
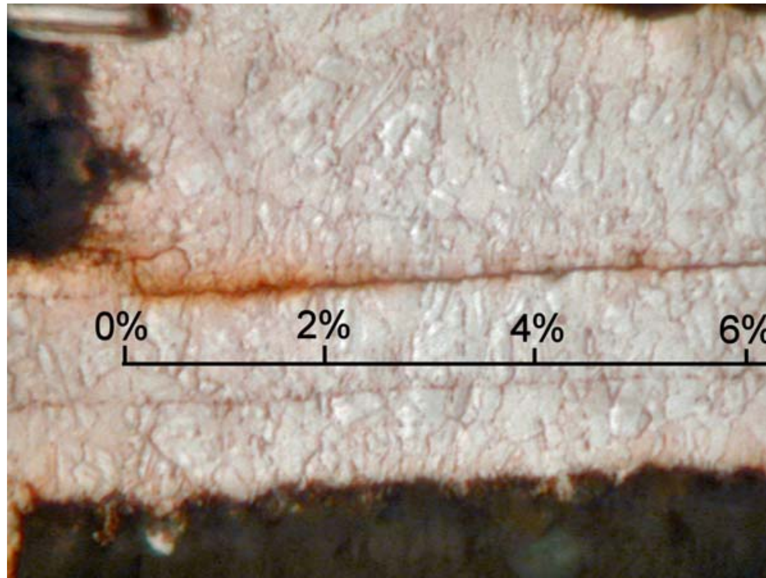


Photo 2 depicts a higher magnification image in the area of failure initiation; it is now possible to distinguish between the various levels of electroless and electrolytic coppers to better determine which specific demarcation line is demonstrating low adhesion. In the case below the copper flash did not chemically bond to the underlying plated target pad, this information enables the PWB manufacturer to greatly narrow down the possible causes in the processing through the metallization chemistry to identify the root cause responsible for the problem.

Photo 2



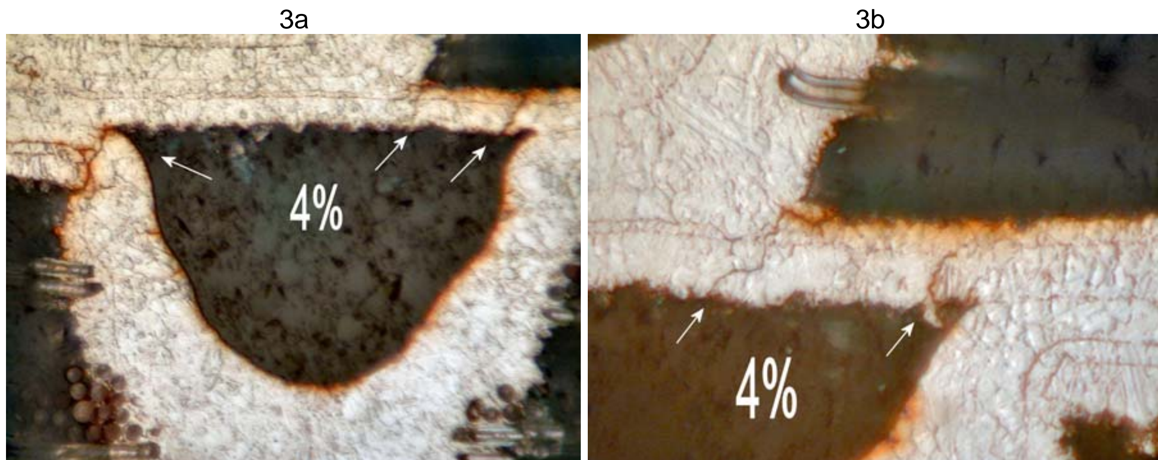
The decreasing density of HDI devices is causing designers to adopt multi-levelled microvia structures to facilitate the necessary increased routing between components. Design rules are applied that either stack or stagger the levels of microvias from the surface to a sub-laminated location. Each level requires the PWB manufacturer to process the substrate again through virtually the entire production process. Each production cycle compounds the need to understand interconnect reliability, with the added consideration that materials are now experiencing multiple exposures to high temperature curing and pressure cycles for each distribution layer lamination. The condition at the microvia to target pad interface are now different. Laser ablation and metallization are required to deal with an electrolytic plated target pad instead of copper foil, which is generally the case with single lamination microvia structures. The sub-level plated surfaces are commonly "planerized" to remove excess surface copper, to enable the PWB manufacturer to print and etch the line and space geometries in the design. This critical process step has demonstrated the ability to cause latent defects in situations where inadequate controls caused insufficient copper thickness to remain above or below a microvia. Reliability testing has confirmed that with each added level of microvias introduced into the product design it not only increases the level of total strain, but it also increases the risk that one of the critical processing steps was not adequately controlled, which can result in poor interconnect reliability.

There are two standard methodologies for filling microvias: a) Copper filled, sometimes called "plated shut". b) Resins filled and capped. Both are perfectly viable options if processed correctly, but each have inherent failure modes. In the case of copper filled the via plug is virtually unbreakable, making the interfacial adhesion to the target pad the dominant failure mode. The secondary failure mode is commonly called "pull out" it is caused by cracking of the foil in the target pad, or the plated cap on an underlying buried via. The third failure mode found is circumferential cracking around the corner/knee of the surface pad; this is generally found if aggressive removal of surface coppers is involved. This condition can also be influences by the presence of high resin content bonding layers

Resin filled and capped microvias inherit the same interfacial adhesion issues as copper filled, but also experience fatigue in the copper plated sidewalls and junctions between the different levels. Photo's 3a through 3d are low and high magnification images of the same product where microvia testing stopped at a 4% increase in bulk resistance. Fatigue cracks are clearly evident, crack propagation is virtually circumferential. Photo 3a confirms that the PWB manufacturer employed different laser ablation techniques and plating conditions between the upper and lower level microvias, fatigue cracks were only found at the junction between the two microvias. The ability to examine the structures at this early phase of damage accumulation permits effective analysis without concern for collateral damage adding confusion to the diagnosis.

3a 3b

3a 3b



The situation for understanding microvia reliability and especially the capability to precipitate latent defects to a point of failure is both justified and further complicated by the reality that a device is commonly located on, or adjacent to the surface pad that contains an underlying microvia structure. This design option introduces the possibility of an additional CTE movement (mismatch) between materials used to construct and connect the device and those used to construct the substrate. The substrate and device interconnection is formed with a solder joint; the resulting strain will focussed toward the weakest area of the structure. This is directed firstly to the surface pad and then downward toward the base of the microvia. The resulting movements generate a mechanical (bending moment) stress onto the pad; many electronic companies are experiencing a problem called pad cratering, which compromises the dielectric material directly under the surface pad.

It is logical to expect that the stresses involved could easily accelerate damage into the critical adhesive bond between microvia and target pad. The combination of thermal and mechanical strain requires a strong adhesive bond to be assured that it is capable of withstanding the short and long term exposures to thermal gradients. In this paper we will limit the discussions to thermal stress/strain.

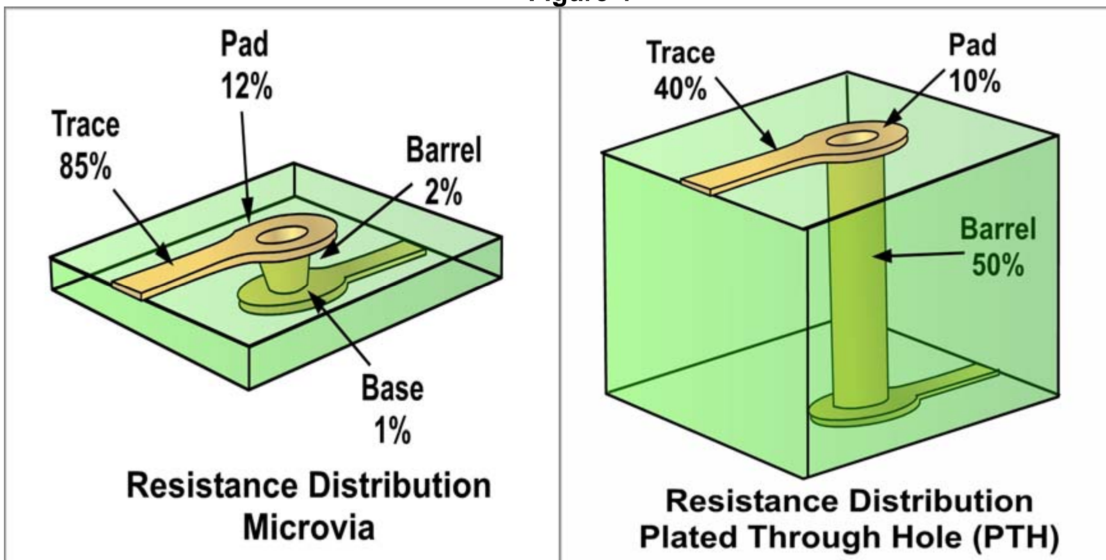
Intelligent Test Vehicle Design

The combination of intelligent test vehicle design, test system design and applied methodology become the critical relationship that establishes the ability to successfully detect a "hard to find" failure mode. Most reliability engineers understand the reality that during electrical measurement the sensitivity of the critical areas of interest are small fractions of the test circuit's bulk resistance. This situation is dramatically amplified when testing microvias, due to the smaller geometries involved and the nature of the interfacial failure mode. The major responsibility of any microvia reliability effort is the ability to create specifically designed test vehicles containing interconnect structures that are electrically sensitive enough to measure low-level increases/changes in resistance that occur after damage is initiated.

Before starting the coupon design it is important to understand why it's configuration is so critical to the testing methodology and criterion. The acceptance and rejection standards contain a single criterion for reliability testing, "any product under test that exceeds a 10% increase in resistance is deemed failed".

Refer to Figure 4 for an illustration of how the resistance distribution changes between a microvia and PTH structure. Understanding these realities is crucial to good test vehicle design. Consider a situation where PTH barrel/via fatigue is responsible for the coupon's failure; this would require that the PTH effectively increases the test circuit's bulk resistance by only 20% (10% change divided by the barrel's ratio of 50%). This situation changes dramatically when the microvia is tested; to achieve the same 10% increase, the microvia would need to increase it's bulk resistance by between 500% to 1000% (10% change divided by the barrels ratio of 2%, or the critical microvia to target pad interface ratio of 1%).

Figure 4



To better understand the resistance distribution of various microvia configurations see table 1 for a 0.15mm (.006") ablated via and table 2 for a 0.1mm (.004") ablated via. Each table compares the relationship of barrel, trace and pad and identifies the effective resistance increase required to reach the existing specified (10%) rejection criteria.

The premise for all calculated resistance distribution is as follows:

a) The surface copper foil = 17 micron (1/2oz or .00065"), which was subsequently copper plated to a total thickness of 45 microns (.0018").
b) The target pad = 17 micron (1/2oz or .00065") copper foil.
c) The pad diameters = 0.3mm (.012").
d) The trace widths = 0.3mm (.012").
e) The via to via spacing (grid) = 0.8mm (.032")
f) The dielectric distances between the microvia layers = 0.075mm (.003").
g) Total board (10 layer) construction = 1.0mm (.040")
h) The microvias are copper filled

Table 1
Ablated diameter = 0.15mm (.006")

Microvia Structure	% Via Ratio	% Trace Ratio	% Pad Ratio	Effective Increase
Single	2	86	12	500%
2 Stack	5	84	11	200%
3 Stack	7	82	11	143%
4 Stack	9	80	11	111%
4 + 4 Stack	36	51	13	28%

Table 2
Ablated diameter = 0.1mm (.004")

Microvia Structure	% Via Ratio	% Trace Ratio	% Pad Ratio	Effective Increase
Single	4	85	11	250%
2 Stack	9	81	10	111%
3 Stack	13	77	10	77%
4 Stack	17	74	9	59%
4 + 4 Stack	54	38	9	19%

Note 1: The resistance at the microvia and target pad are usually calculated at less than 1%
Note 2: Both 4 + 4 stack configurations are continuous connections between layer 1 and layer 10 (4 stack on either side of a filled/capped buried via)

The conclusion from table 1 and 2 dramatically brings into question the logic of applying a common rejection criterion for different types and levels of interconnections. This situation is further confounded when minimal consideration is put into the test vehicle design, which could results in a microvia that equates to an insignificant factor in the test circuit's bulk resistance.

The second component of how the resistance distribution impacts the test methodology is the ability to measure low-level change associated to structural damage. As the ratio of microvia and critical interface resistance reduces relative to the tracks and pads, it becomes more difficult to determine the critical points of failure initiation and damage accumulation.

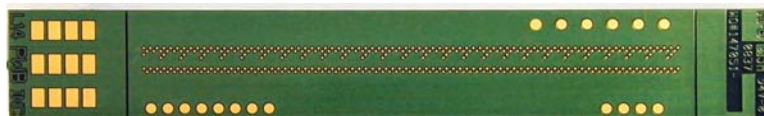
Microvia test circuit designs would ideally employ a combination of mathematical and thermal modeling, in combination with prior experience in the fields of PWB processing, chemistry, materials and statistics. The collaboration of skill sets would permit an ability to engineer a coupon that duplicates the product attributes and geometries with strong consideration given to the processing techniques and controls necessary to achieve a reliable interconnection. The intelligent coupon configuration would require a consultation with the OEM designer and the PWB manufacturer. Negotiations would take place to reach an agreement on coupon size that can be located adjacent to the product on the perimeter of the production panel. The coupon must be large enough to contain a statistically significant number of each critical interconnect structure..

At no time should the PWB manufacturing process be compromised by the introduction of the coupon, it should be "invisible" during the processing of the actual product. The coupons would generally have at least two types of circuits; a) A resistance monitoring circuit, used to heat/measure the critical surface and internal interconnections, for each structure of interest and b) A capacitance test circuit used to measure changes in dielectric properties during or after exposure to assembly/rework temperatures. See photo 4 for microvia coupon design with PTH

Microvia / Buried Via IST Coupon
Photo 4

For increasing numbers of HDI products the test vehicle would not contain drilled holes; this is due to the fact that increasing numbers of products (primarily implantable and hand held devices) are designed with surface mount only components. The two or three test circuits in each coupon design would commonly include structures with the highest combination of vias stacked or staggered with each other, the smallest ablated diameter, vias ablated onto buried vias, and/or (in 4simpler product designs) microvias ablated from the outer layers. See photo 4 for microvia coupon design with SMT connectors For statistical purposes and if enough real estate is available/permitted, each test circuit should contain approximately 300 (or more) microvias; this is necessary because the product panel will contain many thousands of microvias.

Microvia Only (Surface Mount) IST Coupon
Photo 5



Additional features are designed into the coupons which deliver critical information related to certain PWB processing steps. Each circuit is configured to measure whether controls are in place that can compromise microvia reliability, if not controlled correctly. The data collected from these test circuits enables the PWB manufacturer, and their customer, a confirmation of the capability and consistency of their ability to build predictable products. Their inclusions are designed to compliment the reliability testing by focusing increased attention toward critical process steps or material conditions. In addition, the material integrity test circuits make it possible to collect performance impacting measurements before, during and after exposure to the critical thermal stresses associated with component assembly and rework.

The reliability portion of the coupon includes the customer's product design rules, which establishes the products construction and critical structure geometries. These rules are followed to enable a representative assessment of the interconnects reliability. To understand the influence of material change it is necessary to enhance/modify some of the coupon design rules, or introduce a second coupon that has specific functions as follows: a) be able to determine important information related to how the product is constructed, b) measure whether the materials are changing after exposure to the assembly or rework environments, c) give a non-destructive capability to confirm product construction (panel by panel, lot by lot). d) measure how the heat is being distributed throughout the product construction. Each individual test circuit is configured to achieve the highest level of sensitivity for measuring the changes that signify if the PWB manufacturers have the ability to control their process and have the added function of measuring fatigue or failure to the interconnect structures. When required, the coupon is also configured to measure for material degradation (delamination), moisture removal, Tg, Dk (Dielectric constant), dielectric thickness and temperature distribution (both across the surface and from the surface to the centre of the construction). Additional information is available from the authors that details each of the test circuits associated to an HDI coupon design.

Test Methodology

There are two standard methods for completing accelerated reliability testing to determine PWB substrate reliability; they are traditional thermal ovens and Interconnect Stress Testing (IST). Microvia testing is increasingly using the IST methodology, in some cases using modified methodologies. The documentation can be found in the IPC Test Methods Manual TM650, Method 2.6.26, titled DC Current Induced Thermal Cycle Test. IST is not a thermal chamber; it heats each coupon individually by passing an electrical current (unique to each coupon) through a specifically designed heating circuit. The heating circuit is commonly located on the surface layers, or one layer into the construction. This duplicates the same thermal characteristics of how heat is applied during assembly, and from the device that is conducted into the surface of substrate, which subsequently penetrates into the product construction. Forced air cooling is applied; this closely simulates how electronic assemblies are thermal cycled in their end use environments.

The primary change, when applying Method 2.6.26, for microvias, modifies the reliability testing test temperature from the 150°C default by raising the upper temperature level to 190°C for epoxy/phenolic materials and 210°C for polyimide materials. The temperature increase is necessary to enunciate microvia failures without producing artefacts or artificial failure modes. Testing in thermal ovens that operate at lower default temperatures of 125°C to 160°C can not effectively or accurately find microvia failures within 1000 cycles (40+ days of testing) on coupons associated with printed circuit boards that experienced a 30% fall-out rate in surface mount assembly (Andrews, Parry, Reid 2005). Testing has also confirmed that well fabricated (robust) single level microvias do not fail for thousands of cycles, when tested to the temperature of 190°C.

Two of the unique advantages of IST technology are the ability to complete high speed continuous resistance monitoring during the thermal cycle for each test circuit, and secondly, stress testing can be stopped individually and immediately on each coupon precisely at the specified increase in bulk resistance, for any required test circuit. This capability is not possible with a thermal oven unless an operator intervenes and removes the test vehicle from the chamber. A typical protocol for oven testing requires the operator to measure all test circuits at specific intervals, the coupons are removed from the oven and measured at ambient. Failures in microvia are elastic by nature which causes them to be electrically stable when measured in an ambient state. As stated previously, the measured increase in resistance has a direct relationship to the level of damage accumulated within the specific test circuit. At a level of 10% change, cracks or separations are fully established, but have not fully progressed to a point of an open circuit or intermittent high resistance. The capability to halt testing and prevent further damage accumulation allows failure analysis to be completed before the failure site is compromised, as happens with thermal ovens where the testing continues beyond a low level of resistance change.

When a test system is configured it is important to anticipate the timings involved between two incremental measurements of an individual test circuit; this is commonly referred to as the loop time. In traditional thermal cycle testing, the large capacity of the oven permits a high quantity of test vehicles to be situated and monitored simultaneously. The number of circuits that can be included is based on the cabling and number of input channels available in the measurement hardware. In the IST systems, the number of heads is limited to eight, with each test head capable of measuring three test circuits per coupon. The maximum total of twenty four measurements permits incremental measurements to be completed in approximately four seconds. This rapid loop time is necessary to avoid the possibility of missing an intermittent measurement. Many conventional thermal oven configurations are capable of completing each individual measurement in approximately one second, this equates to an extended loop time and excessive delay between incremental measurements when multiple test circuits are involved. When testing PTH structures the extended loop time will not impact the ability to measure resistance degradation caused by copper fatigue, but when the failure mode of interfacial separations in microvias are considered, the lengthy delay between measurements can easily miss an event.

The configured hardware and software are multiplexed at extremely high speeds to enable a series of individual real time measurements to be collected. The data is immediately compared to a series of internal references which includes the relative rejection criteria. In real time, the data is captured onto the hard drive, collated into graphical format and displayed to the operator. State of the art measurement systems permit multiple measurements to be taken simultaneously; the data completes an immediate averaging function to determine if a stable reading is established. Microvia failures are intermittent by nature therefore the software must be intelligent enough to distinguish between measurement noise and a resistance change consistent with a microvia to target pad separation.

Measuring low-level resistance change in the IST test system requires proprietary noise cancelling hardware and software algorithms. The test circuit's bulk resistance must be sufficiently high enough that the total measurement error can only equate to 10% of the rejection criteria. The measurement error is the combination of influences from all aspects of the configured test system, which includes accuracy, precision, stability, repeatability and reproducibility. In the case of IST test equipment, onboard calibration and diagnostic systems quantify and minimize the effects of measurement variation to the location where the test coupon is installed onto the tester. In addition, local environmental changes in temperature are continually monitored; changes outside of an acceptable range receive compensation to the systems temperature calculation algorithms.

A test coupon measuring a bulk resistance of 200 millions, using a 10% rejection criterion (20 milliohms) requires a maximum measurement error of 2 milliohms. A change in temperature of +/- 1°C is capable of exceeding the maximum allowable measurement error. If the rejection criterion was further reduced to the level of 4% this would equate to a maximum measurement error of 0.8 milliohms. Test equipment specifications are commonly +/- 1 milliohm, but this does not consider all of the peripheries and cabling associated with traditional reliability testing.

The test system establishes coupon specific resistance profiles that become an effective reference for all subsequent measurements. This permits the ability to quantify relative resistance changes throughout the entire thermal excursion (heating and cooling). This capability is very important when testing microvia structures because interfacial separations do not commonly occur during the heating phase of testing due to z-axis expansion that "forces" the target pad into intimate contact with the base of the plated via. It is necessary to complete rapid measurement at the onset of cooling phase to detect the electrical instability associated with via to pad separations.

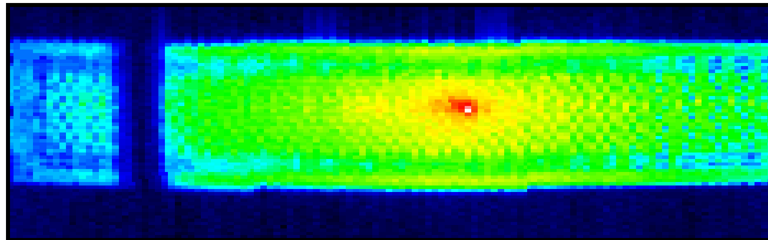
In most thermal cycling test methods the test circuit is measured passively, meaning the environmental temperature raised and lowered in a chamber and the coupon's test circuit follows this environment. An additional feature unique to IST test equipment is the ability to stress the test circuit by passing electrical current through the structure of interest; this permits the ability to uncover electrical instability very rapidly. If a low-level constant current is passed through the site of electrical instability, the local resistance will be higher which results in localized increases in voltage. The slightly higher voltage raises the immediate temperature, creating an avalanching effect of damage accumulation. The minor changes in resistance continue until the coupon exceeds the specified rejection criterion. A shunt resistor is installed into the test circuit to divert the passing of current through a high resistance situation, which could lead to excessive heating of the failing microvia. The principle of this direct heating methodology is that microvias structures or interconnections should not electrically degrade. Historical testing has demonstrated that robust microvias can withstand extended exposures to cyclic current applications without electrical degradation.

The importance of measurement repeatability and reproducibility can not be understated, especially when measuring the reliability of HDI structures used in implantable devices, monitoring systems, or any equipment where human life can be put at risk if failure should occur.

Identifying Failed Microvia Location

Stressing of the microvia structure that result in a catastrophic failure (open) is relatively easy to find using conventional electrical continuity meters. When IST testing is stopped at the level of 4% resistance increase, the failing microvia is still electrically conductive, due to the low-level of damage accumulated. Using thermo-graphic techniques it is possible to identify the exact microvia that contributes the highest resistance within the test circuit. Since the failed circuit has experienced only a 4% increase in resistance, a low level DC current can be applied, permitting the failing interconnection to exhibit localized increases in temperature. The compromised microvia has a slightly higher resistance, compared to other (robust) microvias, and it will become the hottest structure in the coupon, and easily found using a thermographic camera. The thermographic camera allows direct visualization of the exact location of the weakest microvia (See Photo 6). The worst case failing microvia is seen as a high temperature hot spot on the surface of the coupon, the difference in temperature is generally within 5°C. This is a powerful tool for identifying failure locations to enable effective root cause analysis.

Thermograph of a Failing Microviia
Photo 6



Why the electronics industry must adopt a new accelerated reliability testing standard

The following discussion will step through each critical aspect of reliability testing and give recommendations for establishing an effective methodology.

The existing interconnect reliability standard developed back in the early 1960's is based on a measured electrical degradation in PTH structures. The criterion of a 10% increase in the bulk resistance of a test circuit is relative to the test circuit's initial measurement. The level of 10% change was established due to the requirement to microsection and visually confirm that cracks had completely propagated through the thickness of the copper plating, present on both sides of the barrel. The 10% requirement would translate to an interconnect structure in the final phases of damage acceleration before a determination of rejection is considered. The unnecessary collateral damage can make root cause analysis very difficult. The magnitude of additional damage confounds the ability to understand failure initiation. When the criterion was established there were limited techniques available for isolating defect sites. Thermo-graphic analysis (IR camera) is now used to identify the location of a failing interconnect at a low level of resistance change, enabling a visual understanding of failure initiation.

The need to change the standard is premised on the following: The influence of the resistance increase **only** becomes important if the failure mode is a latent defect that experiences a wear-out or fatigue driven condition. In situations where the resistance change is immediate (intermittent opens) the small differences in rejection criterion are overwhelmed by the magnitude of the localized resistance change, relative to the bulk. If due diligence is not applied the existing standard would commonly result in "no fault found", unless an open circuit is generated.

Conclusion

Measuring for microvia wear-out or precipitating latent failures makes it necessary to employ advanced measurement systems that are capable of detecting low level resistance activity. It is understood that microvia structures are a small percentage of the bulk resistance, making it logical that the rejection criteria for resistance increase should also be lowered to permit root cause analysis to be completed before collateral damage confounds the failure site. Reliability testing of microvia structures has confirmed that a 4% change is adequate to pass a point of irreversible change and interfacial defects can be found and confirmed during microsection analysis.

Reducing the criteria from 10% to 4% has proven effective for OEM's with microvia products that had previously established conformance testing protocol to a specified number of cycles. In previous testing, resistance activity was detected but not sufficient to exceed the 10% rejection criteria. Failure analysis subsequently found unacceptable quality conditions in the product.

The principle of lowering the criteria is that microvia structures should not electrically degrade; if resistance increases are measured it is an indication of "potential failure". For products using HDI technology the ability to avoid defective substrates being used in high reliability environment it is necessary to design the test circuit appropriately with electrical sensitivity and employ test equipment with sufficient measurement capability to detect low level activity.

Technology advances in the areas of measurement systems have improved accuracy and speed of data transfer which now permits the ability to measure lower levels resistance activity.

The documented 10% criteria does not specify the test vehicle design, the via type, or number of via structures. The specification does not consider whether the resistance change is localized or globally generated. In many cases it is not even required to expose the test vehicle to multiple assembly level temperature excursions prior to accelerated reliability testing.

This potential liability and the inability to complete effective reliability testing is created by poor test vehicle design, insufficient thermal energy to detect, or propagate latent defects, inadequate measurement capability and the use of continuous resistance monitoring. The combined lack of understanding is further confounded by the diversity and complexity related to the hierarchy of failure modes. The existing interconnect reliability standard did not anticipate microvia structures when the original criteria was established; the basis of this paper is designed to recommend changes to the existing methodology and acceptance criteria.

References

Microvia Reliability - Concerns in the Lead Free Assembly Environment (Andrews, Parry, Reid 2005). Presented at IPC-Apex 2006

Reliability Testing for Microvias In Printed Wire Boards (Bill Birch, 2011) Presented at EIPC-Conference 2011