## 4 QUALIFIED TECHNOLOGY FLOWS

The following Technology Flows are qualified:

### 4.1 ATMEL, FRANCE: MH1RT

**NOTES:**

1. An end of life notification affected the MH1RT process at the end of 2011, setting last delivery dates in June 2013.
2. LFoundry in Rousset ceased to supply MH1RT chips in December 2013 as well.
3. ATMEL MH1RT is therefore not available for any new designs. However, assembly and test operations (on legacy product designed and fabricated before January 2014) have remained possible beyond the scheduled last time delivery dates, within the ESCC qualified Technology Flow as described in the rest of this paragraph.
4. This entry will finally be removed from the ESCC QML in January 2015.

#### 4.1.2 Contact Information

| Address | ESCC Chief Inspector |
|---|---|
| Atmel Nantes<br>BP 70602<br>44306 Nantes Cedex 3<br>France | Mr C. Ferré<br>Tel. +33 24 01 81 913<br>FAX +33 24 01 81 946 |

#### 4.1.3 Qualification

| Current Qualification Certificate No. | In QML since: | Type Designation |
|---|---|---|
| 278C | Dec. 2006 | Integrated Circuits, Silicon Monolithic, CMOS Gate/ Embedded Array based on type MH1RT |

ESCC Generic Specification No. 9000

ESCC Detail Specification No. 9202/076

Atmel Process Identification Document PID 0026

#### 4.1.4 List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Atmel for use in conjunction with the ESCC Detail Specification No. 9202/076. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

| ASIC Sheet | Component Type | |
|---|---|---|
| FPK | **Integrated Motor Controller for Mechanisms** | * |

4.1.5 Technology Flow Abstract

1. Technology Flow

See Paragraph 5.1 Notes 1 and 2

The MH1RT gate array family is designed with a 0.35µm radiation tolerant CMOS technology. The offering is based on a 4 metal layer 3.3volts AT56KRT process.

The family features arrays with up to 1.6 million routeable gates and 596 pads. The MH1RT is suitable for high speed, low power digital applications working in a radiation intensive environment.

The Technology Flow covers the foundry design, fabrication, assembly and testing of the

MH1RT Sea of Gates family.

| | Scope | Site |
|---|---|---|
| Design Centre | Array Sizes:<br>- 99K<br>- 156K<br>- 242K<br>- 332K<br>- 3V and 5V tolerant/compliant | Atmel Nantes<br>BP 70602<br>44306 Nantes Cedex 3<br>France |
| Wafer Fabrication | Process Flow: AT56KLRT | LFoundry Rousset<br>Zone Industrielle<br>131106 Rousset Cedex<br>France |
| Assembly | Packages:<br>- Multilayer Quad Flat Pack<br>196, 256, 352 pins | E2V Grenoble<br>BP 123<br>38521 Saint-Egrève Cedex<br>France |

| | Scope | Site |
|---|---|---|
| Test | Lot Formation<br>Wafer Acceptance Inspection<br>- SEM<br>- Wafer Lot Acceptance In-process Inspection<br>Test<br>Testing Flow Sampling Plans Test Procedures<br>- Test Vector Generation<br>- Test Program Validation Customer Source Inspection Qualification Testing<br>Lot Acceptance<br>Support Qualification Test Plan/Report<br>Technology Characterization<br>Reliability Monitoring | Atmel Nantes<br>BP 70602<br>44306 Nantes Cedex 3<br>France |
| | Incoming Inspection<br>Final Test<br>- Credence, Type Octet<br>Screening<br>External Visual Inspection | Atmel Nantes<br>BP 70602<br>44306 Nantes Cedex 3<br>France |

(b) Basic Information

- 0.35 µm CMOS technology AT56KRT Process.
- High Speed Performance
  - 170 ps typical gate delay (NAND, fanout 2) @ 3V
  - 800 MHz typical toggle frequency @ 3.3V
- Triple Supply Operation
- 3.3, 3 and 2.55 V operation
  - 5V compliant
- Low Supply Current
  - Operating Maximum Value
    0.32 W/gate/MHz @ 2.5V,
    0.54 W/gate/MHz @ 3V,
    0.69 W/gate/MHz @ 3.3V
  - Maximum Stand-by Value
    4nA/gate@ 2.5V
    5nA/gate@ 3 and 3.3V
- I/O Interface
  - CMOS, LVTTL, LVDDS, PCI, USB
  - Output Currents Programmable from 2 to 24 mA, by Steps of 2 mA
  - Cold Sparing Buffers (2 µA maximum leakage current at 3.6V and 125oC)
- Radiation
  - qualified to 1000 Gy(Si) letter R per ESCC Basic Specification No. 22900, tested successfully to 2000 Gy(Si)
  - No Single Event Latch-up below a LET Threshold of 70 MeV/mg/cm$^2$
  - SEU Hardened Flip-flops
- Four Arrays and Four Composite Arrays
  - Device Types

- Refer to ESCC Detail Specification No. 9202/076

(c) Component Types

This table presents the available couples (array, package) as defined in the Variants table in the Detail Specification.

| Array Designation | TH1099E<br>TH1M099E | TH1156E<br>TH1M156E | TH1242E<br>TH1M242E | TH1332E<br>TH1M332E |
|---|---|---|---|---|
| Array size | 99K | 156K | 242K | 332K |
| Package | | | | |
| MQFP-T352 | X | X | X | X |
| MQFP-F256 | X | X | X | |
| MQFP-F196 | X | | | |

2. Design

See Paragraph 5.1 Notes 1 and 2.

The design manual and the ASIC library data books cover design at the Atmel Nantes Design Centre.

- MH1RT Design Manual ATD-TS-LR-R0232
- MH1RT 2V5 ASIC Library Data book ATD-TS-LR-R0236
- MH1RT 3V ASIC Library Data book ATD-TS-LR-R0235
- MH1RT 3V3 ASIC Library Data book ATD-TS-LR-R0238

ASIC designs are performed by the Atmel customer at their own site, with Atmel supported tools (front end) provided as a design tool kit.

3. Fabrication

See Paragraph 5.1 Notes 1 and 2

The AT56KRT Radiation Tolerant process at Atmel Rousset is a 0.35 µm CMOS, 4 metal, Ti, TiN and AlCu process.

4. Assembly

See Paragraph 5.1 Notes 3 and 4

Atmel Nantes assembles the MH1RT devices at E2V Grenoble. This Technology Flow covers the following capabilities. Solderability testing for MCGA packages is included.

Die attach for MQFP package is Cyanate Ester (JM7600).

| Package | Die Attach | Wire Bond | Lid Seal | Leads |
|---|---|---|---|---|
| MQFP | Cyanate Ester (JM7600) | Ultrasonic Wedge, 32 µm Al | Brazed Sealed with Au/Sn Alloy | Au Plated |

5. Test
See Paragraph 5.1 Notes 3 and 4

TCVs and SEC

The TH1156E matrix is used for both test vehicles.

(a) Test Vehicle V37
The V37 is a buffer test vehicle representative of the range of buffers available for performance testing in the MQFP 256 package.

(b) Test Vehicle V38
The V38 is developed for performance and radiation testing in the MQFP 256 package. It tests the following library elements;

- LVDS input and output buffers
- PCI 3V and 5V output buffers
- PLL (125 MHz and 250 MHz)
- DPRAM memory cell for GENESYS tool

(c) SEC
The standard evaluation circuit for reliability testing is the 65609E.

(d) The use of Transition Delay Fault (TDF) vectors are recommended.

6. Radiation Characteristics
The MH1RT family has been developed to fulfil the following characteristics in terms of radiation tolerance:

- Tested up to 2000 Gy(Si)
- No Single Event Latch-up below a LET Threshold of 70MeV/mg/cm$^2$
- Availability in the library of SEU hardened cells

The radiation capability of the MH1RT family has been tested during development and evaluated in total dose and for single event effects to confirm the stated characteristics. Lot radiation verification testing is performed if specified by the procurer's purchase order requirements.

4.2 ATMEL FRANCE: ATC18RHA

**NOTES**

1. LFoundry (LF) in Rousset ceased to supply ATC18RHA chips in December 2013
2. A second source of supply, UMC has been successfully added to the scope of Technology Flow qualification for this technology by Atmel.
3. New designs and fabrication after January 2014 make use of the UMC source.

4.2.2 Contact Information

| Address | ESCC Chief Inspector |
|---|---|
| Atmel Nantes<br>BP 70602<br>44306 Nantes Cedex 3<br>France | Mr C. Ferré<br>Tel. +33 24 01 81 913<br>FAX +33 24 01 81 946 |

4.2.3 Qualification

| Current Qualification Certificate No. | In QML since: | Type Designation |
|---|---|---|
| 312A | Aug. 2012 | Integrated Circuits, Silicon, Monolithic, CMOS, Cell-Based Array, based on Type ATC18RHA |

Applicable documents:

ESCC Generic Specification No. 9000

ESCC Detail Specification No. 9202/080

Atmel Process Identification Document PID 0030 (LF), PID 32 (UMC) and e2v PID DF 31S 100730 (assembly, common to both sources LF and UMC).

4.2.4 List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Atmel for use in conjunction with the ESCC Detail Specification No. 9202/080. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

| ASIC Sheet | Component Type |
|---|---|
| | |

In the case of ATC18RHA, standard components are also available. These are listed below with their full ESCC Detail Specification.

| Detail Specification | Component Type |
|---|---|
| 9512/004 | Integrated Circuits, Silicon, 32-bit SPARC Processor, based on Type AT697F |

4.2.5 Technology Domain Abstract
See NOTES under Para. 5.2

ATC18RHA standard cells family is designed with a 0.18µm radiation hard CMOS technology. This offering is based on 6 metal layers at 1.8V +/-0.15V for the core and 3.3V +/-0.3V for the periphery. This family features arrays with up to 6.5 Mgates and 544 pads. With its high speed performance, its low supply current and its radiation hard level, the ATC18RHA is suitable for digital applications working in radiation intensive environment.

The Technology Flow Definition domain covers the design, fabrication, assembly and testing of the ATC18RHA standard cells family.

| | Scope | Site |
|---|---|---|
| Design Centre | Matrix Sizes:<br>ATC18RHA95_216: 1.1 Mgates<br>ATC18RHA95_324: 2.2 Mgates<br>ATC18RHA95_404: 3.5 Mgates<br>ATC18RHA95_504: 5.5 Mgates<br>ATC18RHA95_544: 6.5 Mgates<br>AT697F : 0.85Mgate | Atmel Nantes<br>BP 70602<br>44306 Nantes Cedex 3<br>France |
| Wafer Fabrication | Process Flow: AT58KRHA | Up to December 2013:<br>LFoundry<br>Zone Industrielle<br>131106 Rousset Cedex<br>France |
| | | From January 2014:<br>UMC FAB8S<br>Hsin-Chu<br>Taiwan |
| Assembly | Packages:<br>- Multilayer Quad Flat Pack<br>100, 160, 196, 256, 352 pins<br>- Land Grid Array 349, 472 and 625 pins<br>- MCGA 349, 472 | E2V Grenoble<br>BP 123<br>38521 Saint-Egrève Cedex<br>France |
| Test | | |
| | Lot Formation<br>Wafer Acceptance Inspection<br>- SEM<br>- Wafer Lot Acceptance<br>In-process Inspection<br>Test | Atmel Nantes<br>BP 70602<br>44306 Nantes Cedex 3<br>France |

| | Scope | Site |
|---|---|---|
| | Testing Flow<br>Sampling Plans<br>Test Procedures<br>- Test Vector Generation<br>- Test Program Validation<br>Customer Source Inspection<br>Qualification Testing<br>Lot Acceptance<br>Support Qualification Test Plan/Report<br>Technology Characterization<br>Reliability Monitoring | |
| | Incoming Inspection<br>Final Test<br>- Credence, Type Octet<br>Screening<br>External Visual Inspection | Atmel Nantes<br>Atmel Nantes<br>BP 70602<br>44306 Nantes Cedex 3<br>France |

(a) Basic Information

- CMOS technology AT58KRHA
- 40 to 70 kgates per mm² - Up to 6.5M gates
- Double supply operation
  - Periphery power supply 3.3V
  - Core power supply 1.8V
- Low supply current :
  Operating maximum value: 85nW/gate/MHz with a duty cycle at 20%
- I/O Interfaces:
  - Cold sparing
  - High speed LVDS (655 Mps) and LVPECL
  - PCI
- 544 pads (+ 8 pads power only)
- Embedded memories: Compiled and Synthesized
- EDAC library
- Radiation (LF):
  - No Single Event Latch-Up below a LET Threshold of 80 MeV/mg/cm² at ambient & high temperature
  - SEU hardened DFF's to 30 MeV/mg/cm2
  - Tested up to 300 KRad (Si), Radiation Level is 100 KRads (Si).

- Radiation (UMC):
  - No single event latch-up below a LET Threshold of 67.7 MeV/mg/cm² (range = 37µm) at 125C up to a fluency of $1.10^{7}$ particles/cm² for a considered active thickness of 15µm.
  - The LET Threshold for the SEU hardened DFF is around 25 MeV/mg/cm² with a maximum cross-section of $1.10^{-7}$ cm² .
  - The LET Threshold of the standard DFF is around 2 MeV/mg/cm² with a maximum cross-section of $4.\ 10^{-7}$ cm²
  - The LET Threshold of the SRAM Virage memories is around 1 MeV/mg/cm² with a maximum cross-section of $4.10^{-8}$ cm². Very few MBU are noticed at 67.7 MeV/mg/cm² depending on the architecture
  - MBU can be avoided with ECC

– Matrices
  - Device Types – per individual custom ASIC sheets and ESCC Detail Specification 9202/080

(a) 1.3 Component Types
This table presents the available couples (matrix, package) as defined in the Detail Specification.

| | ATC18RHA 95_216 | AT697F | ATC18RHA 95_324 | ATC18RHA 95_404 | ATC18RHA 95-504 | ATC18RHA 95-544 |
|---|---|---|---|---|---|---|
| MQFP-T352 | | | X | X | X | |
| MQFP-F256 | X | X | X | X | X | |
| MQFP-F196 | X | | X | | | |
| MQFP-160 | X | | X | | | |
| MQFP-100 | X | | | | | |
| LGA 625 AIN | | | | | | X |
| LGA 625 | | | | | X | X |
| LGA 472 | | | | X | X | |
| LGA 349 | | X | X | X | X | |
| MCGA 472 | | | | X | X | |
| MCGA 349 | | X | X | X | X | |

2. Design
The design manual and the ASIC library data books cover design at the Atmel Nantes Design Centre.

– ATC18RHA Design Manual ATD-DE-GR-R0212
– ATC18RHA Buffers library databook ATD-TS-LR-R0252
– ATC18RHA Cells library databook ATD-TS-LR-R0251
– ATC18RHA Memory cells library databook ATD-TS-LR-R0254
– ATC18RHA specific library databook ATD-TS-LR-R0253

All ASIC designs will be performed by the customer at the customer site, with Atmel supported tools (front end).

3. Fabrication
The ATC18 Radiation Tolerant process at LFoundry Rousset is a 0.18 µm CMOS, 6 metal, Ti, TiN and AlCu process.

4. Assembly
Atmel Nantes assembles the ATC18RHA devices at E2V Grenoble.

This Technology Flow covers the following capabilities.

| Package | Die Attach | Wire Bond | Lid Seal | Leads |
|---|---|---|---|---|
| MQFP | Cyanate ester (JM7000) | Ultrasonic Wedge, 32 µm Al | Brazed Sealed with Au/Sn Alloy | Au Plated |
| LGA & MCGA | Cyanate ester (JM7000) | Ultrasonic Wedge, 32 µm Al | Brazed Sealed with Au/Sn Alloy | Au Plated |

5. Test

Atmel Nantes tests the ATC18RHA devices at Atmel Nantes.

(a) TCVs and SEC

The choice of test vehicles to qualify for LF and UMC supplier were agreed with the ESCC Executive and included devices calles V40,V47, AT697 and others.

(b) The use of Transistion Delay Fault (TDF) vectors are recommended.