

HEAVY IONS RADIATION TEST REPORT

Part Type : ADC14161

Package : 52-Pin TQFP

14-Bit, 2.5 MSPS A/D Converter

National Semiconductor

Report Reference : ESA_QCA991203S_C

Issue : 01

Date : December 27th 1999

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HEAVY IONS RADIATION TEST REPORT

on

National Semiconductor ADC14161 14-Bit A/D Converter.

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1 Abstract

Under ESA/ESTEC contract n° 13602/99/NL/GD dated 18/06/99 covering "Radiation Pre-screening of High-resolution High-speed ADC's", three different 14-bit Analog to Digital converters were radiation assessed. Results from these assessments, primarily focused on the radiation sensitivity of the ADC's to Total Ionizing Dose (TID) and Single Event Effects (SEE), are reported in individual TID and SEE reports. Below summary table lists manufacturer and evaluated types, and gives references to the various reports issued.

Manufacturer	Туре	TID Report	SEE Report
Analog Devices	AD9243	ESA_QCA991201T_C	ESA_QCA991201S_C
Linear Technology	LTC1414	ESA_QCA991202T_C	ESA_QCA991202S_C
National Semiconductor	ADC14161	ESA_QCA991203T_C	ESA_QCA991203S_C

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2 Introduction

This report presents the results of a heavy ion Single Event Effects (SEE) test program carried out on National Semiconductor ADC14161 Low-distortion, Self-calibrating 14-bit, 2.5 MSPS, 390mW A/D Converter.

Standard devices were tested at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.

Test set-up allowed for the detection of both Single Event Latch-up (SEL) errors and Single Event Upset errors (SEU).

This work was performed for ESA/ESTEC under ESA Contract No 13602/99/NL/GD dated 18/06/99

3 Documents

3.1 Applicable documents

AD1. SOW Radiation Pre-screening of High-resolution High-Speed ADC's Ref. APP-JP/99-02-057/PS/ps

3.2 Reference documents

- RD1. National Semiconductor, ADC14161 data sheet.
- RD2. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
- RD3. The Heavy Ion Irradiation Facility at CYCLONE, UCL document, Centre de Recherches du Cyclotron (IEEE NSREC'96, Workshop Record, Indian Wells, California, 1996)

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4 DEVICE INFORMATION

4.1 Device Description

Low-Distortion, Self-Calibrating 14-bit, 2.5 MSPS, 390mW A/D Converter

4.2 **Procurement of test samples**

15 samples have been procured by Hirex through distribution.

4.3 **Preparation of samples**

5 devices were picked for this SEE test and serialized from #1 to #5.
#1 was used as the golden chip.
#3 as control sample.
#2 and #4, and #5 were chemically opened (by Hirex Lab).
Further each test sample was then mounted on individual adapter boards.

4.4 Functional Test of samples

All opened samples were functional tested before use.

4.5 Device description

Description of the devices is as follows:

Part type :	ADC14161CIVT
Manufacturer :	National Semiconductor
Package :	52-Pin Plastic Thin Quad Flat Pack
Quality Level :	Standard
Date Code :	9752
Serial Number :	#001, #002, #003, #004, #005
Die Technology :	CMOS
Top Marking:	E9752AD
	ADC14161
	CIVT
Die Size :	4.7 mm x 4.1 mm approximately
Die Marking :	See Figure 1
Heavy ion test samples (delidded) :	3, #002, #004, #005

External and Internal Photos are shown in Figure 1.

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(x 10) Top view

(x 17) Die, Full view



(x 200) Die, Marking

(x 500) Die, Marking, Detail





Figure 2 – DUT Adapter Board

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5 Device Test Pattern Definition

5.1 Preparation of Test Hardware and Program

Overall device operation, SEU and Latch-up detection, data storage and processing were implemented using an in-house test hardware and application specific test boards.

The generic in-house test equipment is driven by a PC computer through a RS232 line. All power supplies and input signals are delivered and monitored by the in-house equipment which also stores in its memory the output data from the device under test.

The application specific test board allowed to interface the standard test hardware with the device under test, in order to correctly test the relevant part, to record all the different types of errors during the irradiation and to set output signal for processing and storage by the standard test equipment.

At the end of each test run, data are transferred to the PC computer through the RS232 link for storage on hard disk or floppies.

5.2 Generic Test Set-up

Generic device test set-up is presented in Figure 3 and is constituted of the following equipment units :

- A PC computer (to configure and interface with the test system and store the data),
- An electronic rack with the instrumentation functions provided by a set of electronic modules,
- A mother board under vacuum. This board provides the electronics needed for each test sequence, calibration, simulation and test.
- A digital oscilloscope to store analog upset waveform

5.2.1 <u>Mother board description (ref. IL170A)</u>

Main board characteristics are :

- Specially designed to test up to 16-bit ADC at a sampling frequency of 20 Mhz,
- Based on a golden chip approach.
- On-board analog pattern generator
- A common analog signal (linear ramp for calibration, sinus during test) is applied to both DUT and reference device inputs.
- Possibility to calibrate the DUT with the reference device by recording the errors values for each output word.
- Possibility to adjust a programmable voltage Vref to compensate for gain dispersion between DUT and ref. device.
- Both outputs are compared numerically thanks to the use of on-board CPLDs. For each comparison, the error value previously recorded for the output Ref. device word is subtracted.
- DUT output and comparison signals are converted with high-speed 8-bit DACs to allow for scope observation.
- Three on-board counters are used to sort the errors in the following categories, small, medium and large (A medium error is also counted as a small, a large error is also counted as a medium and a small error)

Mother board synoptic is shown in Figure 4.

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Figure 3 - Generic Device Test Set-up



Figure 4 - Mother board synoptic

5.2.2 <u>DUT Test board description</u>

Both the DUT and the reference device (golden chip) are mounted on adapters PCBs for easy interchangeable motherboard set-up.

This approach allows cost effective SEE testing of different ADC devices and types at the same time. Figure 2 show the DUT arrangement for AD14161 #2

Note : Beam focus diameter is limited to maximum 25 mm, to prevent the exposure of others devices which might be sensitive.

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5.3 Test configuration

The test configuration is as follows :

Sampling frequency is set to 2 MHz

Prior to the irradiation, a calibration run is performed which allows to record into the on-board memory the error value found for each output reference device word. This is done with a slow linear ramp (2ms period) applied to the inputs of both DUT and reference devices.

Calibration duration is such that, for each word, corresponding error is averaged on more than 20 values.

Eventually, DUT Vref is adjusted to minimize the error range.

With this approach, it is possible to match both output devices with a precision of \pm 5 LSBs.

Each irradiation run is performed with a 2 Hz sine waveform applied at both DUT and ref. inputs.

The different errors which can be detected are :

- Single errors which can be classified as small (threshold = +/- 6 LSBs), medium (threshold = +/- 96 LSBs) or large (threshold = +/-768 LSBs).
- Permanent errors : This was considered for this device which present an internal calibration.
- Latch-up errors : each power supply (Analog + and Logic) is monitored separately.

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6 TEST FACILITIES

6.1 Heavy Ions

Test at the cyclotron accelerator was performed at Université de Louvain (UCL) in Louvain la Neuve (Belgium) under HIREX Engineering responsibility.

6.1.1 Beam Source

In collaboration with the European Space Agency (ESA), the needed equipment for single events studies using heavy ions has been built and installed on the HIF beam line in the experimental hall of Louvain-la-Neuve cyclotron.

CYCLONE is a multi particle, variable energy, cyclotron capable of accelerating protons (up to 75 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU. For these ions, the maximal energy can be determined by the formula :

$110 \text{ Q}^2/\text{M}$

where Q is the ion charge state, and M is the mass in Atomic Mass Units.

The heavy ions are produced in a double stage Electron Cyclotron Resonance (ECR) source. Such a source allows to produce highly charged ions and ion "cocktails". These are composed of ions with the same or very close M/Q ratios. The cocktail ions are injected in the cyclotron, accelerated at the same time and extracted separately by a fine tuning of the magnetic field or a slight changing of the RF frequency. This method is very convenient for a quick change of ion (in a few minutes) which is equivalent to a LET variation.

6.1.2 Beam Set-up

6.1.2.1 Ion Beam Selection

The LET range was obtained by changing the ion species and incident energy and changing the angle of incidence between the beam and the chip.

For each run, information is provided on the beam characteristics in the detailed results table provided in paragraph 7.

6.1.2.2 Flux Range

For each run, the averaged flux value is provided in the detailed results table of paragraph 7.

6.1.2.3 Particle Fluence Levels

Fluence level was set to 1 x10E6 ions/cm²

6.1.2.4 Dosimetry

The current UCL Cyclotron dosimetry system and procedures were used.

6.1.2.5 Accumulated Total Dose

For each run, the computed equivalent cumulated doses received by the DUT sample, are provided in the detailed results table of paragraph 7.

6.1.2.6 Test Temperature Range

All the tests performed were conducted at ambient temperature.

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7 Heavy ions Results

The detailed results per run are presented in Table 1.

SEU cross-section versus LET for small, medium and large errors, is plotted respectively in Figure 6, Figure 7 and Figure 8.

Significant variations may be observed for a given LET. This is bounded to the fact that errors detected at the output of the device may be the consequence of an upset in the DUT calibration memory.

These errors can induce either a continuous flow of errors or a repetitive but not consecutive error pattern. Criterion for the detection of such errors has then been changed from 20 consecutive errors to more than 20 errors in less than 500 μ s and the corresponding SEU cross-section for such permanent errors is plotted in Figure 9.

Finally SEL errors have been observed for both An+ and logic power supplies and the corresponding SEL error cross-section per device are plotted in Figure 5.

Observation with the digital scope during the different runs, allowed to illustrate the different error waveforms as shown in Figure 10.

Figure 10 a) represent the effect of a permanent error in the calibration memory which induce repetitive but not consecutive errors.

In Figure 10 b) detection of permanent errors with the new criterion has been applied (> 20 errors in 500μ s). reset can be observed after each permanent error.

Figure 10 c) represent the small error envelop detected in run 49 (errors affect only one conversion cycle as error duration is 500ns which corresponds to the conversion frequency).

Lastly, in few occasions, analog events which could last several tens of microseconds have been observed and an example is presented in Figure 10 d). These types of errors were much less frequent than the other errors and are assumed to be generated in an analog part of the circuit (ref. area, for instance). Each error of this type was counted as one small or medium error (counter hold-off was set to 1 ms).

HIREX Er	ngineering		Heavy I	ons Test Repor	t	Réf. : HRX/99.4739 Issue : 01
Part T	Sype :	ADC14	161	Manufacturer :	Nat	ional Semiconductor
1E	-03					△ SN04 An+ △ SN02 An+
					\bigtriangledown	∇ SN02 logic
1 2	-				\forall	-
⁰ 1E	-04			\bigtriangledown	·	_
-section			∇		٨	
SS IE	-05				Æ	
Ö	-		Δ		\bigtriangleup	
U	-					
1F-	-06		₫			
	0.0	20,0	40.0) 60.0	0	80.0
		, I	LET MeV	/mg/cm²		
	Run ID	Error Type	Fluence (p/cm ²)	LET (Mev/mg/cm ²)	Nb Errors	Sigma (cm ²)
	SN04 An+		-	-		<u> </u>
	R00079	LU An+	5.00 E+05	34.0	0	2.000 E-06 *
	R00080	LU An+	1.79 E+05	48.1	0	5.591 E-06 *
	R00081	LU An+	1.90 E+05	68.0	I	5.252 E-06
	R00074	LU An+	4 82 E+05	34.0	0	2 075 E-06 *
	R00075	LU An+	1.00 E+06	34.0	4	4.000 E-06
	R00076	LU An+	2.47 E+05	48.1	0	4.041 E-06 *
	R00077	LU An+	1.66 E+05	68.0	2	1.203 E-05
	R00078	LU An+	4.00 E+05	68.0	4	1.000 E-05
	SN04 Logic	1		1	•	
	R00079	LU Logic	5.00 E+05	34.0	0	2.000 E-06 *
	R00080	LU Logic	1.79 E+05	48.1	18	1.006 E-04
	R00081	LU Logic	1.90 E+05	68.0	35	1.838 E-04
	SINU2 logic	LULogia	1 82 E 105	34.0	10	2 075 E 05
	R00074		4.02 E+03 1 00 F±06	34.0	10	2.075 E-05 3.000 E-06
	R00075	LULogic	2.47 E+05	48.1	47	1 899 E-04
	R00077	LU Logic	1.66 E+05	68.0	89	5.351 E-04
	R00078	LULogic	4.00 E+05	68.0	83	2.075 E-04

Figure 5 – AD14161 SEL device cross-section

HIREX Eng	gineering		Heavy Io	ons Test Repo	rt	Réf. : HRX/99 Issue : 01
Part Ty	pe :	ADC14	161	Manufacturer :	Na	ational Semiconductor
1E-()1	1				∆ SN04 ▽ SN02
8 . – .		57		∇		
E 1E-()2		✓	Δ	♦	
)-31 sectic		\$				
စို့ 1E-(ပိ	D4					
1E-0	0,0	20,0	40,0 ET MeV/	60	,0	80,0
	Run ID	Error Type		LFT	Nh Errors	Sigma (cm^2)
	Kull ID	Entor Type	(p/cm ²)	(Mev/mg/cm ²)	THE LITCHS	Sigma (cm)
	SN04		·	·	-	<u>.</u>
	R00048	Small	1.00 E+06	1.7	30	3.000 E-05
	R00047	Small	1.00 E+06	3.4	69	6.900 E-05
	R00042	Small	6.94 E+05	5.8	131	1.887 E-04
	R00043	Small	6.88 E+05	5.8	526	7.640 E-04
	R00044	Small	4.30 E+05	5.8	451	1.049 E-03
	R00045	Small	5.16 E+05	8.3	487	9.430 E-04
	R00046	Small	3.94 E+03	11./	48/	1.255 E-05 2 304 E 02
	R00003	Small	4.23 E+04	14.1	70 60	2.304 E-03 3 794 F-04
	R00004	Small	5.17 E+04	19.9	259	5.007 E-03
	R00006	Small	4.82 E+04	28.2	136	2.819 E-03
	R00079	Small	5.00 E+05	34.0	577	1.154 E-03
	R00080	Small	1.79 E+05	48.1	588	3.288 E-03
	R00081	Small	1.90 E+05	68.0	672	3.529 E-03
	SN02					
	R00050	Small	1.00 E+06	1.7	33	3.300 E-05
	R00049	Small	1.00 E+06	3.4	84	8.400 E-05
	R00029	Small	2.21 E+04	5.8	5	2.262 E-04
	R00028	Small	7.30 E+04	8.3	17	2.328 E-04
	R00027	Small	9.39 E+04	11.7	12	8.30/ E-04
	R00024	Small	5.79 E+04	14.1	13	3.42/ E-04
	R00025	Small	4.91 E+04	19.9	080 526	1.390 E-02
	R00020	Small	4.07 E+04	34.0	560	1.123 E-02
	R00074	Small	2.47 E+05	48.1	6470	2.613 E-02
	R00077	Small	1.66 E+05	68.0	463	2.778 E-03

Figure 6 – Small	errors, SEU	device	cross-section
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HIREX	Engineering	Ş		Heavy I	ons Test Repor	rt	Réf. Issue	: HRX/99.4739 : 01
Par	t Type :		ADC14	161	Manufacturer :	Na	tional Semicon	ductor
1	E-02						△ SN04 ▽ SN02	
1 cm²	E-03			Δ	$\stackrel{\wedge}{\bigtriangledown}$	$\stackrel{\bullet}{\bigtriangleup}$		
Cross-sectio L	E-04 E-05	▽ ▽		∞ ▽				
1	E-06		20,0 L	40,0 _ET Me∨) 60, //mg/cm²	0	80,0	_
	Run	D	Error Type	Fluence (n/cm ²)	LET (Mey/mg/cm ²)	Nb Errors	Sigma (cm ²)	
	SN04		I	(p/em)	(ivie v/ing/cm)			
	R000	48	Medium	1.00 E+06	1.7	0	1.000 E-06 *	
	R000	47	Medium	1.00 E+06	3.4	0	1.000 E-06 *	
	R000	42	Medium	6.94 E+05	5.8	30	4.321 E-05	
	R000	43	Medium	6.88 E+05	5.8	66	9.586 E-05	
	R000	44	Medium	4.30 E+05	5.8	188	4.374 E-04	
	R000	45	Medium	5.16 E+05	8.3	247	4.783 E-04	
	R000	46	Medium	3.94 E+05	11.7	296	7.506 E-04	
	R000	03	Medium	4.25 E+04	14.1	1	2.351 E-05	
	R000	04	Medium	1.82 E+05	14.1	1	3.849 E-05	
	R000	05	Medium	3.17 ± 04 4 82 E+04	19.9	4	7.755 E-05 8 291 E-05	
	R000	79	Medium	5.00 E+05	34.0	194	3 880 E-04	
	R000	80	Medium	1.79 E+05	48.1	516	2.885 E-03	
	R000	81	Medium	1.90 E+05	68.0	435	2.285 E-03	
	SN02		•	L				
	R000	50	Medium	1.00 E+06	1.7	0	1.000 E-06 *	
	R000	49	Medium	1.00 E+06	3.4	0	1.000 E-06 *	
	R000	29	Medium	2.21 E+04	5.8	0	4.525 E-05 *	
	R000	28	Medium	7.30 E+04	8.3	1	1.369 E-05	
	R000	27	Medium	9.39 E+04	11.7	1	1.065 E-05	
	R000	24	Medium	3.79 E+04	14.1	0	2.636 E-05 *	
	R000	23 26	Madium	4.91 E+04	19.9	3	0.112 E-05	
	R000	∠0 74	Medium	4.07 E+04	28.2	4	0.330 E-03	
	R000	76	Medium	4.02 E+03	<u> </u>	403	1.204 E-04	
	R000	77	Medium	1.66 E+05	68.0	763	4.588 E-03	

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Run ID	Error Type	Fluence	LET	Nb Errors	Sigma (cm ²)
		(p/cm ²)	(Mev/mg/cm ²)		0
SN04					
R00048	Large	1.00 E+06	1.7	0	1.000 E-06 *
R00047	Large	1.00 E+06	3.4	0	1.000 E-06 *
R00042	Large	6.94 E+05	5.8	38	5.473 E-05
R00043	Large	6.88 E+05	5.8	7	1.017 E-05
R00044	Large	4.30 E+05	5.8	200	4.653 E-04
R00045	Large	5.16 E+05	8.3	86	1.665 E-04
R00046	Large	3.94 E+05	11.7	108	2.739 E-04
R00003	Large	4.25 E+04	14.1	0	2.351 E-05 *
R00004	Large	1.82 E+05	14.1	2	1.100 E-05
R00005	Large	5.17 E+04	19.9	0	1.933 E-05 *
R00006	Large	4.82 E+04	28.2	2	4.145 E-05
R00079	Large	5.00 E+05	34.0	206	4.120 E-04
R00080	Large	1.79 E+05	48.1	479	2.678 E-03
R00081	Large	1.90 E+05	68.0	549	2.883 E-03
SN02					
R00050	Large	1.00 E+06	1.7	0	1.000 E-06 *
R00049	Large	1.00 E+06	3.4	0	1.000 E-06 *
R00029	Large	2.21 E+04	5.8	0	4.525 E-05 *
R00028	Large	7.30 E+04	8.3	0	1.369 E-05 *
R00027	Large	9.39 E+04	11.7	0	1.065 E-05 *
R00024	Large	3.79 E+04	14.1	0	2.636 E-05 *
R00025	Large	4.91 E+04	19.9	1	2.037 E-05
R00026	Large	4.67 E+04	28.2	3	6.418 E-05
R00074	Large	4.82 E+05	34.0	34	7.055 E-05
R00076	Large	2.47 E+05	48.1	825	3.334 E-03
R00077	Large	1.66 E+05	68.0	928	5.580 E-03

Figure 8 – Large errors, SEU device cross-section

HIREX Eng	ineering		Heavy Io	ons Test Repo	rt	Réf. : HRX/99.4739 Issue : 01
Part Typ	be :	ADC141	61	Manufacturer :	Na	ational Semiconductor
1E-0	3					△ SN04 ▽ SN02
	-		_	X	XX	
0-31 cm ²	4					
1E-0	6 L _{XXX}					
	O, Ø∕	20,0	40,0	60,	,0	80,0
		L	.ET MeV/	′mg/cm²		
	Run ID	Error Type	Fluence	LET	Nb Errors	Sigma (cm ²)
			(p/cm ²)	(Mev/mg/cm ²)		
	SN04					
	R00048	Permanent	1.00 E+06	1.7	0	1.000 E-06 *
	R00047	Permanent	1.00 E+06	3.4	0	1.000 E-06 *
	R00042	Permanent	6.94 E+05	5.8	44	6.337 E-05
	R00043	Permanent	6.88 E+05	5.8	33	4.793 E-05
	R00044	Permanent	4.30 E+03	9.3	24 58	5.384 E-05
	R00045	Permanent	3.10 E+03	0.5	50 65	1.125 E-04
	R00040	Permanent	4 25 E+04	14.1	8	1 881 F-04
	R00004	Permanent	1.82 E+05	14.1	23	1.265 E-04
	R00005	Permanent	5.17 E+04	19.9	12	2.320 E-04
	R00006	Permanent	4.82 E+04	28.2	14	2.902 E-04
	R00079	Permanent	5.00 E+05	34.0	89	1.780 E-04
	R00080	Permanent	1.79 E+05	48.1	93	5.200 E-04
	R00081	Permanent	1.90 E+05	68.0	115	6.040 E-04
	SN02			· -	-	
	R00050	Permanent	1.00 E+06	1.7	0	1.000 E-06 *
	R00049	Permanent	1.00 E+06	3.4	0	1.000 E-06 *
	R00029	Permanent	2.21 E+04	2.8 9.2	3	1.337 E-04
	R00028	Permanent	9 39 F+04	11 7	18	1 917 E-04
	R00024	Permanent	3.79 E+04	14.1	4	1.055 E-04
	R00025	Permanent	4.91 E+04	19.9	6	1.222 E-04
	R00026	Permanent	4.67 E+04	28.2	14	2.995 E-04
	R00074	Permanent	4.82 E+05	34.0	180	3.735 E-04
	R00076	Permanent	2.47 E+05	48.1	154	6.223 E-04
	R00077	Permanent	1.66 E+05	68.0	95	5.712 E-04

Figure 9 – Permanent errors (calibration), SEU device cross-section



On each scope view presented herein, the curve at the top, correspond to the DUT output converted with a 8-bits fast DAC (see Figure 4), while the curve at the bottom of the view, represent either the small, medium or large error converted also with a similar fast 8-bit DAC (see Figure 4) :

Verror = Vout(Ref)-Vout (DUT)-V(Calib)

For each error channel, +/- 500 mV corresponds to +/- 7 bits.

Figure 10 – Scope observation of error waveforms

HIREX Engineering	Heavy I	ons Test Repor	t	Réf. : HRX/99.4739 Issue : 01
Part Type :	ADC14161	Manufacturer :	National S	emiconductor

Table 1 - Detailed results per run on AD14161 @ 1Hz Input

ID	Sample	Ion	Date	Angle	Eff. LET	Run Time	Eff. Time	Flux	TID per Sample	Fluence	Eff. Fluence		SEU	errors		SEL	errors	Comments
ID No	ID No	ID No		0	Mev/mg/cm ²	sec	sec	P/cm ² /sec	Rads (Si)	P/cm ²	P/cm ²	Small	Medium	Large	Permanent	An+	Logic	
R00003	04	40-Ar	12/06/99	0	14,1	120	102	4,17 E+02	3,39 E+01	5,00 E+04	4,25 E+04	98	1	0	8	0	0	
R00004	04	40-Ar	12/06/99	0	14,1	503	457	3,98 E+02	7,91 E+01	2,00 E+05	1,82 E+05	69	7	2	23	0	0	
R00005	04	40-Ar	12/06/99	45	19,94	464	401	1,29 E+02	9,82 E+01	6,00 E+04	5,17 E+04	259	4	0	12	0	0	
R00006	04	40-Ar	12/06/99	60	28,2	684	660	7,31 E+01	1,21 E+02	5,00 E+04	4,82 E+04	136	4	2	14	0	0	
R00022	02	40-Ar	12/06/99	0	14,1	117	-	1,46 E+03	3,87 E+01	1,71 E+05	-	0	0	0	0	0	0	
R00023	02	40-Ar	12/06/99	0	14,1	546	-	1,83 E+03	2,65 E+02	1,00 E+06	-	0	0	0	0	0	0	
R00024	02	40-Ar	12/06/99	0	14,1	153	116	3,27 E+02	2,76 E+02	5,00 E+04	3,79 E+04	13	0	0	4	0	0	
R00025	02	40-Ar	12/06/99	45	19,94	258	253	1,94 E+02	2,92 E+02	5,00 E+04	4,91 E+04	685	3	1	6	0	0	
R00026	02	40-Ar	12/06/99	60	28,2	244	228	2,05 E+02	3,14 E+02	5,00 E+04	4,67 E+04	526	4	3	14	0	0	
R00027	02	20-Ne	12/06/99	60	11,7	248	233	4,03 E+02	3,33 E+02	1,00 E+05	9,39 E+04	78	1	0	18	0	0	
R00028	02	20-Ne	12/06/99	45	8,273	141	103	7,09 E+02	3,46 E+02	1,00 E+05	7,30 E+04	17	1	0	7	0	0	
R00029	02	20-Ne	12/06/99	0	5,85	77	17	1,30 E+03	3,56 E+02	1,00 E+05	2,21 E+04	5	0	0	3	0	0	
R00042	04	20-Ne	13/06/99	0	5,85	131	91	7,63 E+03	2,15 E+02	1,00 E+06	6,94 E+05	131	30	38	44	0	0	
R00043	04	20-Ne	13/06/99	0	5,85	302	208	3,31 E+03	3,08 E+02	1,00 E+06	6,88 E+05	526	66	7	33	0	0	
R00044	04	20-Ne	13/06/99	0	5,85	163	140	3,07 E+03	3,55 E+02	5,00 E+05	4,30 E+05	451	188	200	24	0	0	
R00045	04	20-Ne	13/06/99	45	8,273	425	313	1,65 E+03	4,48 E+02	7,00 E+05	5,16 E+05	487	247	86	58	0	0	
R00046	04	20-Ne	13/06/99	60	11,7	441	349	1,13 E+03	5,42 E+02	5,00 E+05	3,94 E+05	487	296	108	65	0	0	
R00047	04	10-B	13/06/99	60	3,4	215	-	4,65 E+03	5,96 E+02	1,00 E+06	-	69	0	0	0	0	0	
R00048	04	10-B	13/06/99	0	1,7	119	-	8,40 E+03	6,23 E+02	1,00 E+06	-	30	0	0	0	0	0	
R00049	02	10-B	13/06/99	60	3,4	239	-	4,18 E+03	4,10 E+02	1,00 E+06	-	84	0	0	0	0	0	
R00050	02	10-B	13/06/99	0	1,7	134	-	7,46 E+03	4,38 E+02	1,00 E+06	-	33	0	0	0	0	0	
R00074	02	84-Kr	14/06/99	0	34,0	297	143	3,37 E+03	9,82 E+02	1,00 E+06	4,82 E+05	560	58	34	180	0	10	
R00075	02	84-Kr	14/06/99	0	34,0	208	-	4,81 E+03	1,53 E+03	1,00 E+06	-	0	0	0	0	4	3	
R00076	02	84-Kr	14/06/99	45	48,083	274	113	2,19 E+03	1,99 E+03	6,00 E+05	2,47 E+05	6467	403	825	154	0	47	

HIREX Engineering	Heavy I	ons Test Repor	t 1	Réf. : HRX/99.4739 Issue : 01	
ADC14161	ADC14161	Manufacturer :	National Semiconductor		

ID	Sample	Ion	Date	Angle	Eff. LET	Run Time	Eff. Time	Flux	TID per Sample	Fluence	Eff. Fluence		SEU	errors		SEL	errors	Comments
ID No	ID No	ID No		0	Mev/mg/cm ²	sec	sec	P/cm ² /sec	Rads (Si)	P/cm ²	P/cm ²	Small	Medium	Large	Permanent	An+	Logic	
R00077	02	84-Kr	14/06/99	60	68,0	259	108	1,54 E+03	2,43 E+03	4,00 E+05	1,66 E+05	462	763	928	95	2	89	
R00078	02	84-Kr	14/06/99	60	68,0	213	-	1,88 E+03	2,86 E+03	4,00 E+05	-	0	0	0	0	4	83	
R00079	04	84-Kr	14/06/99	0	34,0	148	-	3,38 E+03	8,96 E+02	5,00 E+05	-	577	194	206	89	0	0	
R00080	04	84-Kr	14/06/99	45	48,083	163	73	2,45 E+03	1,20 E+03	4,00 E+05	1,79 E+05	588	516	479	93	0	18	
R00081	04	84-Kr	14/06/99	60	68,0	235	112	1,70 E+03	1,64 E+03	4,00 E+05	1,90 E+05	672	435	549	115	1	35	

HIREX Engineering	Heavy I	Heavy Ions Test Report						
Part Type :	ADC14161	Manufacturer :	National Semiconductor					

8 Conclusion

SEU test have been conducted on Low-Distortion, Self-Calibrating 14-bit, 2.5 MSPS, A/D Converter, AD14161 from National Semiconductor, using the heavy ions available at the University of Louvain.

This device has been found sensitive to SEL for both An+ and logic power supplies when tested with an LET of 34 MeV/mg/cm² or higher.

Heavy ion SEU susceptibility was obtained through the error cross section versus LET curve for three different errors magnitudes. However, errors in the calibration memory can induce DUT output errors and distinction between the output errors which can occur during a conversion cycle and the ones which are the consequence of an error inside the calibration area may not be possible. This then makes the reading of DUT output SEU cross-section curves difficult.

SEU calibration error cross-section versus LET errors has been plotted and corresponding LET threshold and asymptotic cross-section are given in Table 2 here below.

Error Type	LET Threshold (MeV/mg/cm²)	Device Asymptotic cross-section (cm ²)
Calibration (Permanent)	3,4	~ 6 E-4

 Table 2 – SEU errors characterization summary