Doc. No.: **RHM-ASG-RP-0002** Issue: **01** Date: **18.12.2014**

Radiation Hard Memory

Radiation testing of candidate memory devices for Laplace mission

Final Synthesis Report

Prepared by:	H. Schmidt (Airbus DS GmbH) K. Grürmann (IDA) M. Herrmann (IDA) F. Gliem (IDA)
Technical officer:	V. Ferlet-Cavrois (ESA/ESTEC)
Contract number:	ESTEC Contract No. 4000101358/10/NL/AF

© Airbus DS GmbH

CHANGE INDEX

Issue	Date	Section(s)	Description
01	18.12.2014	all	Initial issue

TABLE OF CONTENTS

1 Introduction and Scope 5
1.1 Introduction 5
1.2 Scope 5
1.3 Abbreviations and Terms 6
1.4 Vendor List 7
2 Documents 8
2.1 Applicable Documents 8
2.2 Deliverable Documents 8
2.3 Publications 9
2.4 Reference Documents 9
3 Feasibility Analysis 11
4 Test Equipment 12
4.1 NAND Flash 12
4.1.1 SEE Test Equipment 12
4.1.2 TID Test Equipment 14
4.1.3 Test Modes 16
4.1.4 Error Classification 16
4.2 DDR3 SDRAM 18
4.2.1 DDR3 Test Equipment 18
4.2.2 TID Test Equipment 21
4.2.3 Test Modes 22
4.2.4 Error Classification 23
5 NAND Flash Characterisation 24
5.1 SEE Heavy Ions Test Results 24
5.1.1 DUT Preparation 24
5.1.2 Samsung K9WBG08U1M (4 x 8 Gb) 27
5.1.3 Micron MT29F8G08AAAWP-ET:A 32
5.1.4 Micron MT29F16G08ABACAWP-IT:C (16 Gb) & MT29F32G08ABAAAWP-IT:A (32 Gb) 34
5.1.5 SEU Annealing 46
5.1.6 Annealing of SHE (stuck bits) 47
5.1.7 Further investigations on destructive events 48
5.2 SEE Protons Test Results 51
5.2.1 Static SEU 52
5.2.2 SEU Annealing 54

© Airbus DS GmbH

5.2.3 SEFI 55
5.2.4 Destructive Failures 59
5.3 TID Test Results 60
5.3.1 Definition of Parameter Limits 60
5.3.2 Storage Mode 61
5.3.3 Refresh Mode 63
5.3.4 Comparison with unbiased Pre-Test 67
5.3.5 Conclusion 69

6 DDR3 SDRAM Characterisation 70
6.1 SEE Heavy Ions Test Results 70
6.1.1 DUT Preparation 70
6.1.2 1st SEE test campaign on 2Gb DDR3 SDRAM devices at RADEF (SEE_HI_1) 72
6.1.3 Further SEE tests on 2Gb and 4 Gb DDR3 SDRAM devices at RADEF and TAMU (SEE_HI_2 to SEE_HI_4) 75
6.2 SEE Protons Test Results 88
6.2.1 Error Pattern 89
6.2.2 SEU 90
6.2.3 SHE (stuck Bits) 92
6.2.4 Transient SEFI 92
6.2.5 Persistent SEFI (Device SEFI) 95
6.3 TID Test Results 97
6.3.1 1st in-situ TID test (TID_1) 97
6.3.2 Further unbiased TID tests (TID_2 & TID_3) 107
6.3.3 Final in-situ TID test (TID_4) 110
6.3.4 Annealing 116
6.4 Conclusions on DDR3 TID Test Campaigns 120

7 Conclusions 121

Appendix A. Performed Test Campaigns 124

Appendix B. Procured Parts 125

1 Introduction and Scope

1.1 Introduction

According the statement of work [AD-01] investigations on radiation effects on heritage as well as latest SLC NAND flash memories as well as on a wide spread of 2 Gb and 4 Gb DDR3 SDRAM devices were performed.

Prime contractor is Airbus DS GmbH (formerly Astrium GmbH). Preparation, execution and analysis of radiation test campaigns - including the development and operation of sophisticated test equipments - has been subcontracted to IDA of Technische Universität Braunschweig.

1.2 Scope

This document provides the synthesis of the performed radiation testing activities in the frame of ESA Rad Hard Memory study. Further details on the several test campaigns and its results are provided in the specific test reports listed in the documents section.

© Airbus DS GmbH

1.3 Abbreviations and Terms

AD	Applicable Document
DDR	Double Data Rate
DF	Destructive Failure
DLL	Delay-Locked Loop
DUT	Device Under Test
EOL	End of Life
FBGA	Fine-pitch Ball Grid Array
FPGA	Field Programmable Gate Array
FIFO	First In First Out
Gb	Giga bit
GB	Giga bytes
HV	High Voltage
IDA	Institut für Datentechnik und Kommunikationsnetze
JUICE	Jupiter Icy Moon Explorer
MBU	Multiple Bits Upset
MCU	Memory Cell Upset
MLC	Multi-Level Cell
PHY	Physical Interface
RD	Reference Document
SBU	Single Bit Upset
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SEB	Single Event Burnout
SEDR	Single Event Dielectric Rupture
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SET	Single Event Transient
SEU	Single Event Upset
SHE	Single Event Hard Error (stuck-bit)
SLC	Single-Level Cell
SODIMM	Small Outline Dual Inline Memory Module
SSD	Solid State Disk
TBC	To Be Confirmed
TBD	To Be Determined
TID	Total Ionizing Dose
TIDL	TID Level
TIDS	TID Sensitivity
WC	Worst Case
WW	Worst Week
ZIF	Zero Insertion Force

1.4 Vendor List

ELP J	Elpida Memory Inc., Japan
MIC U	Micron Technology Inc., USA
NAN TW	Nanya Technology Corp., Taiwan
SAM K	Samsung Electronics Co., Ltd., South Korea
SKH K	SK Hynix Inc., South Korea

2 Documents

2.1 Applicable Documents

The documents, specified and listed in order of precedence hereafter, are applicable to their full extent unless expressively stated otherwise.

[AD-01]	TEC-QEC/xx/SOW/2009-1	SOW, Radiation Hard Memory; Radiation (T222-016QC) Testing of Candidate Memory Devices for Laplace Mission

2.2 Deliverable Documents

Unless stated otherwise, the latest issue of the deliverable documents at the date of the issue of this document is valid.

[DD-01]	TN-IDA-RAD-11/3	Test Plan of the May 2011 SEE Test at RADEF.
[DD-02]	TN-IDA-RAD-11/5B	Heavy Ions SEE Test of 2-Gbit DDR3 SDRAM Devices and of 8-Gbit NAND Flash Memory Devices.
[DD-03]	TN-IDA-RAD-11/8E	Test Plan of the January 2012 SEE Test at RADEF.
[DD-04]	TN-IDA-RAD-12/6	Heavy Ion Test, Jyväskylä, April 2012, Test Plan.
[DD-05]	TN-IDA-RAD-12/12	Heavy Ions SEE Test of 16-Gbit/32-Gbit Micron SLC NAND-Flash Memory Devices.
[DD-06]	TN-IDA-RAD-12/13	Heavy Ion SEE Test of 2-Gbit and 4-Gbit DDR3 SDRAM Devices
[DD-07]	TN-IDA-RAD-12/14	TAMU, Dec., 4 – Dec. 7, 2012, SEE Test of DDR3 SDRAM, Preliminary Test Concept
[DD-08]	TN-IDA-RAD-12/15	TID Test of 4-Gbit DDR3 SDRAM, Preliminary Test Approach
[DD-09]	TN-IDA-RAD-13/1A	Heavy Ion SEE Test of 4 Gbit DDR3 SDRAM Devices
[DD-10]	TN-IDA-RAD-13/2B	Heavy Ions SEE Test of 4 x 8 Gbit Samsung and 16-Gbit Micron SLC NAND Flash Memory Devices
[DD-11]	TN-IDA-RAD-13/4	TID Test of 4 Gbit DDR3 SDRAM Devices
[DD-12]	TN-IDA-RAD-13/9B	Unbiased TID Test of 2-Gbit and 4-Gbit DDR3 SDRAM Devices, Proposal for Revision of the Test Strategy
[DD-13]	TN-IDA-RAD-13/12	Unbiased preselection TID Test of 4-Gbit DDR3 SDRAM Devices, Approach or in-situ test
[DD-14]	TN-IDA-RAD-14/2	Functional TID Test of 4-Gbit Micron and Hynix DDR3 SDRAM and 16-Gbit/32-Gbit Micron SLC NAND Flash Memory Devices, Test Plan
[DD-15]	TN-IDA-RAD-14/3	In-situ and unbiased TID Test of 4-Gbit DDR3 SDRAM Devices

[DD-16]	TN-IDA-RAD-14/4	Functional TID Test of 16-Gbit/32-Gbit Micron SLC NAND-Flash Memory Devices, ESA-ESTEC, January, 17-24, 2014
[DD-17]	TN-IDA-RAD-14/5	Proton Test of 16-Gbit/32-Gbit Micron SLC NAND Flash Memory Devices, PSI PIF, April 4-6, 2014, Test Plan
[DD-18]	TN-IDA-RAD-14/6	Proton Test of 4-Gbit DDR3 SDRAM Memory Devices, PSI PIF, March, 21-23, April 4-6, 2014, Test Plan
[DD-19]	TN-IDA-RAD-14/7	Proton Test of 16-Gbit/32-Gbit Micron SLC NAND Flash Memory Devices
[DD-20]	TN-IDA-RAD-14/8	Proton SEE Test of 4-Gbit DDR3 SDRAM Devices from Hynix, Micron and Samsung

2.3 Publications

[PD-01]	NSREC 2011, W-24	K. Grürmann et al., "SEU and MBU Angular Dependence of Samsung and Micron 8-Gbit SLC NAND Flash Memories under Heavy-Ion Irradiation," 2011 IEEE Radiation Effects Data Workshop Record.
[PD-02]	RADECS 2011, C-5	K. Grürmann et al., "MBU characterization of NAND Flash Memories under Heavy-Ion Irradiation," RADECS 2011.
[PD-03]	RADECS 2011, DW-28	M. Herrmann et al., "Heavy ion SEE test of 2 Gbit DDR3 SDRAM," RADECS 2011.
[PD-04]	NSREC 2012, W-9	K. Grürmann et al., "Heavy Ion sensitivity of 16/32-Gbit NAND Flash and 4-Gbit DDR3 SDRAM," 2012 IEEE Radiation Effects Data Workshop Record
[PD-05]	RADECS 2012, DW-23L	K. Grürmann et al., "New SEE Test Results of 16/32-Gbit SLC NAND-Flash," RADECS 2012.
[PD-06]	RADECS 2012, DW-25L	M. Herrmann et al., "New SEE Test Results for 4 Gbit DDR3 SDRAM," RADECS 2012.
[PD-07]	NSREC 2013, W-41L	M. Hermann et al., "In-situ TID Test of 4-Gbit DDR3 SDRAM Devices," 2013 IEEE Radiation Effects Data Workshop Record.
[PD-08]	RADECS 2013, DW-21L	M Herrmann et al., "New SEE and TID Test Results for 2-Gbit and 4-Gbit DDR3 SDRAM Devices," RADECS 2013.

2.4 Reference Documents

Unless stated otherwise, the latest issue of the reference documents at the date of the issue of this document is valid.

[RD-01]	NSREC 2008, W-6	H. Schmidt et al., "TID and SEE Tests of an Advanced 8-Gbit NAND Flash Memory," 2008 IEEE Radiation Effects Data Workshop Record.

[RD-02]	TN-IDA-RAD-09/3C	Heavy Ion SEE Test of 4 x 8 Gbit Samsung NAND Flash Memory Devices (K9WBG08U1M-PIB0/ TSOP 1-48)
[RD-03]	RHM-ASG-RP-0001	Rad Hard Memory: Study Status
[RD-04]	JPL Publication 11-8 10/11	Radiation Tests of Highly Scaled, High-Density, Commercial, Nonvolatile NAND Flash Memories — Update 2011.
[RD-05]	JPL Publication 12-19 12/12	Radiation Tests of Highly Scaled, High-Density, Commercial, Nonvolatile NAND Flash Memories — Update 2012.
[RD-06]	RADECS 2007, PC-2	H. Schmidt et al., "Annealing of Static Data Errors in NAND-Flash Memories," RADECS 2007.
[RD-07]		F. Irom et al., Catastrophic Failure in Highly Scaled Commercial NAND Flash Memories," IEEE TNS, vol. 57, no. 1, pp. 266-271, 2010.
[RD-08]		T. R. Oldham et al., Investigation of Current Spike Phenomena during Heavy Ion Irradiation of NAND Flash Memories," 20th Annual Single Event Effects Symposium, San Diego, April 2011.

3 Feasibility Analysis

At time of start of the study, only a very limited number of NAND Flash memory devices in SLC technology and sufficient density (≥8 Gb) were available. The former tested 8 Gb SLC devices from Samsung were announced End-of-Life (EOL) for Q3/2010. Even though, Toshiba/SanDisk and Samsung were producing SLC devices up to monolithic densities of 16 Gb, these devices were not available on free market and could not be procured. SK Hynix (Hynix at this time) was offering monolithic densities up to 4 Gb only, Micron was offering SLC NAND Flash of 8 Gb and 16 Gb density in 34nm feature size. Nevertheless, according the road maps at time they were subjected for EOL until end of 2011. The new 25nm technology was just introduced by Micron. The next generation (20nm) was introduced not before end of 2013 / start of 2014 and could not be included in this study.

Hence, additional to 4 x 8 Gb devices from Samsung from stock as reference parts, the latest Micron SLC NAND Flash in 25nm technology were subjected to be characterized in Rad Hard Memory study. They were announced for Q1/2011 but could not be procured before Q3/2011 delaying the testing activities on these devices to start of 2012.

For dynamic memories the most promising technology was DDR3 SDRAM. On consumer market, the change from DDR2 SDRAM to DDR3 SDRAM was just started - according manufacturer road maps DDR3 SDRAM was the only technology providing monolithic densities up to 4 Gb. Hence, a variety of available 2 Gb and 4 Gb DDR3 SDRAM devices were subjected for further radiation characterisation.

At start of this study Samsung 4 Gb and Elpida 4 Gb DDR3 SDRAM devices have been selected for further characterisation. Nevertheless, Elpida was overtaken by Micron, their SDRAM products will not be continued. Hence, further candidates from Micron, SK Hynix and Nanya were at least partially characterized in this study.

Single Data Rate (SDR) SDRAMs are of low interest. Even though, these devices are the standard technology for Solid State Disk (SSD) applications these days, their availability is limited. Only a very few manufacturers will provide the market with SDR SDRAMs in future, the available density of these devices is mainly limited to 256 Mb. Furthermore, as these devices are mainly manufactured in heritage technology i.e., feature sizes ≥ 50nm, no sufficient TID performance is expected for the use in envisaged JUICE mission.

In Appendix B a list of all procured memory parts is provided. Furthermore, IDA has provided some additional parts for testing also listed there.

4 Test Equipment

4.1 NAND Flash

4.1.1 SEE Test Equipment

The used memory test-bed RTMC-5 is in heritage of the test-bed RTMC-3, developed for ESA and operated by IDA. There are two configurations: (A) for Heavy Ion testing and (B) for Protons testing (see Figure 4-1 and Figure 4-2 below).

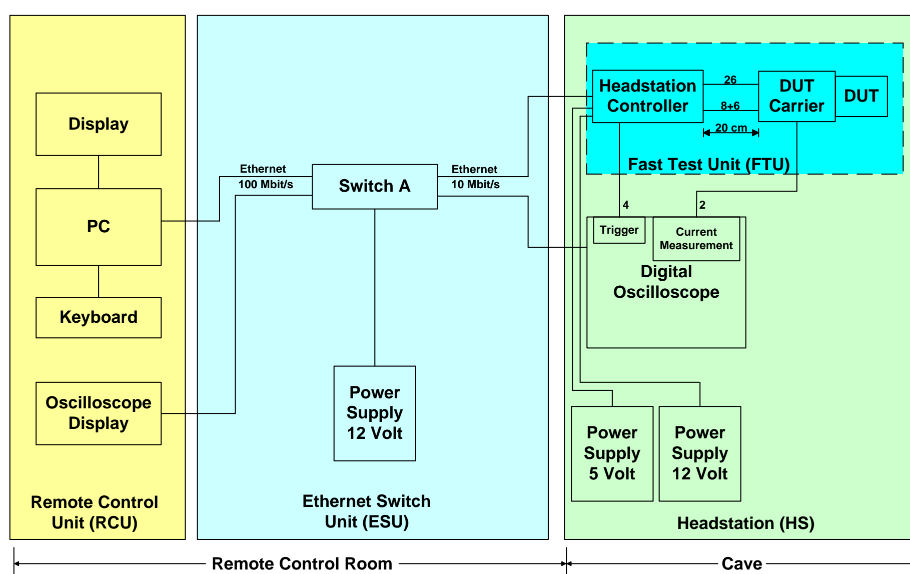

Figure 4-1: SEE memory test bed RTMC-5 for use for Heavy Ions testing (Configuration A)

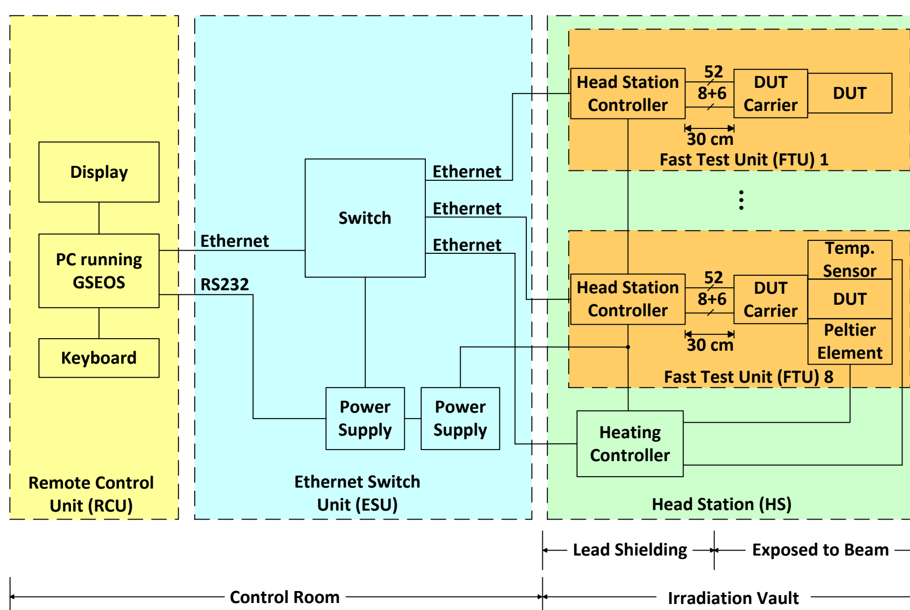

Figure 4-2: SEE memory test bed RTMC-5 for use for Protons testing (Configuration B)

The RTMC-5 test bed is composed of three units:

- **Head Station (*HS*)** with up to 8 **Fast Test Units (*FTU*)** composed of a Head Station Controller and the Device Under Test (*DUT*)
- **Ethernet Switch Unit (*ESU*)**, HS-RCU communication via network
- **Remote Control Unit (*RCU*)** PC based H/W supported system, running under GSEOS V, for sending commands and receiving data from the FTUs

The DUT are mounted on a DUT carrier. Each DUT carrier is served by its own Fast Test Unit (FTU).

The FTUs are supplied by 5 and 12 V and generate a DUT sup-ply voltage between 2.7 V and 3.6 V, settable by the Remote Control Unit (RCU). The FTUs measure continuously the standby current and the operating current of the DUTs. The FTUs are equipped with a Latch Up Switch. Its current threshold is RCU settable between 50 mA and 200 mA, and its delay time between 1 µs and 1 ms. Measurement of program time and erase time is an additional feature of the FTUs. The Remote Control Unit is based on a PC running our proprietary configurable GSEOS V test S/W package. On the PC, an error map is displayed for preliminary visual analysis, along with a total error count and various statistics. The error vectors are stored on disk for offline analysis.

The RCU provides (i) control of the test sequences (test modes), (ii) generates specific data pattern and address loops, (3) supports the setting of all test parameters, (iv) performs a real time pattern verification, (v) counts data errors in real time, (vi) records all error vectors, cur-rent and time measurements, Latch up trigger actions and all parameter settings for off line evaluation of the test data files, (vii) delivers a real time visualization of the error distribution, of several statistical distributions, etc.

For investigations on the angular dependency of SEU, the DUT mounting was improved providing now rotation of the DUT by 360° at azimuth axis (Θ) and 90° tilting at the elevation axis (Ψ), see Figure 4-3. The connected step motors can be remotely controlled from measurement room.

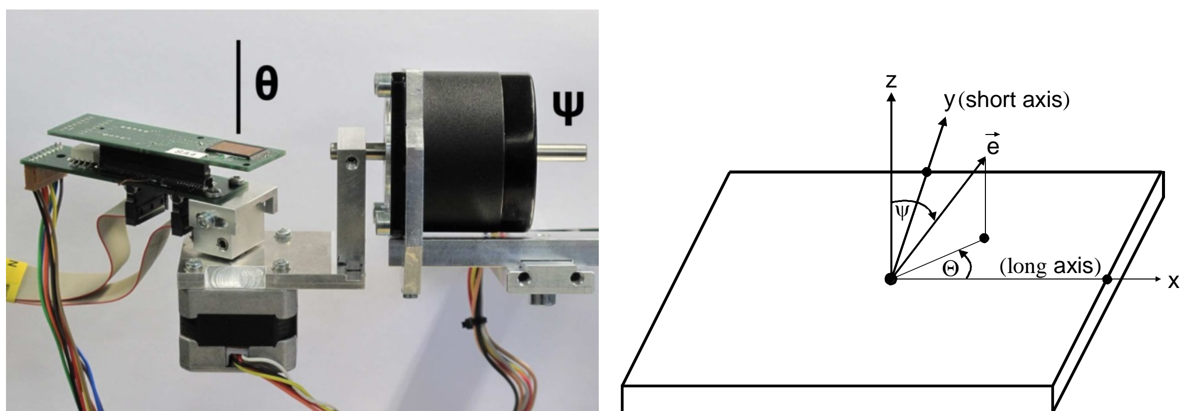

Figure 4-3: Test equipment with adjustable azimuth and elevation tilting.

In the frame of RHM study the mounting and alignment to the beam was further improved to retrieve more symmetric angular cross section diagrams.

4.1.2 TID Test Equipment

In order to perform irradiation tests with a high total dose, all sensitive parts apart from the DUTs must be shielded from the emitted radiation (Figure 4-4 and Figure 4-5). For this purpose, IDA has developed a shielding box made of lead (where space is critical) and steel. The box weighs about 1300 kg and is assembled from individual parts of about 10 kg to 20 kg each. It has several curved channels for feeding electrical wires and water tubes for the cooling system into the box.

The NAND Flash DUTs are shielded against electrons by a 6-mm acrylic glass between the Co-60 source and the DUTs (Figure 4-5).

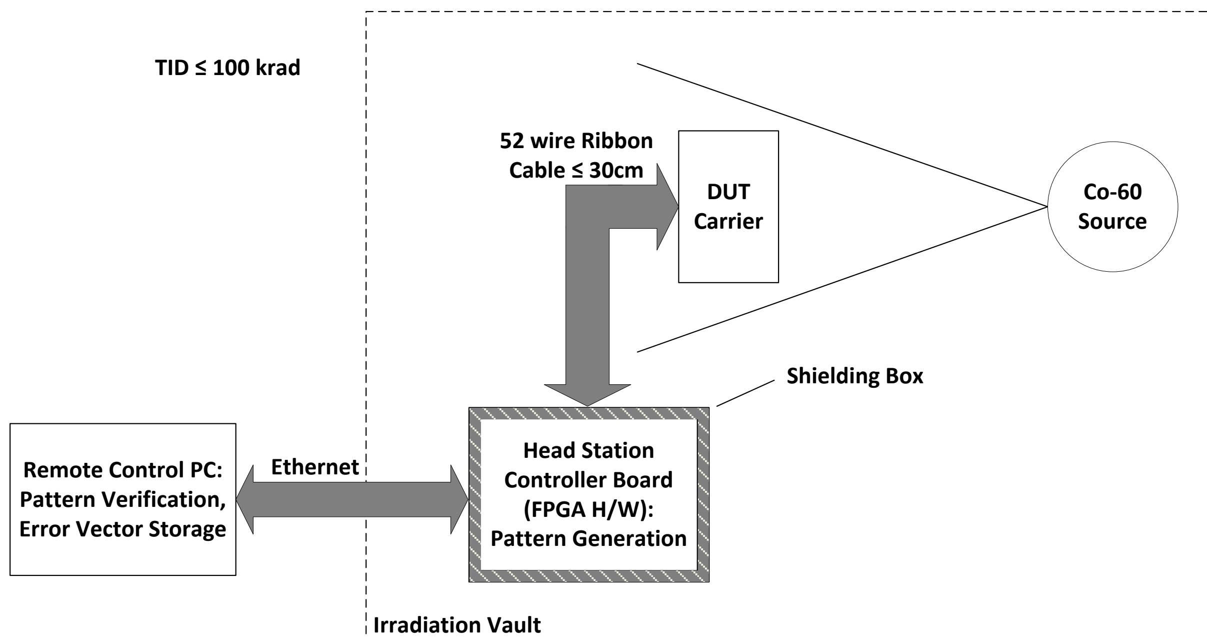

Figure 4-4: Test Setup at the irradiation facility

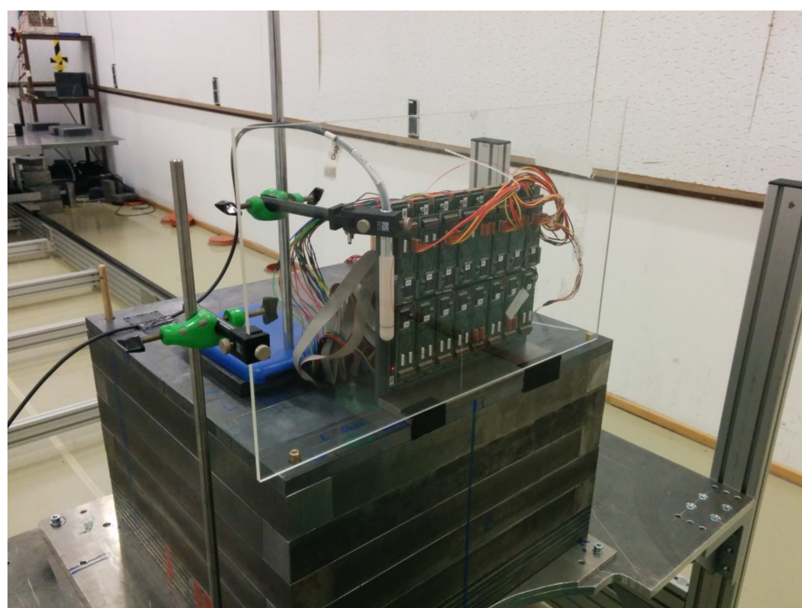

Figure 4-5: Shielding box with 16 NAND Flash DUTs above

© Airbus DS GmbH

Figure 4-6 shows the block diagram of the TID Test Set Up. Up to sixteen DUT Carriers are exposed simultaneously to a beam of 10 cm by 10 cm. Each DUT Carrier is served by its own Fast Test Unit (FTU). In contrast to the DUT Carriers the sixteen FTU boards are allocated outside of the beam, approximately 30 cm below the DUT Carriers inside the shielding box.

The FTUs are supplied by 5 and 12 V and generate a DUT supply voltage between 2.7 V and 3.6 V, settable by the Remote Control Unit (RCU). The FTUs measure continuously the standby current and the operating current of the DUTs. The FTUs are equipped with a Latch Up Switch. Its current threshold is RCU settable between 50 mA and 200 mA, and its delay time between 1 µs and 1 ms. Measurement of Program Time and Erase Time is an additional feature of the FTUs.

Four of the ten DUT Carriers are equipped with a Thermo Electric Cooler (Peltier element) for temperature control between –20°C and +85°C.

The FTUs communicate with the RCU via an Ethernet link.

The Remote Control Unit is based on a PC running our proprietary configurable GESOS V test S/W package.

The RCU provides (i) control of the test sequences (test modes), (ii) generates specific data pattern and address loops, (3) supports the setting of all test parameters, (iv) performs a real time pattern verification, (v) counts data errors in real time, (vi) records all error vectors, current and time measurements, Latch up trigger actions and all parameter settings for offline evaluation of the test data files, (vii) delivers a real time visualization of the error distribution, of several statistical distributions, etc.

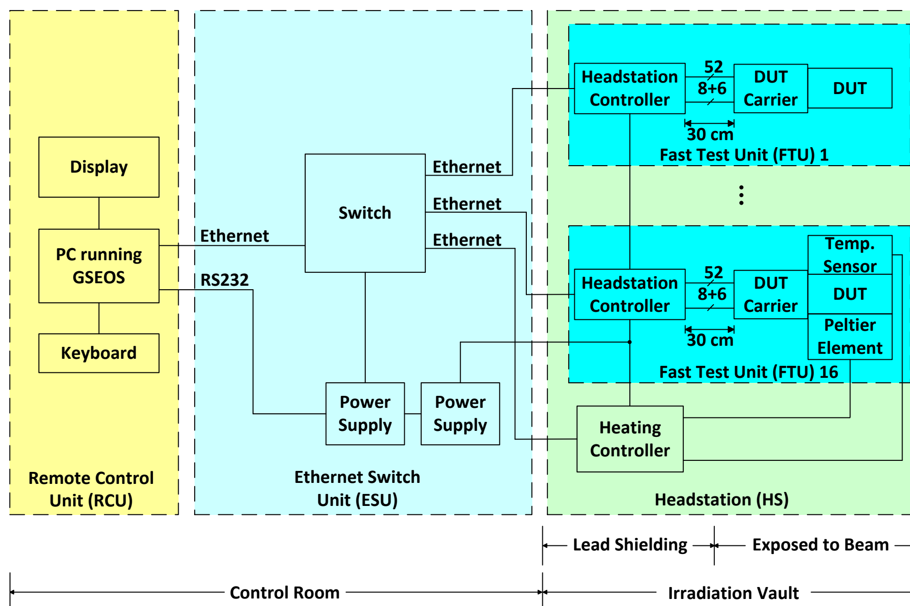

Figure 4-6: Block diagram of the NAND Flash test setup configured for TID tests

4.1.3 Test Modes

The tests were performed with a checkerboard pattern.

To retrieve static and dynamic data errors as well as more sophisticated data error patterns such as error clusters, and also SEFIs, three main test modes with several options each have been developed and were used:

- **Storage Mode (M3)**:
  Before irradiation a pattern (all ones, all zeros, checkerboard, random) is written into the DUT and verified. Default is the checkerboard pattern. Then the device is irradiated biased (M3a) or unbiased (M3b). After exposure the content of the device is read and verified. Only static data errors are delivered by this mode.
- **Read Mode (M2R)**
  Before irradiation a pattern is written into the DUT and verified. During the exposure the content of the device is continuously read and verified, each page either one time or two times. The dual read option provides differentiation between static and dynamic data errors. After the exposure the content of the device is read again. If SEFIs remain a power cycle and a reread is performed.
- **Marching Mode (M1, M5)**
  Before irradiation a pattern is written into the device and verified. During exposure the content of every single block of the device is read and verified; then erased and verified again; and then programmed and verified page by page with the inverted pattern, continuously block by block, again and again. This mode exercises a mixture of read, erase and program operations. In this mode the DUTs are susceptible to SEFIs of all kinds, in particular to Persistent SEFIs and also because of the numerous erase operations to Destructive SEFIs. For some NAND Flash types the insertion of a power cycle (PC) after each erase operation reduces drastically the sensitivity to SEFIs, in particular to Destructive SEFIs. The Marching Mode M1 runs without the insertion of PCs, the Marching Mode M5 with insertion of PCs. The power on duration is selectable (default: 1ms).

4.1.4 Error Classification

Due to the complex device structure of modern NAND Flash memories, comprising a state machine, a large S/P register, a High Voltage Pulser, etc., a large number of different error conditions can occur. These error conditions are classified according to Figure 4-7 into four main classes and several subclasses:

Static Errors appear again at repeated read in contrast to Dynamic Errors. Static Errors originate from the floating gate array and Dynamic Errors from the peripheral data path. These both kinds of spurious Data Errors can be handled easily with a conventional error correction scheme (Hamming EDAC, Reed-Solomon).

Single Event Hard Errors (SHE) i.e., "stuck-bits" are semi-permanent falsifications of single memory cells. They cannot be removed by erase or program operation. Nevertheless, some of these errors anneal with time.

More challenging for the error correction are SEFIs. Transient SEFIs are caused by hits in the control circuitry as in the State Machine or in the S/P Register. Unlike Persistent SEFIs they disappear without the need of a device reset.

Both classes of SEFI are differentiated further into (i) Page Errors (PE) corrupting an amount of bytes per page, (ii) Block Errors (BE) corrupting a series of n device pages up to the end of the respective device block and (iii) Column Errors (CE) corrupting the same byte position of subsequent device pages. Additionally, some Persistent SEFI can also corrupt the complete device i.e., the device is not responding at all anymore.

Device Failure i.e., destructive SEE, lead into permanent destruction of functional units of the device.

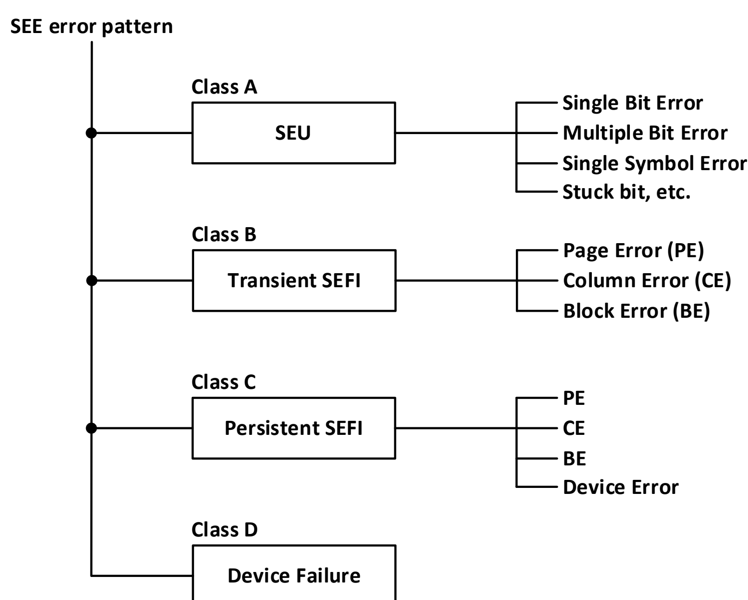

Figure 4-7: Applied error classification scheme

4.2 DDR3 SDRAM

4.2.1 DDR3 Test Equipment

Due to the complicated high speed constrains of the DDR3 interface and DDR3 SDRAM devices an elaborated high speed test equipment, RTMC-6 (Figure 4-8), have been developed and built by IDA. It is based on Xilinx® ML605 evaluation board, which contains a Xilinx® Virtex 6 FPGA and is capable of operating the first rank of one SODIMM with 8 DUTs in x8 organisation at a clock frequency of up to 400MHz.

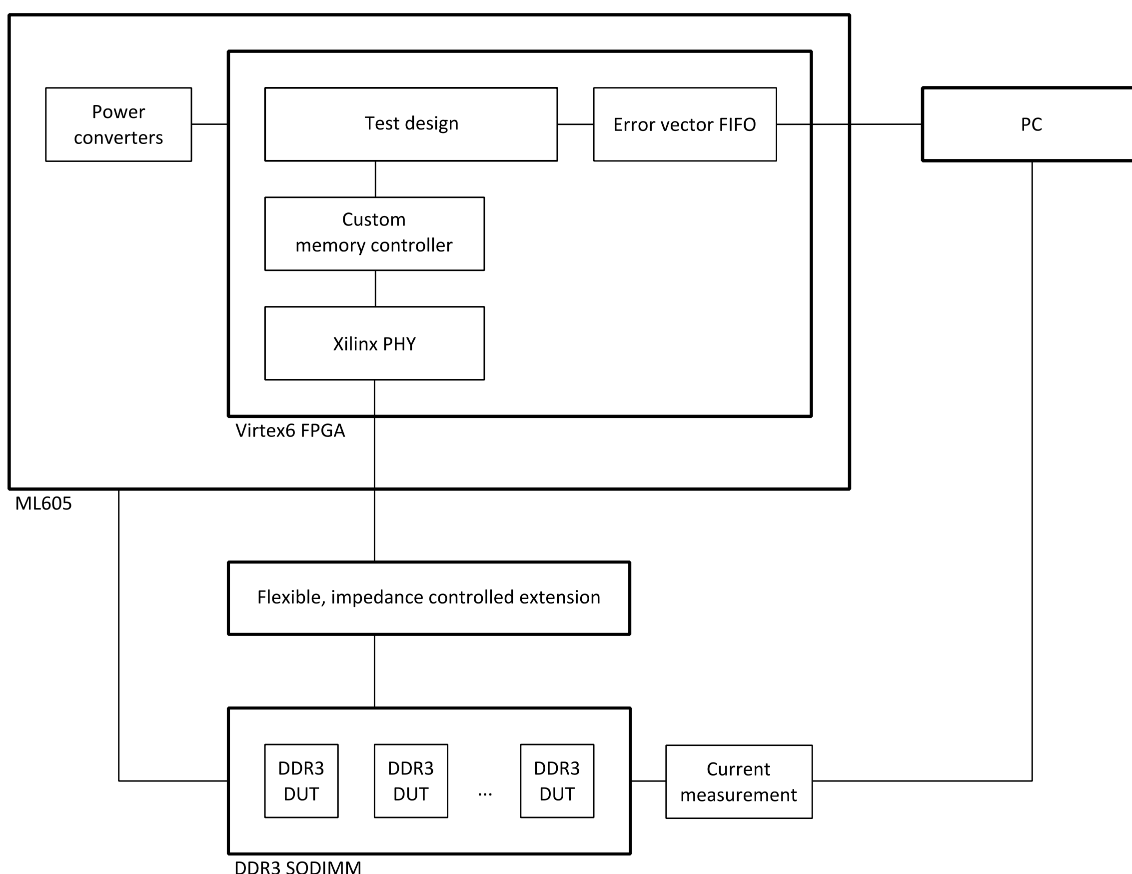

Figure 4-8: Simplified block diagram of RTMC-6 test bed (configuration with flexible extender for Protons and TID testing).

The FPGA contains a custom test design which writes a constant, counting or pseudo-random pattern to one of the DUTs, reads the data from the selected DUT and compares it to the original pattern. If the data is different from the pattern, an error vector is generated and transmitted to a PC via a high speed USB connection. Since the DUTs have a higher data transfer rate than the USB connection, error vectors are buffered in an on-FIFO in order to be able to handle large runs of consecutive errors without slowing down the test. If the error record FIFO runs full due to too many errors, error vectors are either discarded or the test is slowed down, at the user's choice. In the latter case, when the FIFO runs full, the test is stalled until enough error vectors have been transmitted to make sufficient space in the buffer, and then resumed.

On the PC, an error map is displayed for each DUT for preliminary visual analysis, along with a total error count and various statistics. The error vectors are stored for offline analysis.

The ML605 board is equipped with a small outline dual inline memory module (SODIMM) socket designed for commercially available memory modules. Since thinned devices cannot be soldered, a DUT adapter which connects to the SODIMM slot and contains a zero insertion force (ZIF) FBGA socket suitable for DDR3 SDRAM devices. The DUT adapter also contains circuitry for switching power to the DUT (Figure 4-9).

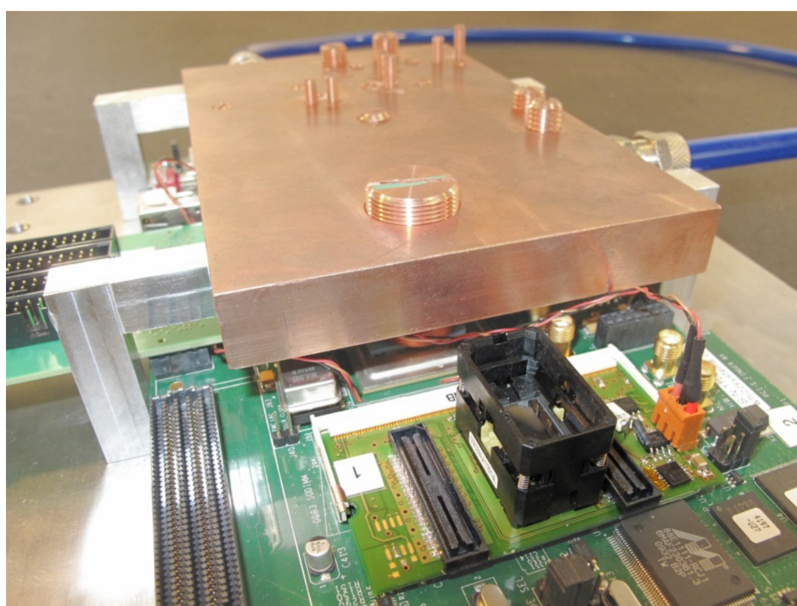

Figure 4-9: RTMC-6 head station with water cooler setup and opened DDR3 device in ZIF socket.

For test campaigns with shielding constrains i.e., TID and Protons testing a flexible extension for the SODIMM socket has been built to increase the distance of the DUTs to the sensitive control logic (Figure 4-10). Due to the common command bus for all devices on an SODIMM, all commands are issued to all DUTs simultaneously and the DUTs generally operate in unison. Writing to one DUT selectively is achieved by using the *data mask* (DM) signal individual to each DUT. The associated activate and precharge commands are still performed by all DUTs simultaneously. Reading from one DUT selectively is not possible, apart from discarding the data from the other DUTs.

The total supply current for the whole SODIMM is measured at a sampling rate of 16 Hz and is logged by the PC. The supply current for individual DUTs cannot easily be measured as this would require a modification of the SODIMM.

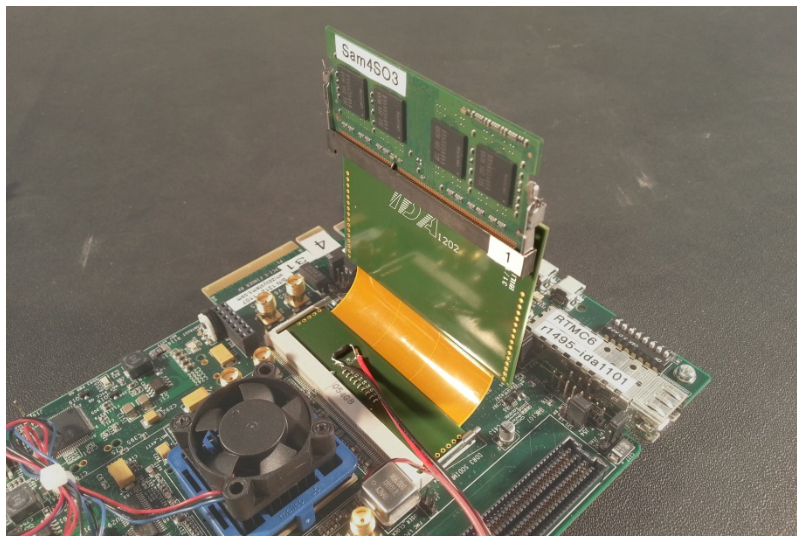

Figure 4-10: Flexible extension for SODIMM socket.

4.2.1.1 Memory Controller

An SDRAM controller consists of two parts (fig): the memory controller proper (MC), which interfaces with the user logic, and the physical interface (PHY), which interfaces with the SDRAM device. The MC is responsible for tracking the state of the DDR3 device and high-level timing. The PHY is responsible, among others, for low level (sub-clock-period) timing, data capturing and DDR translation. MC and PHY are connected via the DDR PHY interface (DFI).

As outcome of the 1st SEE test campaign (SEE_HI_1) a custom memory controller has been developed by IDA specifically for memory tests. It provides fine-grained control over the DUT and allows performing operations such as writing the mode registers, resetting the DLL of the DUT or calibrating the termination resistance at arbitrary times. Our controller implements an open page policy, which means that a row of the DRAM is kept open as long as possible after an access. In addition to simplifying the design, this policy has been shown to significantly increase DRAM performance. It is particularly efficient for highly localized access patterns, as is the case for memory testing.

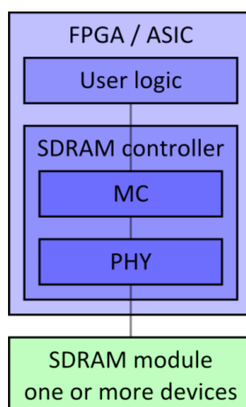

Figure 4-11: A typical design involving an SDRAM controller.

© Airbus DS GmbH

The custom built memory controller interfaces with the PHY developed by Xilinx and included in their Memory Interface Generator (MIG) package. A peculiarity of the Xilinx DDR3 PHY is that it requires a read access (to no particular location) at least every microsecond in order to maintain internal timing parameters. If the user logic does not perform enough read operations, a read operation called “periodic read”, or PRD, is initiated by the MC. The controller uses the address that currently happens to be applied to its inputs, which is typically the last address accessed by the user logic.

4.2.1.2 Cooling

The FPGA and the power regulators dissipate several watts of heat. For use in vacuum chambers or the TID shielding box, a water cooler has been devised consisting of a copper block placed above the board (Figure 4-9). The block is equipped with several threaded bolts to match the different heights of the various components to be cooled.

4.2.2 TID Test Equipment

In order to perform irradiation tests with a high total dose, all sensitive parts but the DUTs have to be shielded from the radiation. For this purpose, a flexible extension for the SODIMM socket and a shielding box made of lead (where space is critical) and steel has been built by IDA (Figure 4-12, Figure 4-13). The DDR3 SDRAM DUTs are shielded against electrons by a box made of 6mm acrylic glass between the Co-60 source and the DUTs (Figure 4-14).

The revised shielding box weights about 1000 kg and is assembled on-site from individual parts of about 10 kg to 20 kg each. It has several curved channels for feeding electrical wires and water tubes for the cooling system into the box.

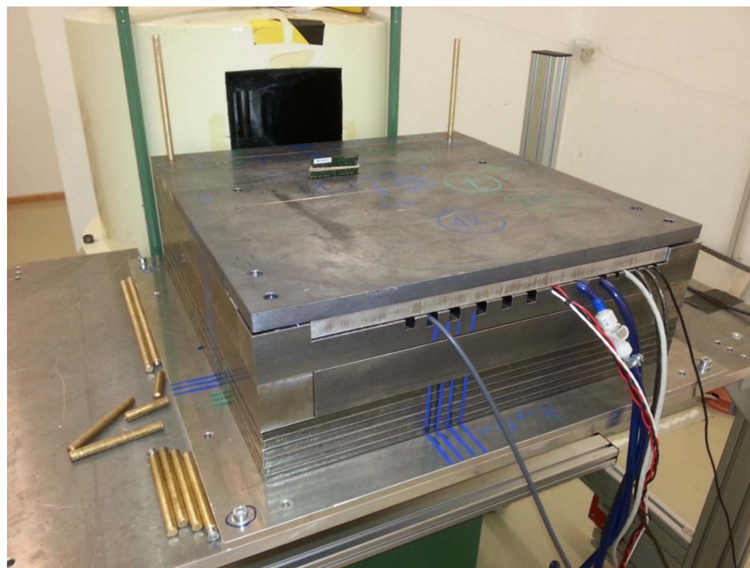

Figure 4-12: Shielding box for DDR3 SDRAM

© Airbus DS GmbH

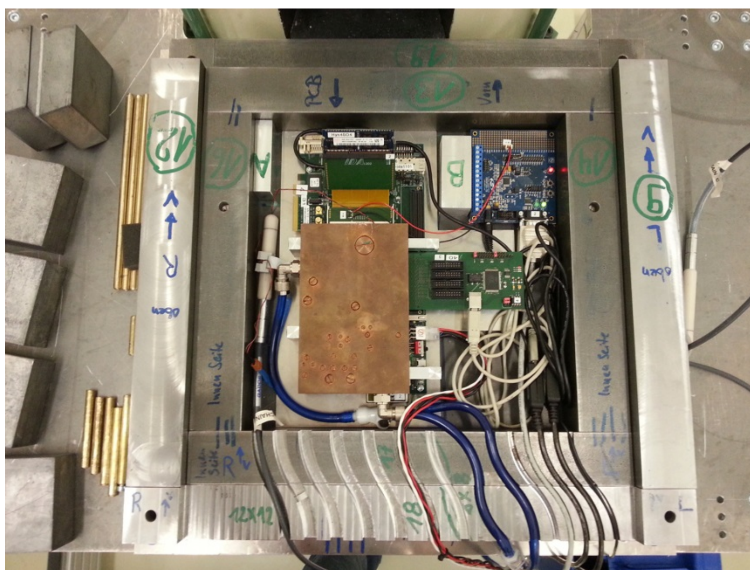

Figure 4-13: Head station inside the shielding box

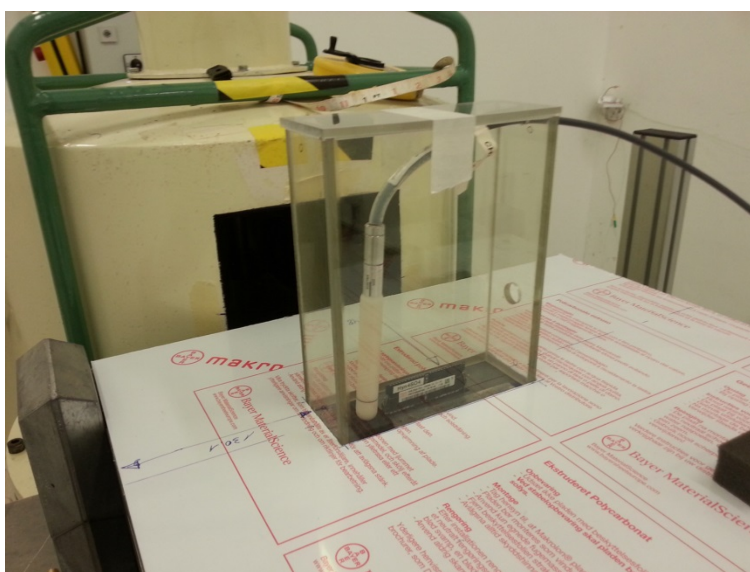

Figure 4-14: Acrylic class box shielding against electrons

4.2.3 Test Modes

The tests were performed with a pseudo-random pattern.

To retrieve static and dynamic data errors as well as more sophisticated data error patterns such as error clusters, and also SEFIs, three main test modes with several options each have been developed and were used:

- **Storage Mode (M3)**:
  Before irradiation a pattern is written into the DUT and verified. Default is the checkerboard pattern. After irradiation the content of the device is read and compared to the pattern. Only static data errors are delivered by this mode.

- **Read Mode (M2)**
  Before irradiation a pattern is written into the DUT and verified. During irradiation the content of the device is continuously read and verified.
- **Write/Read Mode (M1)**
  Before irradiation a pattern is written into the device and verified in order to determine SHE. During irradiation the DUT is continuously written and read and verified.

All test modes can be performed with and without *software conditioning*. Software conditioning consists in a configurable set of operations performed at regular time intervals (storage mode) or after a regular number of read/written pages (other modes). The available operations are:

- Rewriting the mode registers, containing the DUT configuration
- Resetting the DLL internal to the DUT
- Recalibrating the data line termination resistance (ZQ calibration)

4.2.4 Error Classification

Several error classes are distinguished, according to the overview shown in Figure 4-15:

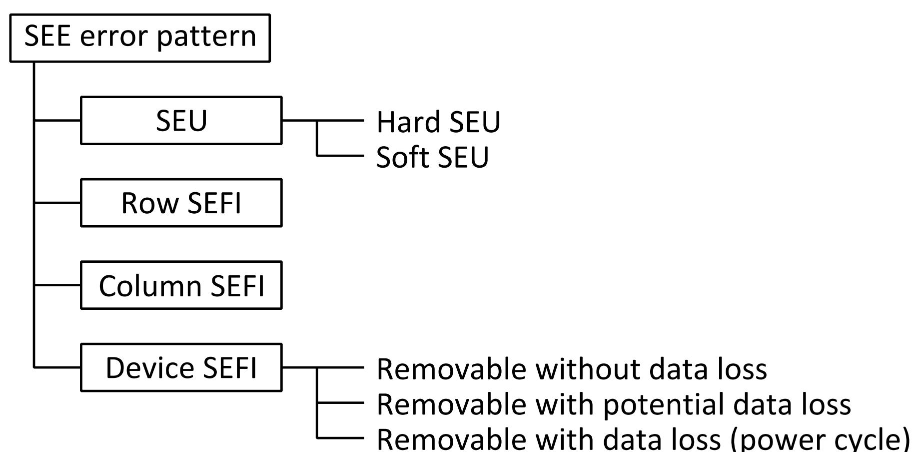

Figure 4-15: Applied error classification scheme.

- SEUs are isolated single-bit or multi-bit errors. In case of a (semi-)permanent upset of the memory cell i.e., if its state cannot be changed by writing the cell again, a Single Event Hard Error (stuck bit, "Hard SEU") occurred. All other SEUs are called here *soft SEUs*.
- Row SEFIs and column SEFIs are errors that corrupt a single row or column, respectively. The row or column may be corrupted completely or in part.
- Device SEFIs are errors that corrupt a whole device or an extended region of a device. Some device SEFIs can be removed by one of the operations that are also used for software conditioning. These operations do not result in data loss. Other device SEFIs can only be removed by resetting the DUT. The specification does not guaranteed data retention in this case, but in practice, no data loss has been observed. Some device SEFIs can only be removed by power cycling the DUT, which always causes data loss.

5 NAND Flash Characterisation

Several test campaigns on different NAND Flash devices were performed, four Heavy Ion SEE campaigns (SEE_HI_1 to SEE_HI_4), one high energy Protons SEE campaign (SEE_P_2) and one in-situ TID test campaign (TID_4). See Appendix A for further details.

5.1 SEE Heavy Ions Test Results

5.1.1 DUT Preparation

First, all DUTs were marked by an individual ID and were checked for factory marked bad blocks. The ID and the bad block table were programmed into block 0 which is guaranteed to be valid by the manufacturer for every DUT. These bad blocks were not accessed by erase or program operations anymore.

The 48-pin TSOP1 packages were opened for direct access of the ion beam to the surface of the die. In case of the Samsung 4 x 8 Gb device the package consists of 4 dies. During the test only the upper die is directly exposed to the ion beam. Therefore only this die is used for the test.

The opening yield of 25nm Micron devices is extremely low. For the 16 Gb DUTs a yield of 40% of fully opened dies was achieved. This is in line with the older 50nm 8 Gb Micron devices. In contrast to the old 51nm 8 Gb Samsung devices, there is only a small time window to get a fully opened die surface and a functional device. For the 32 Gb devices a yield of 0% of fully opened dies was achieved because in contrast to the previous 51nm Samsung and 50nm Micron NAND Flash generations, the new 25nm NAND Flash from Micron is packaged differently (Fig. 2 and Fig. 3 compared to Fig. 4 and Fig. 5). The complete opening of the 32 Gb Micron DUTs is extremely delicate because there is nearly no space between the die edges and the package rim on three of the four sides (Fig. 3). Because of the insufficient yield the Destructive Failure investigations were gained from the 16 Gb Micron device.

Figure 5-1 to Figure 5-4 show the orientation of the dies with respect to the opened TSOP1 package.

The opening is done by drop etching with fuming nitric acid. The device is placed on a mounting plate and is covered with Teflon tape. A window is cut into this tape. Then the device is heated to about 70°C, and an acid drop is given into the window. Thereafter the device is rinsed with water and then with acetone. This process of etching and rinsing is repeated many times until the die surface is free of plastic cover.

After the opening procedure the functionality check was repeated.

© Airbus DS GmbH

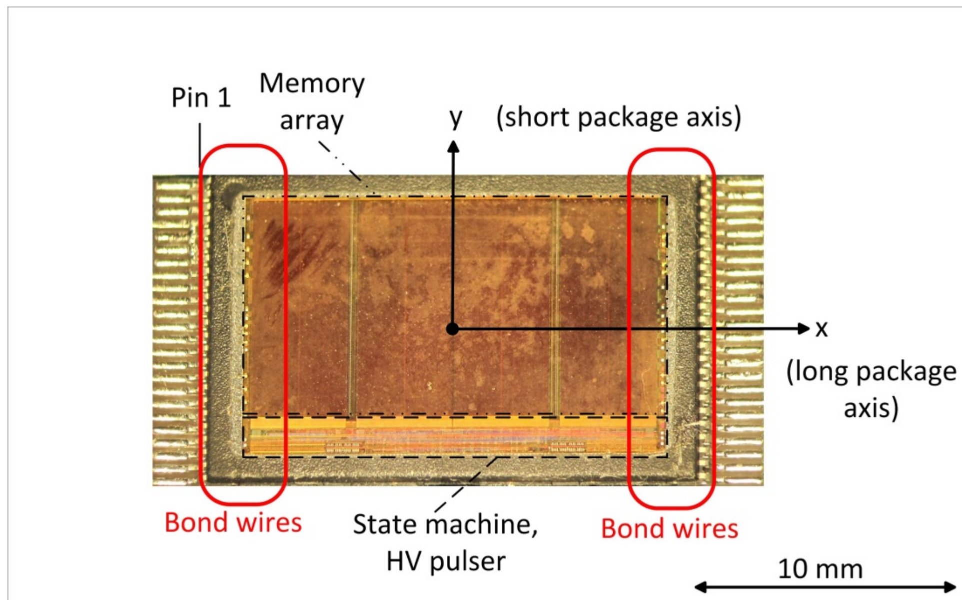

Figure 5-1: Die orientation of opened 51nm Samsung 4x8 Gb NAND Flash with bond wires on the small sides of the TSOP1 package

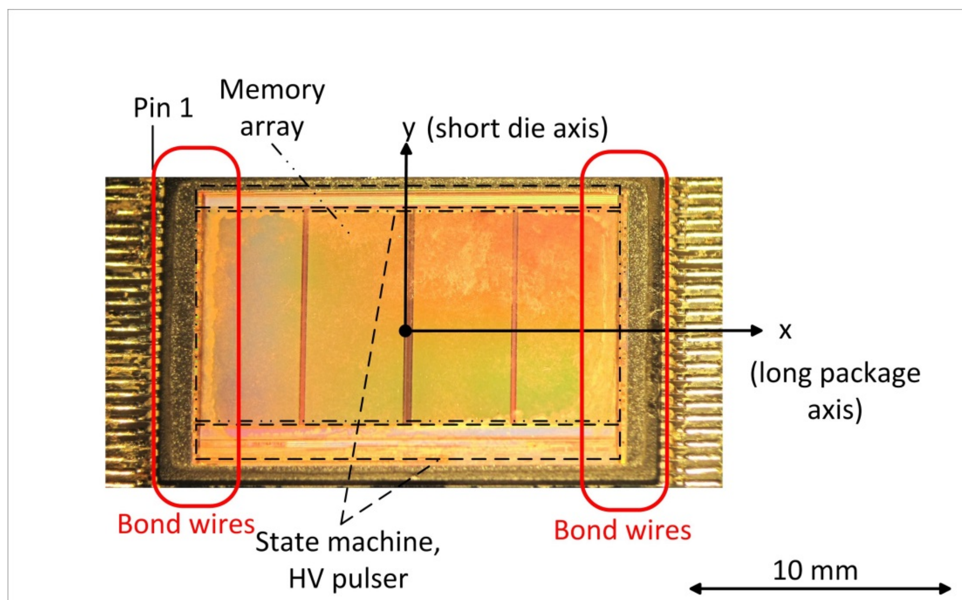

Figure 5-2: Die orientation of opened 50nm Micron 8 Gb NAND Flash with bond wires on the small sides of the TSOP1 package

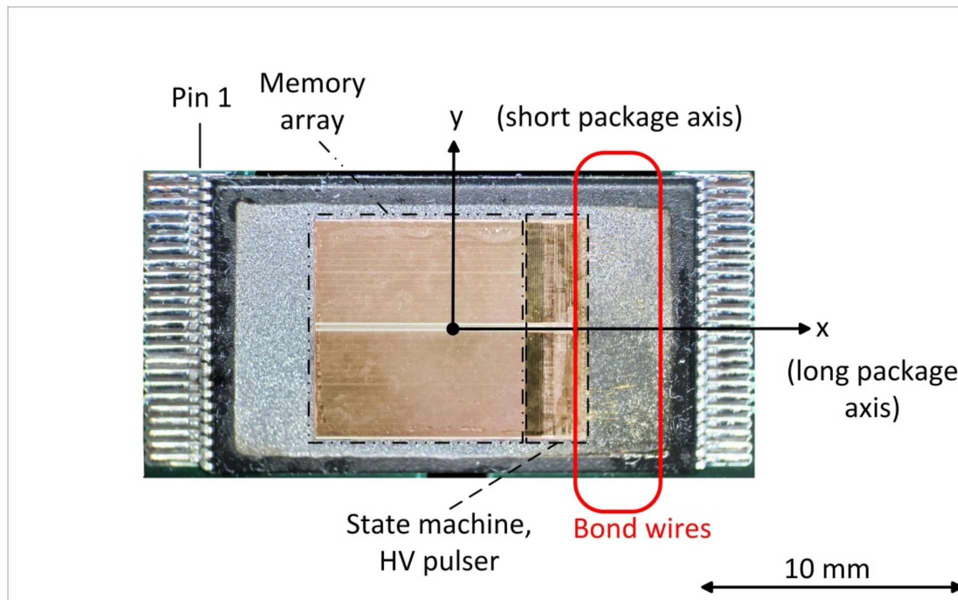

Figure 5-3: Die orientation of the opened 25nm Micron 16 Gb NAND-Flash

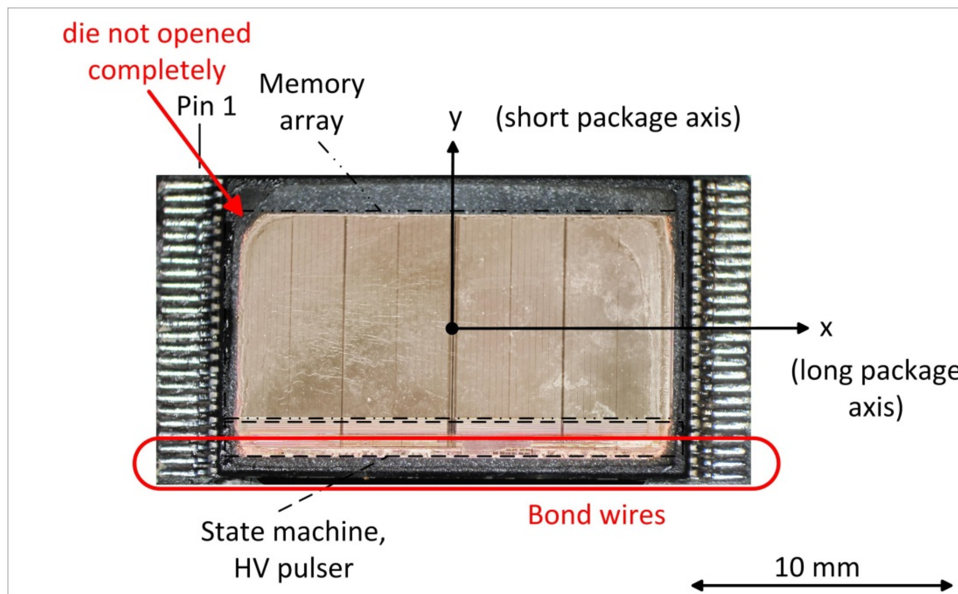

Figure 5-4: Die orientation of the opened 25nm Micron 32 Gb NAND-Flash.
Please note: die couldn't be opened completely without loosing function.

5.1.2 Samsung K9WBG08U1M (4 x 8 Gb)

Even though, these devices went already "End-of-Life", the quad die version of the Samsung 8 Gb SLC NAND flash in 51nm "M"-mask revision, the Samsung K9WBG08U1M 4x8 Gb, was used as reference. In former work, exhaustive test data were retrieved on these devices [RD-01], [RD-02]. Furthermore, the angular dependency of static SEU cross sections i.e., the shape of the sensitive volume was subjected for investigation as already in former campaigns, the applicability of the Cosine Law on these devices was questioned.

5.1.2.1 Investigations on static SEU cross-sections

As baseline for further investigations on the shape of the sensitive volume of the floating gate cell over 2π solid half space, the static cross section at azimuth $\Theta=0°$ and elevation $\Psi=0°$ were compared with former data. In Figure 5-5 the retrieved cross sections for static SEU from several test campaigns are provided. In Table 5-1 date codes and lot IDs of tested devices in the referenced campaigns are listed.

Table 5-1: List of used lots and the applied test campaigns

Manufacturer	Type	Mask	Package	DC	Lot #	Applied Tests
Samsung	K9F8G08U0M	M	Single	0725	1	RADEF 2007 [RD-01]
Samsung	K9WBG08U1M	M	Quad	0816	2 (FFC042X1)	RADEF 2008/04 [RD-01] RADEF 2011/05 [DD-02]
Samsung	K9WBG08U1M	M	Quad	0837	3	RADEF 2008/01 [RD-01]
Samsung	K9WBG08U1M	M	Quad	0837	4	RADEF 2008/04 [RD-01]
Samsung	K9WBG08U1M	M	Quad	0837	5 (FMH030X2)	RADEF 2011/05 [DD-02]
Samsung	K9WBG08U1M	M	Quad	0925	6 (FME071P2)	RADEF 2011/05 [DD-02] TAMU 2012/12 [DD-07]

Obviously, there was already a discrepancy between the published data on single die device [RD-01] and the quad die version [RD-02] though; both devices were using the same technology and mask revision. One could speculate, that through the thinning of the dies in the quad version to about 70µm compared to about 150µm for single die devices, the SEU response might be changed, i.e. improved. However, the thickness of the bulk substrate should have only a very limited impact on the sensitivity of the floating gate cells. Another explanation is the potential lot-to-lot variability of the devices. Nevertheless, in contrast to this theory results from two different campaigns on devices of the same lot differ by a factor of about 25 for medium LET of about 10 $MeVcm^2mg^{-1}$.

© Airbus DS GmbH

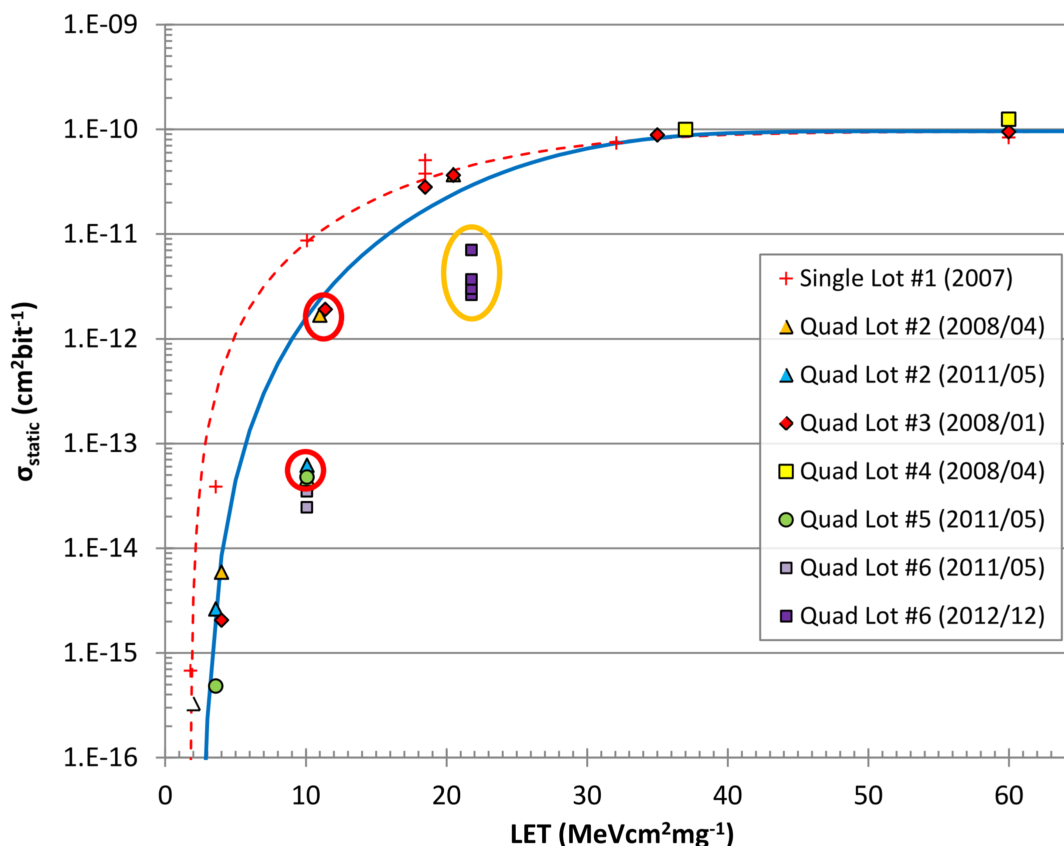

Figure 5-5: Retrieved cross-section data for static SEU (upsets in the memory cell area) for Samsung 8 Gb single die (K9F8G08U0M) and quad die (K9WBG08U1M) NAND flash memories; open symbols indicate “no event up to the applied fluence”.

According the summarized data in Figure 5-5, following observations could be stated:

1. There is a discrepancy between single die data [RD-01] and quad die data [RD-02], onset-LET and shape of the cross-section curves differ, the saturation cross-section is the same for all devices (in the order of 1E-10 cm^2bit^{-1}).
2. Data published in [RD-02] for three different lots and two different date codes, but all at the same test conditions are consistent
3. Cross sections retrieved in Test campaign SEE_HI_1 (RADEF 2011/05) are consistent to former data for low LET (about 4 $MeVcm^2mg^{-1}$); there is a big gap for LET of about 10 $MeVcm^2mg^{-1}$ even though, for the same lot #2 as tested in [RD-02] before. However, the data on three different lots within this campaign fit well together.
4. Cross sections retrieved in Test campaign SEE_HI_4 (TAMU 2012/12) for LET of 21.8 $MeVcm^2mg^{-1}$ differ by a factor of about 10 roughly to the former retrieved cross-sections.

© Airbus DS GmbH

5.1.2.2 Investigations on the angular dependency of static SEU

Exhaustive studies on the angular dependency of static SEU i.e. memory cell upsets have been performed by IDA prior this study. The results were published in [PD-01] and [PD-02]. For Rad Hard Memory study the elaborated test equipment built by IDA has been improved to get a better symmetric alignment. It is capable to rotate the DUT in azimuth Θ and elevation Ψ [DD-02] (see §4.1.1).

Further tests were performed at RADEF with Ar (LET1=10.1 $MeVcm^2mg^{-1}$) at SEE_HI_1 campaign and at TAMU with Kr (LET=21.8 $MeVcm^2mg^{-1}$) at SEE_HI_4 campaign. The polar diagrams relative to normalized SEU cross section at azimuth Θ=0° and elevation Ψ=0° are provided in Figure 5-6 for Ψ=15°…60° and in Figure 5-7 for Ψ≥60° for Ar (SEE_HI_1) and for Ψ=60°…75° in Figure 5-8 and Ψ≥75° in Figure 5-9 for Kr (SEE_HI_4) respectively.

For elevation angles below 60° at Ar respectively below 75° at Kr the resulting static cross sections remains within the cross section value at normal incidence. For higher elevation angles a quite characteristic dipole shape was retrieved. At elevation Ψ=85°, the dipole shape grows along the long axis of the die (Θ=0° and Θ=180°). For Ar (LET=10.1 $MeVcm^2mg^{-1}$) the maximum cross sections of about seven times the cross section at normal incidence were retrieved at Θ=±45°. At higher LET i.e., Kr (LET=21.8 $MeVcm^2mg^{-1}$) the dipole shape is more flat, the maximum cross section along the long axis is about four times the cross section at nominal incidence.

Additionally to the tests at Ar, tests at Kr (LET=32.1 $MeVcm^2mg^{-1}$) have been performed at RADEF at SEE_HI_1 campaign. Nevertheless, most likely due to the limited ion range of about 94 µm compared to about 118µm at Ar the characteristic dipole shape was not retrieved for higher elevation angles. In Figure 5-10 the polar diagram for elevation Ψ=45°…85.5° is provided.

© Airbus DS GmbH

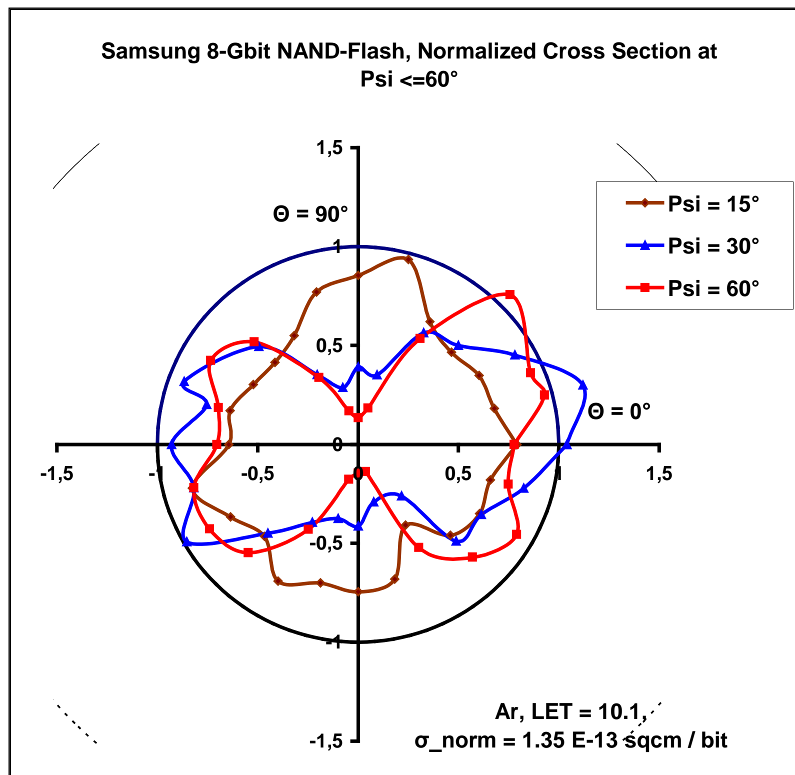

Figure 5-6: Normalized static SEU cross sections, Ψ ≤ 60° at Ar (LET=10.1 $MeVcm^2mg^{-1}$), Samsung 4x8 Gb K9WBG08U1M NAND Flash memory, RADEF

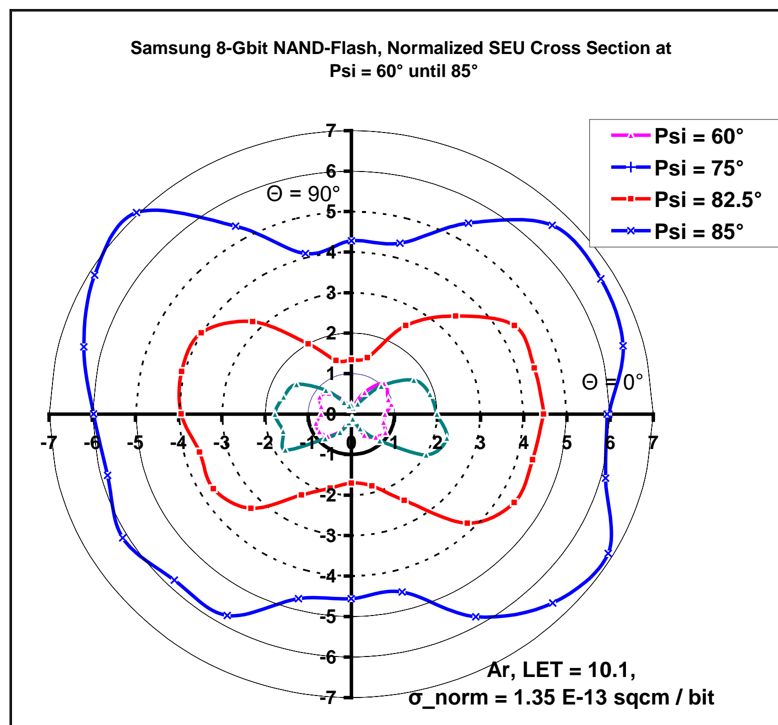

Figure 5-7: Normalized static SEU cross sections, Ψ ≥ 60° at Ar (LET=10.1 $MeVcm^2mg^{-1}$), Samsung 4x8 Gb K9WBG08U1M NAND Flash memory, RADEF

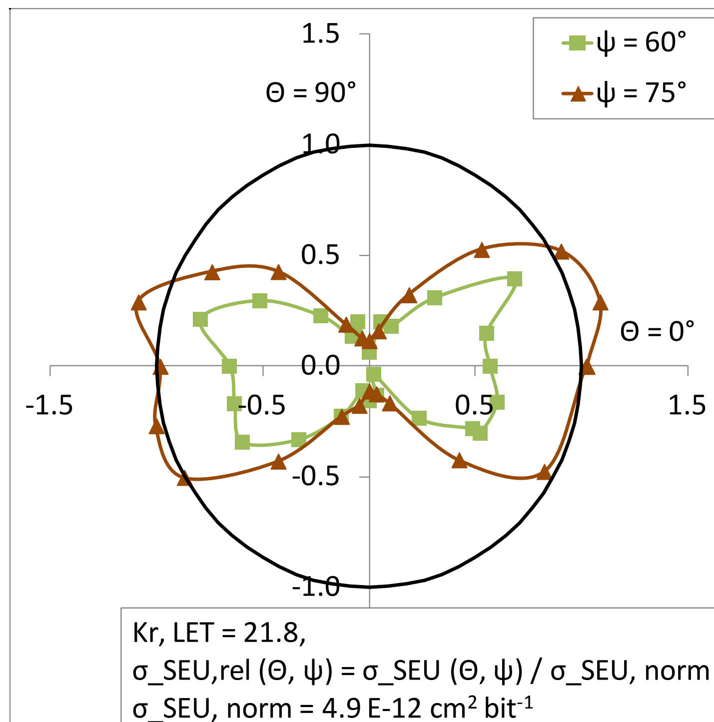

Figure 5-8: Normalized static SEU cross sections, Ψ 60°…75°, at Kr (LET=21.8 MeVcm^{2}mg^{-1}), Samsung 4x8 Gb K9WBG08U1M NAND Flash memory, TAMU

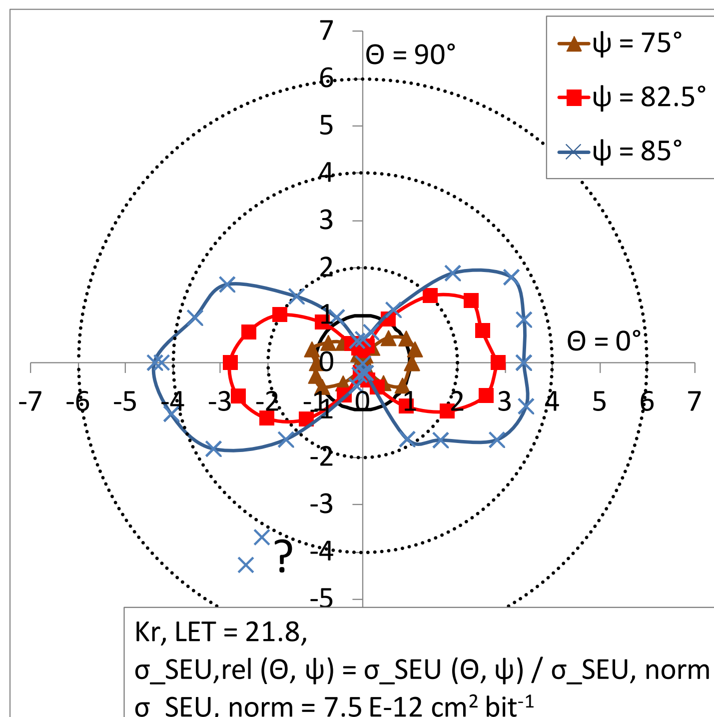

Figure 5-9: Normalized static SEU cross sections, Ψ ≥ 75°, at Kr (LET=21.8 MeVcm^{2}mg^{-1}), Samsung 4x8 Gb K9WBG08U1M NAND Flash memory, TAMU

© Airbus DS GmbH

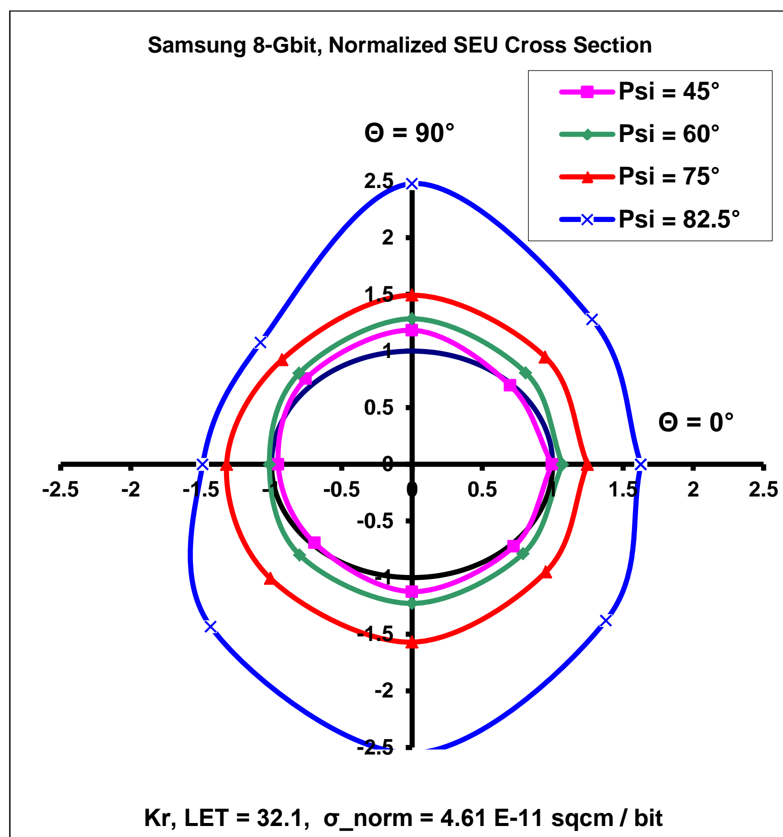

Figure 5-10: Normalized static SEU cross sections, Ψ ≥ 45°, at Kr (LET=32.1 $MeVcm^2mg^{-1}$), Samsung 4x8 Gb K9WBG08U1M NAND Flash memory, RADEF

5.1.3 Micron MT29F8G08AAAWP-ET:A

Additionally to the 4 x 8 Gb reference devices from Samsung, 8 Gb SLC NAND flash of the same technology step (50nm feature size) from Micron has been investigated.

5.1.3.1 Investigations on the angular dependency of static SEU

Compared to former test campaigns by IDA, the symmetry of the retrieved cross section curves to the axis have been improved with the upgraded test equipment, especially for elevation angles Ψ > 75°. For high elevation angles Ψ = 82.5° and Ψ = 85° many 2-bit errors could be observed for Θ = 0° and Θ = 180° i.e., in case of parallel alignment of the beam to the long axis of the DUT.

At Ψ ≤ 60°, i.e. for one half of the hemisphere, the cross section remains for all azimuth angles Θ below its value for normal incidence. With the increase of the elevation angle from Ψ = 0 to Ψ = 60° the cross section for incidence in parallel to the long die axis (Θ = 0) remains nearly unchanged. In contrast the cross section for incidence along the short die axis drops with increasing elevation angle Ψ ψ to about 30% of its value at normal incidence. The polar diagram is shaped similar to that of a dipole antenna.

At larger elevation angles (ψ = 75°, 82.5°, 85°) the diagram expands. It remains its elongation for incidence in parallel to the long die axis. At ψ =85° the cross section exceeds at all azimuth angles its

value for normal incidence, but for all azimuth angles Θ by less than a factor of two. As we will see later on, this makes a significant difference between the Micron and the Samsung device.

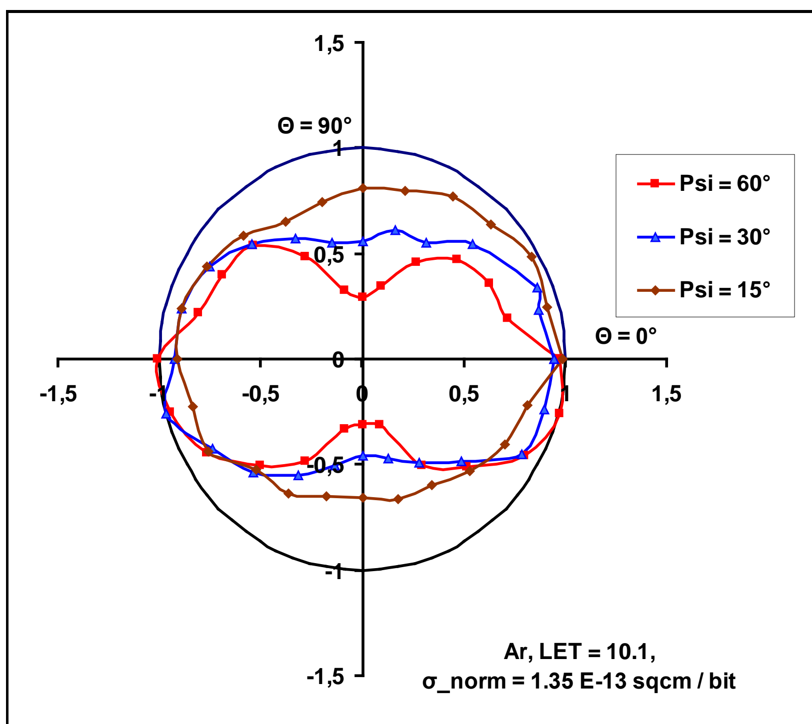

Figure 5-11: Static SEU cross section diagram, elevation angles Ψ ≤ 60°

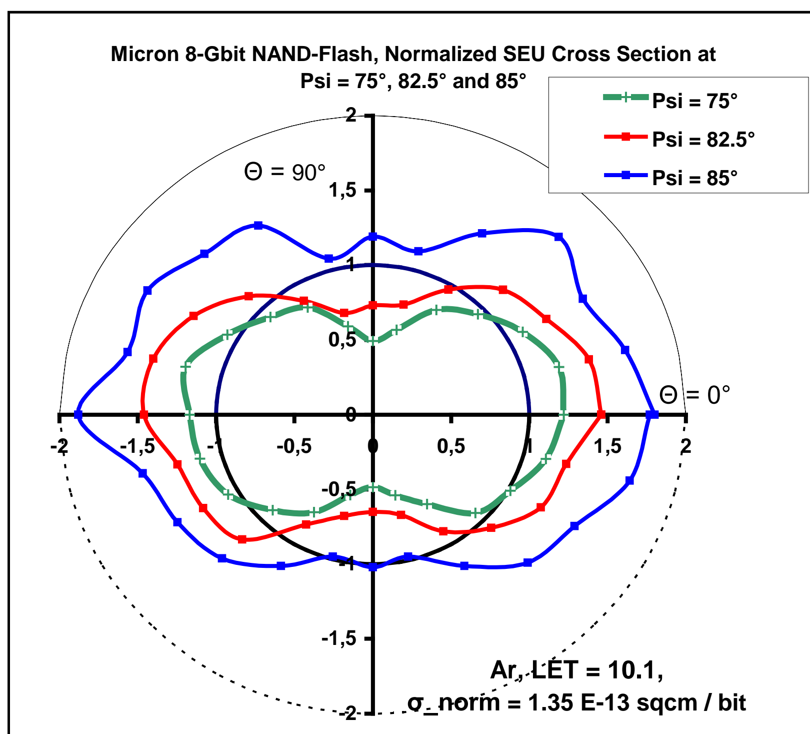

Figure 5-12: Static SEU cross section diagram, elevation angles Ψ ≥ 75°

5.1.4 Micron MT29F16G08ABACAWP-IT:C (16 Gb) & MT29F32G08ABAAAWP-IT:A (32 Gb)

At start of this study, no data on the Micron SLC NAND Flash devices in 25nm technology were published. An exhaustive SEE characterisation including SEU, SEFI and destructive failures, have been performed within this study in three campaigns (HI_SEE_2 to HI_SEE_4). In the meanwhile, there are some additional data published by JPL/NASA in [RD-04] and [RD-05].

5.1.4.1 Static SEU

The SEU cross section (static errors) of 16 Gb and 32 Gb Micron devices have been mainly characterized in the two RADEF SEE campaigns (HI_SEE_2 and HI_SEE_3). In general, the SEU cross sections of the 16 Gb and 32 Gb devices fit well together.

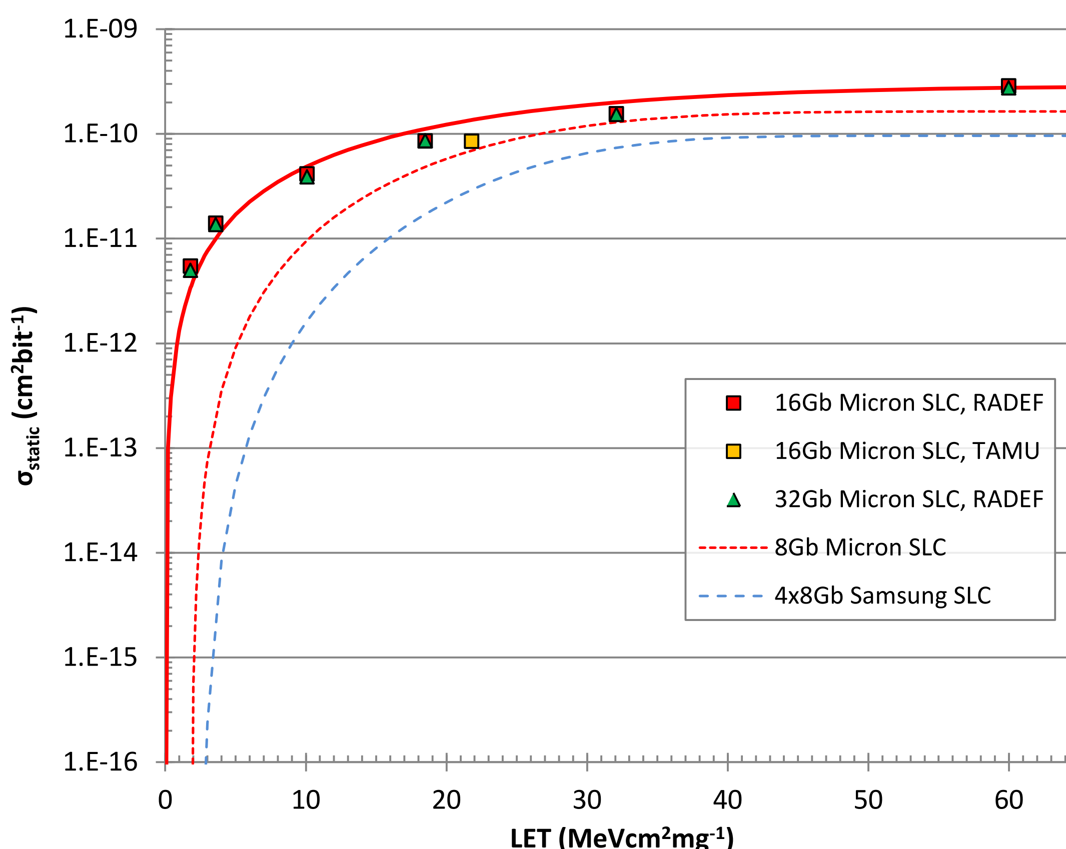

Figure 5-13: Static SEU cross sections for Micron 16 Gb and 32 Gb NAND Flash devices in 25nm feature size compared to Micron 8 Gb devices in 50nm feature size (red dotted line) and Samsung 4x8 Gb devices in 51nm feature size (blue dotted line).

In Figure 5-13 the retrieved cross sections for static SEU are provided. They fit well to the published data in [RD-04] and [RD-05] for LET ≥ 20 MeVcm^{2}mg^{-1}, but at low LET there is a difference by up to two orders of magnitude for unknown reason.

The area of the 16 Gb device is about 0.9 cm^2 i.e., $5.24 \cdot 10^{-11}$ cm^2 bit^{-1} = (72nm)^2 bit^{-1}. The measured static SEU cross section exceeds this value, even at LET = 10 MeVcm^{2}mg^{-1}. This indicates that single hits can induce multiple static SEU i.e. MBU. The inspection of the error records revealed that, in most

of the cases, the same bit in the same byte of adjacent rows is corrupted. MBU in the same byte are rare. With increasing LET the number of measure stuck-bits (SHE) is increasing. At Xe (LET=60 $MeVcm^2mg^{-1}$) about 20% of measured SEU were SHE (see [DD-05] for details).

5.1.4.2 Omnidirectional static SEU cross sections

Additional to the SEU characterisation at normal incidence at RADEF (SEE_HI_2 & SEE_HI_3) investigations on the angular dependency of static SEU has been performed on the 16 Gb Micron SLC NAND Flash at TAMU (SEE_HI_4) at Kr (LET=21.8 $MeVcm^2mg^{-1}$). Analogue to Samsung 4x8 Gb device omnidirectional SEU cross sections have been retrieved for elevation angles Ψ = 60° and Ψ =82.5°, see Figure 5-14 and Figure 5-15. In contrast to Samsung devices, the effect of tilting is less significant. Also at slant ion incidence (Ψ = 82.5°, Fig. 11) the SEU cross section remains near the normal incidence circle.

Furthermore, the Micron device shows MBUs also at normal ion incidence. At slant ion incidence (Ψ = 82.5°) there are different and new effects.

For example at Θ = 0° MBUs have been observed with errors in the same byte address and different page addresses with a mean length of 10 errors. For Θ = 90° only a small amount of MBUs up to a length of 4 have been measured. Nevertheless, clusters of up to 4 falsified bits inside the same byte were observed. For further details see [DD-10].

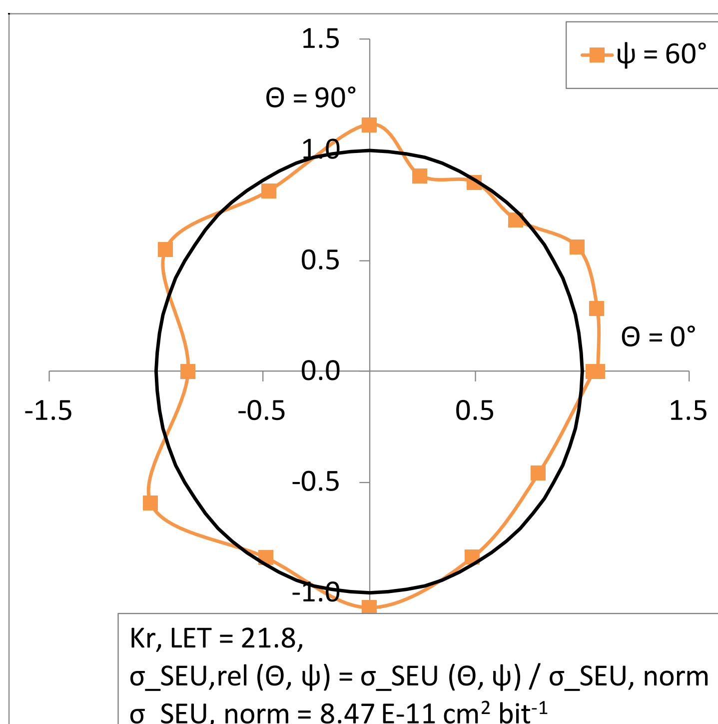

Figure 5-14: Normalized SEU cross section, ψ = 60°, Micron 16 Gb NAND-Flash.

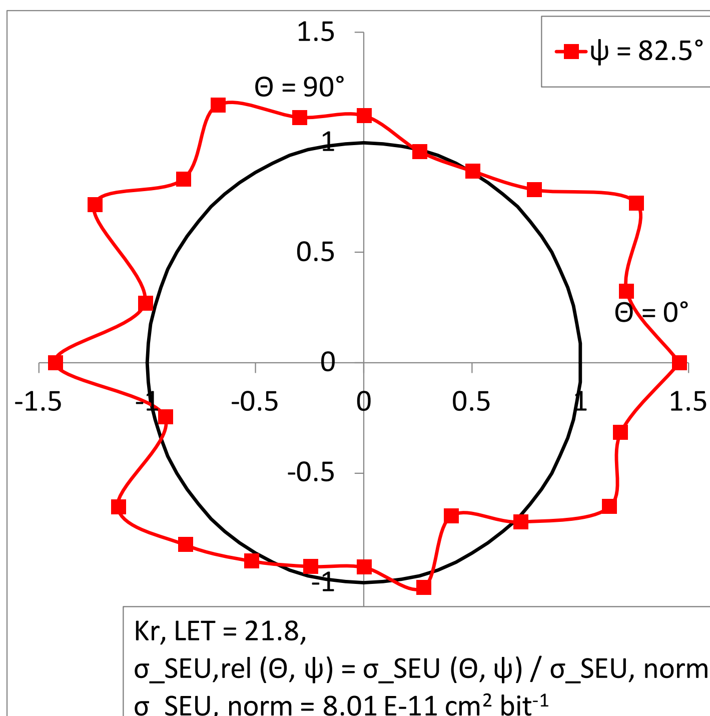

Figure 5-15: Normalized SEU cross section, ψ = 82.5°, Micron 16 Gb NAND-Flash

5.1.4.3 SEFI

SEFI cross sections have been measured individually for each of the dynamic test modes. In contrast to former generations e.g., the Samsung 4x8 Gb devices the impact on the operating mode on the resulting SEFI cross sections is rather low. There is almost no difference between the Marching Mode without any power cycling (M1) and the Marching Mode with intermediate power cycling (M5).

First SEFI were already observed at lowest used LET=1.8 (Column Errors in M5). All other SEFI occurred starting with LET=3.6 $MeVcm^2mg^{-1}$. For former generation devices i.e. Samsung 4x8 Gb SLC NAND Flash the onset LET for any SEFI was >11 $MeVcm^2mg^{-1}$.

The measured cross sections for transient SEFI (Class B) in Read Mode M2R are provided in Figure 5-16 to Figure 5-19, the measured cross sections for persistent SEFI (Class C) in M2R in Figure 5-20 to Figure 5-23. Due to the much larger time needed for both marching modes only a shorter address range could be tested - resulting in lower count of SEFI. Hence, the counts for Class B and Class C SEFI were combined in the cross section diagrams. For Marching Mode M5 the combined Class B & Class C SEFI cross sections are provided in Figure 5-25 to Figure 5-29, and for Marching Mode M1 (without power cycling) in Figure 5-30 to Figure 5-32.

Read Mode M2R

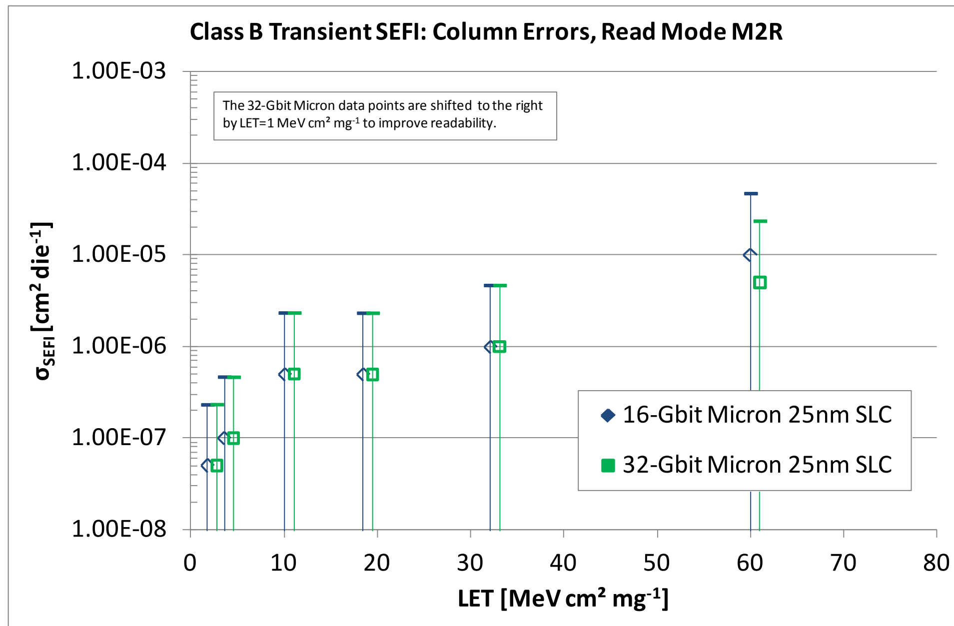

Figure 5-16: Class B Transient SEFI cross section in read mode M2R, Column Errors;, open symbols indicate “no event up to the applied fluence”.
Please note: no column errors where observed.

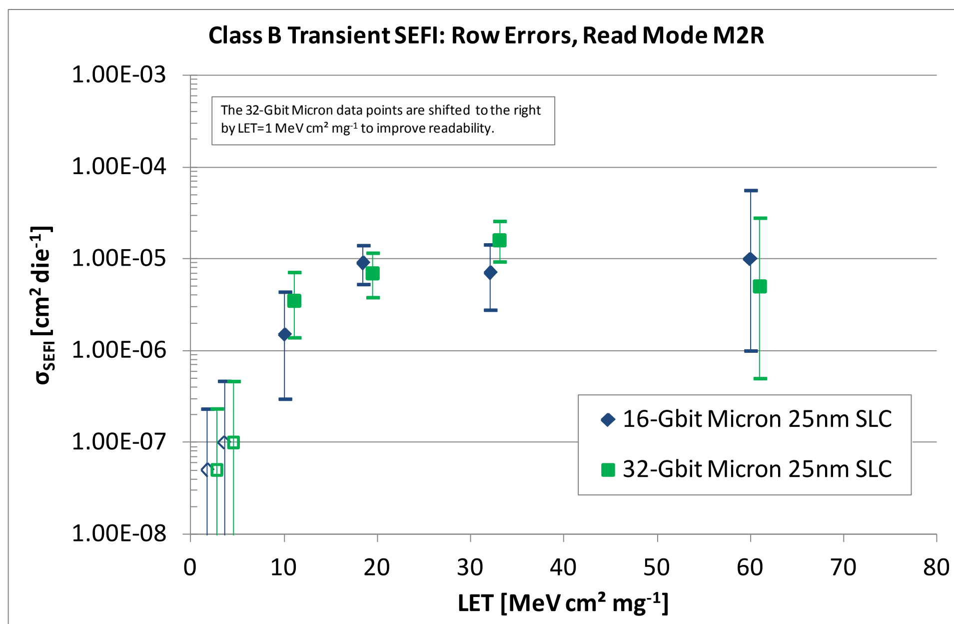

Figure 5-17: Class B Transient SEFI cross section in read mode M2R, Row Errors; open symbols indicate “no event up to the applied fluence”.

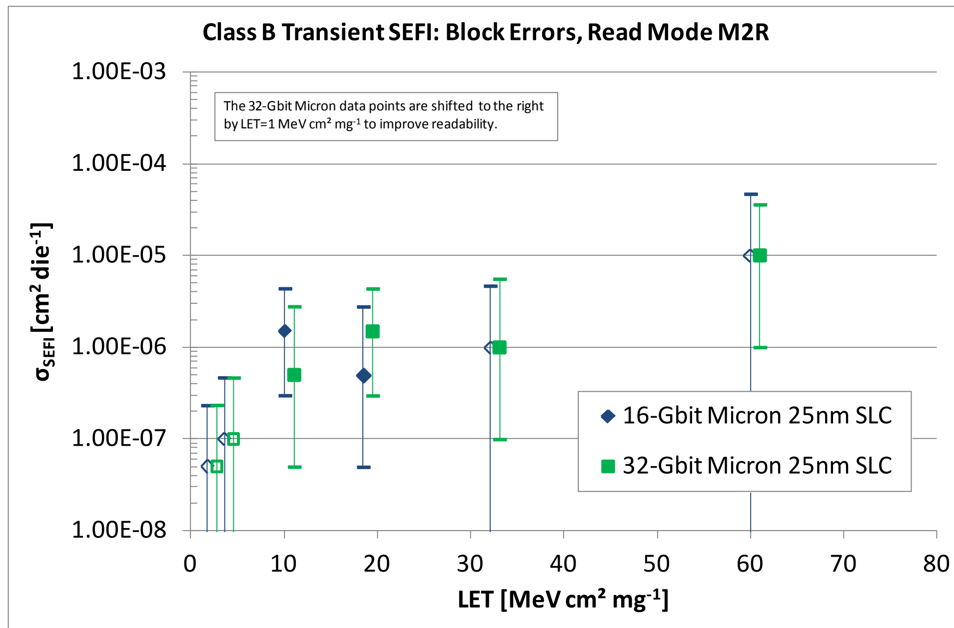

Figure 5-18: Class B Transient SEFI cross section in read mode M2R, Block Errors; open symbols indicate “no event up to the applied fluence”.

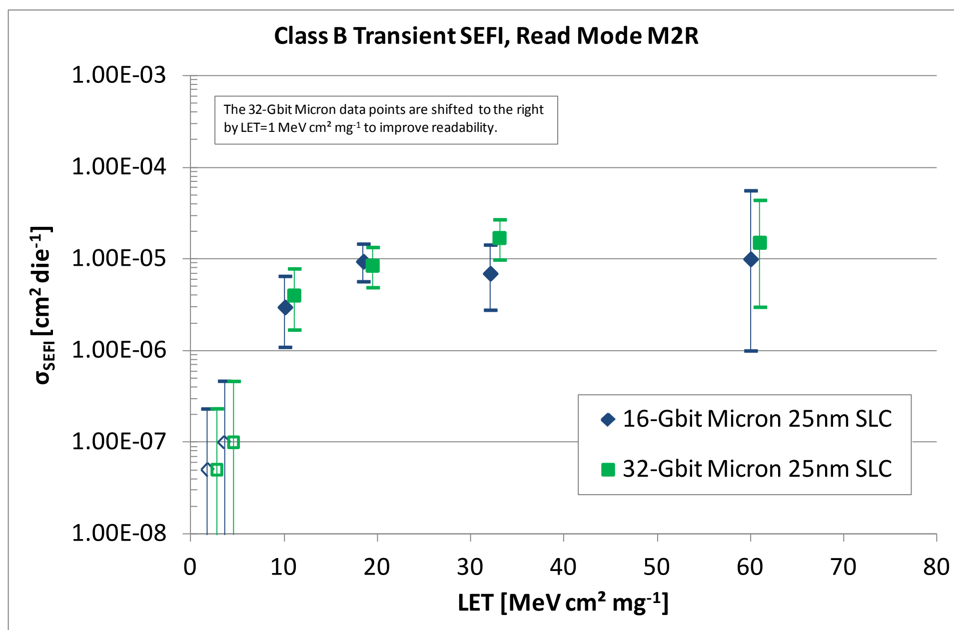

Figure 5-19: Class B Transient SEFI cross section in read mode M2R, all Class B SEFI; open symbols indicate “no event up to the applied fluence”.

© Airbus DS GmbH

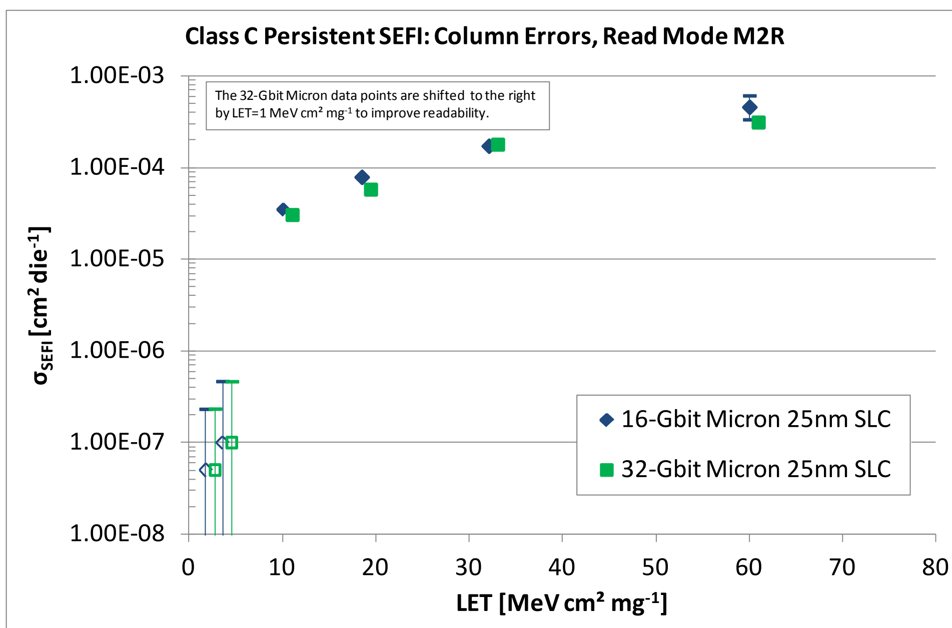

Figure 5-20: Class C Persistent SEFI cross section in read mode M2R, Column Errors; open symbols indicate “no event up to the applied fluence”.

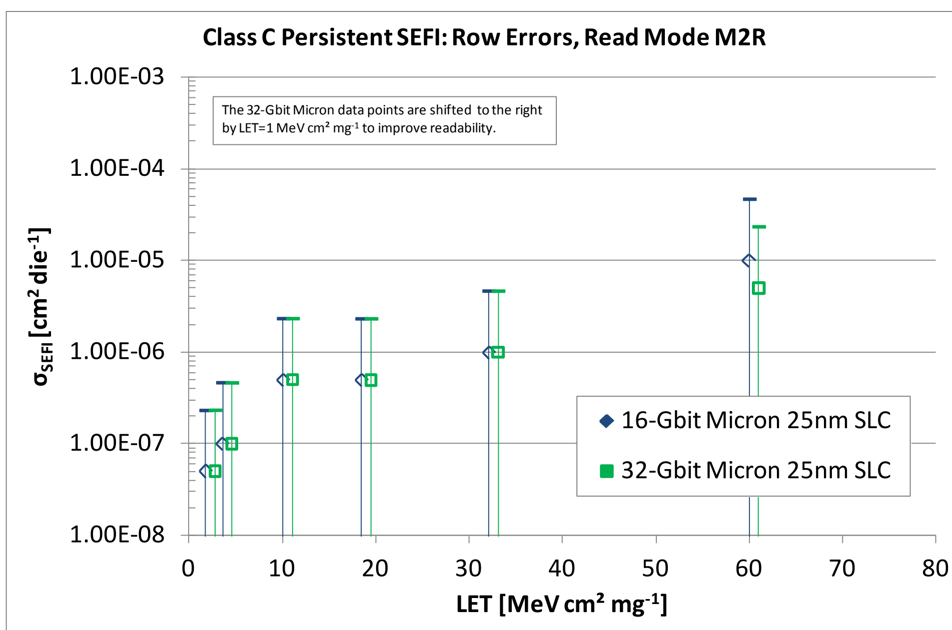

Figure 5-21: Class C Persistent SEFI cross section in read mode M2R, Row Errors; open symbols indicate “no event up to the applied fluence”.
Please note: no row errors where observed.

© Airbus DS GmbH

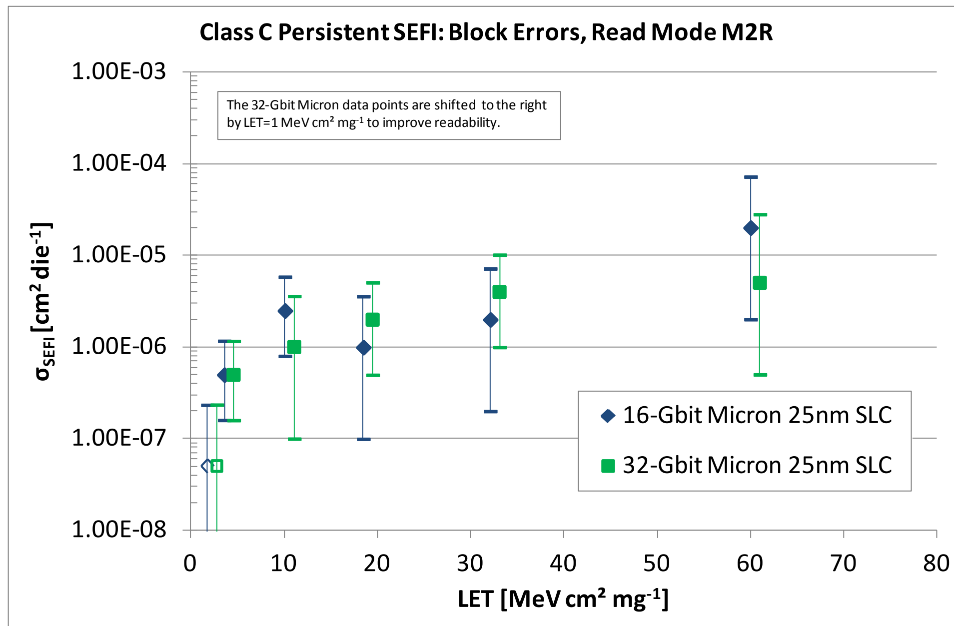

Figure 5-22: Class C Persistent SEFI cross section in read mode M2R, Block Errors; open symbols indicate “no event up to the applied fluence”.

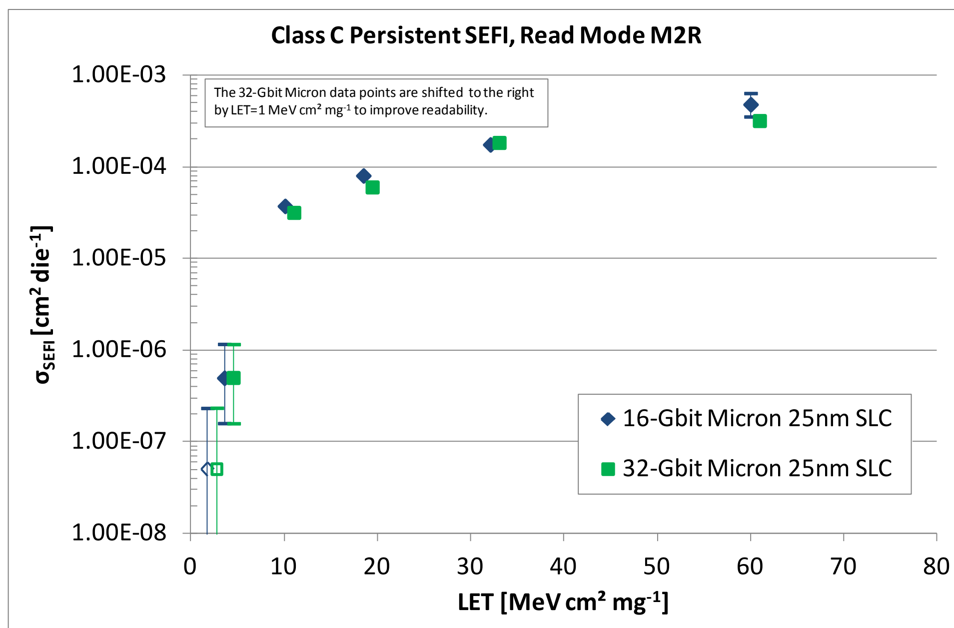

Figure 5-23: Class C Persistent SEFI cross section in read mode M2R, all Class C SEFI; open symbols indicate “no event up to the applied fluence”.

© Airbus DS GmbH

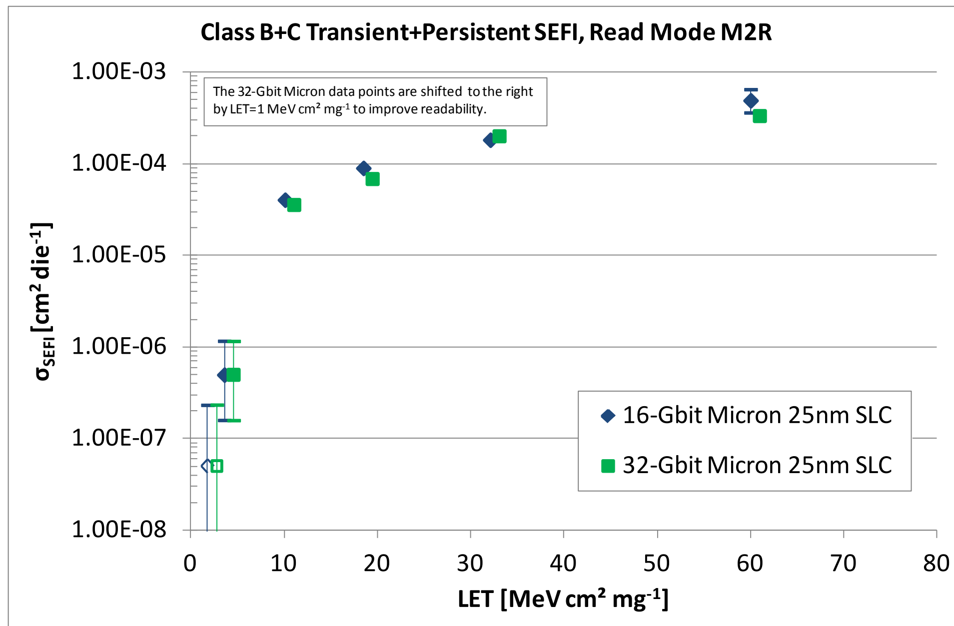

Figure 5-24: Class B+C Transient & Persistent SEFI cross section in read mode M2R, all SEFI; open symbols indicate “no event up to the applied fluence”.

Marching Mode M5

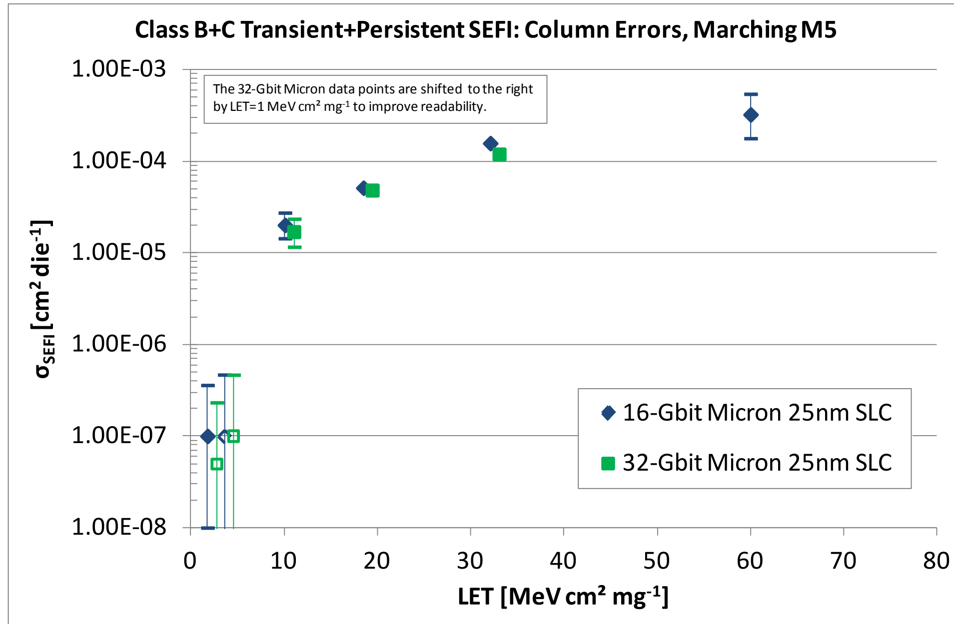

Figure 5-25: Class B+C Transient & Persistent SEFI cross section in marching mode M5, Column Errors; open symbols indicate “no event up to the applied fluence”.

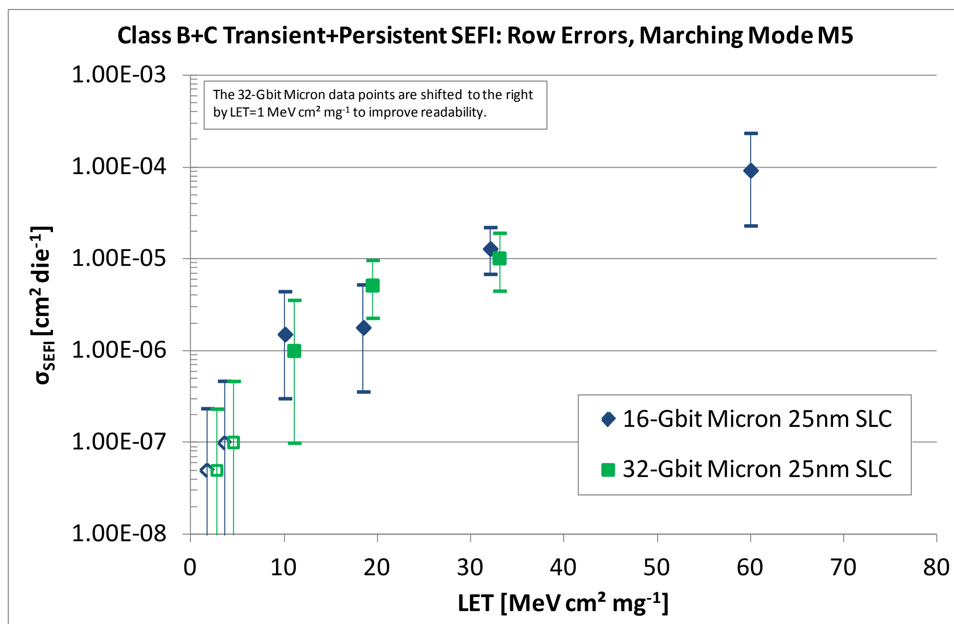

Figure 5-26: Class B+C Transient & Persistent SEFI cross section in marching mode M5, Row Errors; open symbols indicate “no event up to the applied fluence”.

© Airbus DS GmbH

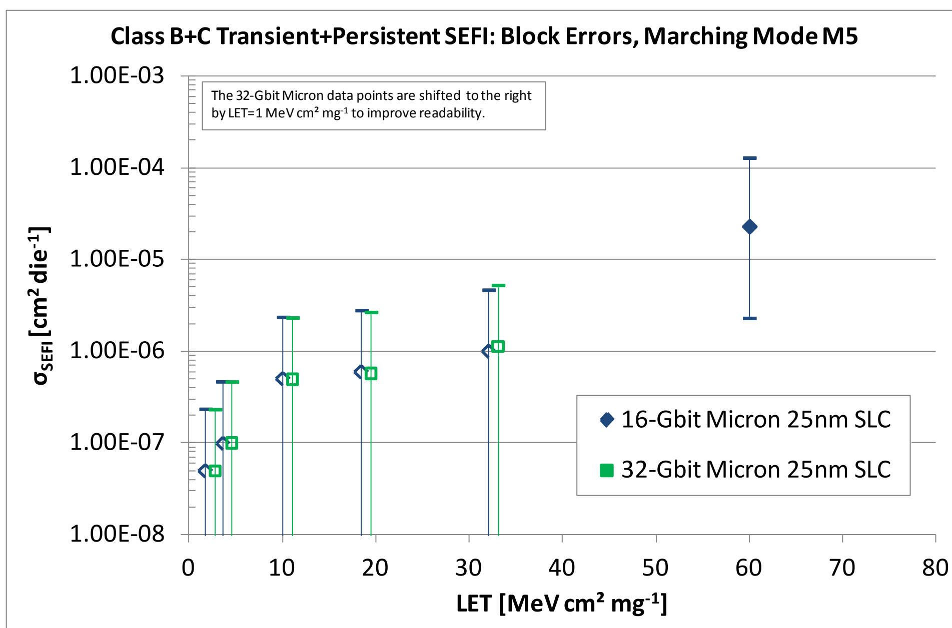

Figure 5-27: Class B+C Transient & Persistent SEFI cross section in marching mode M5, Block Errors; open symbols indicate “no event up to the applied fluence”.

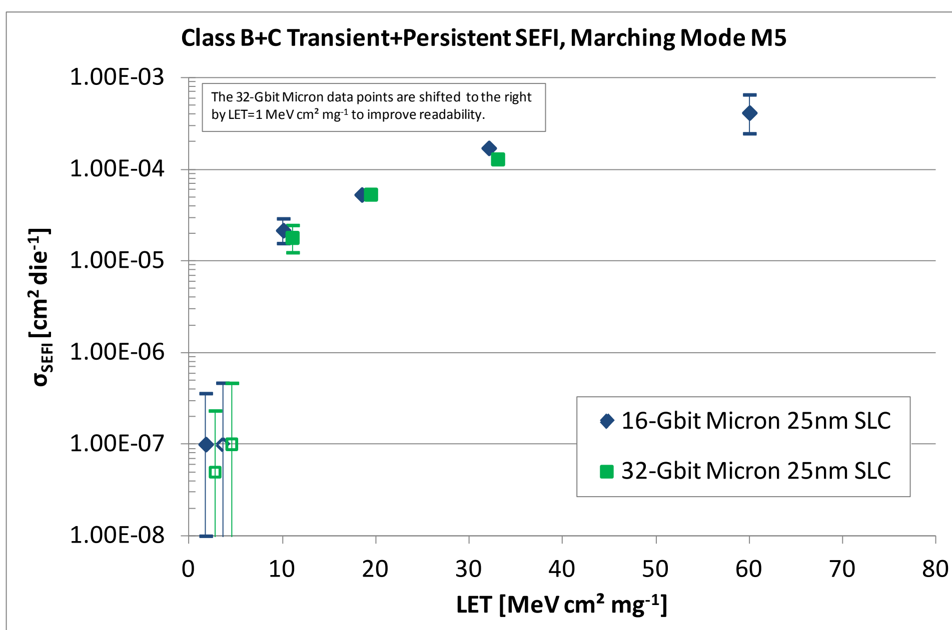

Figure 5-28: Class B+C Transient & Persistent SEFI cross section in marching mode M5, all SEFI; open symbols indicate “no event up to the applied fluence”.

Marching Mode M1

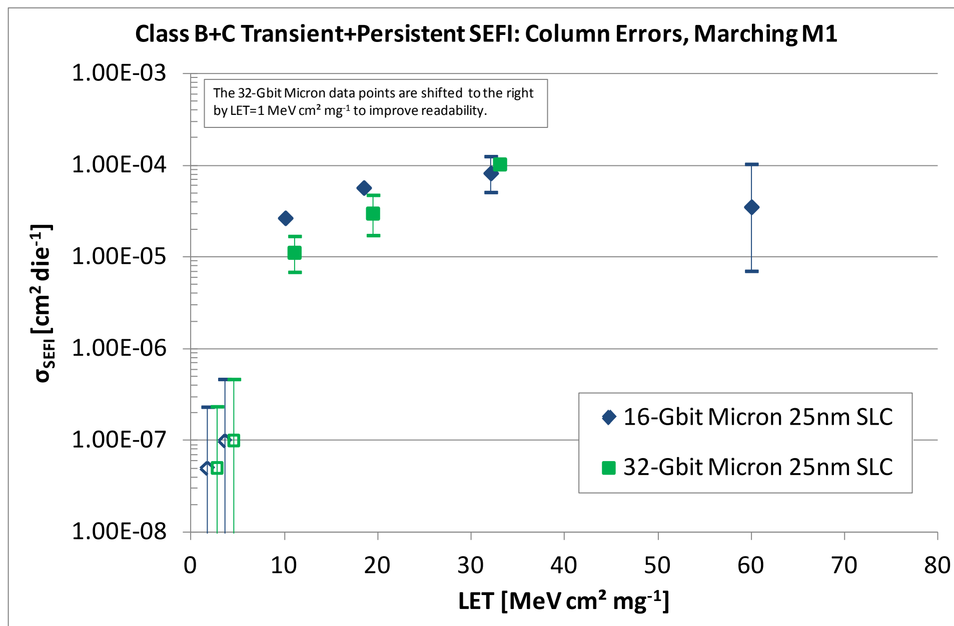

Figure 5-29: Class B+C Transient & Persistent SEFI cross section in marching mode M1, Column Errors; open symbols indicate “no event up to the applied fluence”.

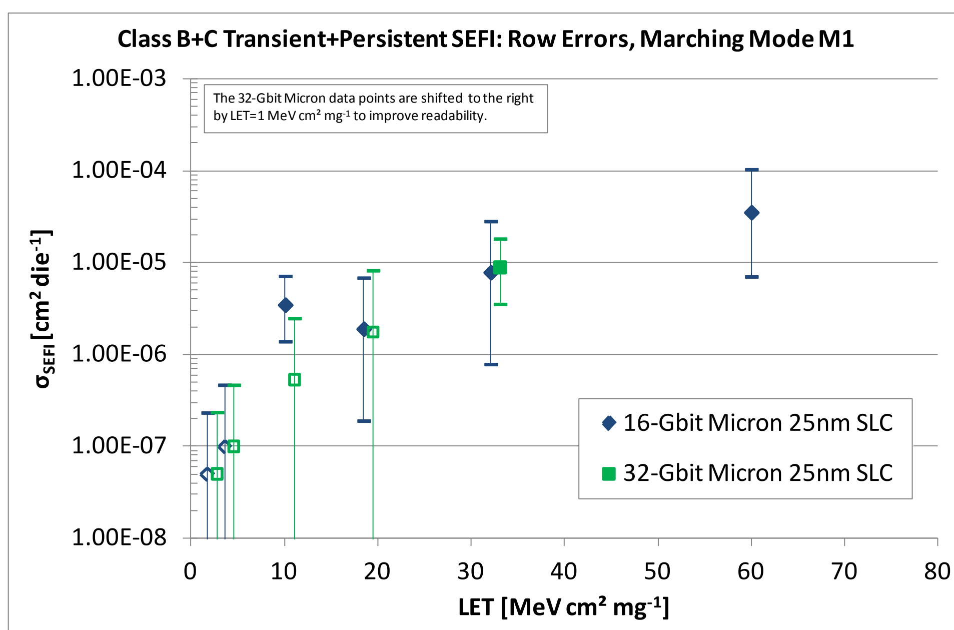

Figure 5-30: Class B+C Transient & Persistent SEFI cross section in marching mode M1, Row Errors; open symbols indicate “no event up to the applied fluence”.

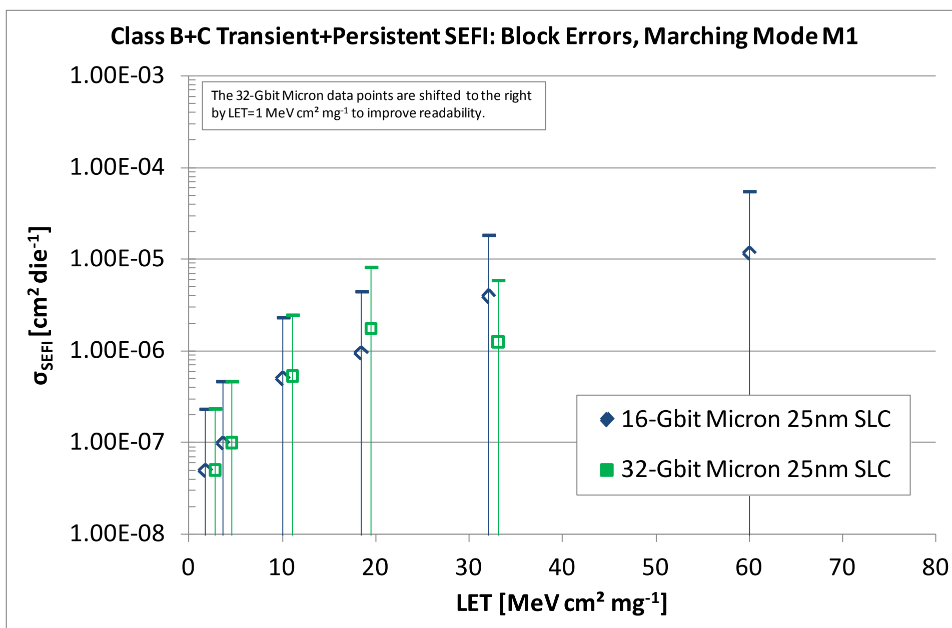

Figure 5-31: Class B+C Transient & Persistent SEFI cross section in marching mode M1, Block Errors; open symbols indicate “no event up to the applied fluence”.

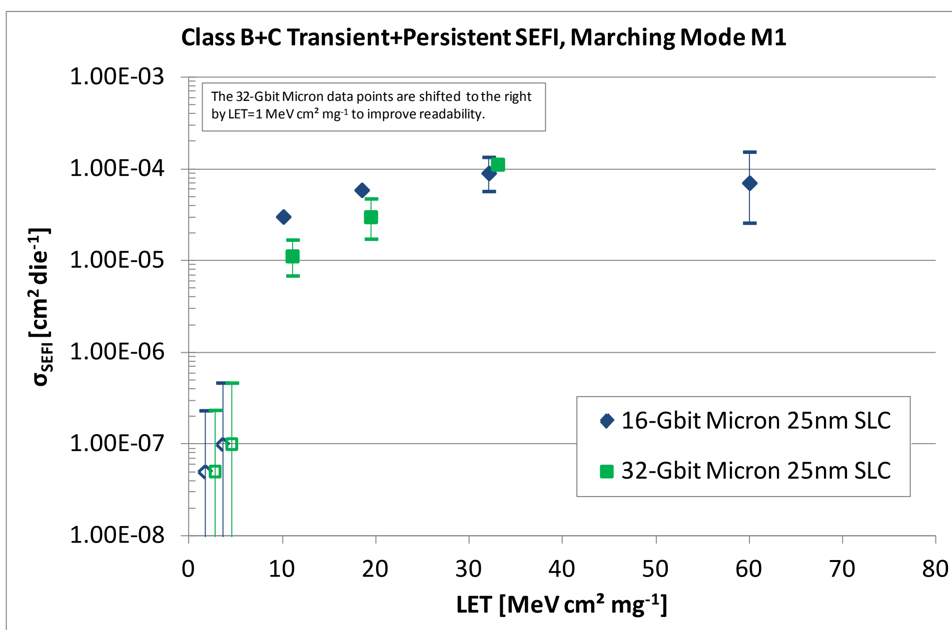

Figure 5-32: Class B+C Transient & Persistent SEFI cross section in marching mode M1, all SEFI; open symbols indicate “no event up to the applied fluence”.

© Airbus DS GmbH

5.1.5 SEU Annealing

The vast majority of observed SEU are falsifications in one direction only, in 0 → 1. Nevertheless, already for former generation SLC NAND Flash memories, annealing of these SEU with time was observed [RD-06]. The amount of annealing depends of the Ion (LET, mass), the higher the LET the lower was the resulting annealing.

Hence, two simplified models were introduced in [RD-06]:

a) loss of the negative floating gate charge (permanent) and

b) positive charge trapping in the oxide close to the floating gate (reversible).

The actual test of the 25nm 16 Gb Micron devices shows significant annealing only for SEUs induced by very low LET ions i.e. Nitrogen (LET=1.8 $MeVcm^2mg^{-1}$). SEU generation by charge trapping is restricted to very low LET. Even at Neon (LET=3.6 $MeVcm^2mg^{-1}$) almost all static SEUs are due to charge loss (see Figure 5-33).

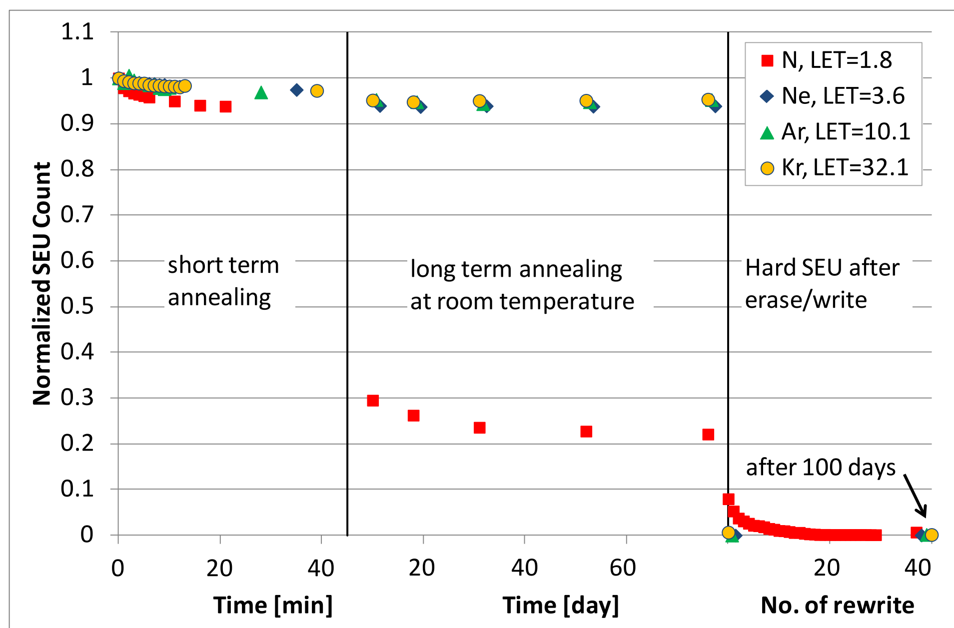

Figure 5-33: Annealing of static SEUs, Micron 16/32 Gb NAND-Flash.

As shown in Figure 5-34 with scaling of feature size, charge loss becomes dominating over charge trapping. The trapped charge domain is restricted more and more to lower LET. Remarkably devices of the same type but different lot code differed substantially with respect to the annealing behaviour.

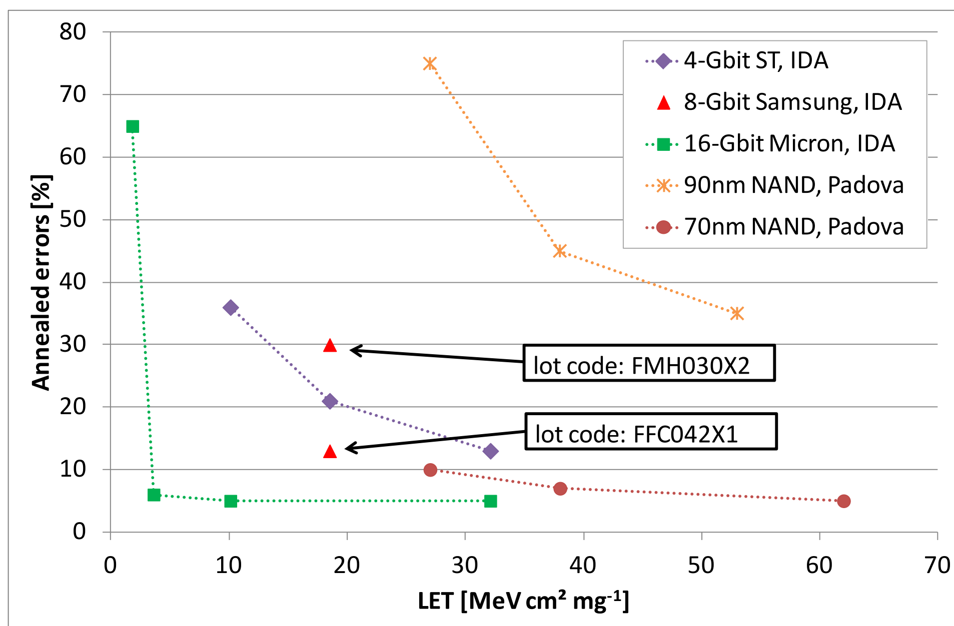

Figure 5-34: Percentage of annealed SEUs, 120 hours after irradiation as a function of ion LET.

5.1.6 Annealing of SHE (stuck bits)

Hard SEUs i.e., Single Event Hard Errors (SHE) or stuck bits, survive a reversal of the cell status by erase-write immediately after beam stop and error verification. Annealing of SHE was investigated for 16 Gb NAND Flash (see Figure 5-35). The logarithmically scaled bar graph shows the cross section of (i) the total of soft and hard SEUs, (ii) the share of SHEs directly after exposure, (iii) the annealing of "soft" SEUs after 20 days, and (iv) the annealing of SHEs after 20 days.

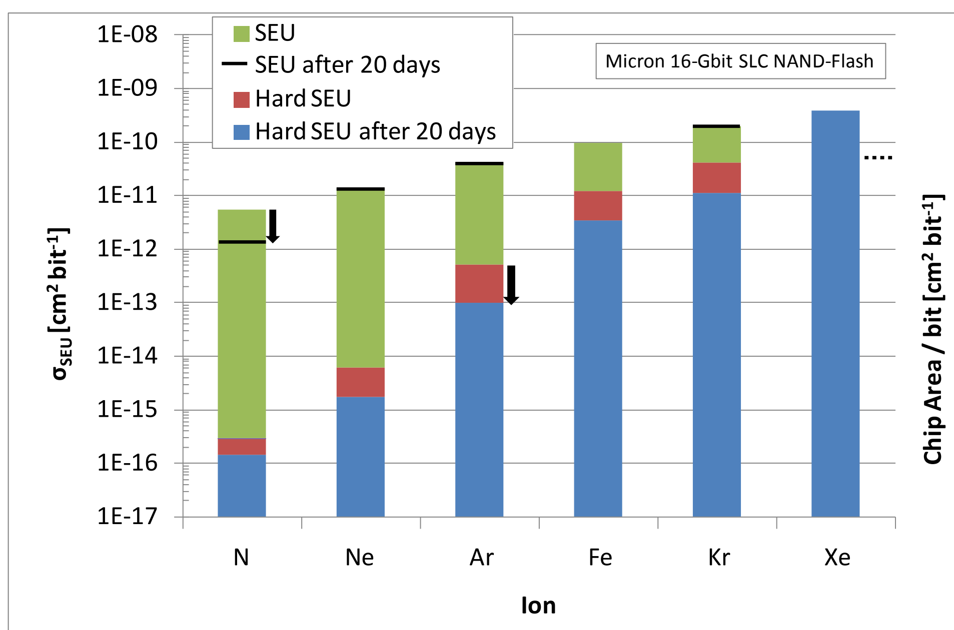

Figure 5-35: Total of soft and hard SEUs, share of hard SEUs directly after exposure and 20 days later, 16 Gb Micron SLC NAND-Flash.

© Airbus DS GmbH

The share of hard SEUs (Fig. 34, blue part of the bar) increases steadily with LET from $3{\cdot}10^{-3}$ % at Nitrogen to nearly 100% at Xenon. Significant annealing of static (soft) SEUs exists only at nitrogen. In contrast the SEUs, typically more than one half of the SHE (hard SEUs) anneal within 20 days.

Fig. 35 shows the respective cross sections over the linear LET scale. Starting with Iron, the cross section per bit exceeds the chip area per bit of $6{\cdot}10^{-11}$ cm^2, which indicates an increasing count of MBU. Further details are given in

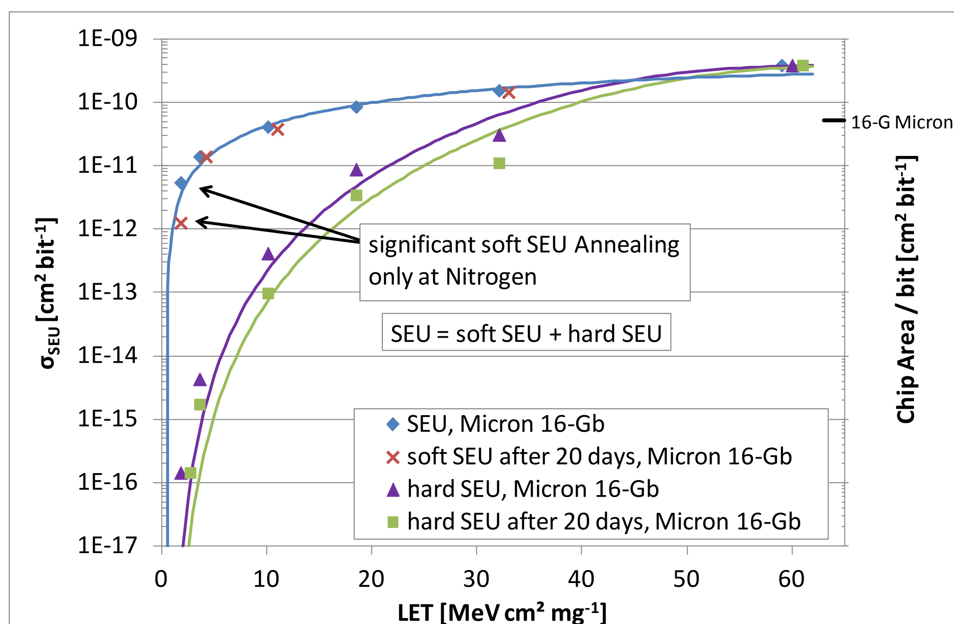

Figure 5-36: Cross section of SEUs, share of SHE directly after exposure and 20 days later, 16 Gb Micron SLC NAND-Flash.

5.1.7 Further investigations on destructive events

In all applied test campaigns no latch-up (SEL) was observed for LET up to 60 MeVcm^{2}mg^{-1}. Nevertheless, NAND Flash have been investigated to be sensitive to destructive failures under heavy ion irradiation. Typically, erase and write are no longer operable, but read is still functional. In contrast to SEL, the DF is not accompanied by an excessive persistent rise of the supply current, but in many cases by a moderate step (factor of 4) of the supply current. The DF event is of statistical nature, just as the SEU and the SEFI events. Figure 5-37 shows DF cross section curves from several test campaigns. Open symbols indicate “no DF until the applied fluence”. The tested 25nm 16 Gb Micron device delivers $\sigma_{sat} \approx 1{\cdot}10^{-5}$ cm^2 and $LET_{th} \approx$ 10…15 MeVcm^{2}mg^{-1}. This threshold LET is quite lower compared to former generations like the 4x8 Gb Samsung device in 51nm feature size.

The saturation cross section of $1{\cdot}10^{-5}$ cm^2 describes a sensitive area of about 30 × 30µm^2. By masking of the chip surface and also by IR hot spot sensing [RD-07], [RD-08], the sensitive area has been located to be the capacitor-switch cascade of the HV generator and its surroundings. Furthermore, it has been demonstrated that in the DF case, the high voltage drops to a significantly lower value [RD-07]. Presumably, the hit of a high LET ion induces a SEGR of the comparatively thick gate oxide of the HV switching transistors.

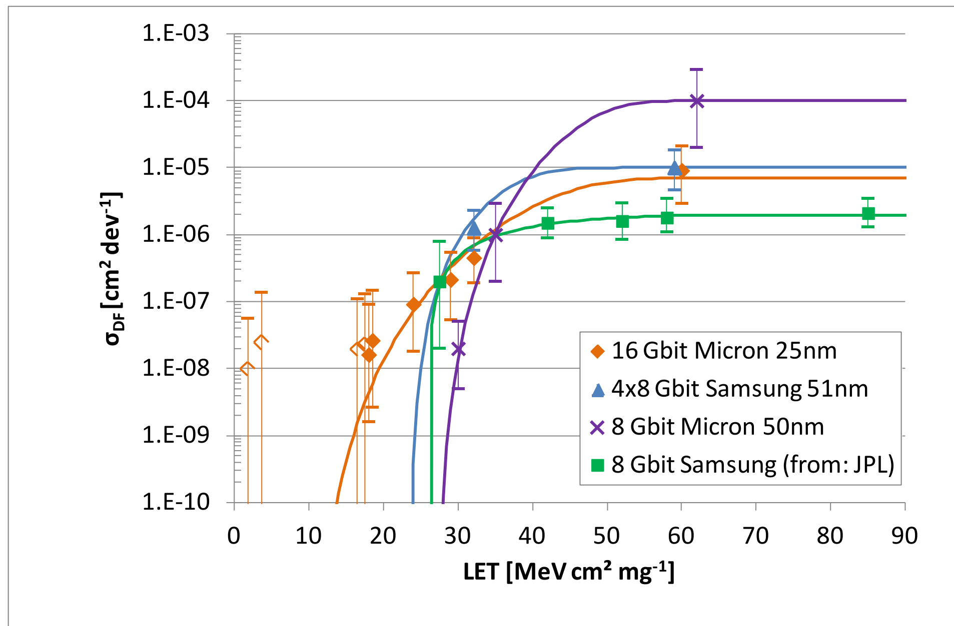

Figure 5-37: DF cross section curves, open symbols indicate "no DF until the applied fluence".

In [RD-02] the flux dependency (flux between 30 and 8000 $cm^{-2}s^{-1}$) of Samsung 4x8 Gb NAND Flash DFs have been examined. From the negative outcome it can be concluded that the DF is triggered by a single hit and not by the coincidence of several hits.

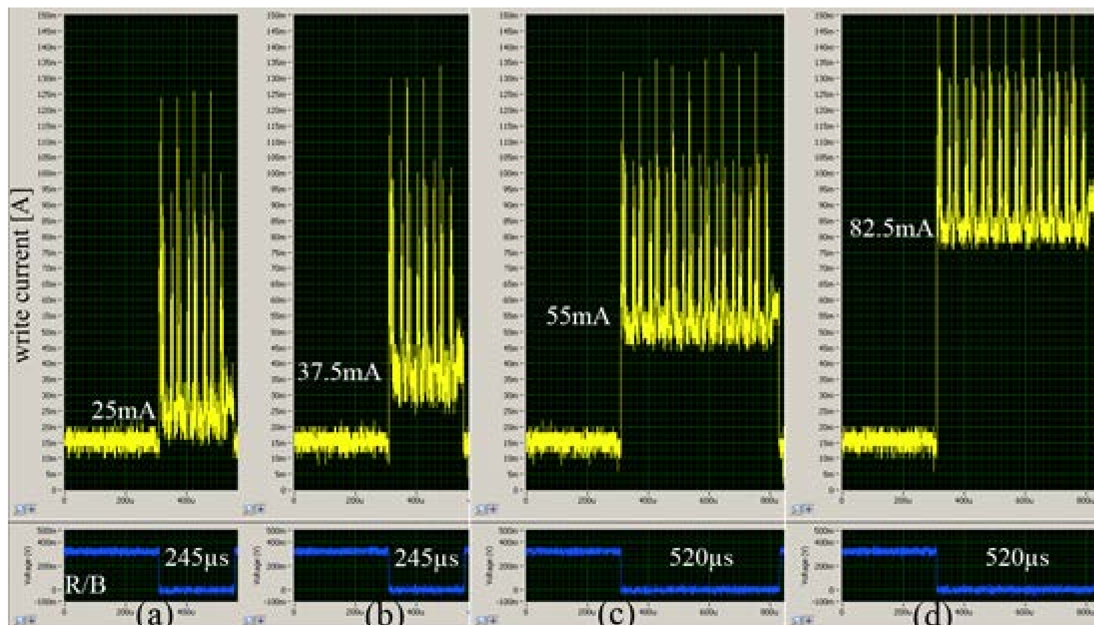

Figure 5-38: Development of the program current window until DF occurrence, (a) soon after irradiation start, (b) midway to the final saturation waveform, (c) the final saturation waveform and (d) after DF occurrence, Samsung 4x8 Gb NAND Flash [RD-02].

At DF occurrence, the program current of the Samsung device jumps from its plateau amplitude of 40mA maximum to a continuous current of 80mA. The DF occurrence is independent of the irregularities of the supply current such as occasional current spikes of several 100 mA or the stepping of the erase / program current pulse. Presumably, these spikes are caused by bus contentions in consequence of a hit induced disturbance of the controlling state machine.

Figure 5-38 shows the supply current waveform during the programming of a page [RD-02]. The current rises to a pulse plateau with superimposed needles. These needles reflect the sequence of HV program pulses. Under irradiation, the plateau widens and its amplitude grows, step by step.

Even though, at the begin of this work there was the impression that the stepping of the supply current leads finally to a DF, a more detailed analysis of the respective waveforms of later test campaigns delivered clearly that such a connection does not exist. DFs occurred as well after steps (b) and (c) as directly after step (a).

© Airbus DS GmbH

5.2 SEE Protons Test Results

In April 2014 one Protons SEE test campaign has been performed in the frame of Rad Hard Memory study (SEE_P_2, [DD-17], [DD-19] at PIF in PSI, Villigen, Switzerland. The used test bed is described in §4.1.1. Protons energies of 13.3, 21.4, 32.9, 49.6, 101.4 and 230 MeV have been used for test. In Table 5-2 and Figure 5-39 the properties of used proton energies are listed.

Table 5-2: Properties of used proton energies (calculated with SRIM)

Energy [MeV]	LET in Si (@surface) [MeV cm^2 mg^{-1}]	Range in Si [µm]	Deposited dose per 10^{10} pcm^{-2} [rad(Si)]
13.3	2.79E-02	1166	1.01E+04
21.4	1.93E-02	2689	6.94E+03
32.9	1.37E-02	5781	4.94E+03
49.6	9.96E-03	11999	3.59E+03
101.4	5.80E-03	42608	2.09E+03
230	3.34E-03	175375	1.20E+03

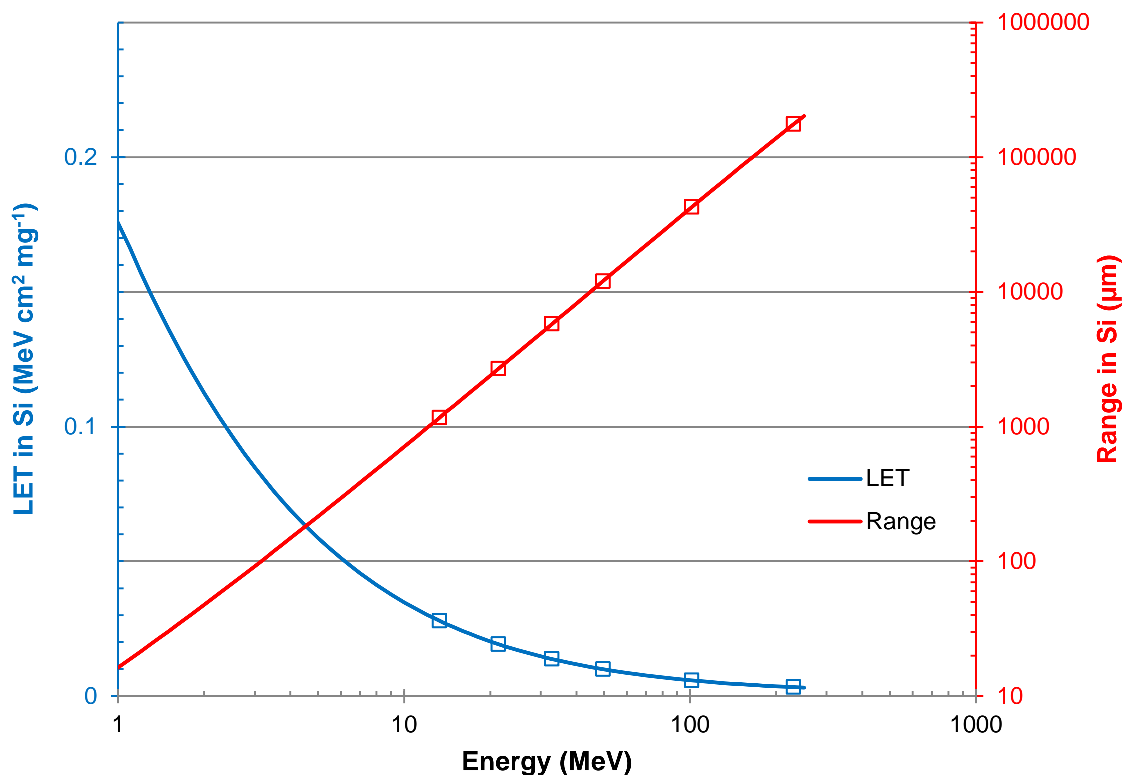

Figure 5-39: Protons energy vs. LET and range in Silicon (according SRIM).

In particular, 16 Gb and 32 Gb Micron NAND Flash in 25nm technology (the 32 Gb in single die and in four die stack) have been tested. The Samsung 4x8 Gb devices were used for comparison reasons:

Type	Density	Vend.	Mask Rev.	DC	Manuf. Lot	DUT
K9WBG08U1M-PIB0	4x8 Gb	SAM K	M / 51nm	0837	FMH030X2	SA26, SA27
MT29F16G08ABACAWP-IT:C	16 Gb	MIC U	C / 25nm	1218	-	M46…M60
MT29F32G08ABAAAWP-IT:A	32 Gb	MIC U	A / 25nm	1134	-	M76…M90
MT29F128G08AJAAAWP-ITZ:A	4x32 Gb	MIC U	A / 25nm, polyimide coating	1314	-	M95…M98

5.2.1 Static SEU

In Figure 5-40 to Figure 5-43 the static SEU cross sections versus energy for the Micron 16 Gb and 32 Gb devices are shown.

For the 16 Gb devices, a dependency on the used PIF x-y table position was found (blue and red diamonds of Figure 5-40). With one exception the DUTs at position 3 showed a lower FG SEU count compared to x-y position 2.

At the energy of 32.9 MeV four fresh DUTs were irradiated. Two of them about 2 hours later than the first two (Figure 5-40, question mark). The error count of both DUTs irradiated at a quarter past one is significantly reduced.

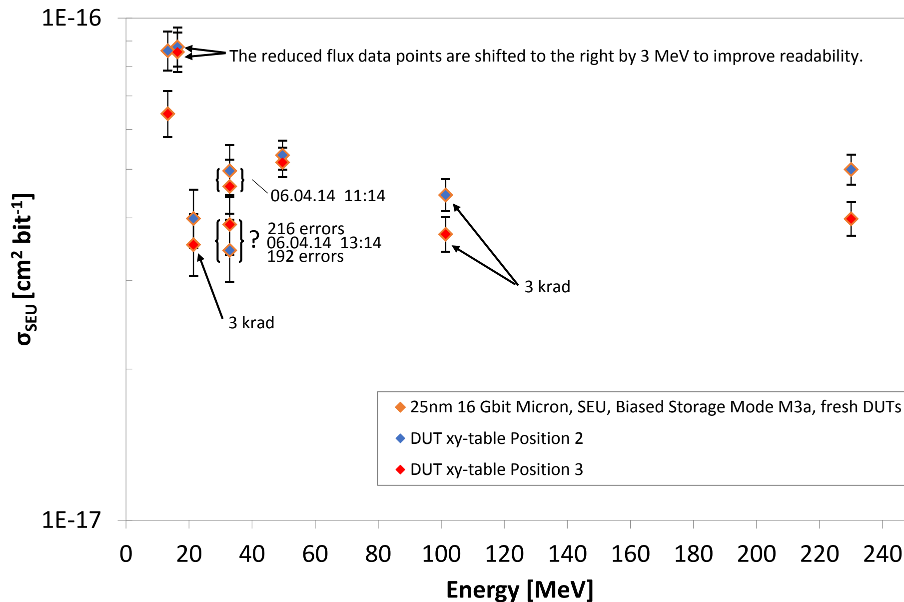

Figure 5-40: SEU cross section versus proton energy in Biased Storage Mode M3a, Micron 16 Gb.

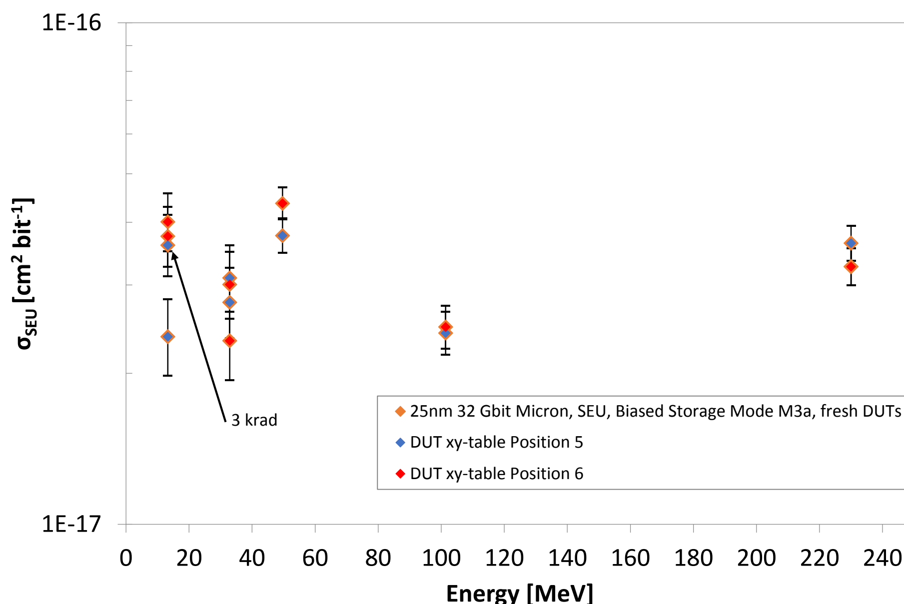

Figure 5-41: SEU cross section versus proton energy in Biased Storage Mode M3a, Micron 32 Gb.

Compared two former generations the retrieved static SEU cross sections for Micron 25nm SLC NAND Flash are about three orders of magnitude higher, see Figure 5-42 below.

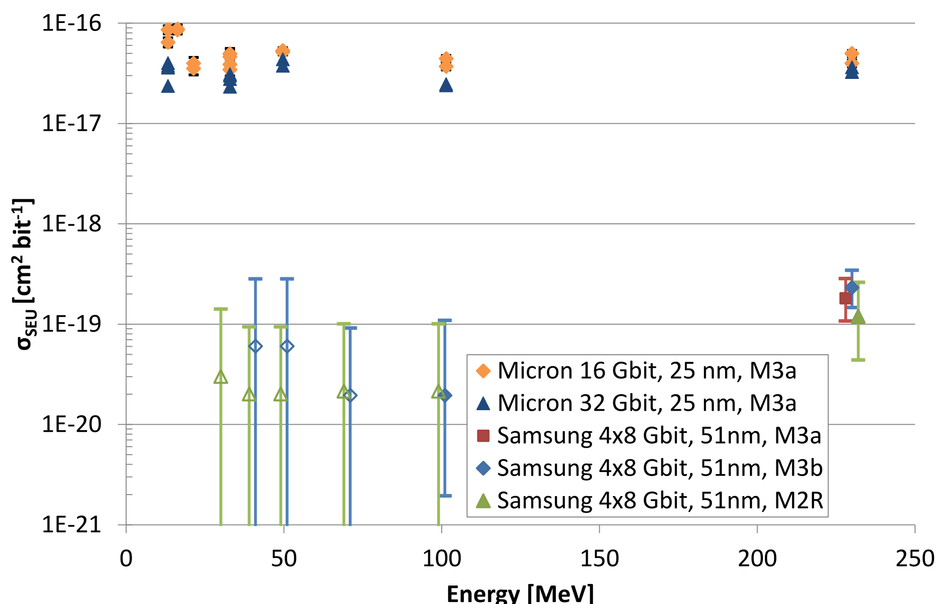

Figure 5-42: Comparison between Micron 25nm and Samsung 51nm SEU cross sections.

In contrast to 51nm Samsung SLC devices with onset energy $E_0 \geq 70$ MeV, SEU were already measured at lowest energy of 13.3MeV for Micron 25nm SLC devices. Furthermore, at least for the 16 Gb Micron device, the static SEU cross section is increasing at low energies ≤ 13.3MeV indicating sensitivity to direct ionisation by Protons. This would be consistent with the Heavy Ion results. Nevertheless, for the 32 Gb device this trend is not that evident.

Because of these ambiguous results, the SEU behaviour at low energies was investigated further. Therefore two fresh 16 Gb and two fresh 32 Gb DUTs were irradiated first at 13.3 MeV and thereafter at 21.4 MeV. The total dose of each DUT remained below 9 krad. The fluence was 1E+10 cm^{-2} and the flux was reduced to about 7E+06 $cm^{-2}s^{-1}$ resulting in 24 minutes of beam time in order to exclude error variations coming from rapid annealing. The cross sections of these low flux runs are shown in Figure 5-43 below.

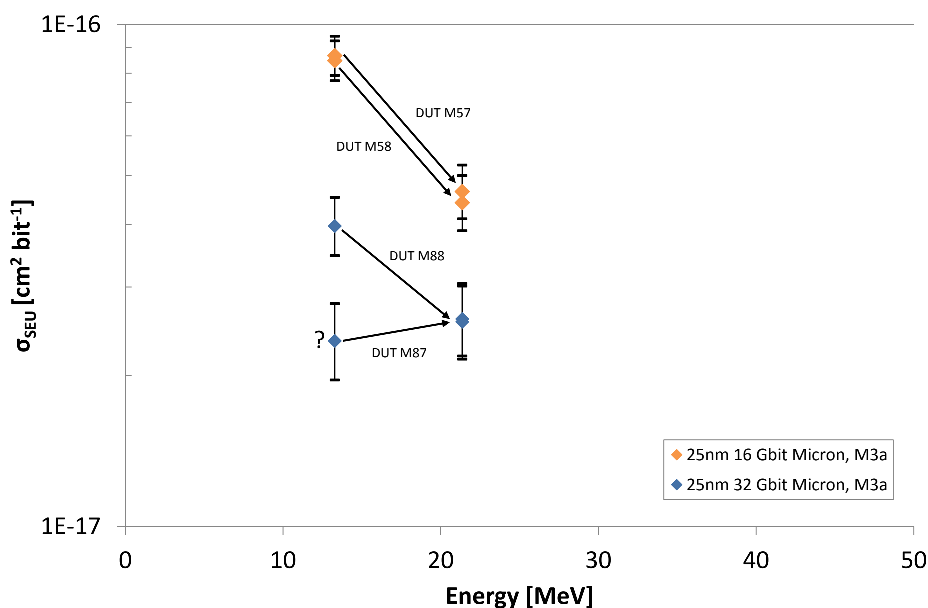

Figure 5-43: Results of the low flux test runs, SEU cross section versus proton energy in Biased Storage Mode M3a, 16 Gb and 32 Gb Micron SLC NAND Flash.

Three out of four comparative low flux measurements between 13.3 and 21.4 MeV show a decrease of the error count in the same range. It is still unclear, why the both 32 Gb DUTs behaved different at 13.3 MeV. At the subsequent test runs at 21.4 MeV, both measurements of 32 Gb DUTs fit perfectly.

5.2.2 SEU Annealing

In general, the annealing of static SEU errors has a strong temperature dependency on the one hand concerning the temperature during the read out phase, on the other hand concerning the temperature between the successive read outs. Here the DUT temperature is regarded as constant because the storage and read out of the DUTs was done in the PIF irradiation room.

Also during proton irradiation, a small number of static SEU disappear with time. Already at the second read out about 1.5h after the irradiation, SEU error count is reduced by 1 – 9 %. After about half a day the static SEU count has reached a stationary value between 94% and 98% of the initial error count.

5.2.3 SEFI

Because time constrains and further investigation on the static SEU behaviour, SEFI test runs with test modes M1 and M2R were conducted only at energies of 101.4 and 230 MeV.

No Class B SEFIs were observed. All 7 SEFIs were Class C SEFIs i.e., they remained during the next read operation but disappeared after a power cycle. The resulting cross section curves are provided in the following Figure 5-44 to Figure 5-52.

Marching Mode M1

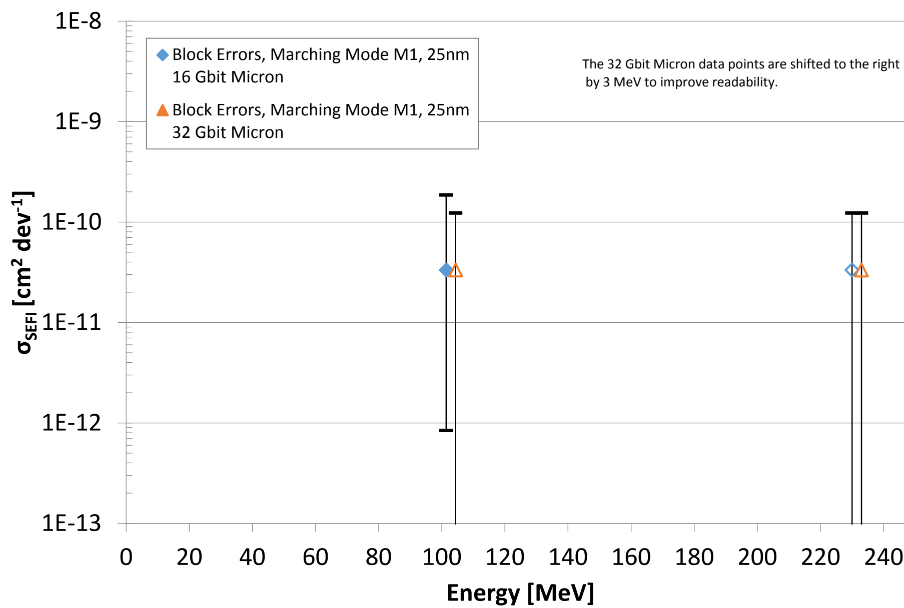

Figure 5-44: Block Error cross section versus proton energy in Marching Mode M1.

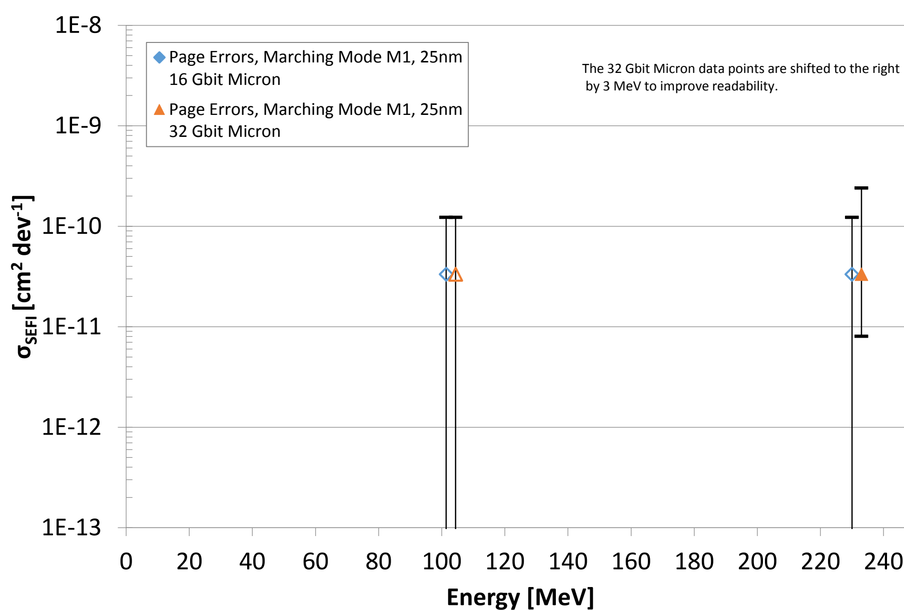

Figure 5-45: Page Error cross section versus proton energy in Marching Mode M1.

© Airbus DS GmbH

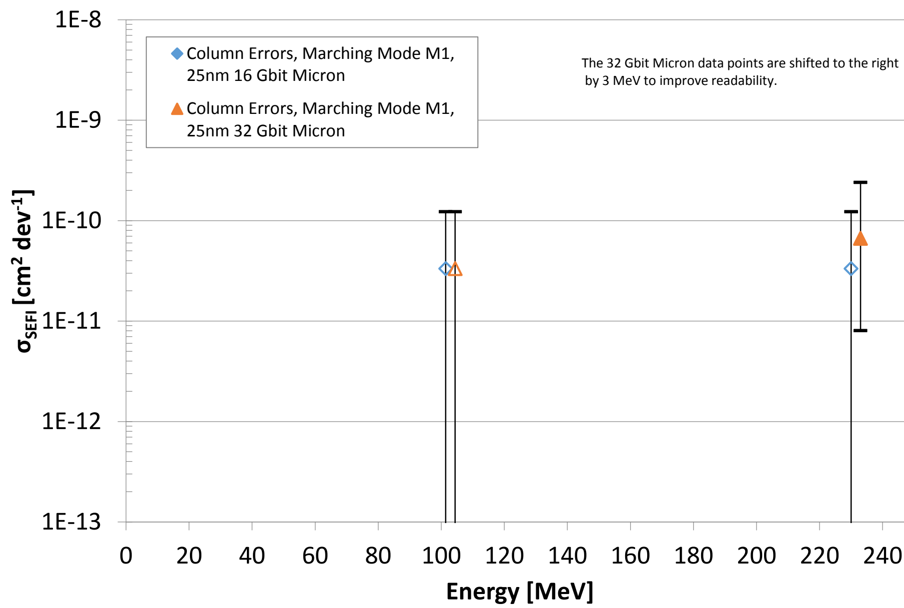

Figure 5-46: Column Error cross section versus proton energy in Marching Mode M1.

Read Mode M2R

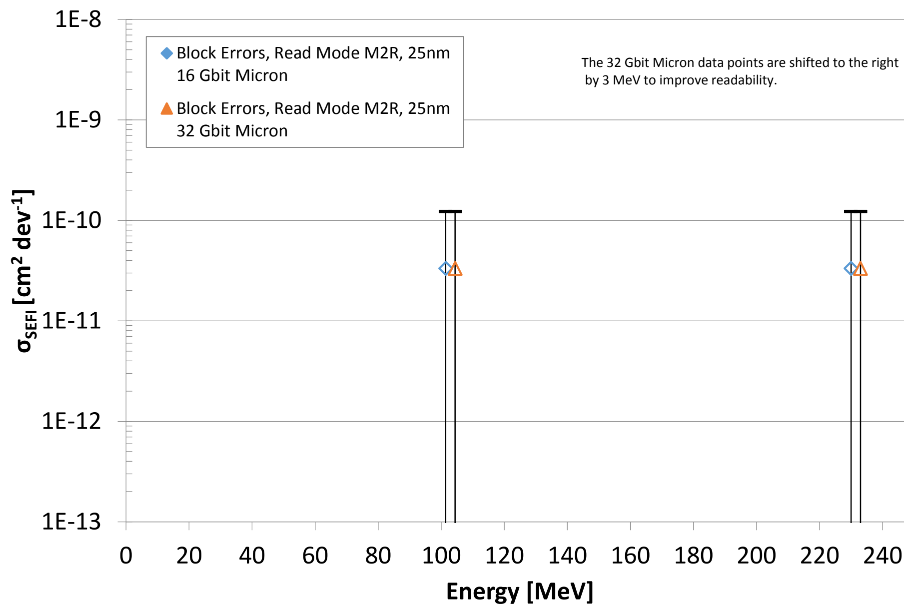

Figure 5-47: Block Error cross section versus proton energy in Read Mode M2R.

© Airbus DS GmbH

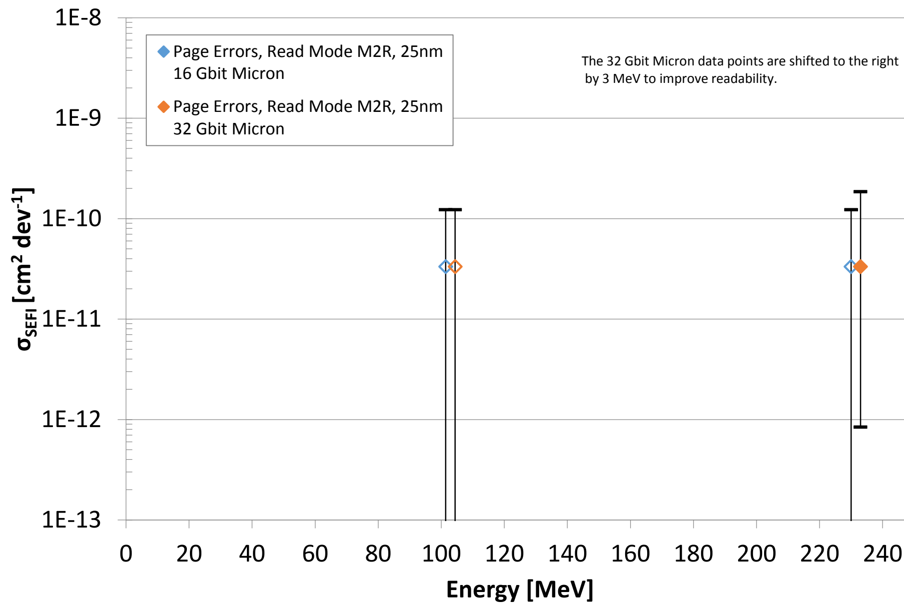

Figure 5-48: Page Error cross section versus proton energy in Read Mode M2R

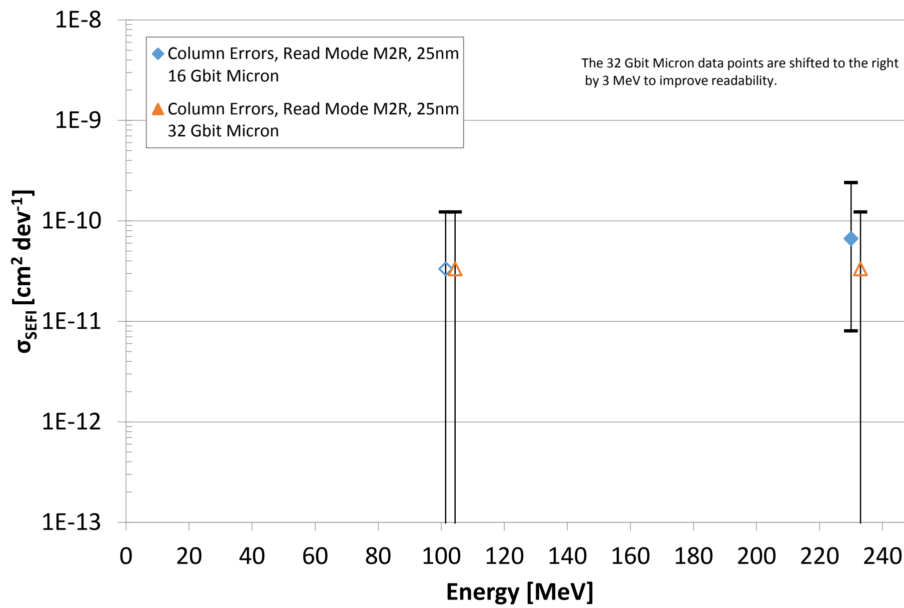

Figure 5-49: Column Error cross section versus proton energy in Read Mode M2R.

© Airbus DS GmbH

Biased Static Mode M3a

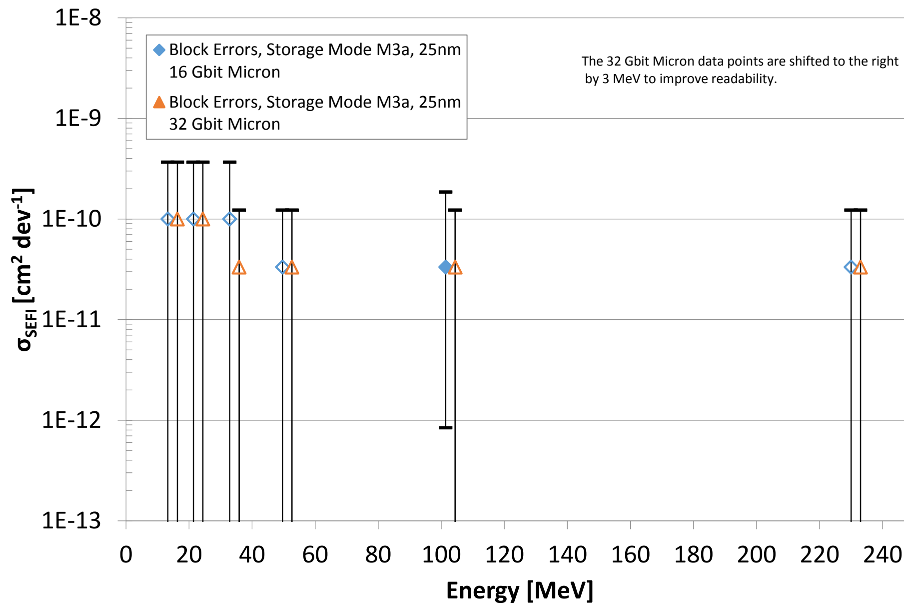

Figure 5-50: Block Error cross section versus proton energy in Storage Mode M3a.

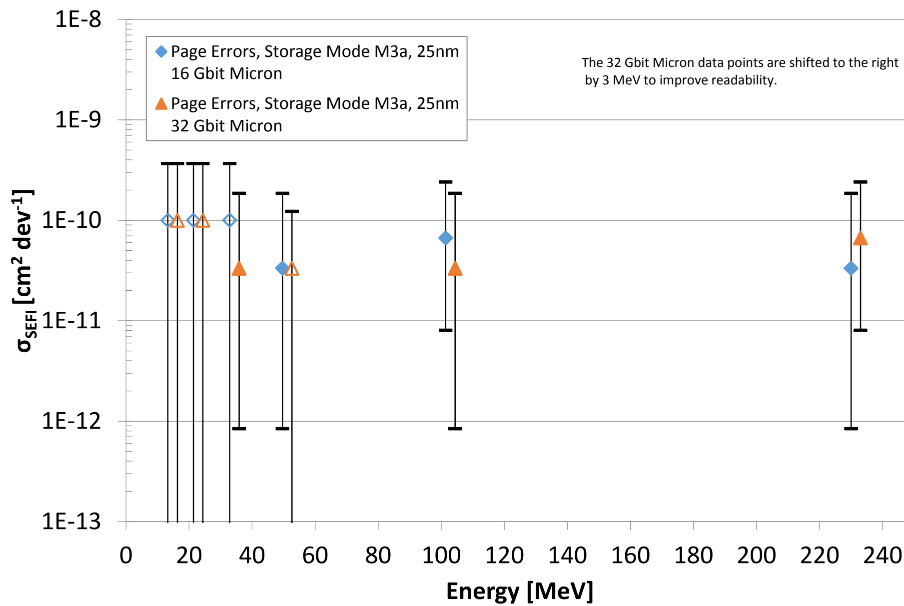

Figure 5-51: Page Error cross section versus proton energy in Storage Mode M3a.

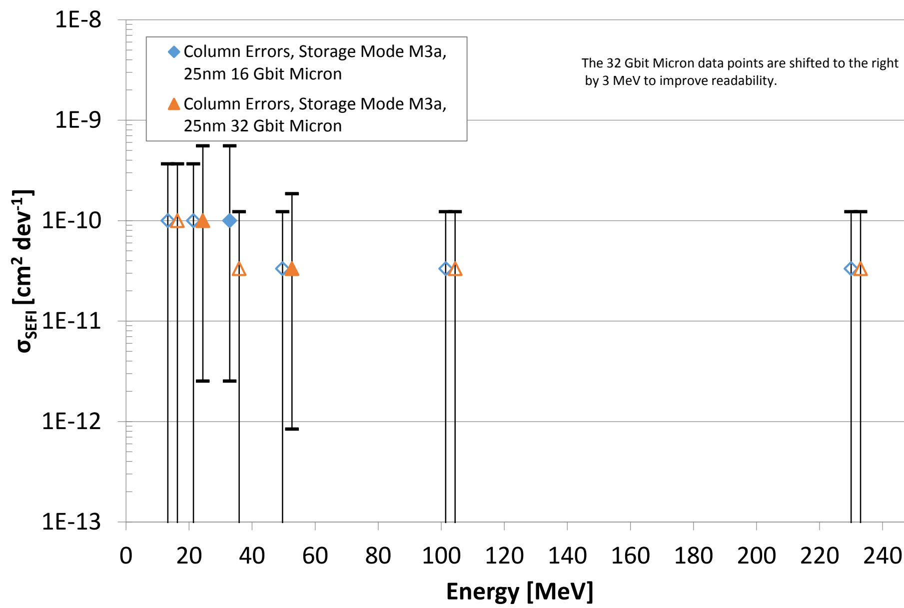

Figure 5-52: Column Error cross section versus proton energy in Storage Mode M3a.

5.2.4 Destructive Failures

No destructive event was observed during all Protons SEE test at energies between 13.3 MeV and 230 MeV.

5.3 TID Test Results

In January 2014 in-situ TID testing was performed on SLC NAND Flash devices in the frame of Rad Hard Memory study (TID_4, [DD-14], [DD-16]) at Co-60 facility at ESTEC. The used test bed is described in §4.1.2.

Four device types were tested:

Type	Density	Vend.	Mask Rev.	DC	Manuf. Lot	DUT
K9WBG08U1M-PIB0	4x8 Gb	SAM K	M / 51nm	0837	FMH030X2	SA20
MT29F16G08ABACAWP-IT:C	16 Gb	MIC U	C / 25nm	1218	-	M40…M45
MT29F32G08ABAAAWP-IT:A	32 Gb	MIC U	A / 25nm	1134	-	M50…M55
MT29F128G08AJAAAWP-ITZ:A	4x32 Gb	MIC U	A / 25nm, polyimide coating	1314	-	M60…M61

The devices were irradiated with a dose rate of about 85 $rad \cdot min^{-1}$(H_2O) respectively 4500 $rad \cdot h^{-1}$ (Si) up to the final dose of 90.2krad(Si).

Several test modes have been applied:

- Storage Mode, no refresh of the stored data
  - Biased Storage @25°C, 3.3V (nominal)
  - Biased Storage @85°C, 3.6V (maximum temperature and operating voltage)
  - Mostly Unbiased Storage (devices are switched on for read operation only)
- Refresh Mode, refresh by Erase and re-write with the inverted pattern every 2.5 krad
  - Biased Refresh @25°, 3.3V (nominal)
  - Biased Refresh @85°C, 3.6V (maximum temperature and operating voltage)
  - Mostly Unbiased Refresh, (devices are switched on during refresh and read operations only)

5.3.1 Definition of Parameter Limits

During TID test the error share and standby current I_{SB} has been measured. In Table 5-3 the specification limits for I_{SB}/I_{SB2} of all tested NAND flash types are listed. However, the specific application has to define the specific limit for this parameter. The measurements are done while all chip enables of the respective DUT are disabled

For the error share, the occurrence of 1st error is no real limit. Even at nominal environment on ground the function is only guaranteed for Micron 25nm devices in case of the application of 8-bit ECC per 540 bytes of data i.e., an error share of 8/4320=1.85E-03 have to be tolerated by the application (see Figure 5-53). To be on the safe side, the tolerable error share limit was set to 10^{-5}.

Table 5-3: Specification limits for standby current.

Manufacturer	Density [Gbit]	Symbol acc. to the datasheet	Typical standby current [µA]	Maximum standby current [µA]
Samsung	4x8	I_{SB2}	40	200
Micron	16	I_{SB}	10	50
Micron	32	I_{SB}	10	50
Micron	4x32	I_{SB}	40	200

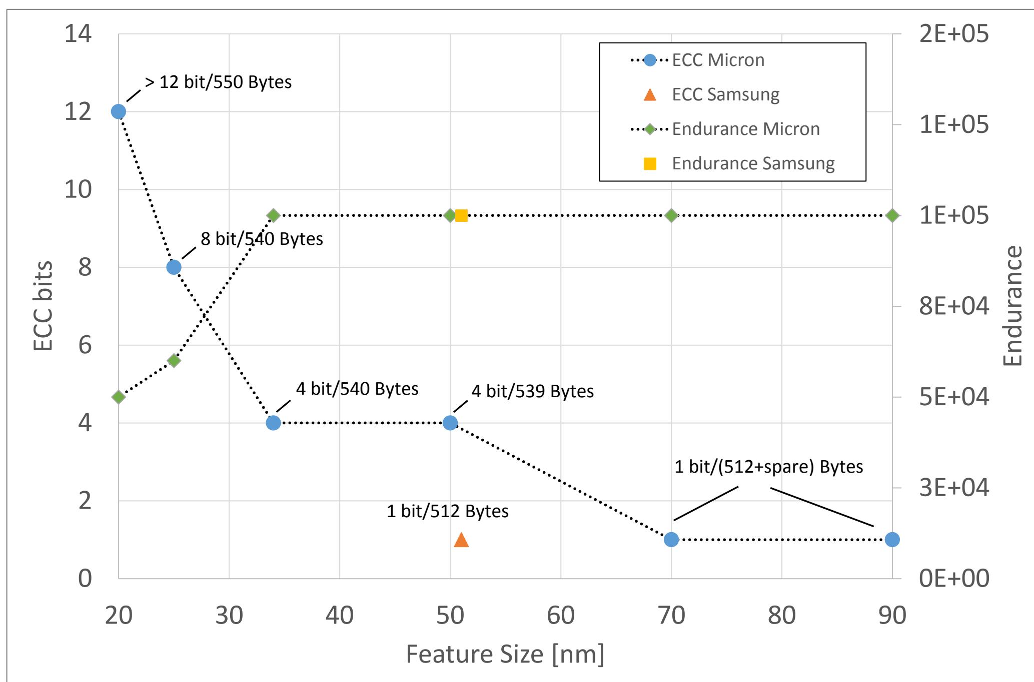

Figure 5-53: Number of ECC bits and endurance over feature size, data taken from various data sheets and roadmaps (the value 12 ECC bits per 550 bytes at 20nm feature size is divided by two for comparability, according to the data sheet: 24 bit / 1110 Bytes, the exact value will be even higher than 12 bits)

5.3.2 Storage Mode

The outcome of Storage Mode on all DUT is shown in Figure 5-54. First random data errors were observed already between 5 to 10 krad(Si). The amount of errors is exponential increasing with dose. The defined tolerable error share limit of 10^{-5} was reached at 18 krad(Si) at 85°C and at 25 krad(Si) at ambient temperature (25°C).

Functional errors were observed at about 32 krad(Si) at 85°C for one DUT and between 38 krad(Si) and 70 krad(Si) for all other DUTs. The bias condition had no visible impact on the results.

© Airbus DS GmbH

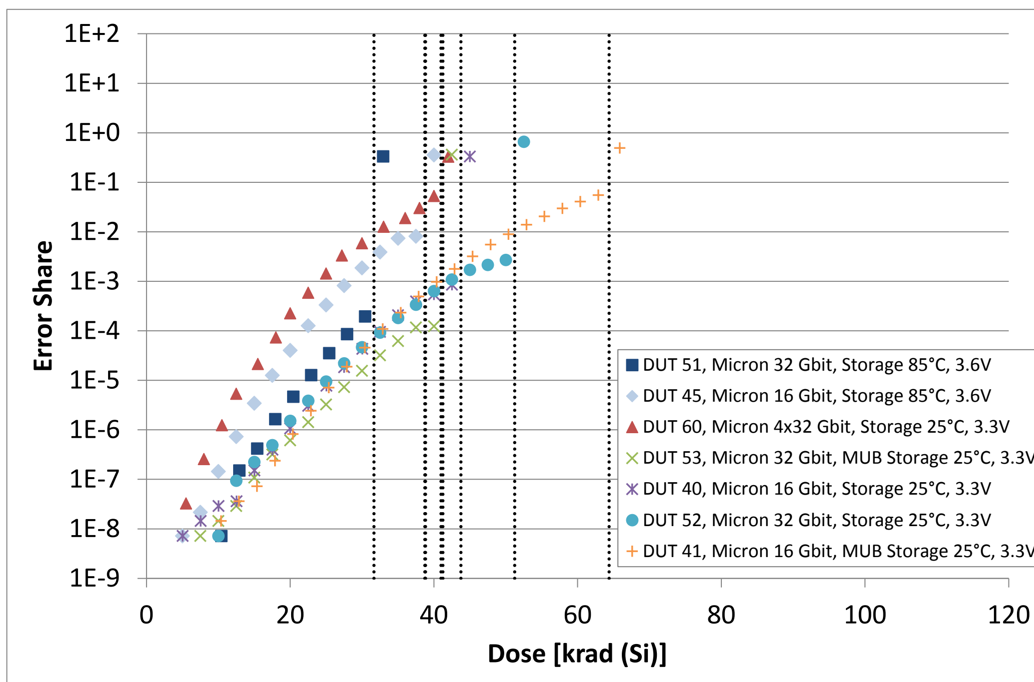

Figure 5-54: Error share versus dose of DUTs in Storage Mode (functional breakdown marked with dotted line)

In Figure 5-55 the evolution of the standby current with dose in Storage Mode is provided.

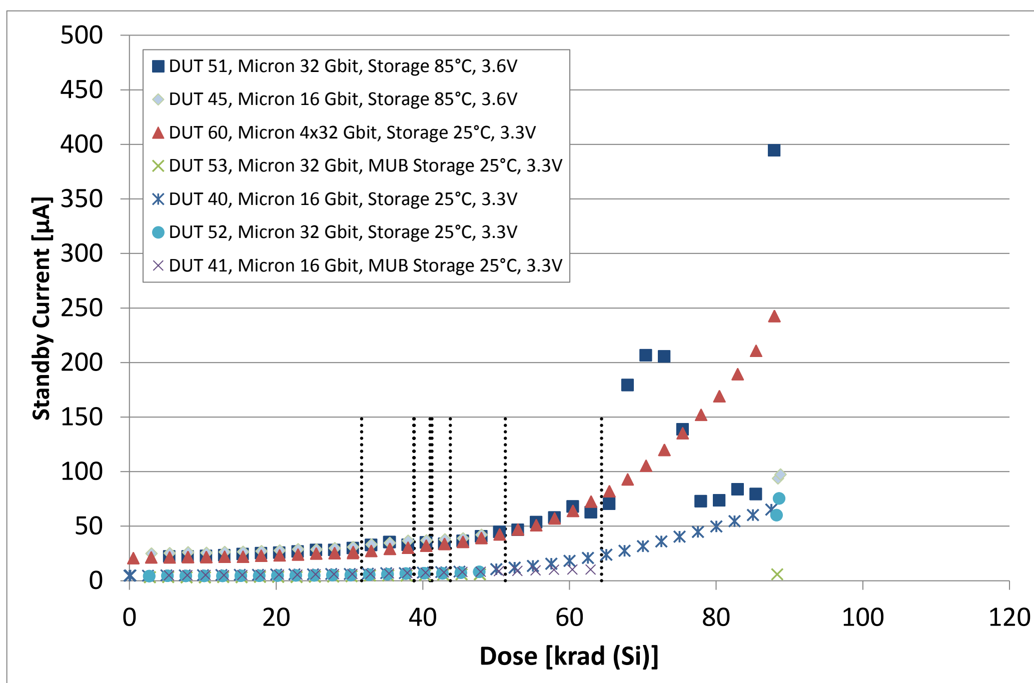

Figure 5-55: Standby current versus dose of DUTs in Storage Mode.

© Airbus DS GmbH

5.3.3 Refresh Mode

The outcome of Refresh Mode on all DUT is shown in Figure 5-56. Even with intermediate refreshes at every 2.5 krad(Si), first data errors occurred between 3 and 30 krad(Si). Nevertheless, the defined tolerable error share limit of 10^{-5} was not reached before functional loss of the DUTs.

Due to the applied refresh operation, compared to Storage Mode the data integrity could be improved. In contrary, the functional TID limit did not change at all. The Micron DUTs lost function between about 36 krad(Si) and 66 krad(Si) which is equivalent to the results for Storage Mode.

In contrast to these results, the 51nm Samsung 4x8 Gb DUT20 remained functional up to the final dose level of 90 krad(Si), first data errors occurred at > 70 krad(Si).

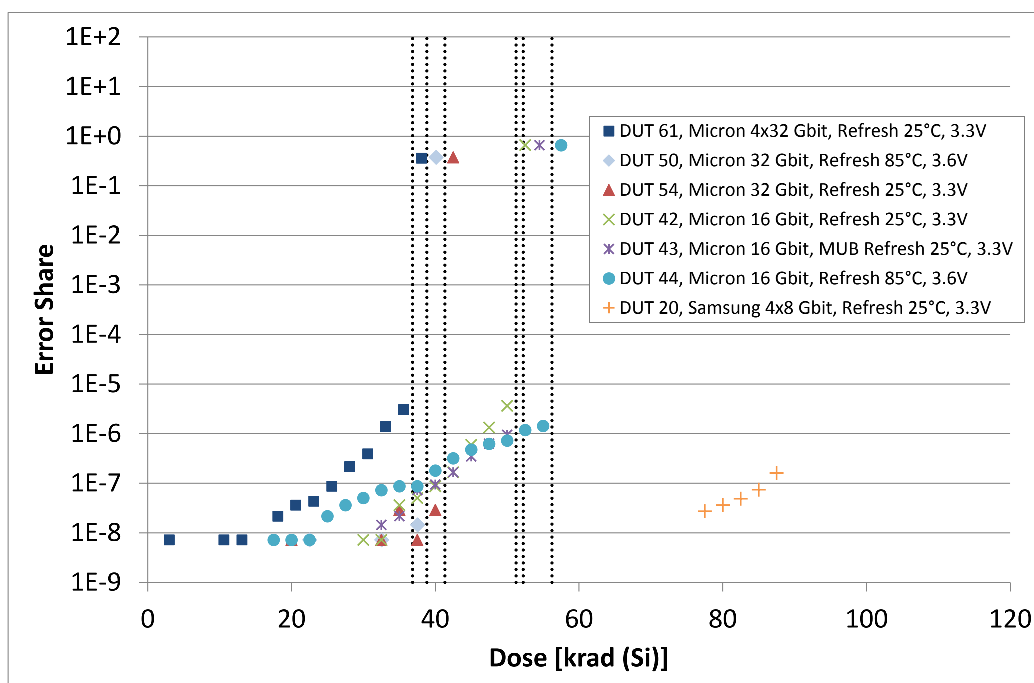

Figure 5-56: Error share versus dose of DUTs in Refresh Mode (functional breakdown marked with dotted line)

To summarize, the Micron SLC devices in 25nm technology are much more sensitive to TID degradation than the reference 4x8 Gb Samsung SLC device. Without refresh, 1st data errors occur after about 5 krad(Si) in worst case. Though, the improvement due to data refresh even at every 2.5 krad was limited. It is an open question whether an even more frequent refresh will improve the data integrity. Nevertheless, starting at 32 krad(Si) 1st DUT lost function. There was no improvement of this limit due to intermediate refresh observable. Overall, the 4x32 Gb DUT seemed to be most sensitive to TID. Heating of the DUT was decreasing the TID level for the 1st data error. The same was observed in former studies for the Samsung 4x8 Gb devices.

In Figure 5-57 to Figure 5-59 the results are presented separately for 16 Gb, 32 Gb and 4x32 Gb Micron SLC NAND Flash devices.

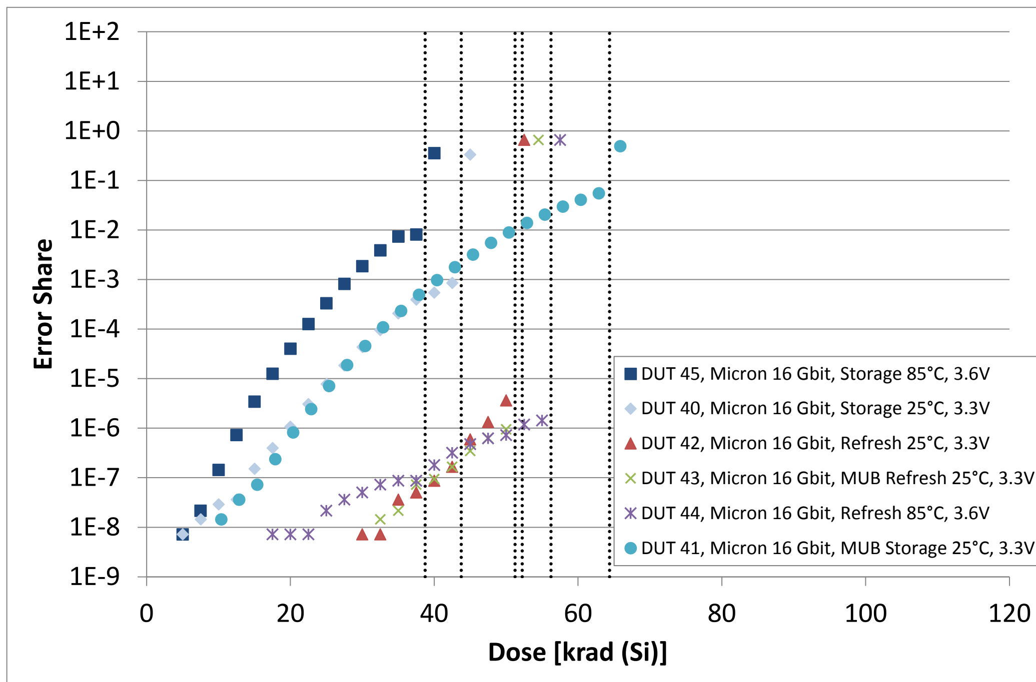

Figure 5-57: Error share versus dose of all Micron 16 Gb DUTs

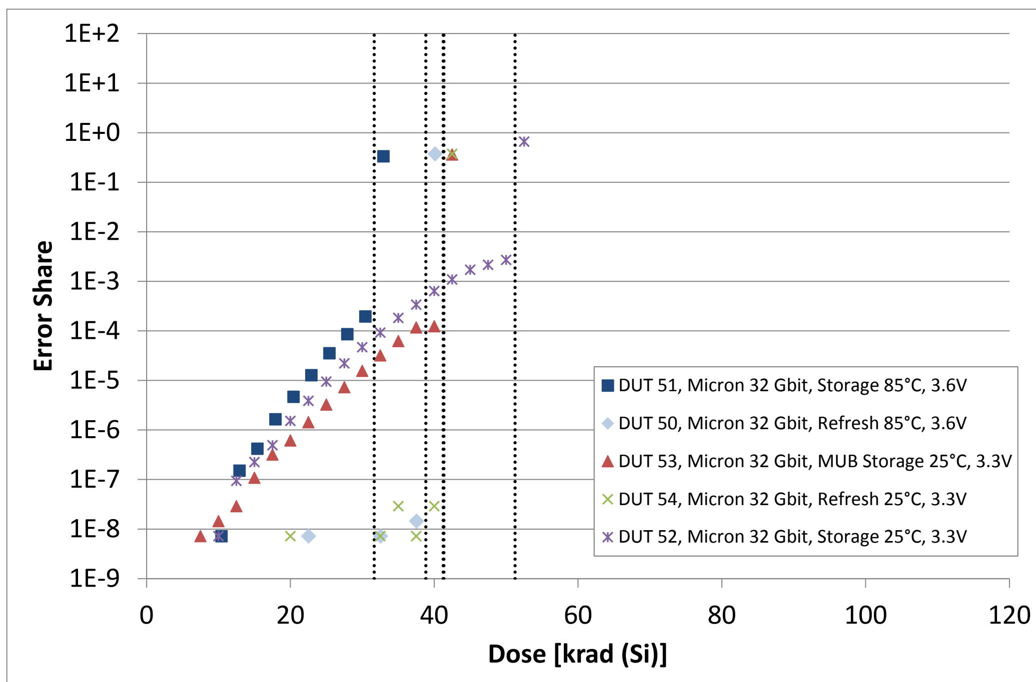

Figure 5-58: Error share versus dose of all Micron 32 Gb DUTs

© Airbus DS GmbH

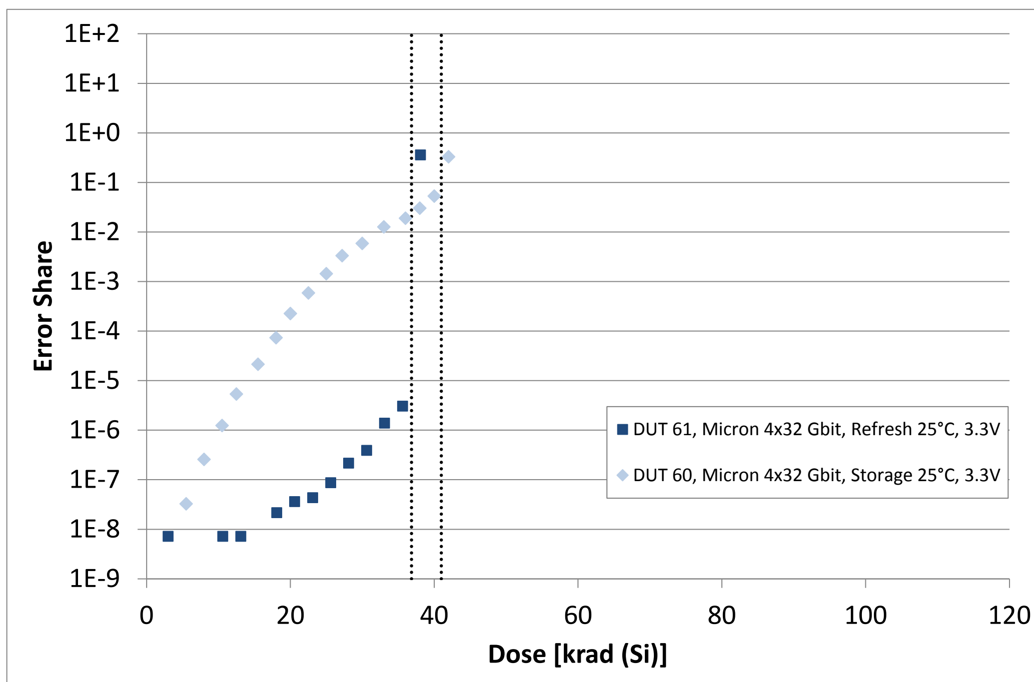

Figure 5-59: Error share versus dose of all Micron 4 x 32 Gb DUTs

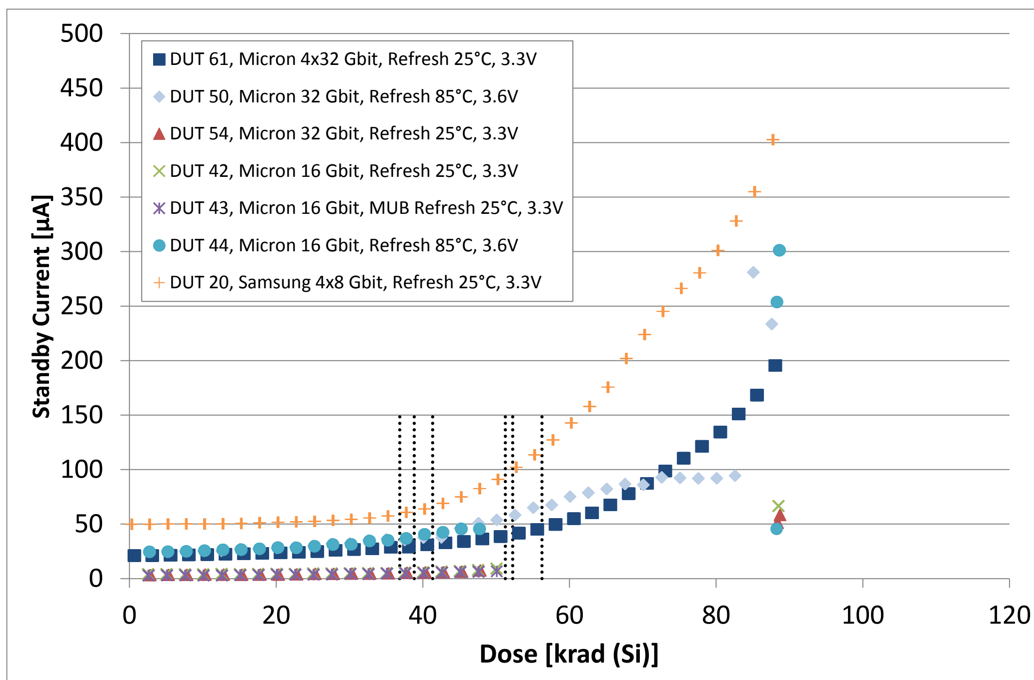

Figure 5-60: Standby current versus dose of DUTs in Refresh Mode

In Figure 5-60 above the evolution of standby currents in Refresh Mode is provided. In Figure 5-61 to Figure 5-63 the standby current evolutions are provided for the different device types.

© Airbus DS GmbH

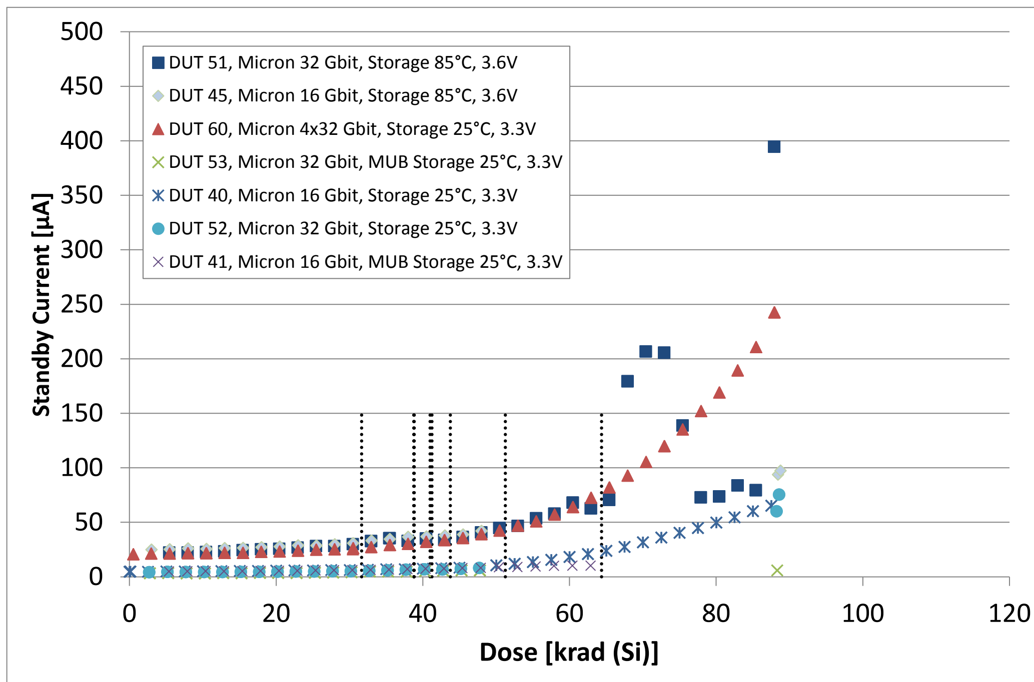

Figure 5-61: Standby current versus dose of all Micron 16 Gbit DUTs

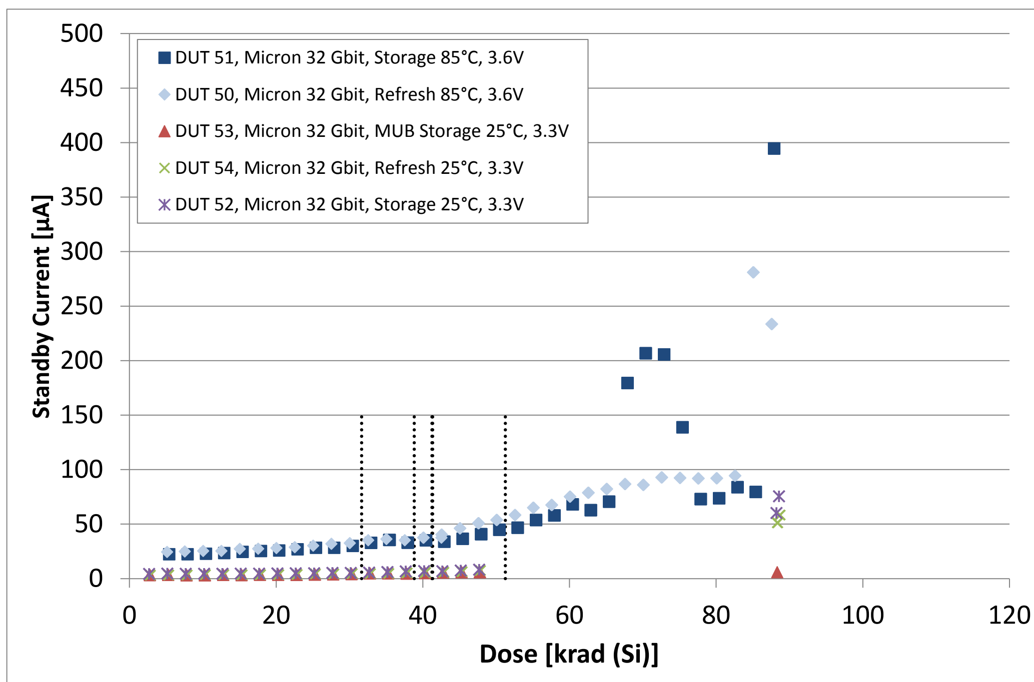

Figure 5-62: Standby current versus dose of all Micron 32 Gbit DUTs

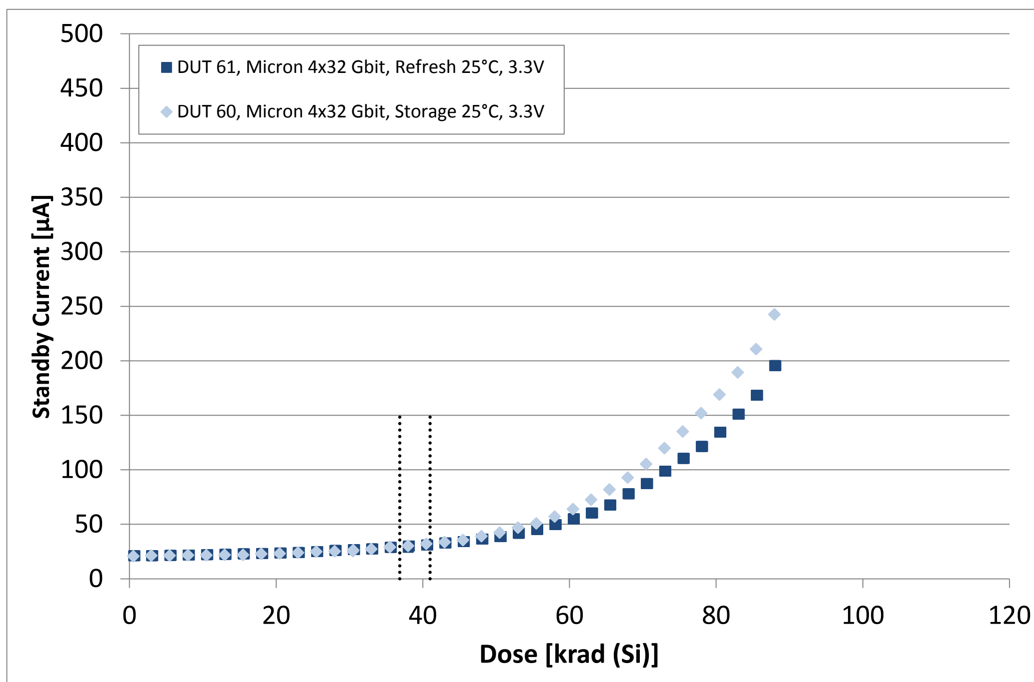

Figure 5-63: Standby current versus dose of all Micron 4x32 Gbit DUTs

Even in the dose regime of the Micron Device Failures the standby current is below the specified maximum datasheet value. After occurrence of Device Failures the standby current of Micron devices increases further. At the majority of the DUTs this increase is smooth but at some DUTs the standby current fluctuates. The standby current of all DUTs stays below 400 µA at 90.2 krad (Si).

The Samsung DUT shows an increase of factor 8 until the end of test at 90.2 krad (Si).

5.3.4 Comparison with unbiased Pre-Test

The different behaviour between Micron 25nm and Samsung 51nm devices is underlined by an unbiased TID test performed from March 11 - 18, 2013 (TID_3). During the unbiased irradiation of DDR3 SDRAM devices also 6 NAND-Flash devices were irradiated unbiased up to 376 krad (Si):

Type	Density	Vend.	Mask Rev.	DC	Lot	DUT
K9WBG08U1M-PIB0	4x8 Gb	SAM K	M / 51nm	0837	FMH030X2	DUT5, DUT6
MT29F16G08ABACAWP-IT:C	16 Gb	MIC U	C / 25nm	1212	-	DUT1
MT29F16G08ABACAWP-IT:C	16 Gb	MIC U	C / 25nm	1218	-	DUT2
MT29F32G08ABAAAWP-IT:A	32 Gb	MIC U	A / 25nm	1130	-	DUT3
MT29F32G08ABAAAWP-IT:A	32 Gb	MIC U	A / 25nm	1134	-	DUT4

All four Micron 25nm devices are no more functional. Again even the basic internal controller functions like Get ID deliver only zeroes instead of 0x2C, 0x48, 0x00, 0x26, 0xA9 for the 16 Gbit Micron device and 0x2C, 0x68, 0x00, 0x27, 0xA9 for the 32 Gbit Micron device.

In contrast, both 51nm Samsung devices are functional. After irradiation, a checkerboard pattern was written into 256 blocks. The read out afterwards delivered 2073 and 39990 SEUs (see Figure 5-64 below).

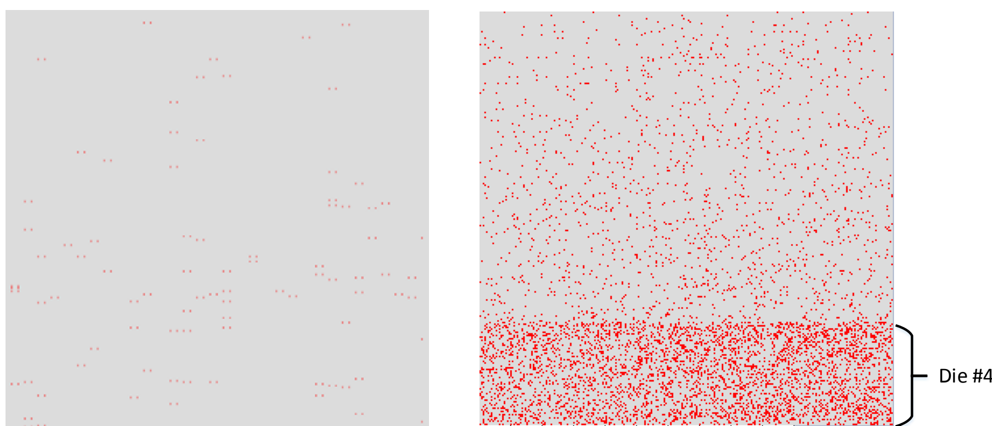

Figure 5-64: Error maps of Samsung 51nm DUT5 and DUT6

The majority of data errors in DUT6 appeared in the fourth die of the quad die package. The partially different error counts in dies assembled in one package were also observed in the in-situ test of Samsung 51nm devices.

At Samsung DUT5 a wear out test was performed in order to check for an impaired endurance which is specified as 100K program/erase cycles.

In contrast to previous IDA wear out tests, when Samsung 51nm devices reached about 1E+06 program/erase cycles with or without gamma irradiation, the test sequence was modified in this test. Instead of programming only one page of the 64 pages of one block with zeroes, in this test all pages of the accessed blocks were programmed with zeroes, which induces the maximum stress to the FG cells and the high voltage generator during the program/erase operations. The reached wear-out cycles are compared in Figure 5-65 for both wear out test routines.

If all pages are programmed to zero the number of erase/program cycles (n_{EPC}) is reduced to between 1.5E+05 and 3E+05. Again different dies of the quad die package behave slightly different (Figure 5-65, black line) with respect to the mean erase program cycle count as shown also for SEUs (Figure 5-64).

The tested five blocks of Samsung DUT5 showed comparable numbers of erase/program cycles (340k - 475k), all well above the specified limit of 100K cycles.

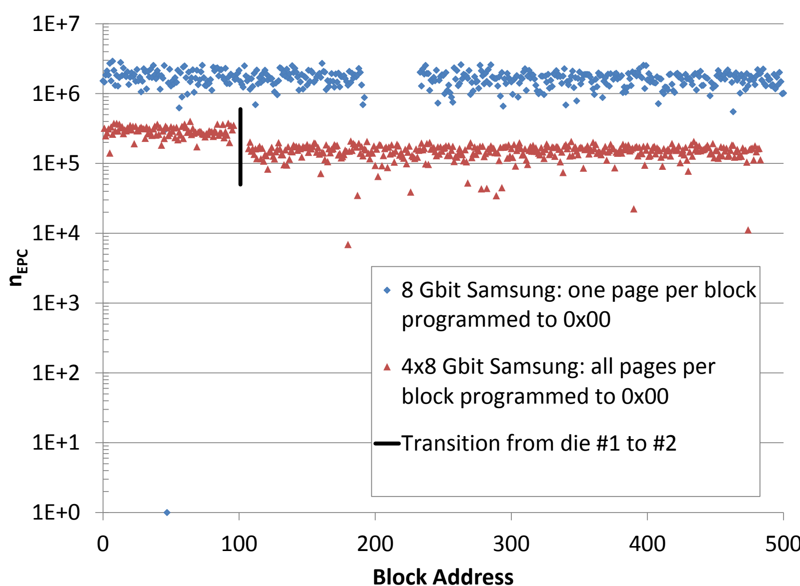

Figure 5-65: Distribution of the wear-out limits in the first 500 blocks, Samsung 8 Gbit and Samsung 4x8 Gbit 51nm NAND-Flash

The stored content (all 0xFF after erase and all 0x00 after program) was checked every 20K erase/program cycles. No errors were detected.

In conclusion compared to the previous 51nm Samsung NAND-Flash generation the TID tolerance of the 25nm Micron NAND-Flash generation is reduced significantly with respect to the complete loss of storage functionality as well as to the SEU sensitivity.

This is well in line with the results presented by F. Irom [RD-05]. In this work five samples of 32 Gb 25nm Micron devices with the same part number (MT29F32G08ABAAA) but different date code were tested. They failed (i) post 40 krad (Si) and post 50 krad (Si) using a refresh mode and (ii) at 55, 75 and 70 krad using a storage mode with read after irradiation.

5.3.5 Conclusion

The general rule that decreasing feature size (from 50nm to 25nm) should result in a better TID tolerance does not hold. It is not the case for the Micron 25nm generation. Neither the error onset nor the Device Failure can be influenced by the operating conditions like test mode, supply voltage or DUT temperature. Only the steep error increase (Fig. 9) can be sup-pressed by periodic refresh of the stored data at least every 2.5 krad (Fig. 10).

From the TID point of view the 25nm Micron generation is suitable for applications up to a total dose of 25 krad using a suitable error correction scheme and using a periodic refresh. The periodic refresh keeps the error share below 10^{-5} which is tolerable before ECC. Therefore with periodic refresh the Device Failure occurrence determines the total dose.

© Airbus DS GmbH

6 DDR3 SDRAM Characterisation

Several test campaigns on 2 Gb and 4 Gb DDR3 SDRAM devices from several manufacturers were performed, four Heavy Ion SEE campaigns (SEE_HI_1 to SEE_HI_4), one Protons SEE campaign (SEE_P_2) and several unbiased and in-situ TID test campaigns (TID_1 to TID_4). See Appendix A for further details.

6.1 SEE Heavy Ions Test Results

6.1.1 DUT Preparation

DDR3 silicon dies are encapsulated in flip-chip plastic ball grid packages in order to reduce the lead inductance (Figure 6-1). Before irradiation, and because of the limited range of the used heavy ions, the plastic has to be removed down to the back surface of the die, and the die may have to be thinned, depending on the available ion range.

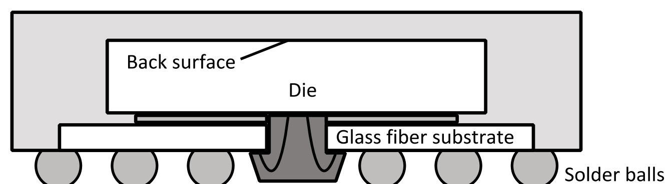

Figure 6-1: Exemplary cross section of a DDR3 device

Two different methods have been applied during Rad Hard Memory Study [PD-04], [DD-09]:

Method A by IDA and Institute of Machine Tools and Production Technology, both Technische Universität Braunschweig:

The cover plastic has been removed by drop etching with fuming nitric acid. The device is fixed to a mounting plate and is covered with Teflon tape. A window is cut into the tape. Then the device is heated up to about 70°C. An acid drop is placed into the window and then the device is rinsed with water and acetone. This step of etching and rinsing is repeated many times until the die surface is free of plastic. Then, the opened device is fixed to a metallic support structure by few small adhesive pads.

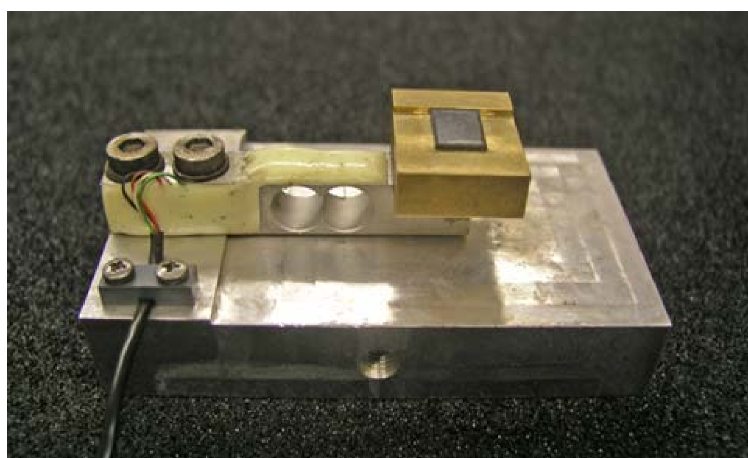

Figure 6-2: Mechanical DUT Support Structure

The force applied by the grinding tools has been monitored by a strain gage on top of the support lever. Grinding wheels were used such as applied for the separation of wafers: (i) diameter 52mm, (ii) thickness 500µm and (iii) a tip profile of 120° in order to reduce the contact volume and thereby, the grinding forces. The synthetic diamond grains with a medium grain diameter of 5µm were supported by a bronze bond. Using the following grinding parameters the die could be machined from an initial thickness of 205µm to a final thickness of 70µm, (i) infeed speed 100mm/min, (ii) cutting speed 60 m/s, (iii) grinding width 20µm. The grinding depth per path was varied in 6 steps: 25µm for the first four steps, and for the final two passes 20µm and 15µm, respectively. In the clamping the die showed a curvature of 5µm in lateral extension and of 10µm in longitudinal extension. Therefore, the path of the grinding wheel had to be adapted to this curvature. By grinding in lateral direction the larger one of the two shape deviations could be reduced definitely. For the chosen setting parameters the grinding time took 8 hours per device.

Method B by Fraunhofer-Institut für Angewandte Optik und Feinmechanik (IOF), Jena:

The method enforces the die in an exactly flat position. This supports grinding and polishing without the need for contour following of the abrasive tool. At first, the layer thickness of the plastic encapsulation and the silicon die to be grinded is determined, based on the cross section of a sample chip. The devices are bilaterally puttied between glass plates. Planarity and parallelism of the chip surface during the mechanical processing is guaranteed by fixing the devices between the glass plates. The deployed machine used (DISCO DAG 810) enables a thickness tolerance of 5 µm.

In the first grinding work step, plastic layer and glass plate were grinded down to the silicon surface of the DDR3 chip. After reaching the silicon surface, the target thickness of the silicon die is entered to the machine and, after that, the silicon die as well as the plastic encapsulation are thinned. Inevitably, the grain size of the tool must be carefully adapted for the silicon material. If the grain size is too rough, micro-scratches due to the high mechanical stress lead to imperfections in the functionality up to the destruction of the DDR3 chip.

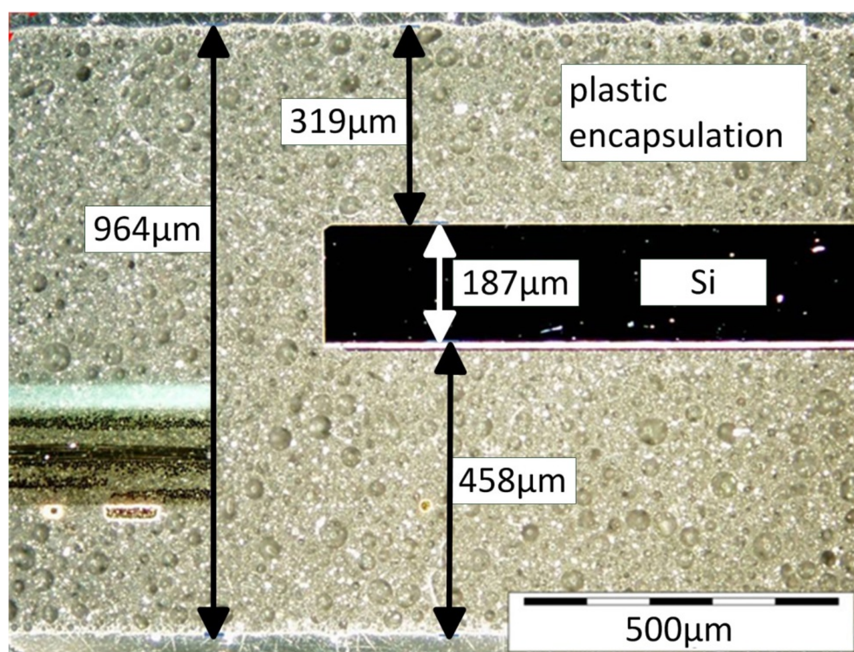

Figure 6-3: Mechanical cross section of a DDR3 device (IOF/IDA)

6.1.2 1st SEE test campaign on 2Gb DDR3 SDRAM devices at RADEF (SEE_HI_1)

Main goal of the 1st SEE test campaign at RADEF in 2011 was the evaluation of the new test bed RTMC-6 (see §4.2.1). Nevertheless, 1st results on 2 Gb DDR3 SDRAM devices could be retrieved on parts of three different manufacturers (Samsung, Micron, Nanya). All parts were prepared according method A (see §6.1.1) with a yield of about 75%. Following parts were tested:

Type	Density	Vendor	Mask Rev.	DC	Lot
K4B2G0846B-HCH9	2 Gb	SAM K	B / 50nm	0949	GLJ423AC
MT41J256M8HX.15E:D	2 Gb	MIC U	D	1006	BYFCM91.21
NT5CB256M8BN-CG	2 Gb	NAN TW	B	1026	01349199GP

In Figure 6-4 to Figure 6-8 the outcome of this 1st SEE campaign is presented. At this time, the RTMC-6 test bed was using the standard DDR3 memory controller from Xilinx® without any access to the mode registers within the read or write operation. Hence, the only chance to return function without data loss after a SEFI was a manual hardware reset of the DUT.

According these 1st results for all error species, Samsung devices showed substantially less errors than Micron and Nanya devices. The cross sections for column errors in marching mode (M1), shown in Figure 6-7, are similar to the ones in storage mode (fig. 5(c)). The same similarity was found for all error classes.

The main outcome of this test was that the number of row and column SEFIs is in the same order of magnitude as the number of SEUs. The onset LET for such SEFI is in the same order as for SEU i.e. close to 1 MeVcm^{2}mg^{-1}. As each SEFI causes several (typically hundreds) of bit errors, the errors induced by SEFIs outweigh the number of random errors by far. The mitigation of SEFI is the main issue for any application of these devices in space environment.

Of all devices, Samsung DDR3 devices (K4B2G0846B, B-mask) showed the most favourable cross section.

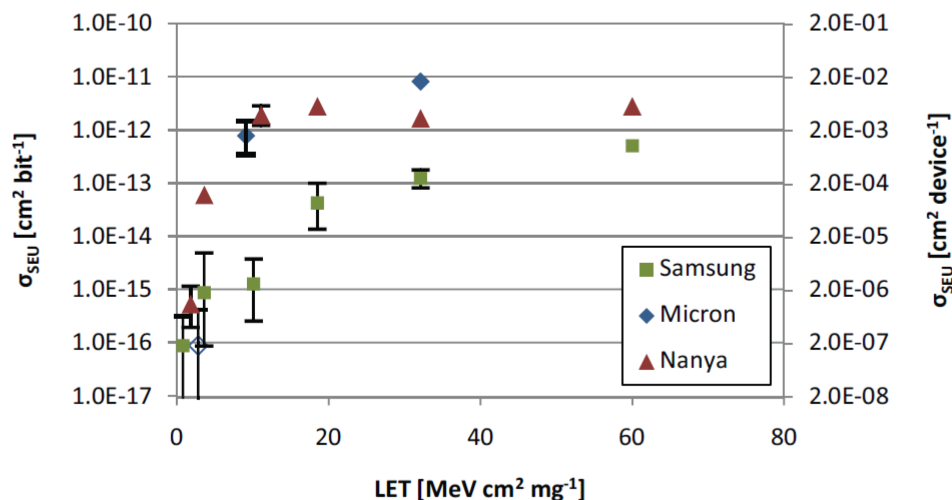

Figure 6-4: SEU cross sections for 2 Gb DDR3 SDRAM in storage mode M3 [PD-03] ; open symbols indicate “no event up to the applied fluence”.

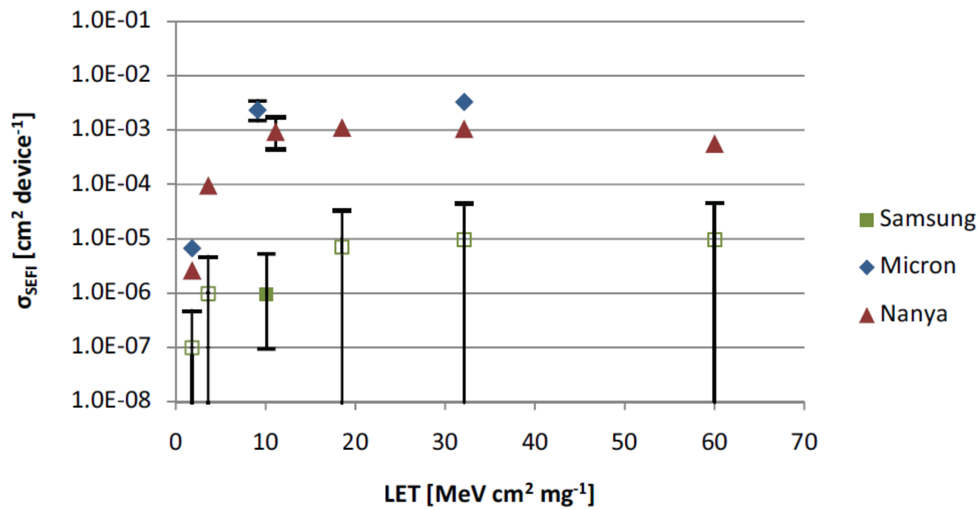

Figure 6-5: Row SEFI cross sections for 2 Gb DDR3 SDRAM in storage mode M3 [PD-03] ; open symbols indicate “no event up to the applied fluence”.

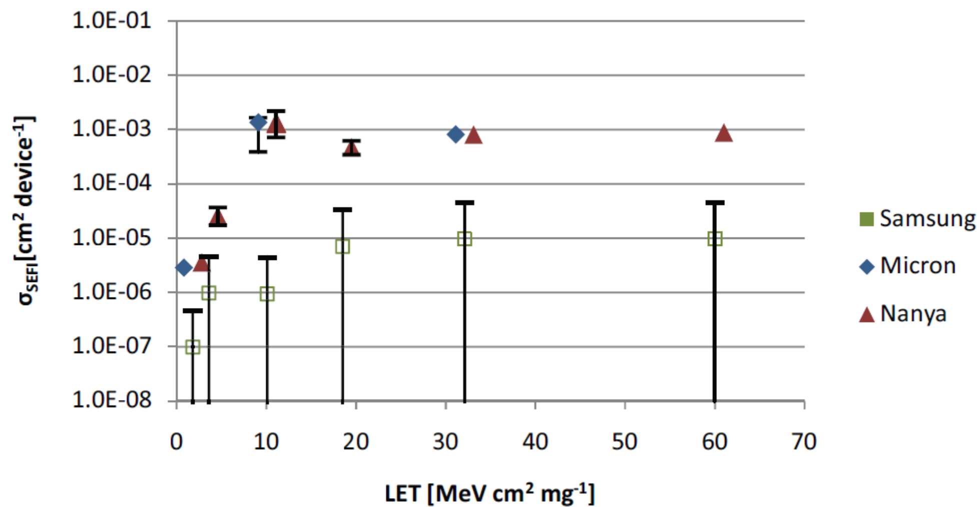

Figure 6-6: Column SEFI cross sections for 2 Gb DDR3 SDRAM in storage mode M3 [PD-03] ; open symbols indicate “no event up to the applied fluence”.

© Airbus DS GmbH

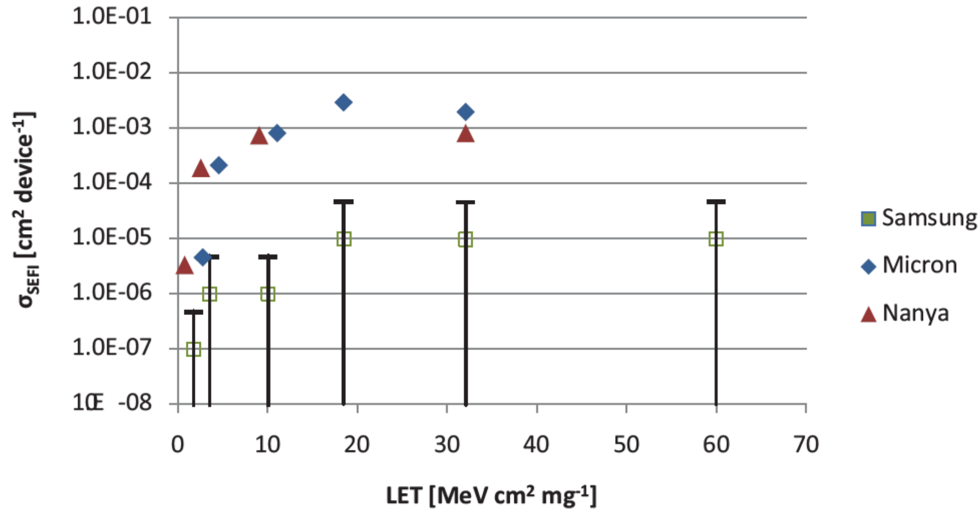

Figure 6-7: Cross sections for column SEFIs in marching mode (M1) ; open symbols indicate “no event up to the applied fluence”.

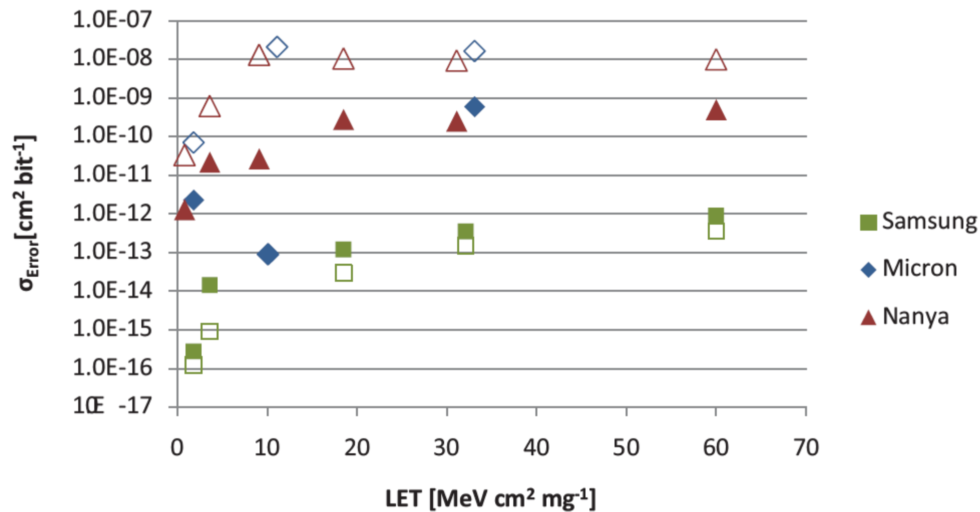

Figure 6-8: Cross sections for bit errors before and after reset (storage mode).Cross sections before reset are denoted by open symbols, cross sections after reset by filled symbols.

After each test, the device was read, reset to cause a reinitialization, and read again. Figure 6-8 shows the cross sections for bit errors (not distinguishing between the different error classes) before and after reinitialization.

Two contrary results have been found:

- For Micron and Nanya parts, the number of errors decreased substantially by a factor of about 200 to 2000 after reinitialization.

- For Samsung parts, the number of errors was either unchanged or increased slightly (by a factor of about 1 to 2) after reinitialization. This corresponds to the fact that Samsung devices showed nearly no SEFIs (Figure 6-6).

No destructive events like Single Event Latch-ups were observed up to maximum LET of 60 $MeVcm^2mg^{-1}$.

Further details on the outcome of this 1st test campaign are provided in [DD-02] and [PD-03].

6.1.3 Further SEE tests on 2Gb and 4 Gb DDR3 SDRAM devices at RADEF and TAMU (SEE_HI_2 to SEE_HI_4)

Further SEE tests on 2Gb and 4 Gb DDR3 SDRAM devices were performed in 2012 at RADEF (SEE_HI_2, SEE_HI_3) and TAMU (SEE_HI_4). As the final outcome of these campaigns was not available yet ([DD-06], [DD-09]) only draft results are presented hereafter.

Type	Density	Vendor	Mask Rev.	DC	Lot / Notes
SEE_HI_2 (RADEF 01/2012)					
K4B2G0846B-HCH9	2 Gb	SAM K	B / 50nm	0949	GLJ423AC
MT41J256M8HX.15E:D	2 Gb	MIC U	D / 50nm	1006	BYFCM91.21
NT5CB256M8BN-CG	2 Gb	NAN TW	B / 50nm	1026	01349199GP
K4B4G0846B-HCH9	4 Gb	SAM K	B / 35nm	1125	GMD02390
EDJ4208BASE-DJ-F	4 Gb	ELP J	A / 4xnm	1044	OWPEY00
SEE_HI_3 (RADEF 04/2012)					
K4B2G0846D-HCH9	2 Gb	SAM K	B / 35nm	1113	GEB701GES
K4B4G0846B-HCH9	4 Gb	SAM K	B / 35nm	1125	GMD02390
EDJ4208BASE-DJ-F	4 Gb	ELP J	A / 4xnm	1044	OWPEY00
SEE_HI_4 (TAMU 12/2012)					
K4B2G0846B-HCH9	2 Gb	SAM K	B / 50nm	0949	GLJ423AC (not thinned, 200µm)
K4B2G0846D-HCH9	2 Gb	SAM K	B / 35nm	1122	GEDN60GKU (not thinned, 200µm)
K4B4G0846B-HCH9	4 Gb	SAM K	B / 35nm	1125	GMD02390 (thinned to 60µm)
K4B4G0846B-HCH9	4 Gb	SAM K	B / 35nm	1204	GKM35990 (thinned to 200µm)
H5TQ4G83MFR-H9CR	4 Gb	SKH K	M / 44nm	1223	DTLB2032HM (thinned to 200µm)

6.1.3.1 SEU

Cross section curves for SEU have been retrieved for all three modes (storage mode M3, read mode M2 and write/read mode M1). In … the different SEU cross section curves of Samsung 4 Gb device (K4B4G0846B) retrieved in the three test campaigns are presented. The SEU cross sections measured at TAMU are about one order magnitude lower than the cross sections from the RADEF campaigns (Figure 6-9). This might have been caused by a difference in DUT temperature: the tests at TAMU were performed in air at a temperature of less than 20°C. The tests at RADEF, on the other

hand, were performed in vacuum. The temperature of the DUT in vacuum is not known, but based on the power dissipation of approximately 150 mW, it is estimated to be about 60°C.

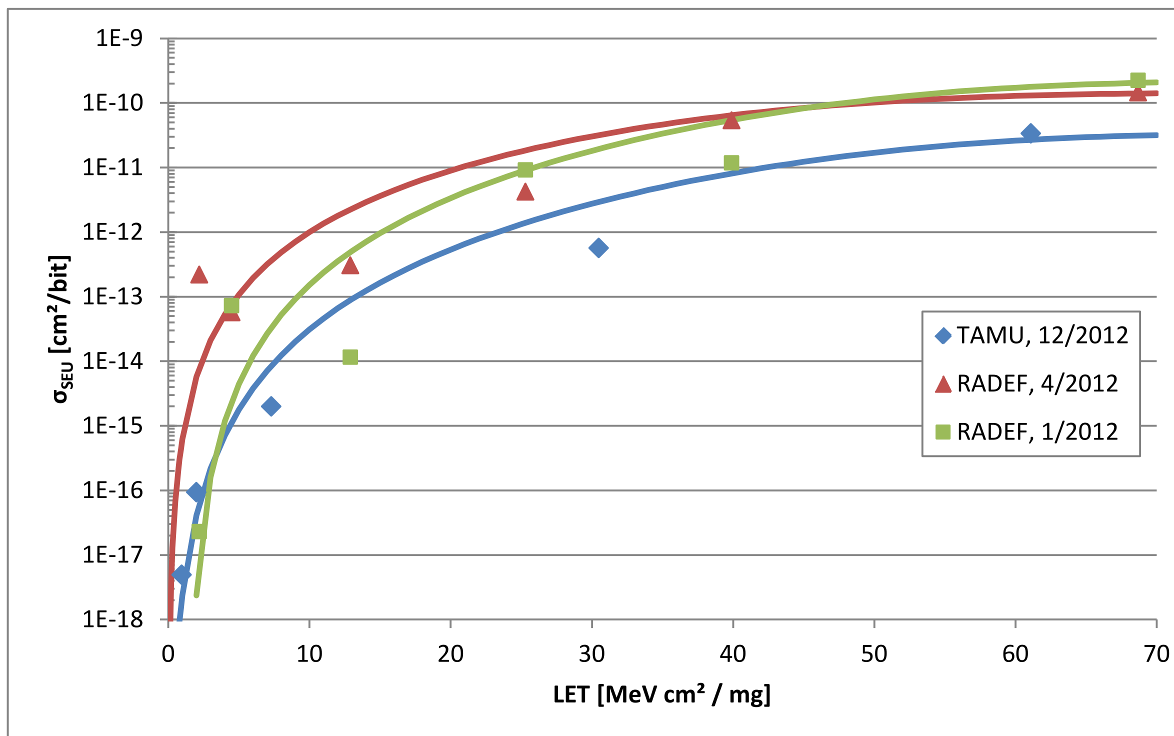

Figure 6-9: Samsung 4 Gb (K4B4G0846B), SEUs, any mode, no software conditioning.

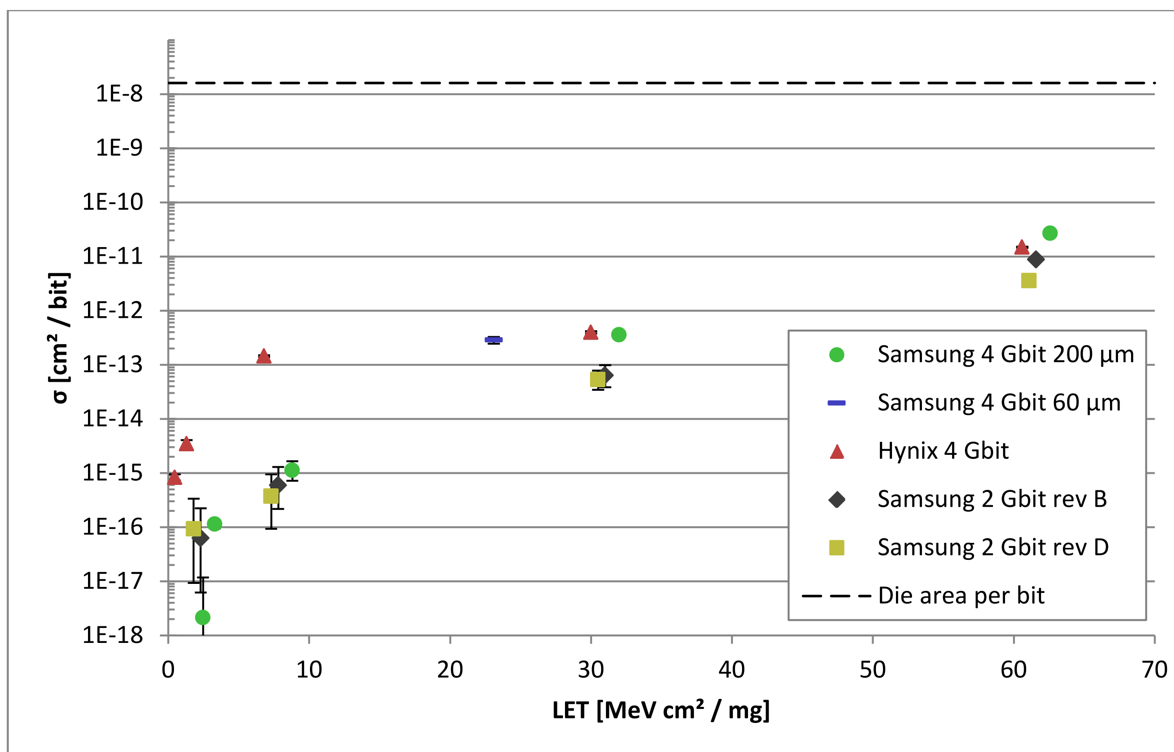

Figure 6-10: SEU cross sections in read mode (M2), TAMU

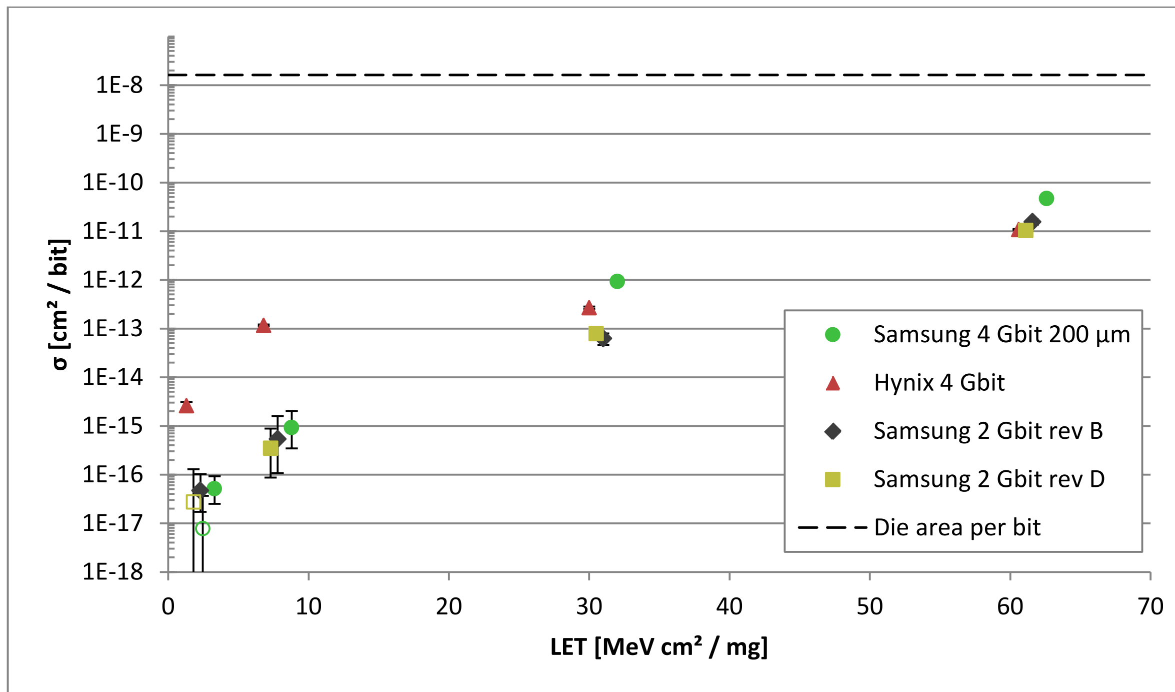

Figure 6-11: SEU cross sections in write/read mode (M1), TAMU

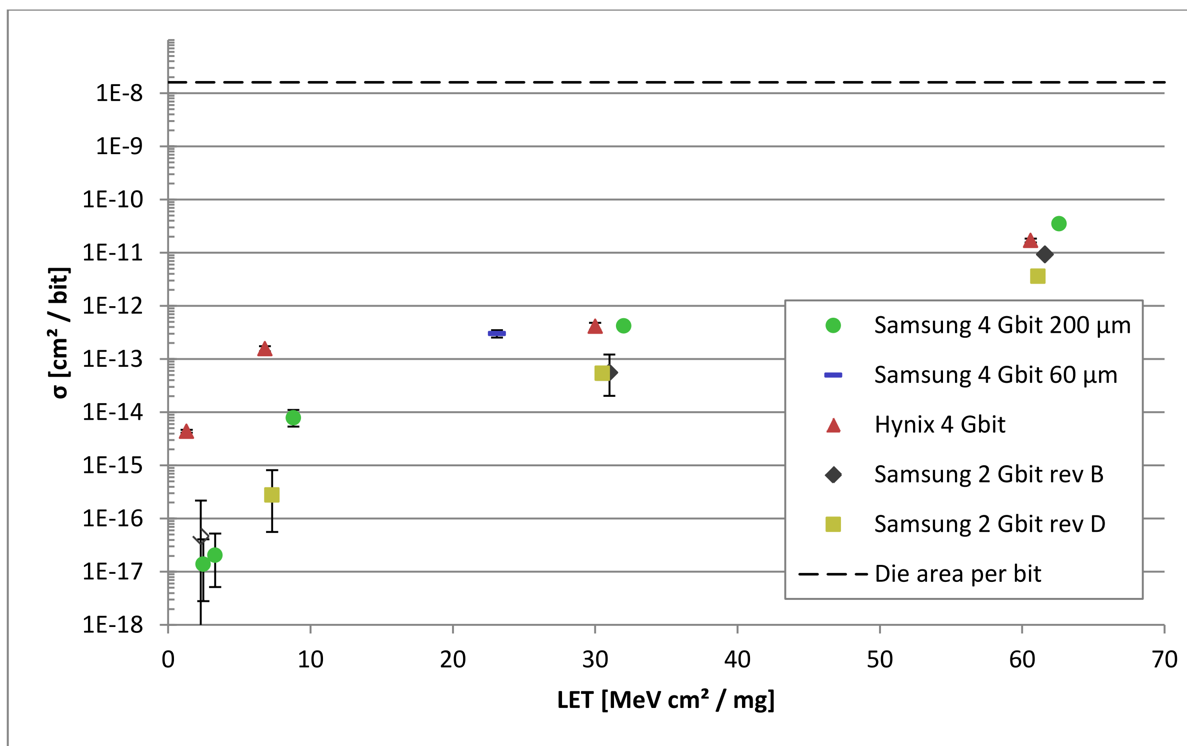

Figure 6-12: SEU cross sections in storage mode (M3), TAMU

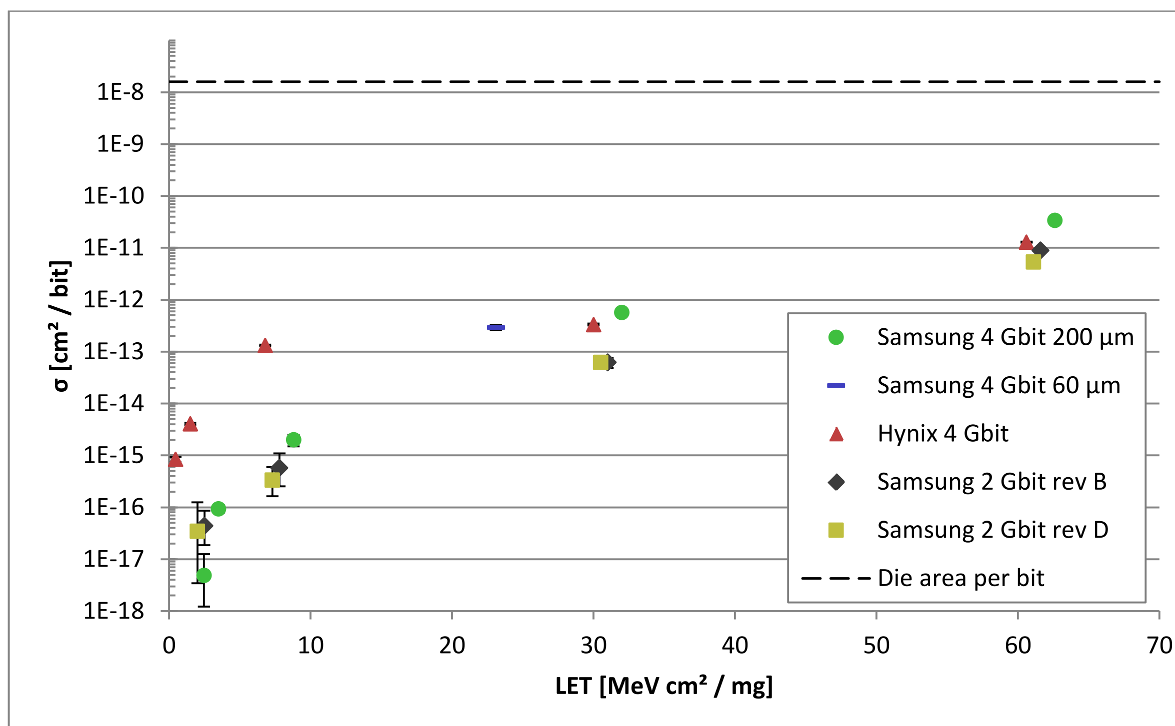

Figure 6-13 SEU cross sections of all modes, TAMU

In Figure 6-9 to Figure 6-13 the retrieved SEU cross sections at SEE_HI_4 campaign (TAMU 12/2012) are presented in detail. The SEU cross sections of Samsung 2 Gb device with mask revision D (35nm) and Samsung 4 Gb device with mask revision B (35nm) fit well together. The Hynix 4 Gb device showed a lower onset LET<1 $MeVcm^2mg^{-1}$ than the Samsung devices. Nevertheless, the saturation cross section is in the same range.

6.1.3.2 Row SEFI

Additional to SEU all DDR3 SDRAM showed row SEFI even at low LET. In contrast to SEU investigations the SEFI cross sections of all three campaigns fit much better, the differences are within the statistical errors (Figure 6-14).

In contrast to SEU the onset LET of the Hynix 4 Gb SDRAM has been measured as higher than for the Samsung devices. In Figure 6-15 to Figure 6-18 detailed row SEFI cross sections at different test modes at SEE_HI_4 campaign (TAMU 12/2012) are presented.

© Airbus DS GmbH

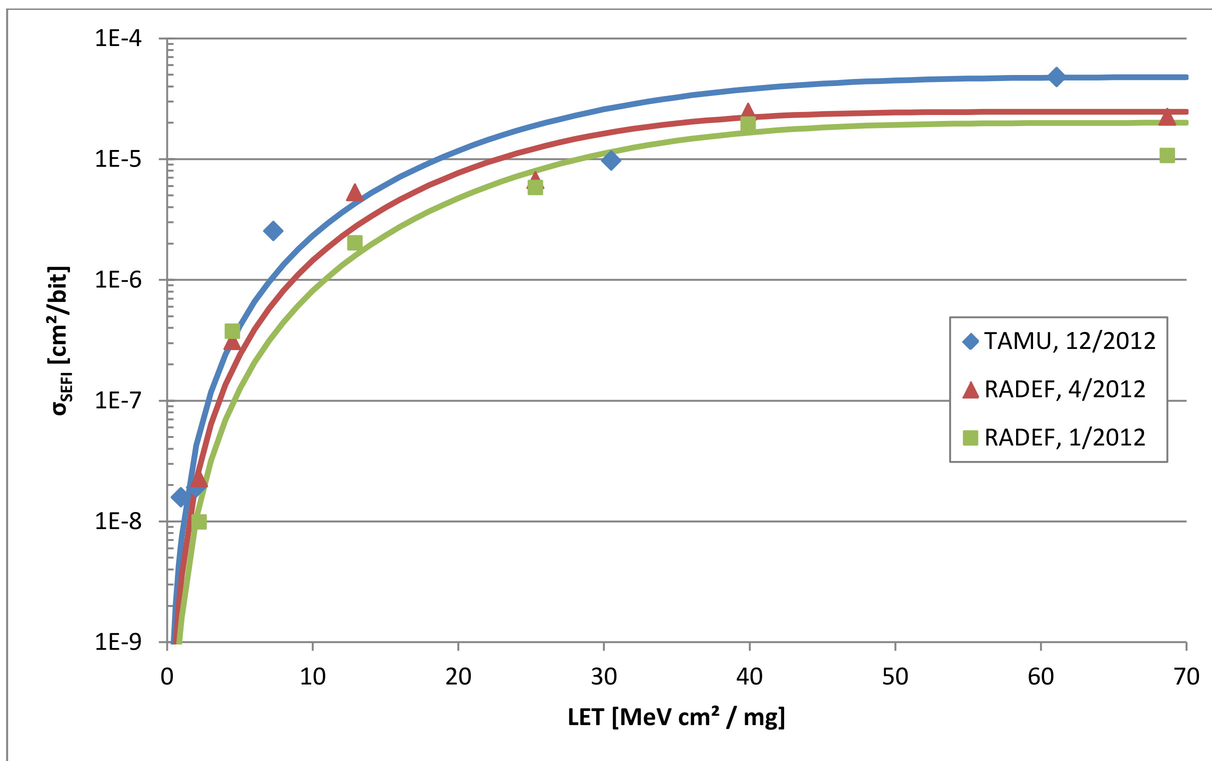

Figure 6-14: Samsung 4 Gbit, row SEFIs, any mode, no software conditioning.

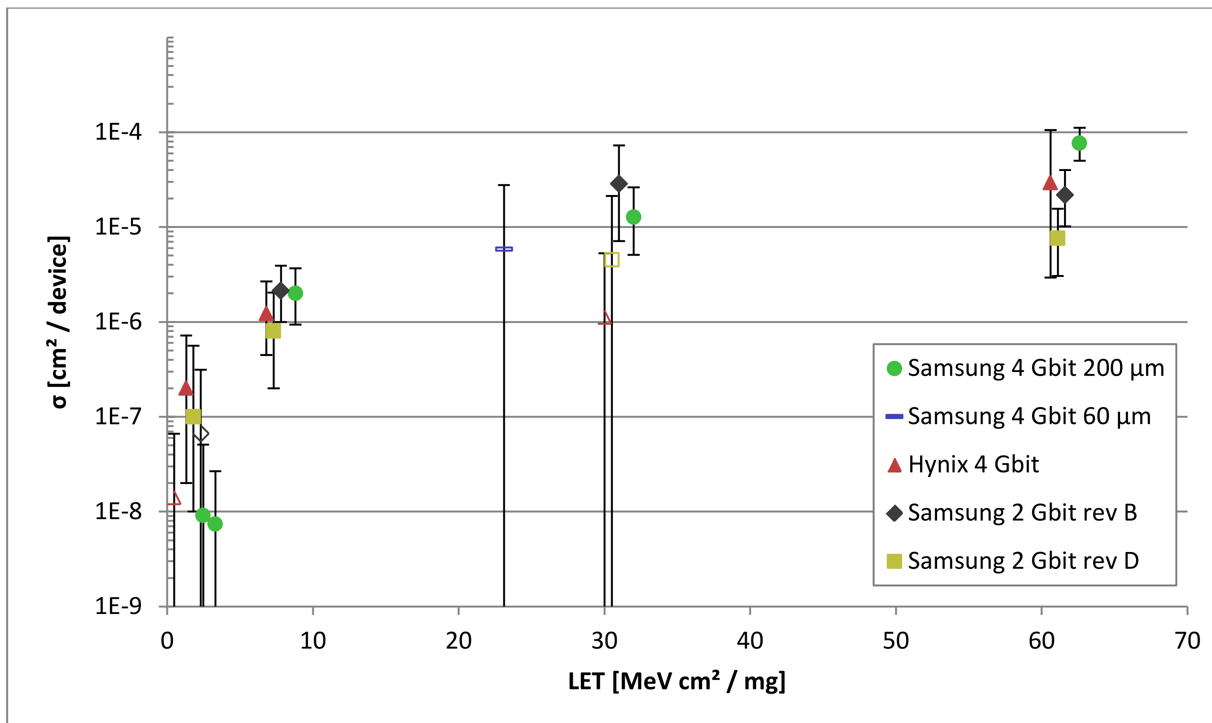

Figure 6-15: Row SEFI cross section in read mode (M2), TAMU, open symbols indicate "no event up to the applied fluence".

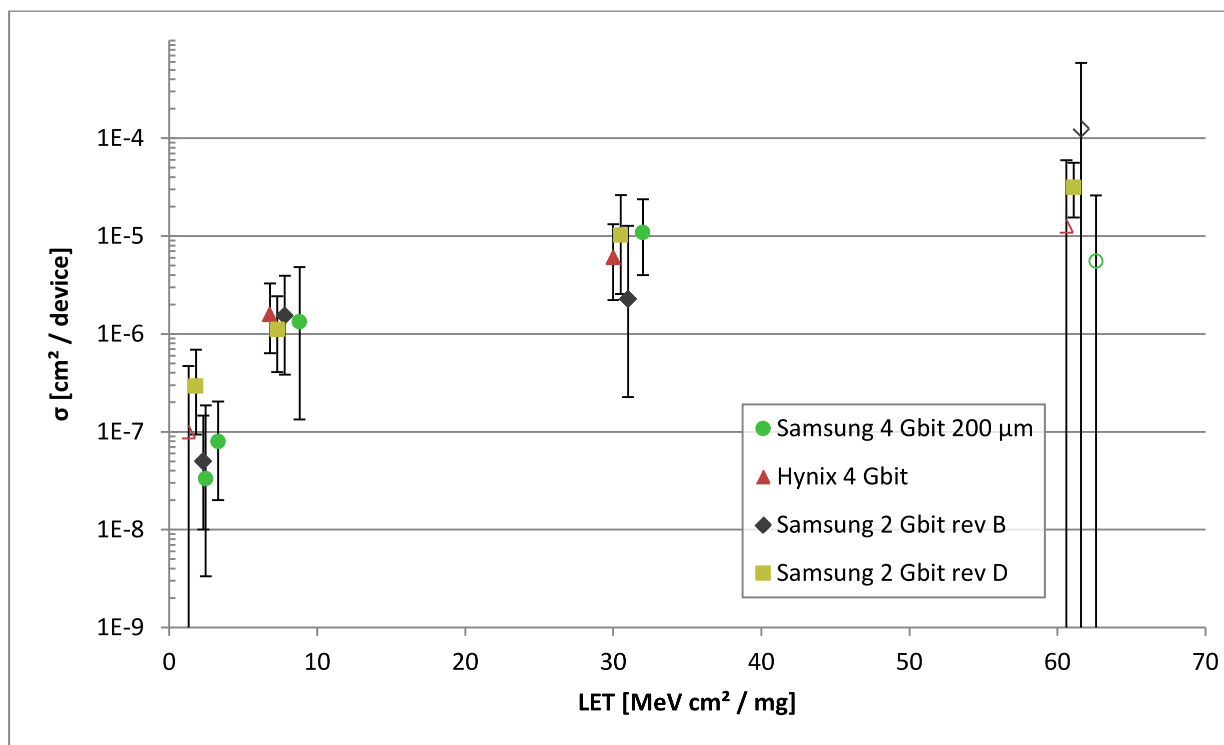

Figure 6-16: Row SEFI cross section in write/read mode (M1), TAMU, open symbols indicate "no event up to the applied fluence".

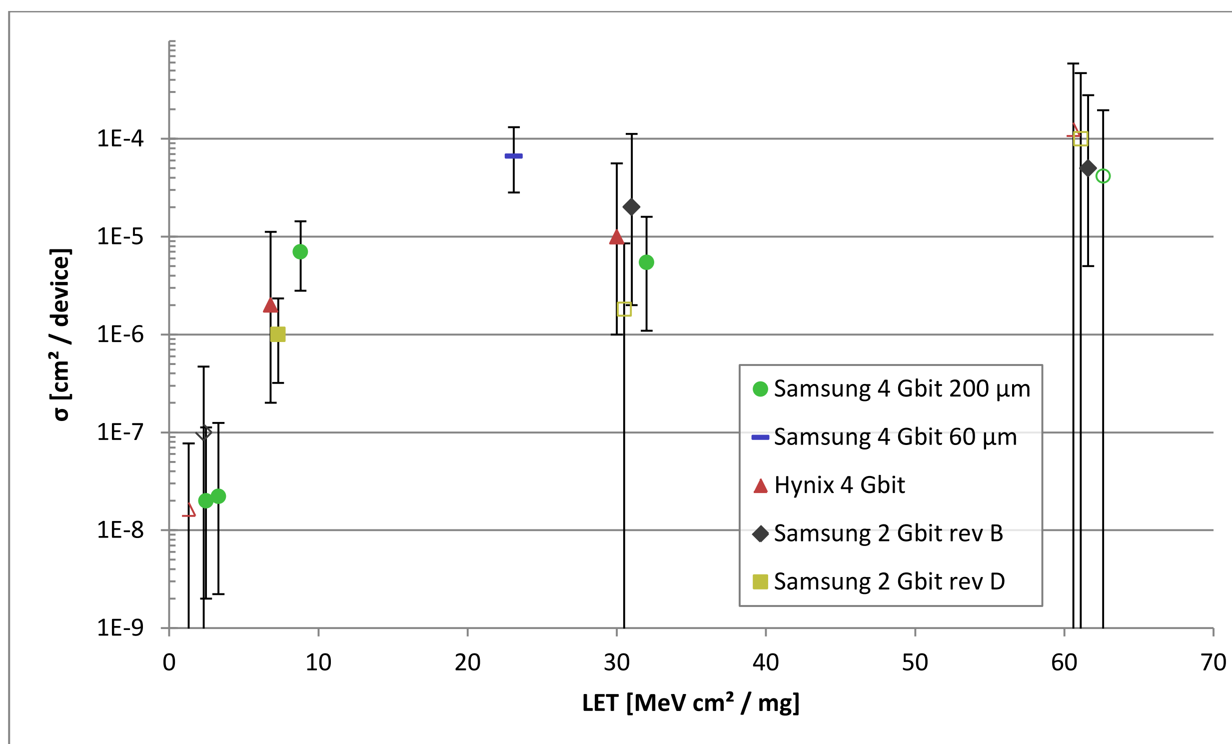

Figure 6-17: Row SEFI cross section in storage mode (M3), TAMU, open symbols indicate "no event up to the applied fluence".

© Airbus DS GmbH

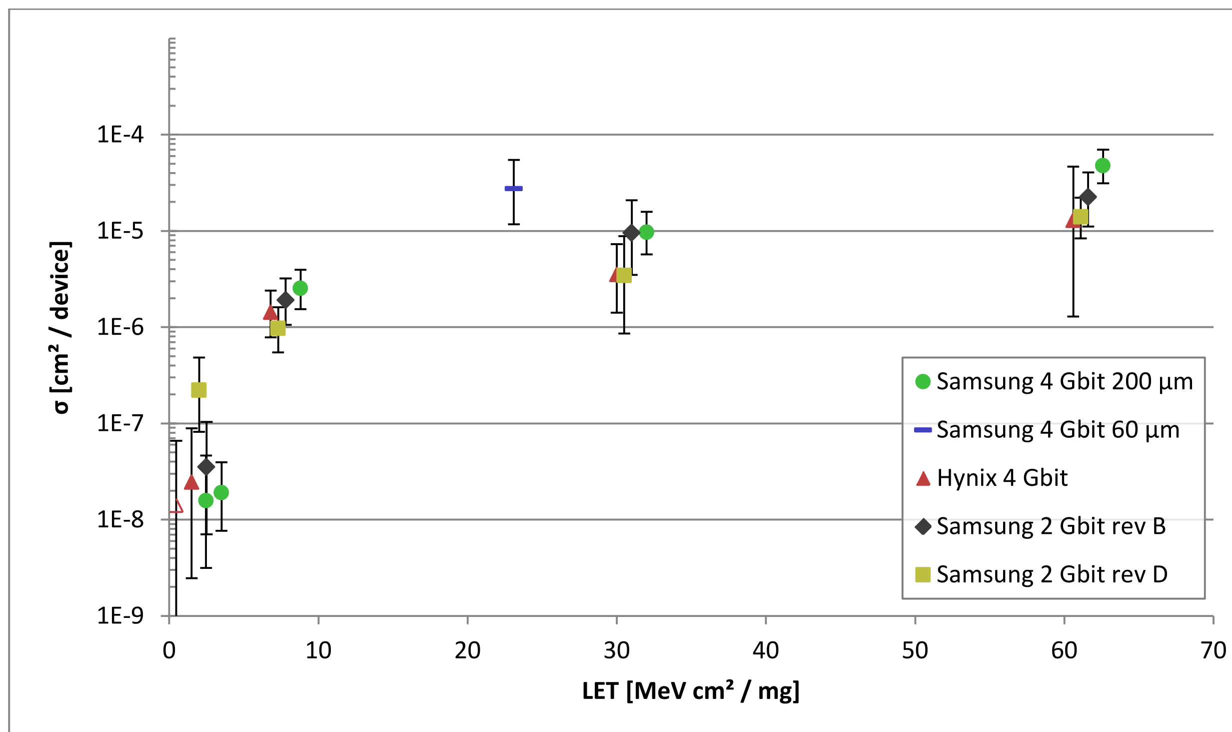

Figure 6-18: Row SEFI cross section of all modes, TAMU, open symbols indicate "no event up to the applied fluence".

6.1.3.3 Column SEFI

In contrast to row SEFI even at lowest LET, column SEFI were only observed for a very few LET for Hynix 4 Gb and Samsung 2 Gb (mask revision B) DDR3 SDRAM devices. In Figure 6-19 to Figure 6-22 the detailed column SEFI cross sections retrieved at the TAMU campaign are presented.

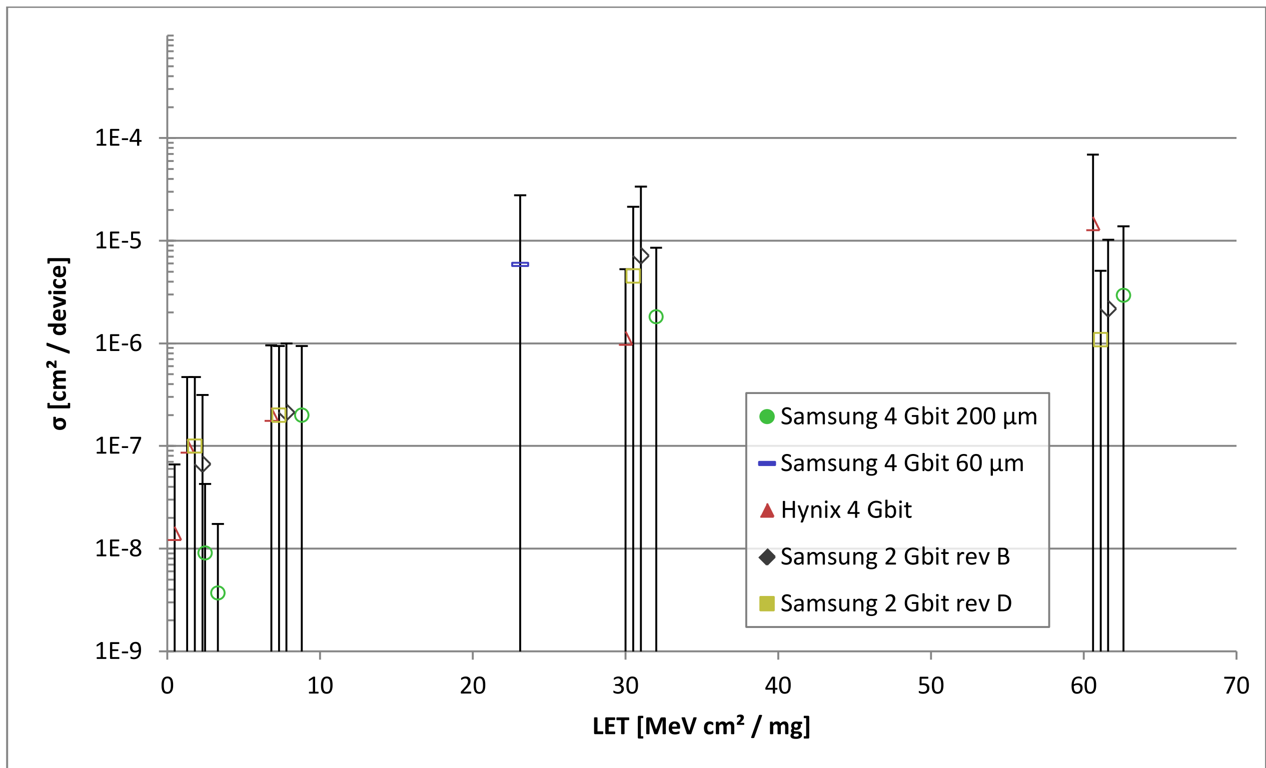

Figure 6-19: Column SEFI cross sections in read mode (M2), TAMU, open symbols indicate "no event up to the applied fluence".

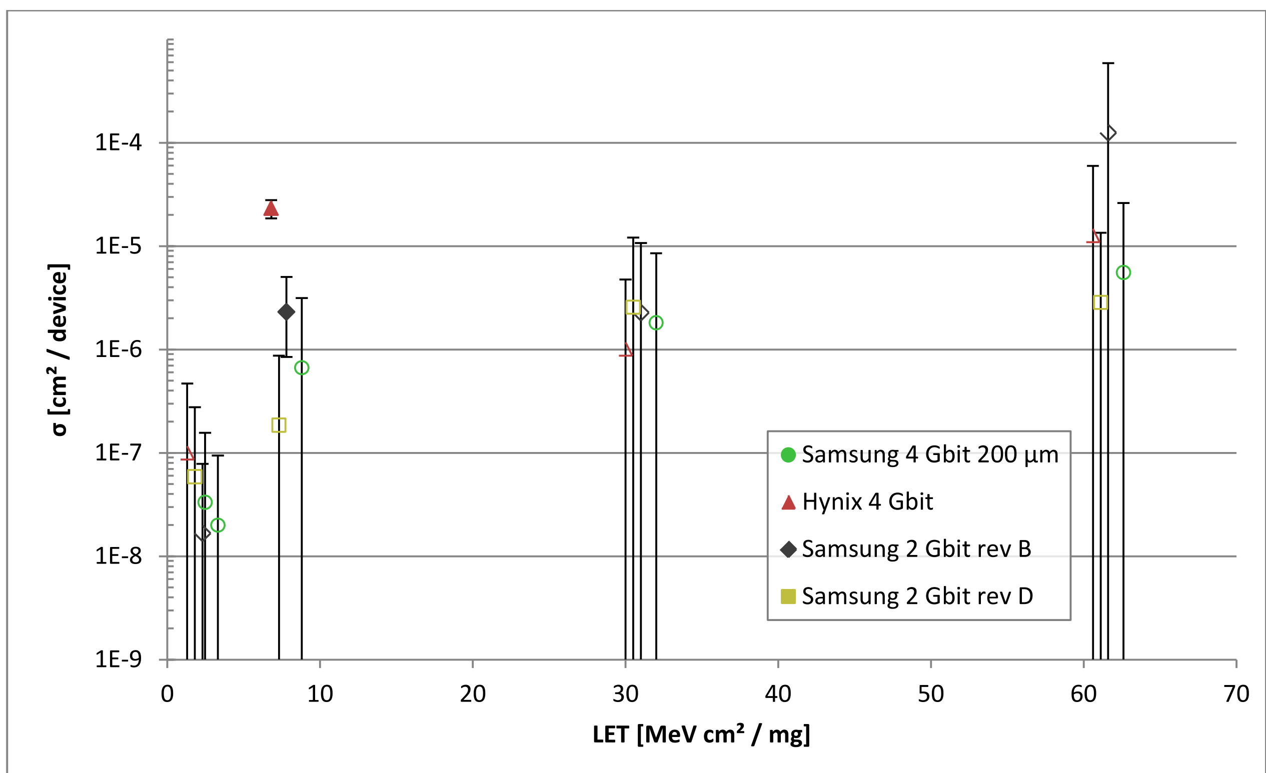

Figure 6-20: Column SEFI cross sections in write/read mode (M1), TAMU, open symbols indicate "no event up to the applied fluence".

© Airbus DS GmbH

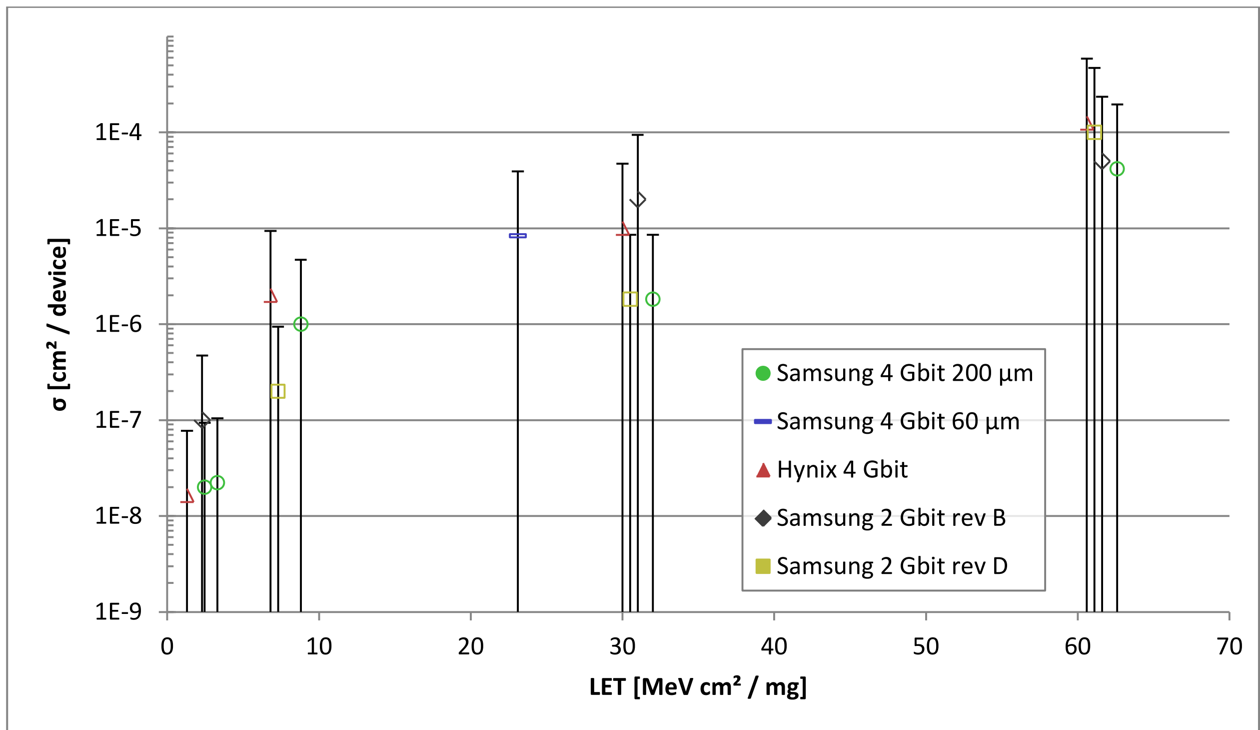

Figure 6-21: Column SEFI cross sections in storage mode (M3), TAMU, open symbols indicate "no event up to the applied fluence".

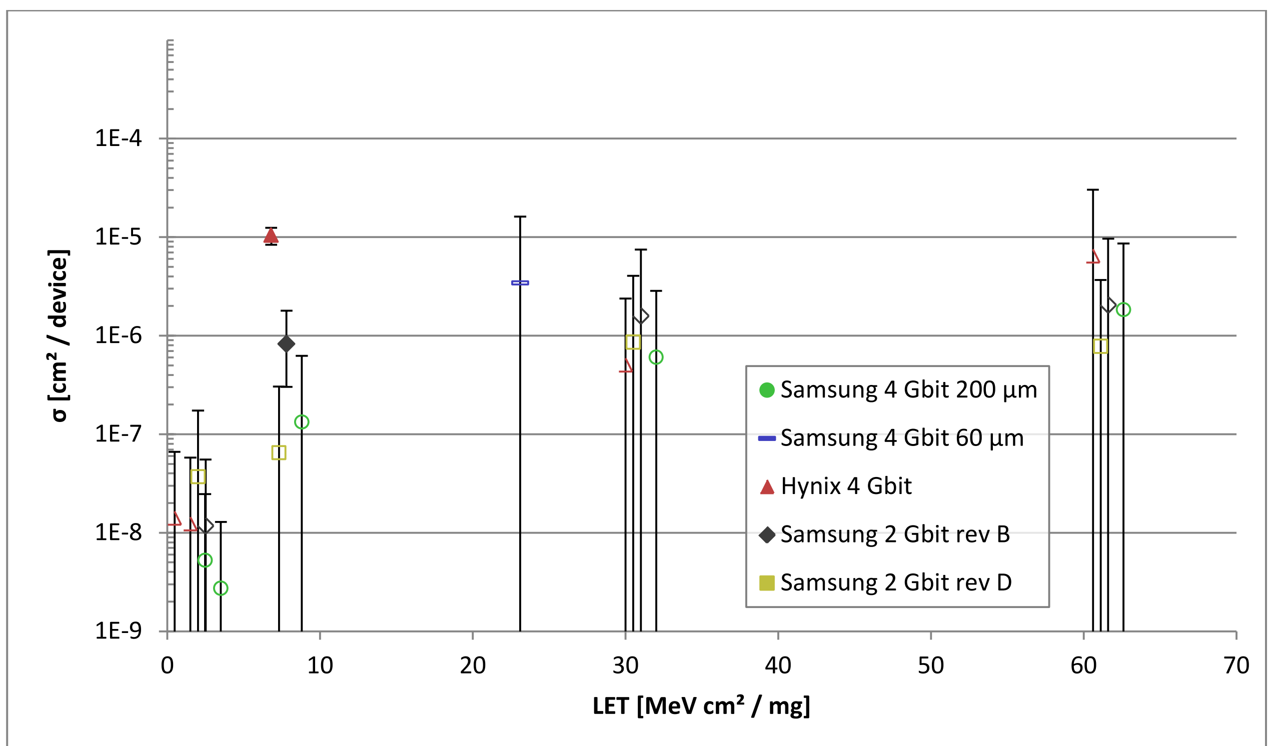

Figure 6-22: Column SEFI cross sections of all modes, TAMU, open symbols indicate "no event up to the applied fluence".

6.1.3.4 Device SEFI

Most severe SEFI, persistent device SEFI have been observed for all DDR3 SDRAM devices even at low LET. These SEFI can be stopped by H/W reset or power cycling only, resulting in data loss.

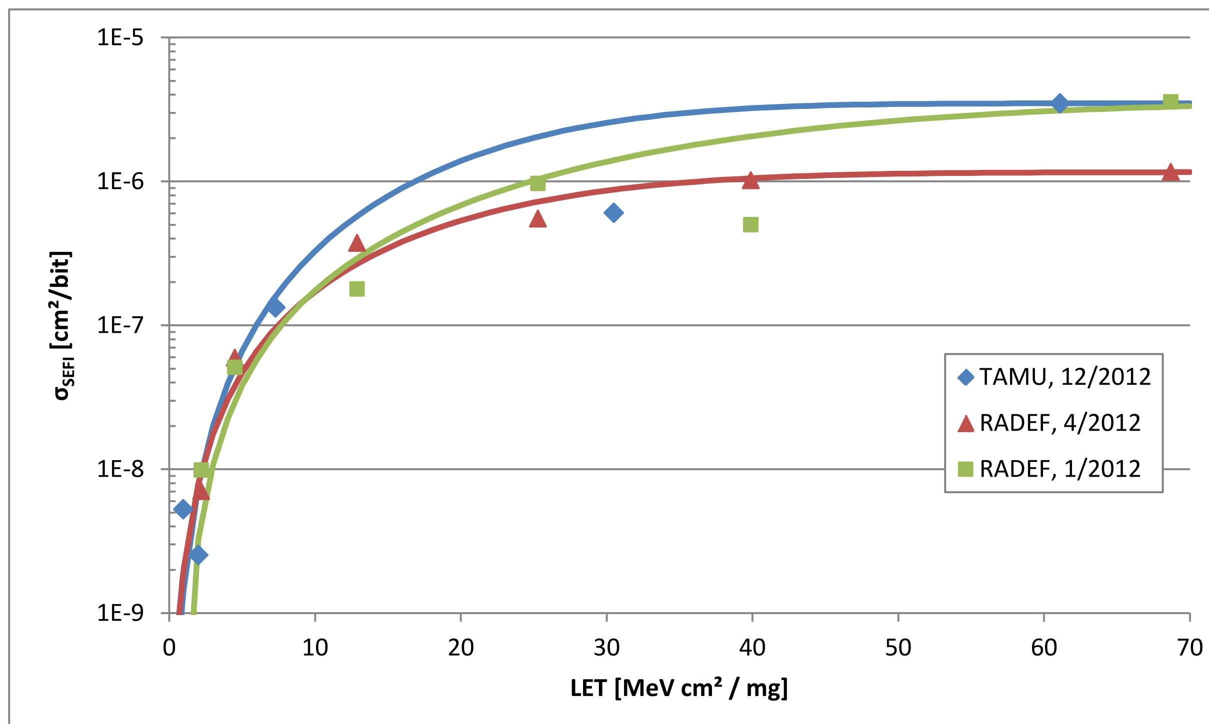

Figure 6-23: Samsung 4 Gbit, device SEFIs, any mode, no software conditioning.

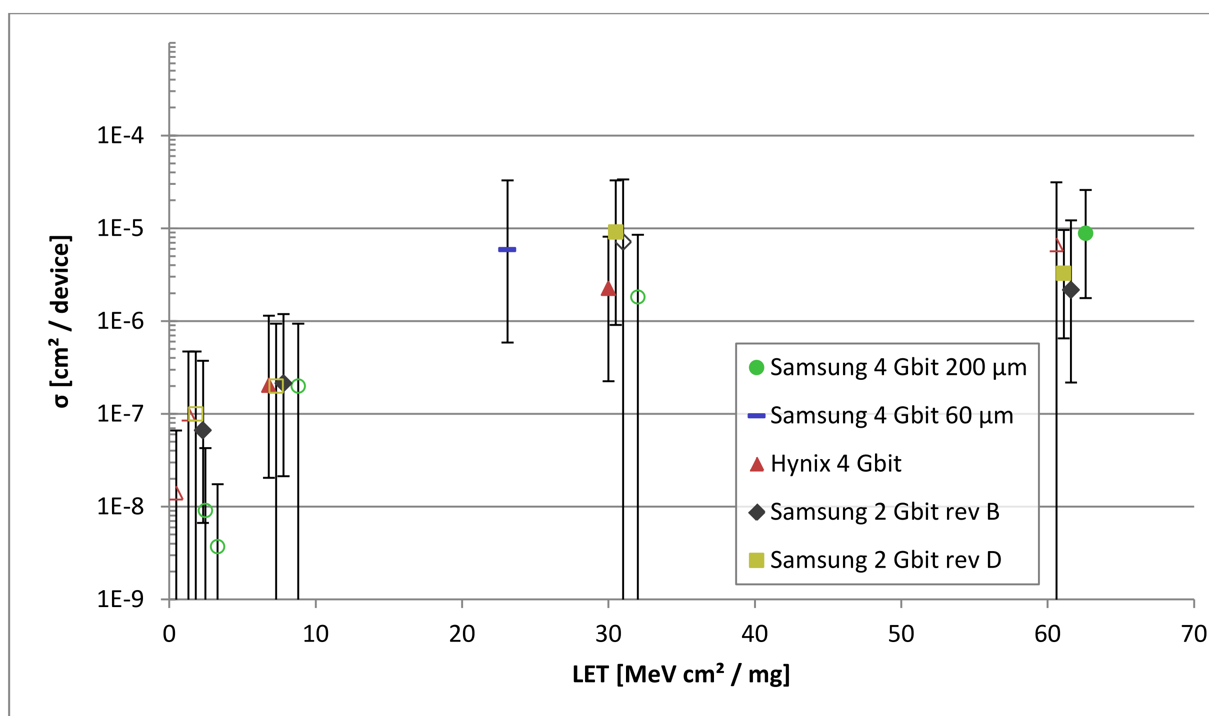

Figure 6-24: Device SEFI cross sections in read mode M2, TAMU, open symbols indicate "no event up to the applied fluence".

© Airbus DS GmbH

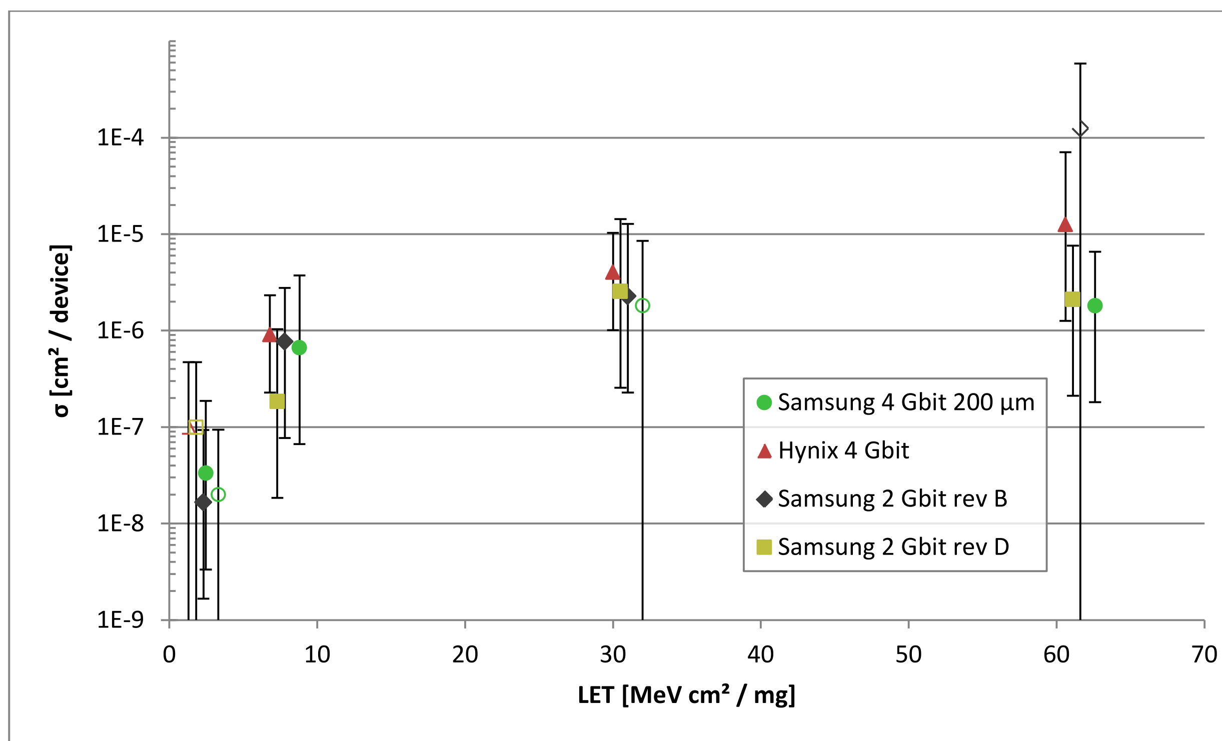

Figure 6-25: Device SEFI cross sections in write/read mode M1, TAMU, open symbols indicate "no event up to the applied fluence".

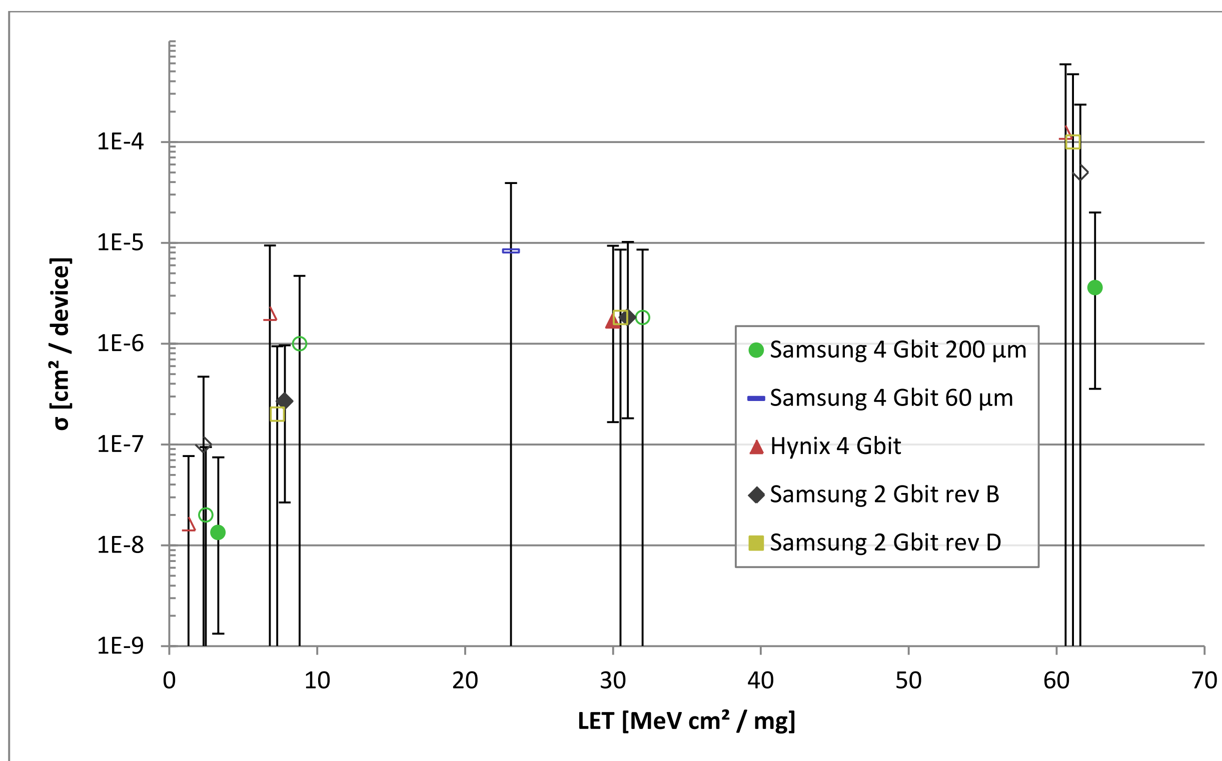

Figure 6-26: Device SEFI cross sections in storage mode (M3), TAMU, open symbols indicate "no event up to the applied fluence".

© Airbus DS GmbH

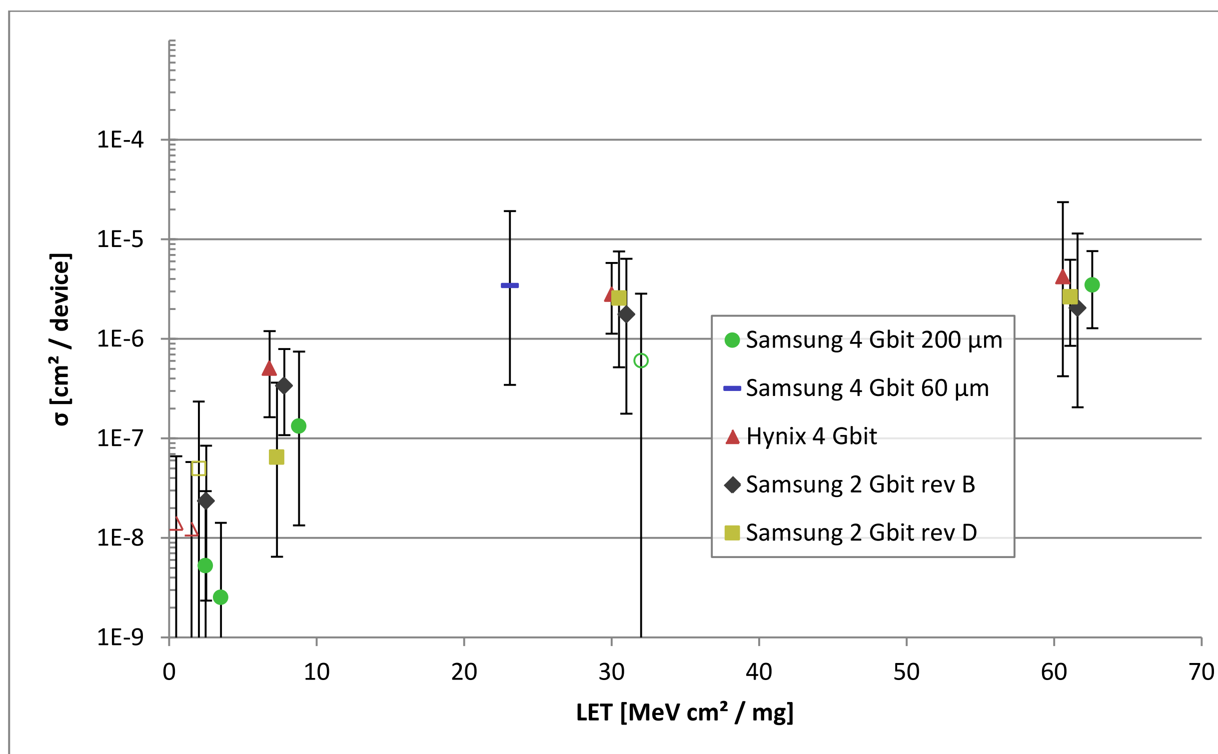

Figure 6-27: Device SEFI cross sections for all modes, TAMU, open symbols indicate "no event up to the applied fluence".

6.1.3.5 Destructive Failures

In order to test for single-event latch-up (SEL) events, five 4 Gbit DUTs (two from Samsung and three from Hynix) were heated to 80 °C and irradiated with $10^7 \cdot cm^{-2}$ 61.1 MeV cm^2 mg^{-1} Xenon ions at high range facility (TAMU) while operating them in write/read mode. The heating was performed using the air flow from a heat gun and monitored with four temperature sensors arranged around the DUT.

No latch-up events were observed for any of the devices at the given LET.

6.1.3.6 Current measurements during irradiation

For the single-event latch-up test (§6.1.3.5), the current was logged with a sampling rate of 1 Hz before, during, and after the irradiation.

The idle current is the current while only performing the required idle operations – refresh (every 7.8µs), periodic read (required by the Xilinx® PHY, every 1 µs) and short ZQ calibration (every 128ms). This value does not represent any of the *IDDx* values defined in the specification.

No significant permanent increase in idle current was observed for any of the devices at the given LET. After the end of the irradiation, the idle current drops to its pre-irradiation value very quickly.

© Airbus DS GmbH

SEE_HI_4 campaign (TAMU) was the first test campaign where current measurement have been performed. While the sample rate was too low to analyze the current in detail, there are still some interesting findings:

- Under irradiation, the idle current (≈ 20mA without irradiation) may jump to values as high as 200mA (e. g. Hynix, sample 3, at 5s), remain there for some time and return to a lower value or the pre-irradiation value some time (in the order of 1 minute) later (e. g. Samsung, sample 2, starting at at 50s).
- No idle current lower than the idle current without irraidation has been observed.
- The read and write current offset over the idle current can also be severly increased, over the respective values without irradiation (e. g. Hynix, sample 2, at 80s). Operating currents as high as 475mA have been observed (Hynix, sample 1, at 356s).
- The read and write current offset over the idle current can also be lower than the respective values without irradiation (e. g. Samsung, sample 1, starting at 120s). Further investigation is required in order to rule out the possibility that this is a sampling artifact.

These measurements were performed at quite high LET and flux. If the increase in current also occurs at lower LET and/or flux, this has severe implications for space applications: if a significant fraction of the devices in a large memory modules has in increased idle and/or operating current, the power supply may not be sufficient.

For further details see [DD-09].

6.2 SEE Protons Test Results

In March 2014 one Protons SEE test campaign has been performed in the frame of Rad Hard Memory study (SEE_P_1, [DD-17], [DD-19] at PIF in PSI, Villigen, Switzerland. The used test bed is described in §4.1.1. Protons energies of 21, 33, 42, 60, 100 and 235 MeV have been used for test. In Table 6-1 and Figure 6-28 the properties of used proton energies are listed.

Table 6-1: Properties of used proton energies

Energy [MeV]	LET in Si (@surface) [MeV cm^2 mg^{-1}]	Range in Si [µm]	Deposited dose per 10^{10} pcm^{-2} [rad(Si)]
21	1.94E-02	2595	6.98E+03
33	1.35E-02	5793	4.86E+03
42	1.13E-02	8907	4.07E+03
60	8.60E-03	16850	3.09E+03
100	5.86E-03	41620	2.11E+03
235	3.29E-03	185600	1.18E+03

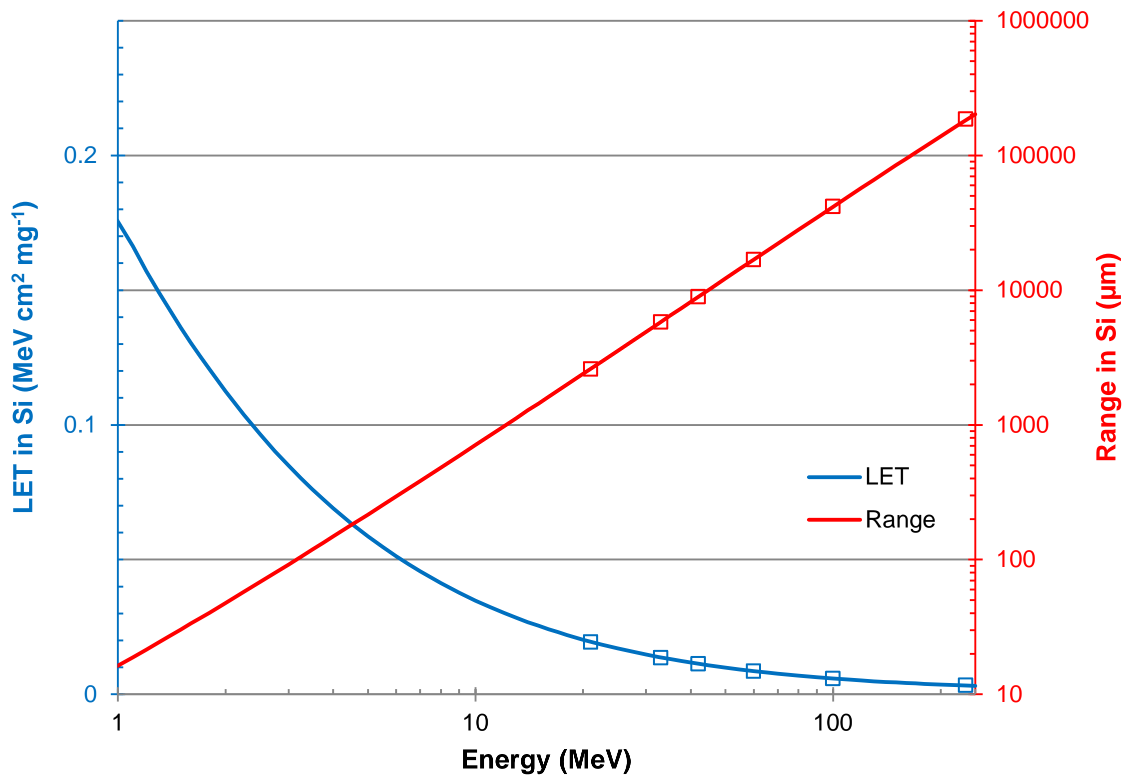

Figure 6-28: Protons energy vs. LET and range in Silicon (according SRIM).

Three different device types From Samsung, SK Hynix and Micron were tested. All parts remained unchanged in their original package and were soldered on SODIMM modules:

Type	Density	Vendor	Mask Rev.	DC	Manuf. Lot
K4B4G0846B-HCH9	4 Gb	SAM K	B / 35nm	1204	GMK3599Q
H5TQ4G83MFR-H9CR	4 Gb	SKH K	M / 44nm	144A	DTLB0213HA
MT41J512M8RH-93:E	4 Gb	MIC	E / 30nm		3LE22

The DUT were tested in two different modes, Storage Mode and Read Mode (see §4.2.3). They were operated at 333 MHz with a pseudo-random pattern without any software conditioning. The deposit dose on each part has been limited to less than 40 krad(Si) for the Samsung und Micron DUTs and about 80 krad(Si) for SK Hynix DUTs at maximum.

6.2.1 Error Pattern

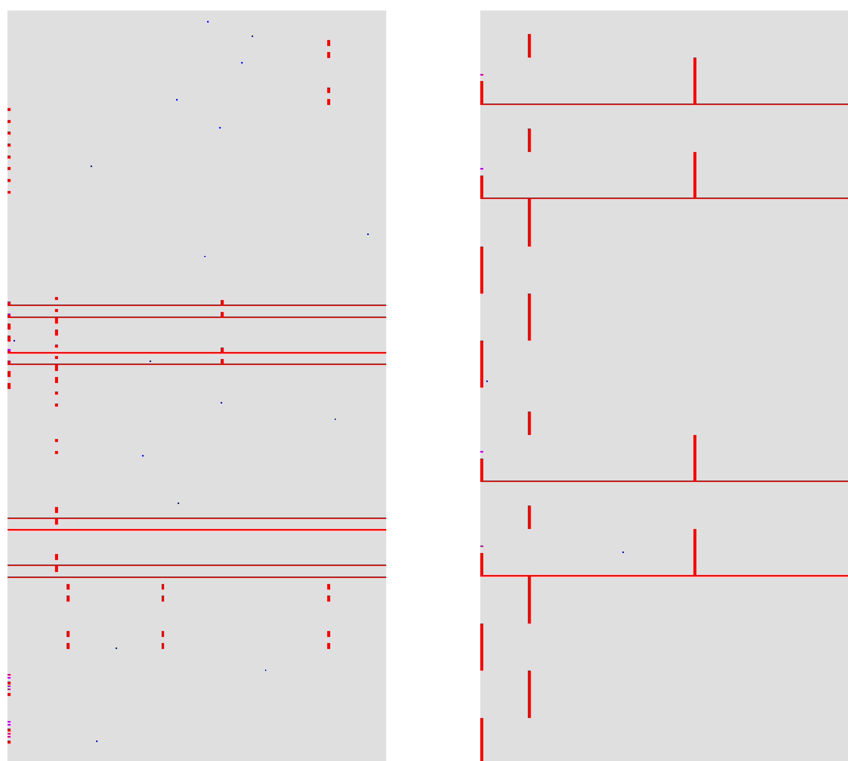

Figure 6-29: left: Row errors typically occur in patterns. Each horizontal line actually consists of two consecutive rows. Micron DUT in storage mode at 60 MeV
right: Close-up of bank #4 in the same run as shown left picture. The column error patterns are linked to the row error patterns

Column errors typically are non-contiguous and affect whole bursts, i. e. the same consecutive 8 columns are affected in a range of rows.

For Micron devices, row errors often occur in groups, as shown in Figure 6-29 (left). Each horizontal line in this figure actually consists of two consecutive rows of errors. In read mode, groups of four pairs typically appear simultaneously (Figure 6-29 (left) contains two such groups).

Figure 6-29 (right) shows a close-up of one eighth of the device address space (one bank, specifically bank #4) of the same run in Figure 6-29 (left). The column errors display a periodicity that coincides with the row error periodicity.

Errors in row and column SEFIs do not have a preferred direction, even for Samsung and Hynix devices, where almost all SEUs have the same direction.

6.2.2 SEU

In Figure 6-30 the observed SEU cross sections (including stuck bits) for read mode and in Figure 6-31 for storage mode respectively are provided. In general, they are very similar for read mode and storage mode. This is plausible because dynamic memories perform a periodic refresh operation (every 7.8 µs in the case of DDR3) which opens and pre-charges banks, similar to what happens during a read operation.

The SEU cross section remains well below the die area per bit (≈$2 \cdot 10^{-10}$ cm^2) for all devices (see Figure 6-32). This is in contrast to heavy-ion tests, where the SEU cross section was close to the die area per bit for high LET ions. Furthermore, at least for Hynix and in particular for Micron DDR3 SDRAM, the SEU cross sections are increasing at lower energies. In contrary, there is no obvious trend for the Samsung devices.

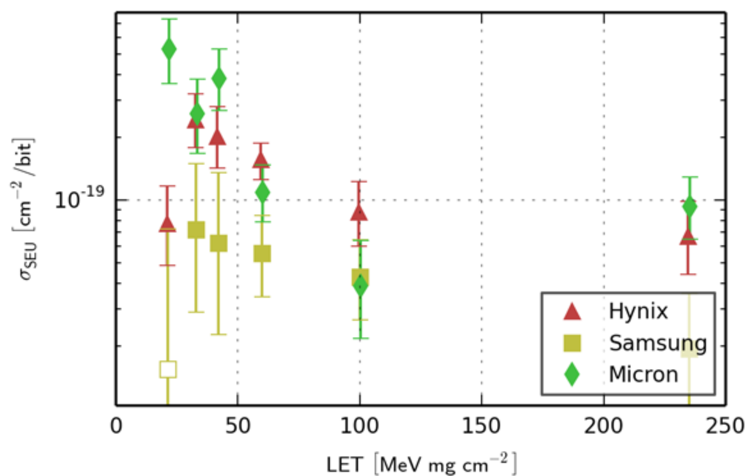

Figure 6-30: SEU cross section in read mode.

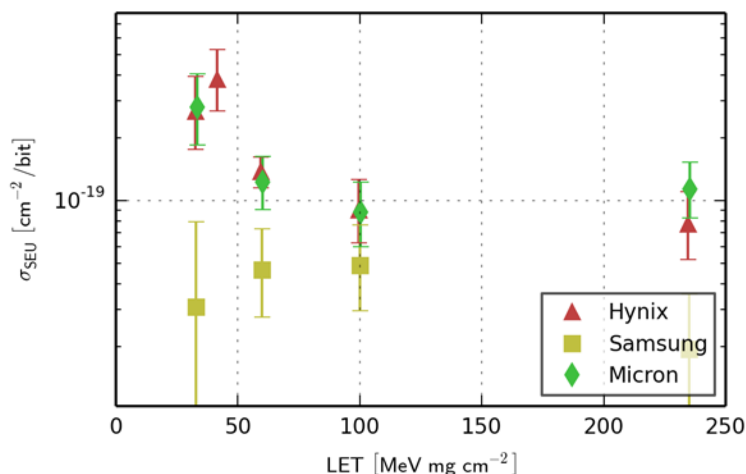

Figure 6-31: SEU cross section in storage mode

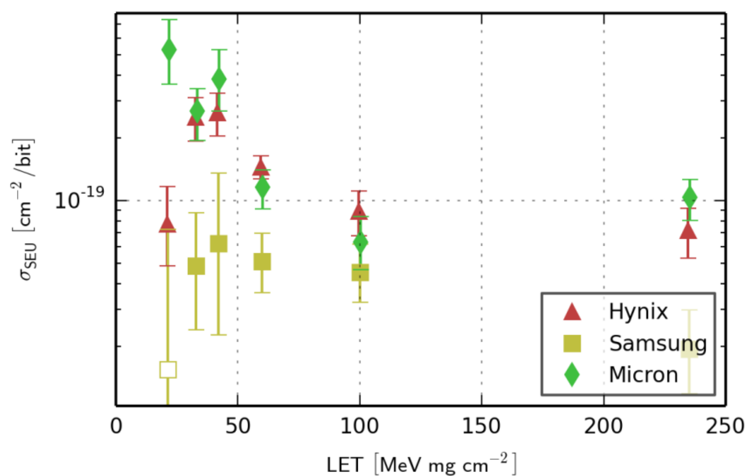

Figure 6-32: SEU cross section in any mode

Errors can either be in the 0 → 1 direction (i. e. bits written as 0, but read as 1 after irradiation) or in the 1 → 0 direction. Figure 6-33 shows the share of 0 → 1 errors (for SEUs only) for the different parts vs. proton energy. The Hynix and Samsung parts have almost only 1 → 0 errors (less than 1% 0 → 1 errors). For the Micron parts, the share of error directions is approximately equal. Very likely, this indicates an equal distribution of logical “1” states to physical “0” and “1” states.

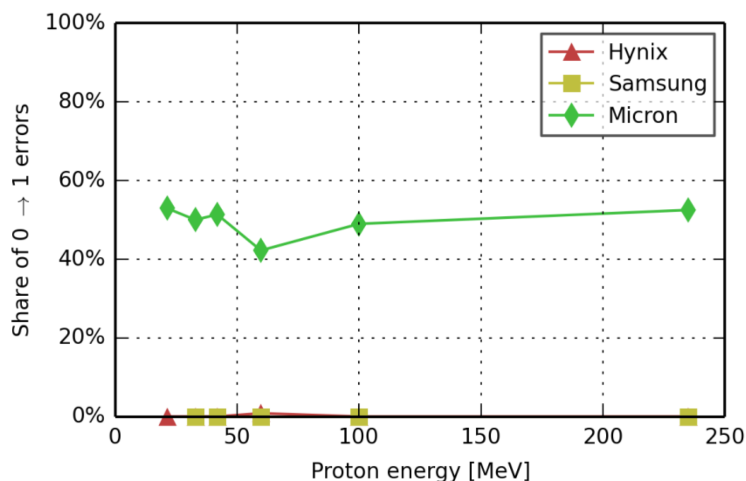

Figure 6-33: Direction of SEU (0→1 vs. 1→0)

6.2.3 SHE (stuck Bits)

To determine the number of SHE (Single Event Hard Error, stuck bits) ,the DUTs were written and read before each irradiation. Additionally, the same operation was performed after each set of irradiations with one DUT.

SHE are created for all part types and at all energies. It is, however, not possible to reliably determine a cross section because (a) the number of SHE is very low and (b) some of the SHE anneal quickly: for some irradiation runs, the number of SHE was lower after the irradiation than before (i. e. the number of SHE that annealed during the irradiation exceeds the number of newly created SHE).

Long-term annealing measurements could not be performed because the DUTs, having been activated by irradiation, had to remain at PSI.

Despite the fact that a proper analysis of SHE was not possible, some qualitative conclusions can still be reached:

- Generally, the number of SHE seems to increase slightly with proton energy. This is in contrast to the SEU cross section, which decreases with proton energy.
- The Micron parts are the most sensitive parts, with an estimated cross section of $5 \cdot 10^{-20}$ cm^2 per bit at 235 MeV.
- The Samsung parts are the least sensitive parts: no SHE were observed except 2 SHE at 235 MeV, corresponding to a cross section of $2 \cdot 10^{-21}$ cm^2 per bit. This corresponds to the fact that the Samsung parts are also the least sensitive to SEUs. These 2 SHE annealed within 4 minutes.

6.2.4 Transient SEFI

In contrary to the Samsung and Hynix DDR3 devices with no or only a very few Row SEFI, Micron DDR3 devices showed Row SEFI at all energies ≥ 33 MeV. In Figure 6-34 to Figure 6-36 the respective Row SEFI cross sections are provided.

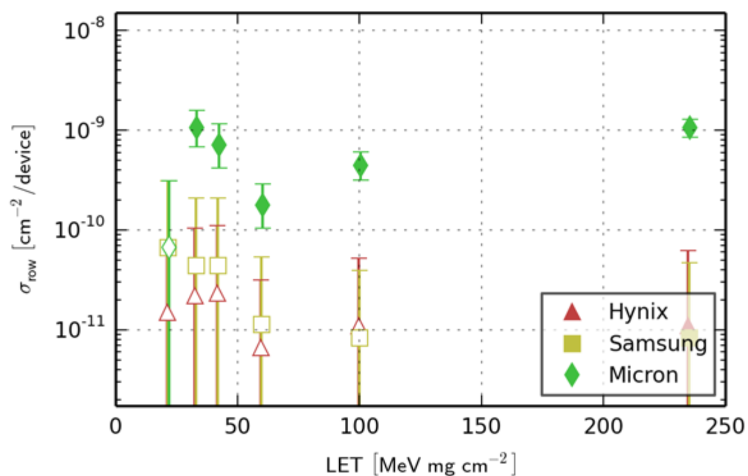

Figure 6-34: Row SEFI cross section in read mode

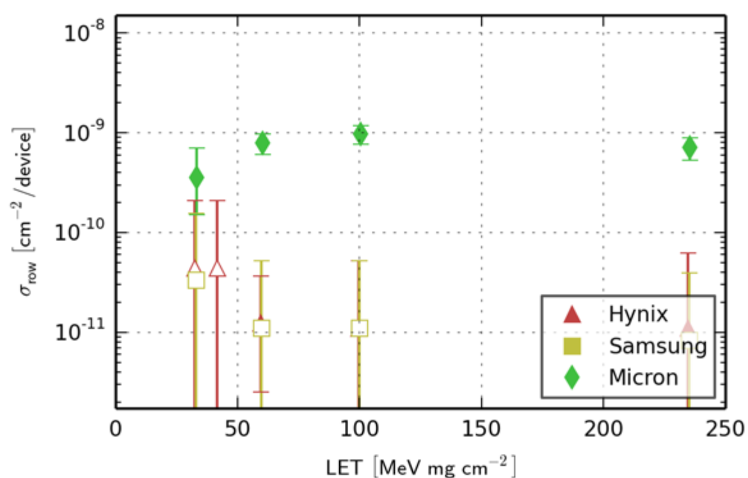

Figure 6-35: Row SEFI cross section in storage mode

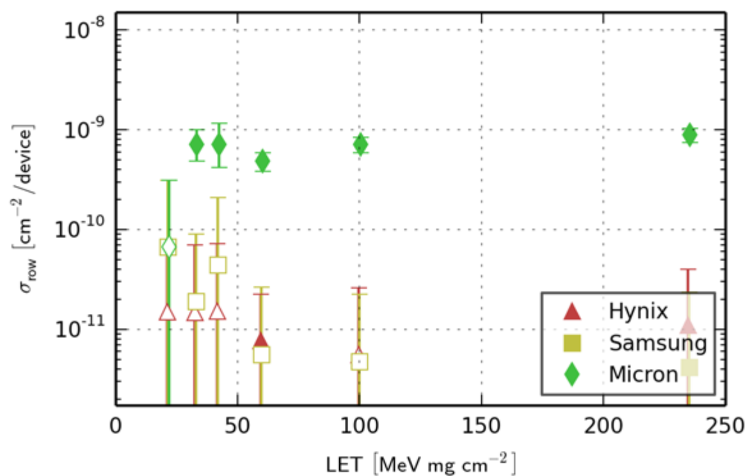

Figure 6-36: Row SEFI cross section in any mode

Column SEFIs were only observed for Micron parts. Samsung and Hynix parts did not show any column SEFIs at all (see Figure 6-37 to Figure 6-39).

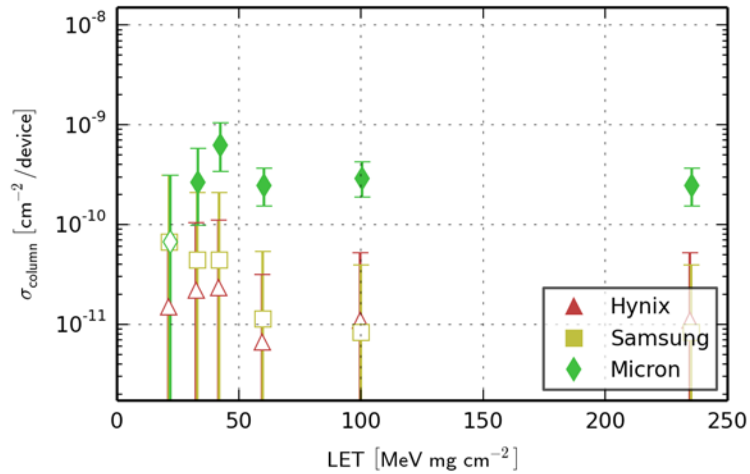

Figure 6-37: Column SEFI cross section in read mode

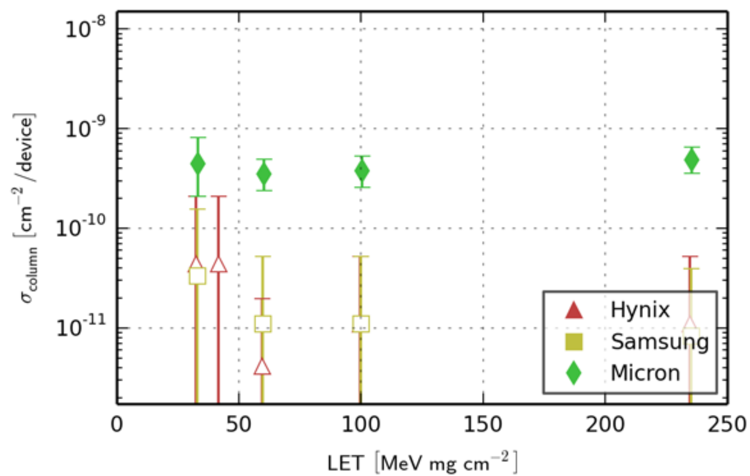

Figure 6-38: Column SEFI cross section in storage mode

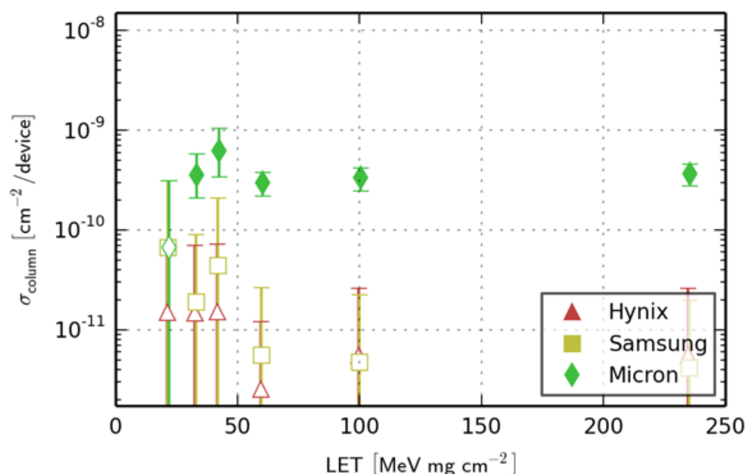

Figure 6-39: column SEFI cross section in any mode

6.2.5 Persistent SEFI (Device SEFI)

Persistent SEFI, i.e. Device SEFI are rare: during 169 irradiation runs, only three device SEFIs were observed:

1. Samsung at 60 MeV in read mode
2. Hynix at 42 MeV in storage mode
3. Micron at 60 MeV; the DUT was in the beam path during several irradiations of an-other DUT while not being exercised. The fluence that caused the SEFI is therefore not known and the SEFI is not included in the cross section calculation.

All device SEFIs could be removed by applying C1 (non-destructive) measures, i. e. rewrite all mode registers, reset the DLL, and perform a ZQ calibration. Which of these measures removed the SEFI was not examined.

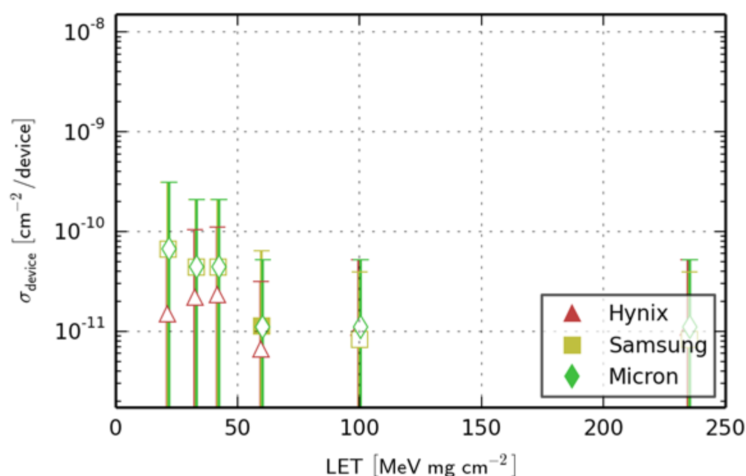

Figure 6-40: Device SEFI cross section in read mode

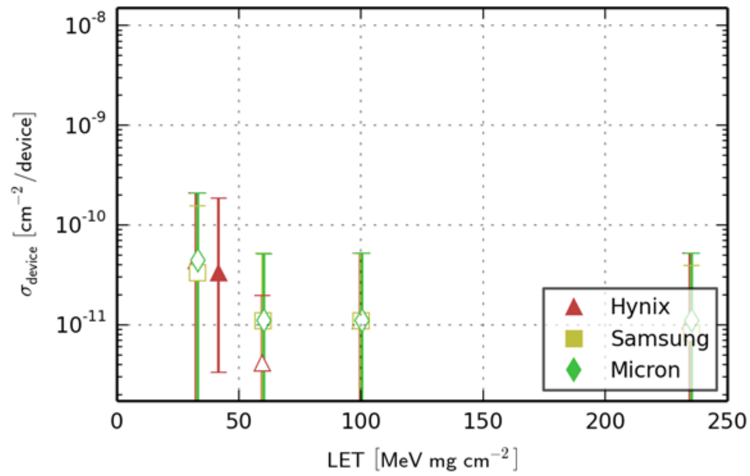

Figure 6-41: device SEFI cross section in storage mode

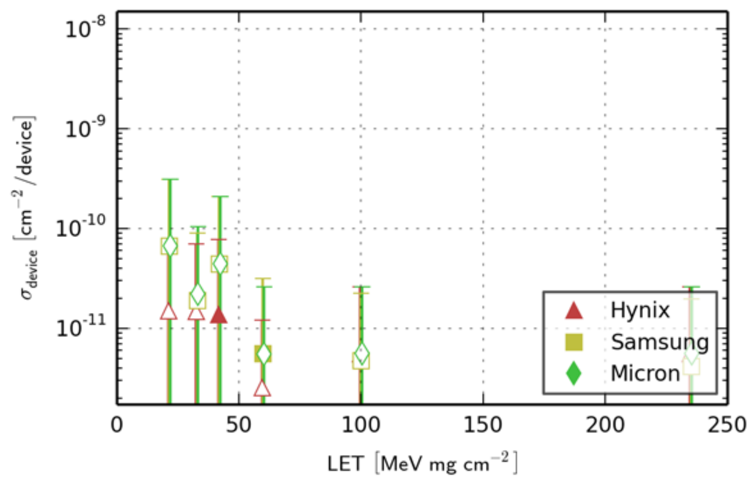

Figure 6-42: device SEFI cross section in any mode

6.3 TID Test Results

Several TID test campaigns have been performed at Co-60 facility at ESTEC in the frame of Rad Hard Memory study (TID_1 … TID_4). Main issue of TID testing are the huge efforts for in-situ testing. Remote testing cannot be applied as the devices need a specific initialisation after power up - otherwise, the state of the several functional blocks is undefined; it is not clear whether all functional blocks of the devices are powered / enabled.

6.3.1 1st in-situ TID test (TID_1)

A sophisticated test setup has been prepared to test DDR3 SDRAM devices in situ up to the required high TID level of JUICE mission of about 400 krad. All of the test bed electronics had to be protected to avoid its degradations. In §4.2.2 the TID test bed is further described.

Following device types were tested:

Type	Density	Vend.	Mask Rev.	DC	Lot	Samples
K4B4G0846B-HCH9	4 Gb	SAM K	B / 35nm	1204	GMK3599Q	8 operated + unbiased
H5TQ4G83MFR-H9CR	4 Gb	SKH K	M / 44nm	144A	DTLB0241BH	8 unbiased
H5TQ4G83MFR-H9CR	4 Gb	SKH K	M / 44nm	144A	DTLB0213HA	8 unbiased

All of the devices were soldered to SODIMM modules, four devices on front side, and four devices on back side. The devices were irradiated at high dose rate up to the final dose of about 420 krad(Si). Further details on the test are given in [DD-11].

6.3.1.1 Test sequence

At the beginning of the test, a pseudo-random pattern was written to all DUTs. After that, the DUTs were tested in a round-robin fashion. Each DUT was first read. After a pause of 15 minutes, the DUT was written with the original pattern and the sequence repeated with the next DUT. This results in a total period of 120 minutes (2 hours) for each DUT, with 105 minutes between a write operation and the following read operation.

DDR3 devices experience significant self-heating during operation. Since all DUTs are operated in unison, accessing any device has an influence on the temperature of other devices. The staggered operation of the DUTs serves to minimize the influence of this effect: were all DUTs to be read one after another, the last DUT would be read immediately following 7 other read operations, and therefore at a higher temperature than the first.

6.3.1.2 TID test results

The unbiased 4 Gb DDR3 SDRAM from SK Hynix didn't show any degradation after final TID level of 420 krad(Si) - in contrast to the Samsung DUTs. Further memory testing after the test confirmed this outcome.

During irradiation, some manual tests were performed. It has been found that, with our test device, reading from one device can cause errors in another device.

In particular, the test device was configured to not discard any errors vectors, but to slow down the test instead if the error vector FIFO runs full. We wrote a pattern to two devices and read the first one in order to verify that it did not have an unusually high number of errors. We then read another device, comparing the data against a different pattern than was written in order to simulate a very high number of errors in the device. When subsequently reading the first device again, it also contained a high number of errors. When reading only a part of the second device, the first device afterwards contained a high number of errors only in the same part of the address space. All of the error bits were changed from 1 to 0. A detailed analysis was not possible at this point due to shortcomings of the test device control software.

Slowing down the test causes the row that is currently open to remain open for a longer time than for regular test operation, up to the maximum row open time (t_{RAS}). Tthis happens on all devices simultaneously. It has been hypothesized that active rows, or the sense amplifiers themselves, are more sensitive to radiation damage than the array, or that the process of activating a row involves other sensitive components within the device:

Detailed analysis of the error patterns was performed with the unbiased Samsung SODIMM after the test campaign. The DUTs were heated to 95 °C, the maximum allowable temperature for the device, because the error patterns are more pronounced at higher temperature.

A detailed inspection of the error vectors reveals three distinct *error classes*, which can be recognized in Figure 6-43:

1. randomly distributed errors
2. four regions, each 512 row wide, of errors
3. two single rows with a high number of errors close to the end of the device

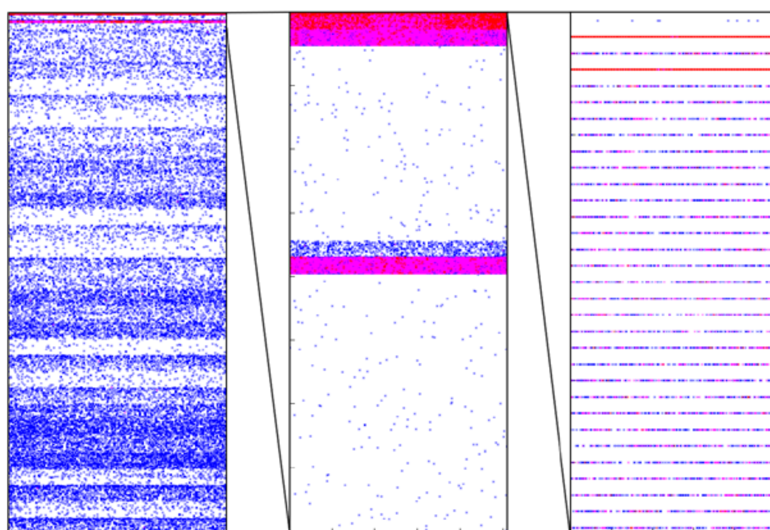

Figure 6-43: Error map at different zoom levels (Samsung 4 Gb, unbiased). The x axis shows the column address, the y axis shows the concatenated bank and row address. The last error map shows individual pages; the white space in between does not represent pages without errors.

The first class consists of randomly distributed bit errors, the majority of which are single-bit errors. In Figure 6-43, these errors are visible in the first and second error map. They exhibit some banding with a period of 2^{14} = 16384 (0x4000) pages.

The second class consists of four *error regions* in the last bank, all 512 consecutive rows long:

- Row address 0xE000 to 0xE1FF
- Row address 0xE200 to 0xE3FF (the error density in this region is about 5% of the error density in the first region, making this region only visible for some of the DUTs and at high temperatures)
- Row address 0xFC00 to 0xFDFF (with the same error density as in the first region)
- Row address 0xFE00 to 0xFFFF (with an error density of about twice the error density in the first region, with the exceptions noted below)

For the "worst" DUT, that is, the one with the highest error count, about one percent of all bits were corrupted in the last error region. In Figure 6-43, these errors can be recognized in the second error map.

The third class consists of the second and the fourth row from the end of the bank, row addresses 0xFFFC and 0xFFFE. In these rows, up to 20% of all bits were corrupted. In Figure 6-43, these rows can be recognized in the third error map.

Surprisingly, the very last row of the bank, row address 0xFFFF, contained very few errors, albeit more than would be expected from the random errors (class 1).

These error patterns (error classes 2 and 3) occur close to the end of the test, regardless of how many banks are tested: if only the first 4 banks are tested, the errors occur close to the end of bank 3. If all 8 banks are tested, the errors occur close to the end of bank 7 and the respective regions of bank 3 (and all other banks) show no particular error pattern (this is the case shown in Figure 6-43). It has therefore been hypothesized that these errors are "caused by ending a test". The mode of operation is not the root cause of the errors but rather triggers an error caused by radiation damage.

Writing all 8 banks, then writing the first 4 banks, and then reading all 8 banks caused the error pattern to appear both near the end of banks 3 and 7. This suggests that errors can be triggered by the end of the write operation.

Writing all 8 banks, then reading the first 4 banks, and then reading the first 4 banks a second time shows no errors during the first read, but shows the error pattern described above during the second read. This suggests that errors can also be triggered by the end of a read operation.

If the test is ended 128 rows before the end of the bank (testing only 0xFF80 rows of the bank), the row address of the four error regions (error class 2) remain the same as when testing the whole bank. This indicates that the errors do not only depend on the mode of operation but also on some property of the device. The last region, of course, is truncated to 384 rows in this case because the test is stopped before the end of the region is reached.

The second and fourth row from the end (error class 3), on the other hand, appear at row addresses 0xFF7C and 0xFF7E in this case, indicating that they depend solely on the mode of operation.

To conclude: the observed error patterns seem to depend in part on the mode of operation and in part on a property of the device.

It has been hypothesized that, due to bit line capacity issues, each bank of the DDR3 device does not contain one but several sense amplifiers, each associated with a subset of the rows in this bank, but only one of which is normally used at a time. This could have an influence on the error regions (error class 2), seeing that their extents seem to be related to some property of the device.

Error share (cell error ratio)

Figure 6-44 shows the cell error ratio versus the dose for all operated Samsung 4 Gb DUTs. The cell error ratio is the number of bit errors in a region of the device, divided by the total number of bits in that region. The gap at 350 krad(Si) represents the time when the manual tests were performed.

The values in Figure 6-44 include the error regions described before. Since these errors are believed to be, at least in part, an artifact of the mode of operation, we are also interested in the cell error ratio excluding these errors. Furthermore, the error regions are large enough to cause overflows of the error vector FIFO in some cases, making the total bit error count unreliable.

Since the aforementioned error regions always occur close to the end of the device (for the relevant test runs), we can filter them out by only considering the first half of the device. The cell error ratio for this case is shown in Figure 6-45.

Figure 6-46 compares the unfiltered with the filtered cell error ratio for some selected DUTs. The influence of the error pattern is large at first. As the dose increases, the influence of the error pattern decreases as the number of errors in the rest of the device increases.

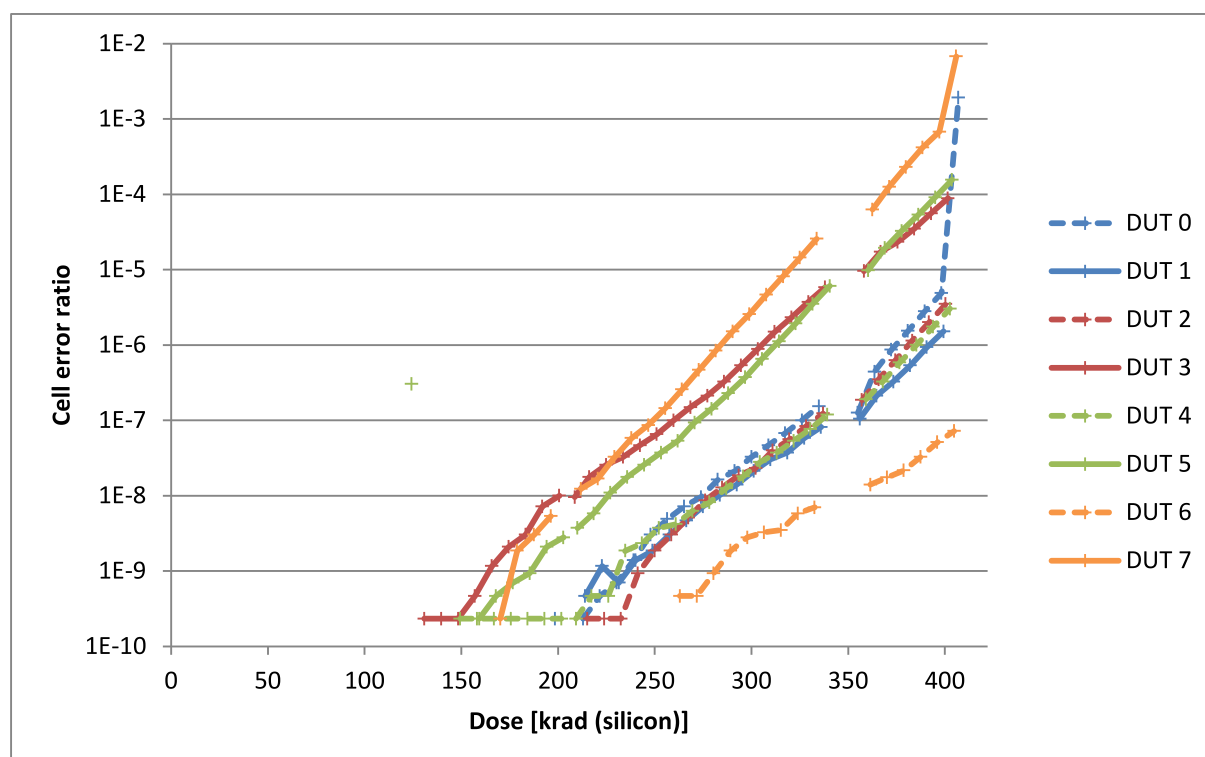

Figure 6-44: Cell errors vs. dose, Samsung 4 Gb, operated, whole device.

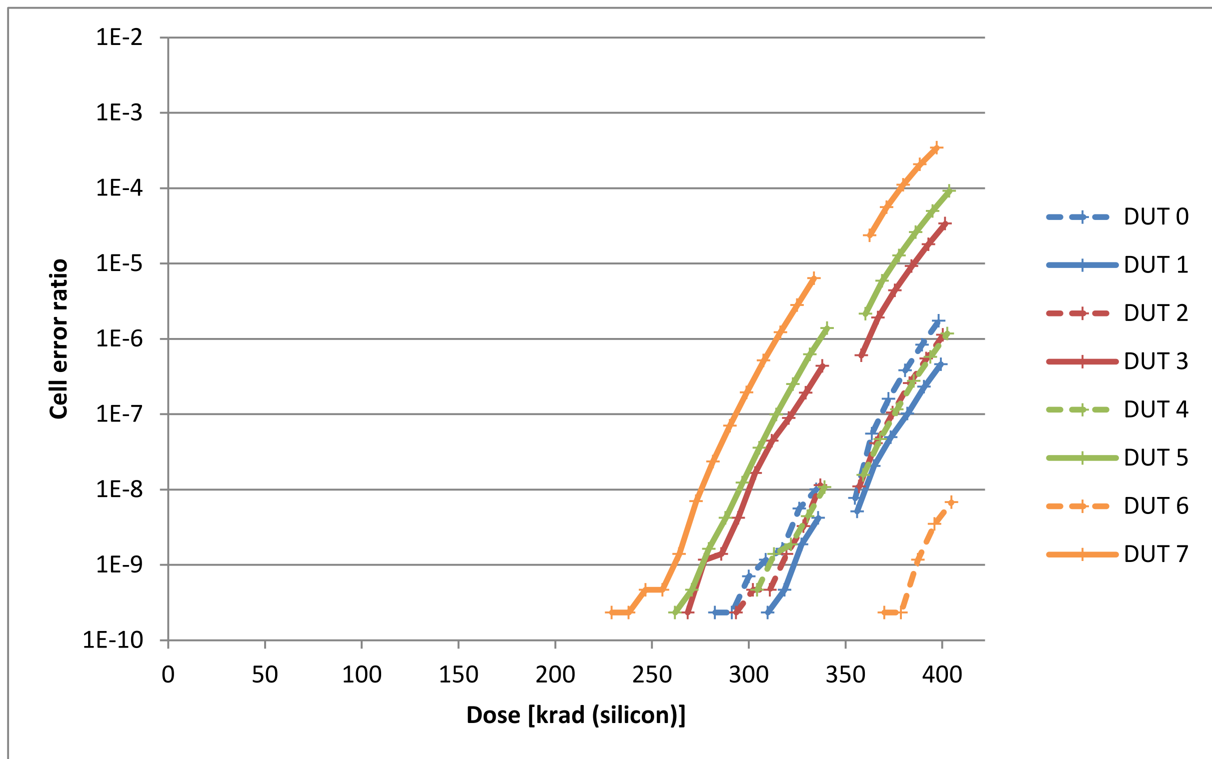

Figure 6-45: Cell errors vs. dose, Samsung 4 Gb, operated, first half of device.

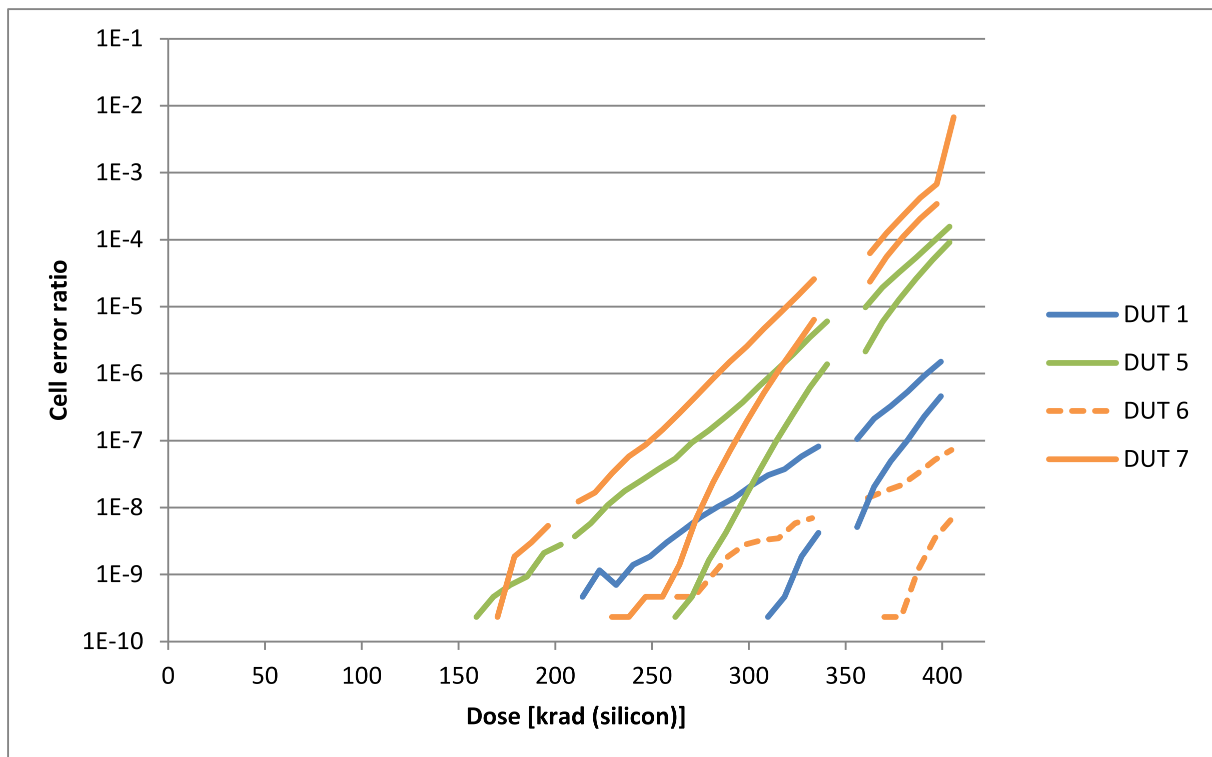

Figure 6-46: Cell errors vs. dose, Samsung 4 Gb, operated, comparison of whole device (higher values) and first half of device (lower values) for selected DUTs

Furthermore, there was observed a strong influence of the DUT position at the test bench and the cell error ratio. It is suspected that the difference might be caused by electrons, either from the β decay of ^{60}Co or from photon scattering in the test chamber.

Idle current

During each loop, the idle current was measured and logged automatically. Nevertheless, due to the operating in SODIMM, the individual current for each DUT could not be measured. The measured current is the total current for the whole SODIMM. Dividing the current by the number of DUTs on the SODIMM yields the average current per DUT.

The current vs. dose is shown in Figure 6-47. Over the course of ≈ 420 krad (silicon), the average idle current increased by less than 25% from 15.7 mA to 19.3 mA.

Some of the automatically measured values are slightly increased over the nearby values. This may be due to the measurement coinciding with the periodic read operation.

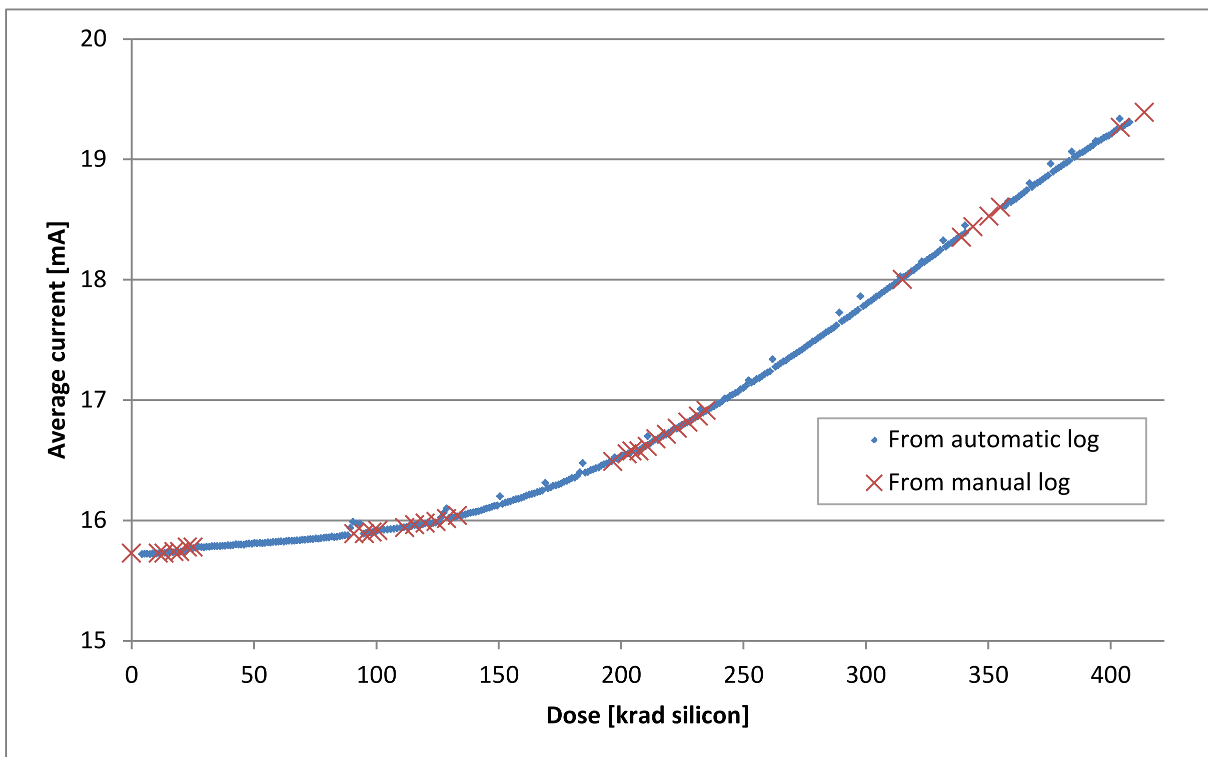

Figure 6-47: Idle current vs. dose, Samsung 4 Gb, operated.

Temperature dependency

After the test, the unbiased Samsung 4 Gb DUT were tested for the influence of the temperature on the number of errors by writing a pseudo-random pattern to the device and reading it back about one second later.

Figure 6-48 shows the total number of bit errors *n* in the whole device vs. the temperature *T*. This relationship is described approximately by $n \propto e^{T/12\mathrm{K}}$. The number of errors thus doubles every 8 K or increases by a factor of 10 every 28 K in temperature change.

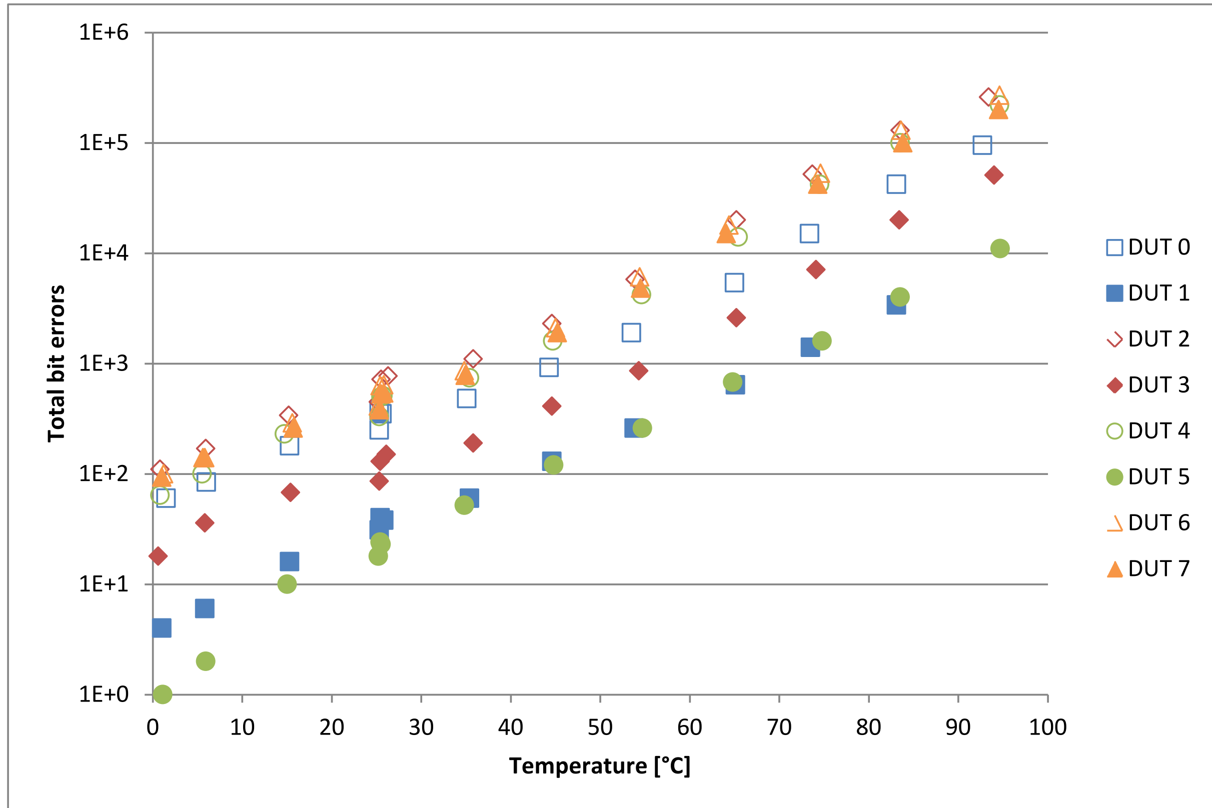

Figure 6-48: Bit errors vs. temperature, Samsung 4 Gb, unbiased ≈ 420 krad(Si), refresh rate 7.8µs.

The first measurement was performed at 25°C. After the device had been heated to 95°C and repeatedly written and read over the course of approximately 2 hours, another measurement was performed at 25°C. Compared to the first measurement at 25 °C, the error count was increased by a factor of approximately 1.5 (a factor that, were it caused by temperature, would correspond to a change in temperature of about 5 K). After cooling the device to 0°C and heating it back up to 25°C, the increased number of errors remained, confirming that the increased error count was not caused by temperature hysteresis.

The refresh interval was kept at the default of 7.8 µs for all tests, even at T > 85°C, where the standard requires the refresh rate to be doubled.

Error annealing

In the days after the test, the number of errors remaining in all tested Samsung 4 Gb DUTs (operated and unbiased) was repeatedly measured. The results are shown in figures Figure 6-49 to Figure 6-53. The values in figures Figure 6-51 and Figure 6-52 are normalized to the first measurement in the days after the test. The values in figure Figure 6-53 are normalized to the values immediately after

irradiation. For the unbiased DUTs these data are not available. The measurements were performed at room temperature without temperature control.

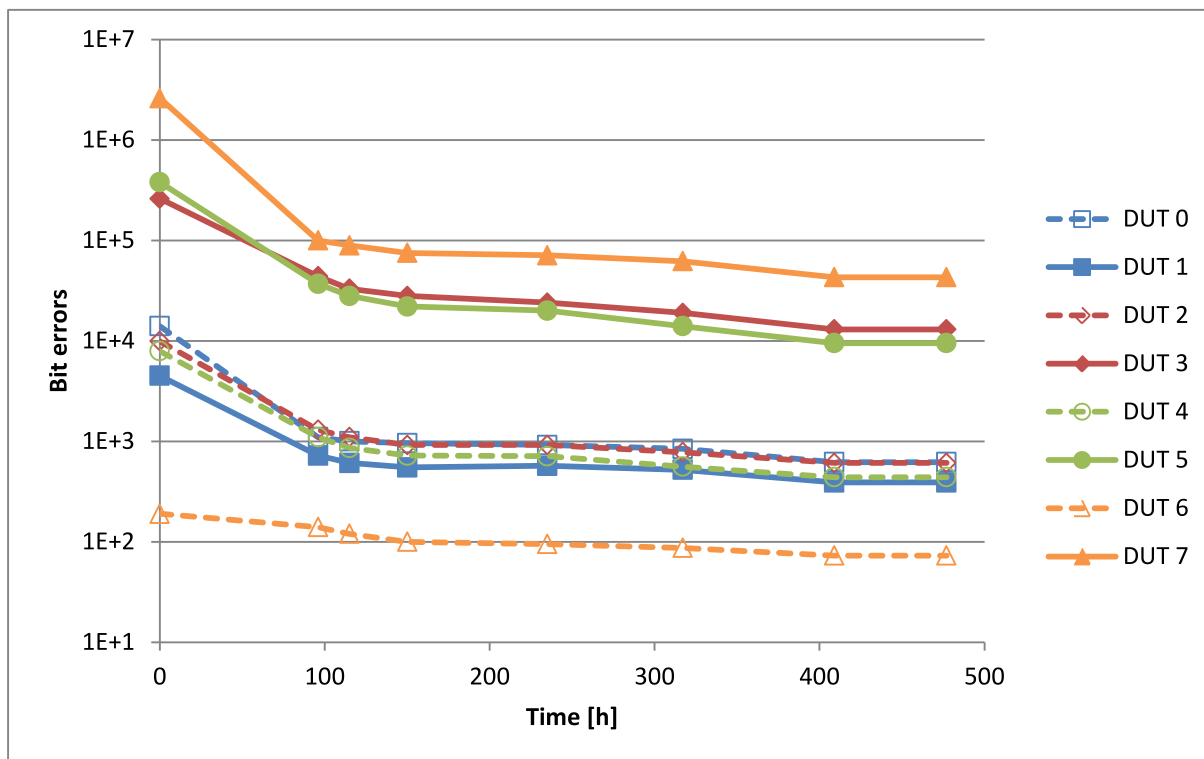

Figure 6-49: Error annealing, Samsung 4 Gb, operated, raw.

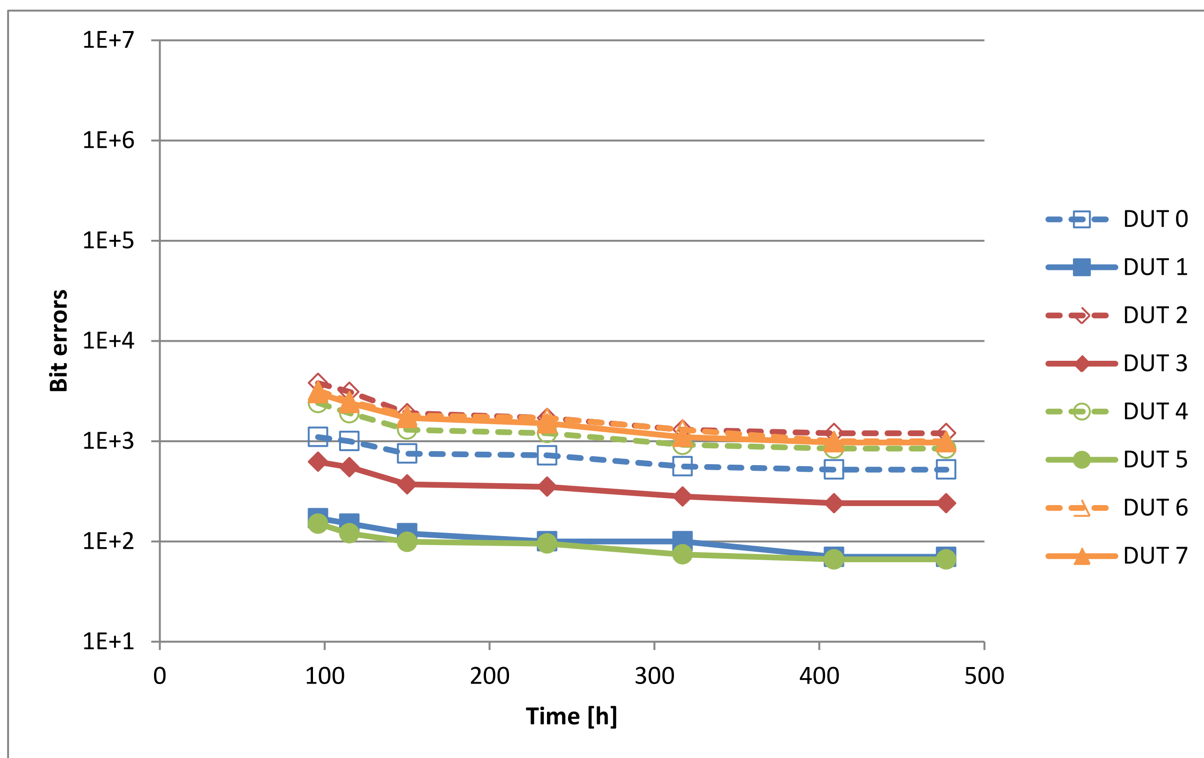

Figure 6-50: Error annealing, Samsung 4 Gb, unbiased, raw.

© Airbus DS GmbH

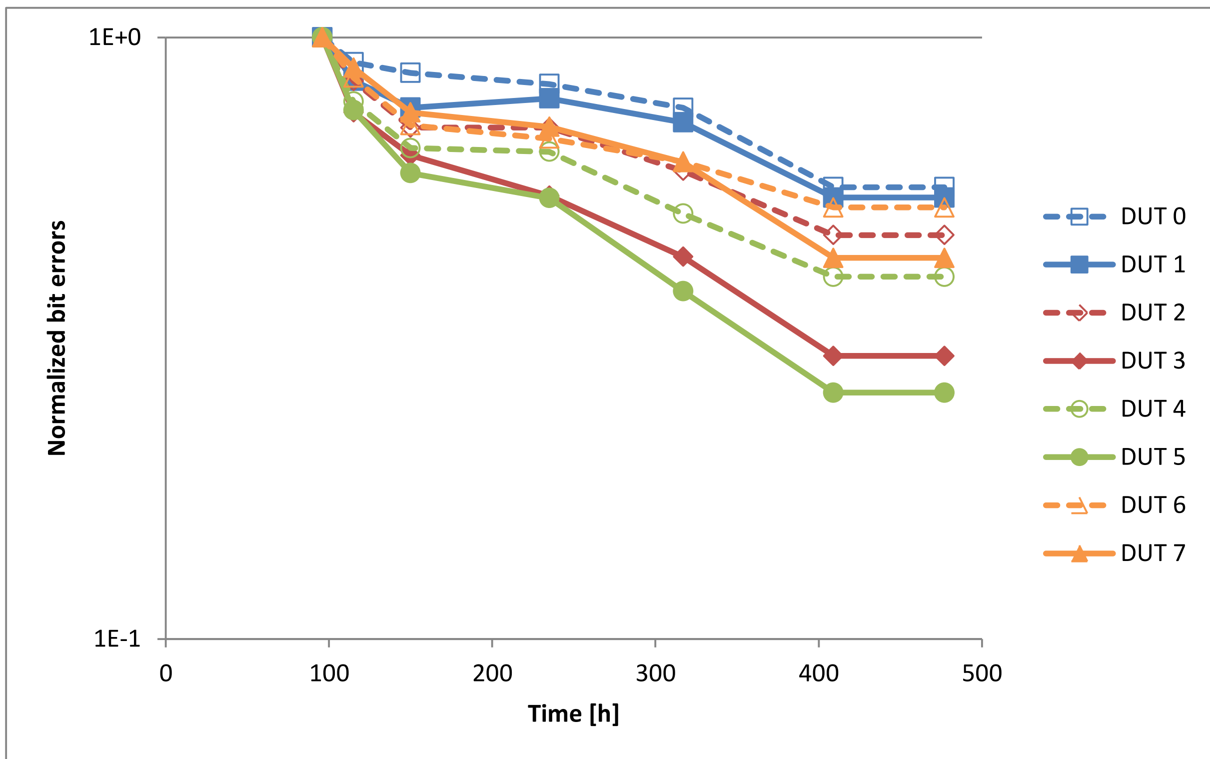

Figure 6-51: Error annealing, Samsung 4 Gb, operated, normalized.

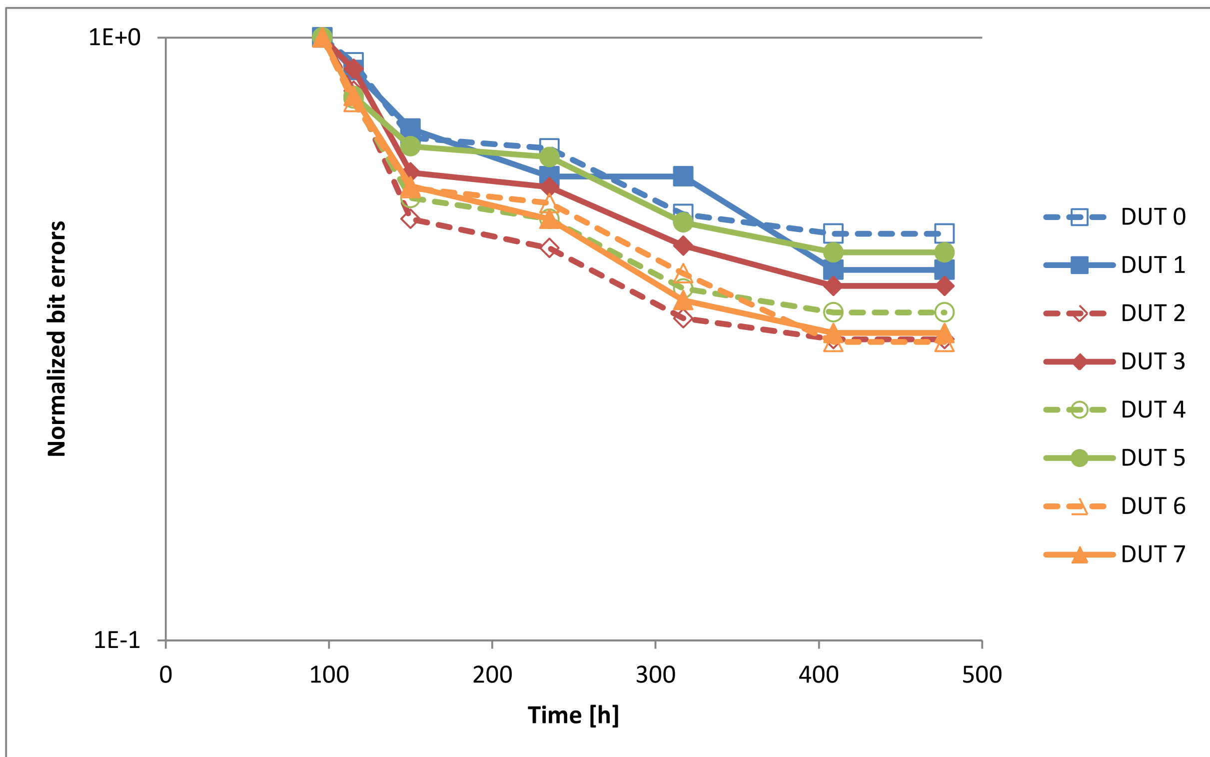

Figure 6-52: Error annealing, Samsung 4 Gbit, unbiased, normalized.

© Airbus DS GmbH

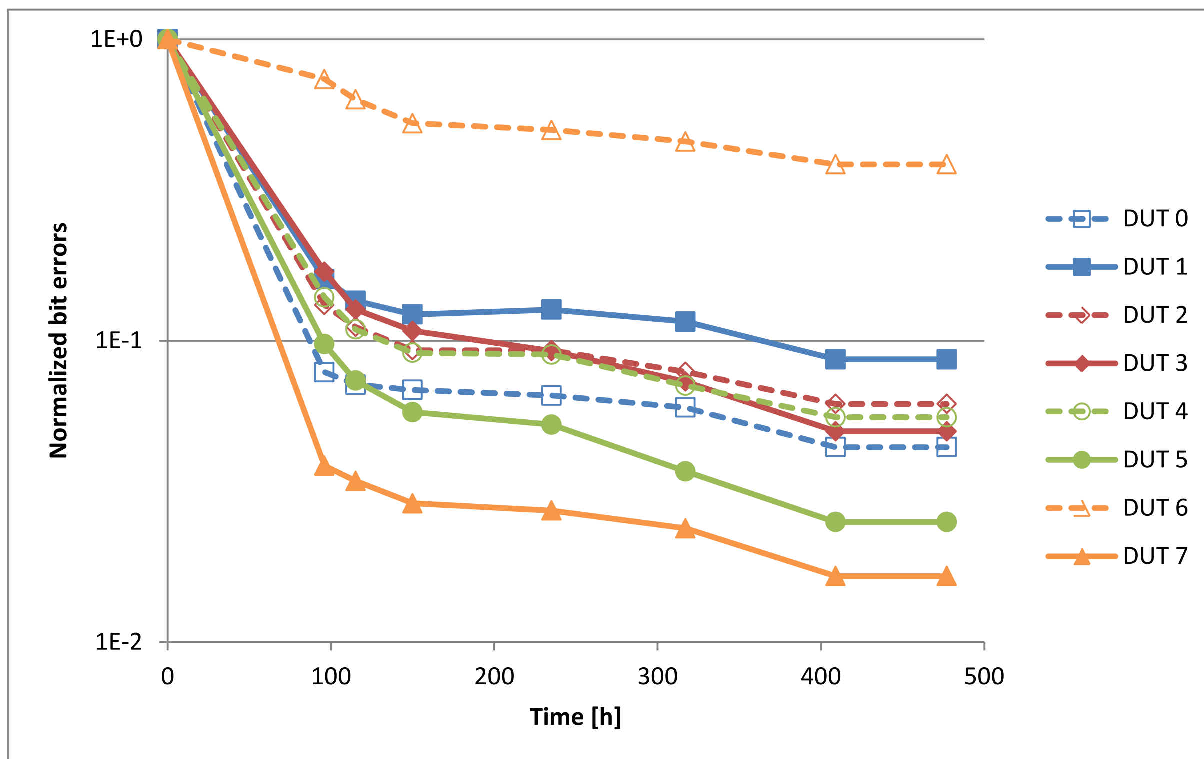

Figure 6-53: Error annealing, Samsung 4 Gb, unbiased, normalized.

6.3.2 Further unbiased TID tests (TID_2 & TID_3)

As outcome of the 1st TID test (TID_1) further unbiased tests were performed on a variety of 2 Gb and 4 Gb DDR3 SDRAM devices (see [DD-12] and [DD-13] for details).

Following device types were tested:

Type	Density	Vend.	Mask Rev.	DC	Lot	Samples
TID_2						
K4B4G0846B-HCH9	4 Gb	SAM K	B / 35nm	1204	GMK3599Q	3
H5TQ4G83MFR-H9CR	4 Gb	SKH K	M / 44nm	144A	DTLB0241BH	8 (SODIMM)
				144A	DTLB0213HA	8 (SODIMM)
					DTLB1237AM	1
					DTLB1254BM	1
					DTLB1284AM	2
					DTLB1088DM	1
					DTLB1591AM	1
H5TQ2G83BFR-H9CR	2 Gb	SKH K	B / ?		DTKBA778H1	6
K4B2G0846B-HCH9	2 Gb	SAM K	B / 50nm		GLJ423AC	6
K4B2G0846D-HCH9	2 Gb	SAM K	D / 35nm		GEDN60GKU	6
					GEB66SFFC	6
EDJ4208BASE-DJ-F	4 Gb	ELP J	A / 4xnm		OWPEYOO	6
MT41J256M8HX-15E:D	2 Gb	MIC U	D / 50nm	1006	BYFCM91.21	6
				1116	BY8F416.21	6
NT5CB256M8BN	2 Gb	NAN TW	B / 50nm	1026	01340100GP	6
				1110	05142700FP	6
				1145	132154F0FF	6
NT5CB256M8BN	2 Gb	NAN TW	G / 3xnm	1218	20726200EP	6
TID_3						
K4B4G0846B-HCH9	4 Gb	SAM K	B / 35nm	1216	GMC7679W	10
MT41J512M8RH-083:E	4 Gb	MIC U	E / 30nm	1324	DRRKDNB.11	10
NT5CB512M8GN-EK	4 Gb	NAN TW	G / 3xnm	1238	22755400G P	10

The two Hynix lots were soldered to SODIMM modules, all other device were shorted on conductive foam, connecting all balls. At TID_2 campaign the devices were irradiated at high dose rate of about 2.3 krad(Si)·h^{-1} to the final dose of about 376 krad(Si) (). At TID_3 campaign the devices were irradiated at about 2.4 krad(Si)·h^{-1} to the final dose of about 393 krad ().

After the devices had been shipped back after the end of the irradiation, various tests were performed. Main focus of the investigations was the formerly observed band error pattern.

6.3.2.1 Test sequence

In regular operation, the memory device is read continuously and rows are kept active for a short time only. The band error pattern is believed to be triggered by keeping a DRAM row active for an extended time (within the maximum time allowed by the specification, t_{RAS} = 9·$t_{REF\ I}$ ≈ 70 µs). In order to cause

rows to be kept active for an extended time, the test bed can be configured to perform intermittent operation. This is similar to read operation, but includes additional pauses which keep the current row active. Subsequently reading the data from the DUT in continuous operation (without rewriting) typically results in a higher number of errors.

6.3.2.2 TID_2 - results at ambient temperature

First, a subset of the irradiated devices (typically 3 out of 6 available samples for each device type and lot) were tested at room temperature:

- The band error pattern was observed for 4 Gb Samsung as in the former in-situ test (TID_1) and also for the 2 Gb Samsung (mask revision D) devices. In the "worst" affected rows, about 5% of all cells contained the wrong value.
- There were no errors for 2 Gb Micron and 2 Gb Nanya devices, with the exception of one single error each in one Micron device (out of the 6 devices tested) and one Nanya device (out of the 12 devices tested). These errors were 1-to-0 transitions in the second to last page (page address 0x7fffe), suggesting that it constitutes a very weak band error pattern.
- There were no errors at all for 4 Gb Hynix, 4 Gb Elpida, and heritage 2 Gb Samsung (mask revision B), 2 Gb Micron, and 2 Gb Nanya devices.

The 4 Gb Samsung devices had a consistent number of bit errors of about 3.8 102 to 8.0. In contrary, the 2 Gb Samsung devices (mask revision D) showed considerable device-to-device and lot-to-lot variation (see [DD-12] for details).

6.3.2.3 TID-2 results at elevated temperature

Since errors are more pronounced at higher temperature, the devices were operated at elevated temperature.

As a first test, the Hynix SODIMM was heated to approximately 80°C using a heat gun while being operated in the PC (timing parameters, as given by Memtest86+: 6-7-7-18) and exhibited some single bit errors, in contrast to operation at room temperature. For a cross-check, an un-irradiated SODIMM with the same devices was operated under the same conditions and showed no errors.

After that, at least 3 samples of each device type were operated at 85°C, the maximum temperature within specification limits, in our test bed. First, several write and read operations were performed without and, in case of errors, with precharge after periodic read. After that, intermittent operation was performed on the first half of the device and the whole device was read.

At 85°C, many devices showed the band error pattern, in contrast to room temperature. The band error pattern includes several error regions with different error intensity. For a *weak* band error pattern, all but the most intense error regions (the second and fourth pages from the end) are not present. A *very weak* band error pattern consists of very few isolated errors in these two pages.

The results of the tests are summarized in Table 6-2. Exemplary plots of the error pattern are provided in [DD-12].

Precharge after periodic read typically reduces the band error pattern significantly. If the band error pattern is weak in the first place, it may be reduced to the point of disappearing completely. An effect on the random errors could not be observed.

Table 6-2: Test results at 85°C (ordered by band error pattern severity)

Device DUTs tested	Random errors	Band error pattern (BEP)	Precharge after periodic read	Intermittent operation	Comments
4 Gb Samsung 8 (1 lot)	Severe	Strong	Reduces BEP	More errors	
2Gb Samsung (D) 4 (2 lots)	Severe	Strong	Reduces BEP	More errors	
2Gb Micron 4 (2 lots)	Significant/ severe	Weak	Removes BEP	No effect	
2Gb Hynix 3 (1 lot)	Few	Weak/very weak	Removes BEP	No effect	
2Gb Nanya (B) 3 (3 lots)	Significant	Very weak	No effect	No effect	
2Gb Nanya (G) 3 (1 lots)	Few	None	No effect	No effect	
4 Gb Hynix 19 (3 lots)	Few	None	No effect	No effect	
4 Gb Elpida 3 (1 lot)	Few	None	No effect	No effect	
2Gb Samsung (B) 3 (1 lot)	None	None	No effect	No effect	

Note that all three 2Gb Samsung (revision B) devices did not show any errors at all, even after intermittent operation at 85°C, in very contrast to the 4 Gb and 2Gb (revision D) devices from the same manufacturer.

In an additional test, of the tested 2 Gb Micron devices, one contained more random errors and the other showed a stronger band error pattern. Another 2 Gb Micron device showed random errors in a pronounced gradient pattern (see [DD-12] for details).

6.3.2.4 TID_3 - results at ambient temperature

First, all devices were tested at room temperature:

- The 4 Gb Samsung devices showed the band error pattern, very similarly to the previously tested devices of the same part number. In particular, all errors were in the 1 → 0 direction again. The error density in the rows affected by the band error pattern was about 1%.
- The 4 Gb Micron devices showed no errors at all.
- The 4 Gb Nanya devices showed a very high number of errors (up to an error density of 50%) in both directions - in contrast to former 2Gb devices. No pattern has been identified so far.

6.3.2.5 TID-2 results at elevated temperature

Since errors are more pronounced at higher temperature, the Micron devices were tested at 80°C. The Samsung devices were not tested at elevated temperature because they appear to behave similarly to the previously tested DUTs of the same type, which have been thoroughly examined. The Nanya devices were not tested at elevated temperature because they already contain a high number of errors at room temperature.

All 10 Micron devices were tested at 80°C. They only contained between zero and nine single-bit errors each, in both directions, randomly distributed throughout the devices address space.

6.3.3 Final in-situ TID test (TID_4)

According the results and lessons learnt of 1st in-situ in October 2012 test (TID_1) and the following investigations on unbiased irradiated devices (TID_2 and TID_3) a final TID characterisation test were performed in January 2014 at Co-60 facility at ESTEC [DD-15].

The sophisticated test setup was further improved to avoid side-effects by electrons. In §4.2.2 the TID test bed is further described. Details to tested devices are listed in Table 6-3. Some of the devices, in particular these ones which were envisaged for in-situ testing, were soldered on SODIMM modules (see Table 6-4).

Table 6-3: Details of tested 4 Gb DDR3 SDRAM devices

Part Type	Density	Vend.	Mask Rev.	DC	Lot	Samples
MT41J512M8RH-093:E	4 Gb	MIC U	E / 30nm		3LE22	16
H5TQ4G83MFR-H9CR	4 Gb	SKH K	M / 44nm	144A	DTLB0241BH	8
H5TQ4G83MFR-H9CR	4 Gb	SKH K	M / 44nm	144A	DTLB0213HA	8
NT5CB512M8CN-EK	4 Gb	NAN TW	G / 3xnm	1238	22755400G P	8

Table 6-4: List of DUTs

ID	Mount	Part Type	Vend.	DUTs	TIDL [krad(Si)]	Irradiation
Mic4SO4	SODIMM	MT41J512M8RH-093:E	MIC U	8	407	In-situ
Mic4SO3	SODIMM	MT41J512M8RH-093:E	MIC U	8	407	Unbiased
Hyn4SO4	SODIMM	H5TQ4G83MFR-H9CR	SKH K	8	423	In-situ
Hyn4SO3	SODIMM	H5TQ4G83MFR-H9CR	SKH K	8	407	Unbiased
Nan4.a[11-18]	Single	NT5CB512M8CN-EK	NAN TW	8	407	Unbiased

6.3.3.1 Test sequence

The in-situ testing was performed analog to TID_1. At the beginning of the test, a pseudo-random pattern was written to all DUTs. After that, the DUTs were tested in a round-robin fashion. Each DUT

was first read. After a pause of 15 minutes, the DUT was written with the original pattern and the sequence repeated with the next DUT. This results in a total period of 120 minutes (2 hours) for each DUT, with 105 minutes between a write operation and the following read operation.

DDR3 devices experience significant self-heating during operation. Since all DUTs are operated in unison, accessing any device has an influence on the temperature of other devices. The staggered operation of the DUTs serves to minimize the influence of this effect: were all DUTs to be read one after another, the last DUT would be read immediately following 7 other read operations, and therefore at a higher temperature than the first.

The irradiation was performed at a dose rate of approximately 100 rad(Si) minute^{-1} respectively 6 krad(Si) hour^{-1}. At this rate, a dose of 400 krad was reached in 67 hours, or more than two and a half days.

6.3.3.2 Evolution of idle current with dose

During each loop, the idle current was measured and logged automatically for the operated DUTs. This measurement was performed as the first action after the 15 minute wait time, in order to avoid the warming caused by the write operation to affect the idle current.

As mentioned in §6.3.3.1 before, individual currents for each DUT could not be measured. The measured current is the total current for the whole SODIMM. Dividing the current by the number of DUTs on the SODIMM yields the average current per DUT.

The evolution of idle currents with dose for the Micron and SK Hynix DUTs is shown in Figure 6-54 and Figure 6-55. For the Micron DUTs, over the course of 407 krad(Si), the average idle current increased by a factor of more than 12, from 9 mA per DUT to 116 mA per DUT. For the Hynix DUTs, the current did not increase at all over the whole 423 krad(Si).

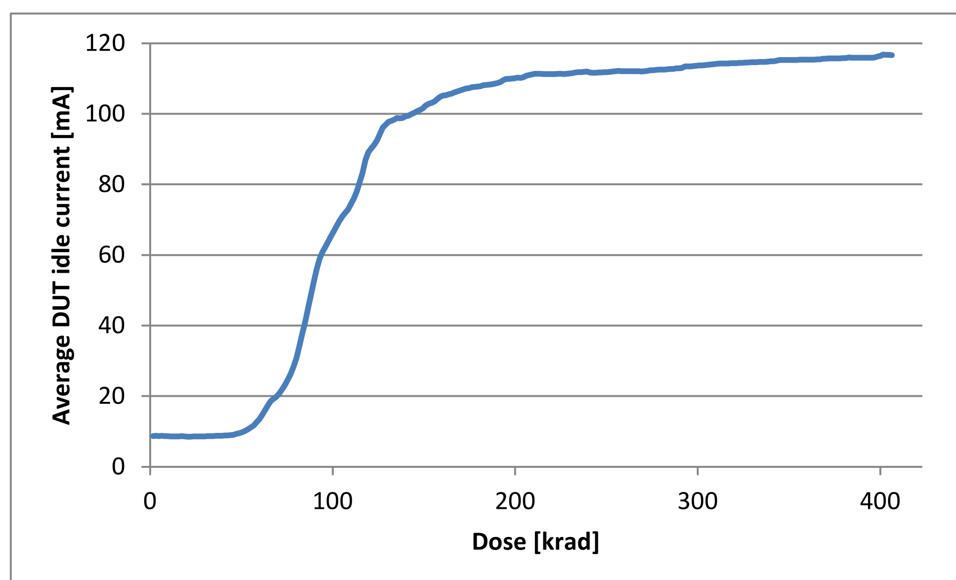

Figure 6-54: Idle current vs. dose, Micron MT41J512M8RH-093:E, operated

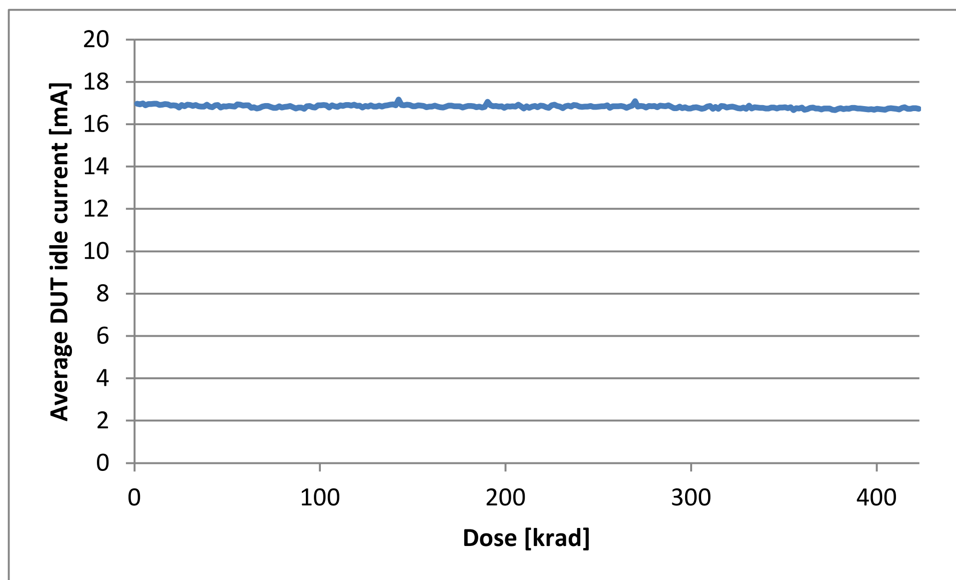

Figure 6-55: Idle current vs. dose, SK Hynix H5TQ4G83MFR-H9CR, operated

After the test, the supply voltage in idle state was measured at approximately 1.35 V, which is lower than the specified minimum of 1.425 V. The reference voltage $V_{REF,DQ}$ was verified to be within the specified limits. On start-up, the controller attempts to initialize the DUT. This includes writing to and reading from the device in order to calibrate the line delays. The initialization procedure does not complete, indicating that writing and reading is not possible.

The current during a write and read operation for the unbiased irradiated SK Hynix DUTs is shown in Figure 6-56. During read operation, the current has a slight periodicity with 8 periods, which may or may not coincide with the 8 banks of the DUT. This periodicity is not present in a pristine (non-irradiated) device of the same type (Figure 6-57).

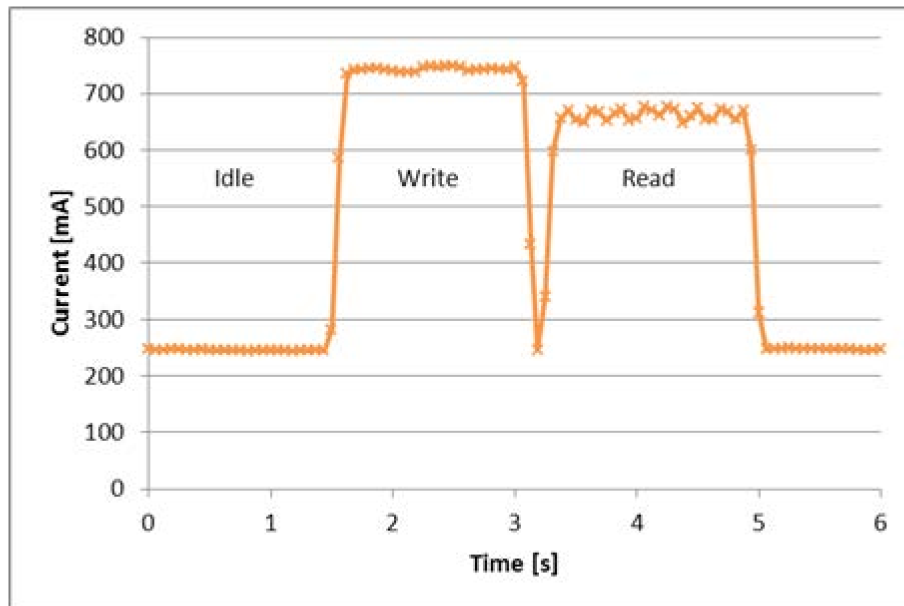

Figure 6-56: Operating current during write and read operation. SK Hynix H5TQ4G83MFR-H9CR, after unbiased irradiation

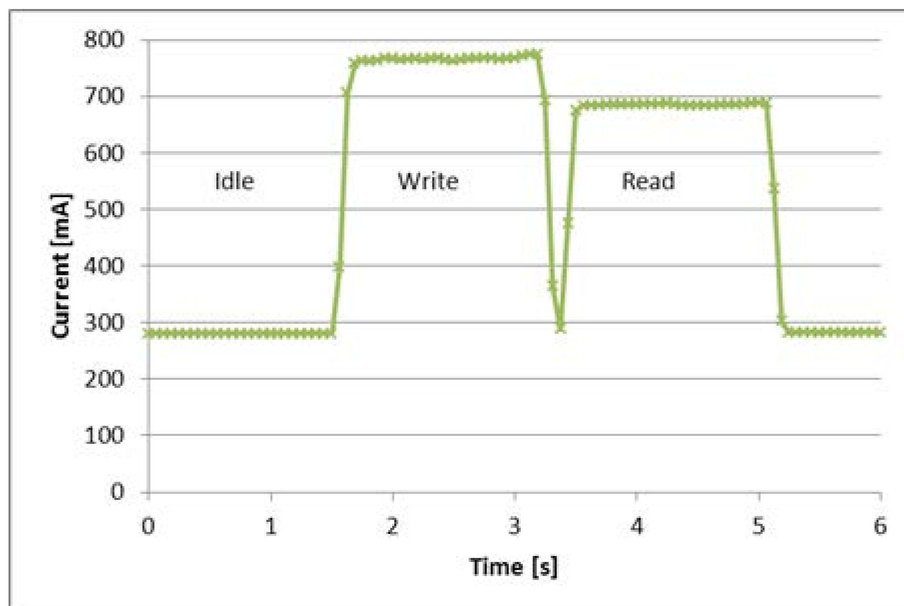

Figure 6-57: Operating current during write and read operation. SK Hynix H5TQ4G83MFR-H9CR, pristine

6.3.3.3 Error count

None of the eight unbiased Micron DUTs showed any errors.

Of the eight unbiased SK Hynix DUTs:

- Four showed no errors at room temperature.
- One showed very few randomly distributed errors, which disappeared after a few days.
- Two showed a substantial number of errors, including some row errors. The error maps are shown in figure 12. Zooming in on the errors in the second and third case reveals that the former consists of two adjacent error pages, while the latter consists of a contiguous error region (see figure 13).
- • One showed a substantial number of errors, including some row errors and many short row segment errors. The error map is shown in figure 14. The pattern is different for each readout, indicating that the errors do not originate from the array.

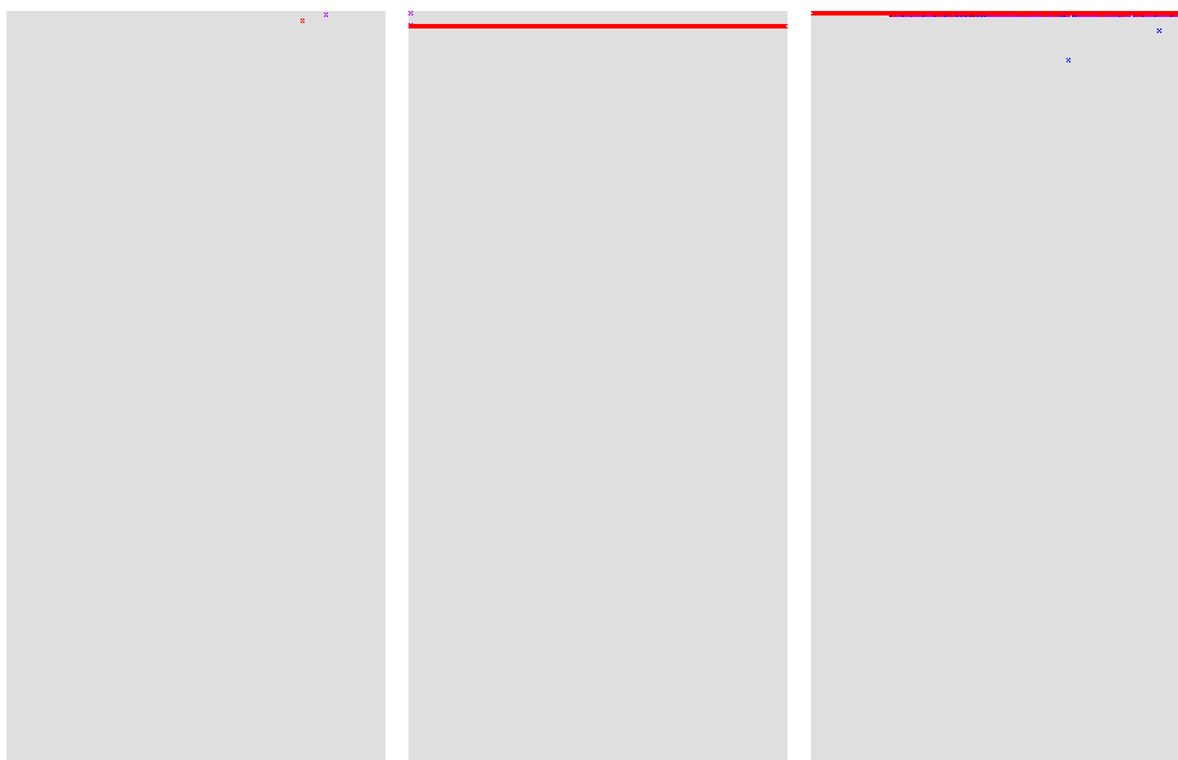

Figure 6-58: Error maps of three DUTs; SK Hynix H5TQ4G83MFR-H9CR, unbiased

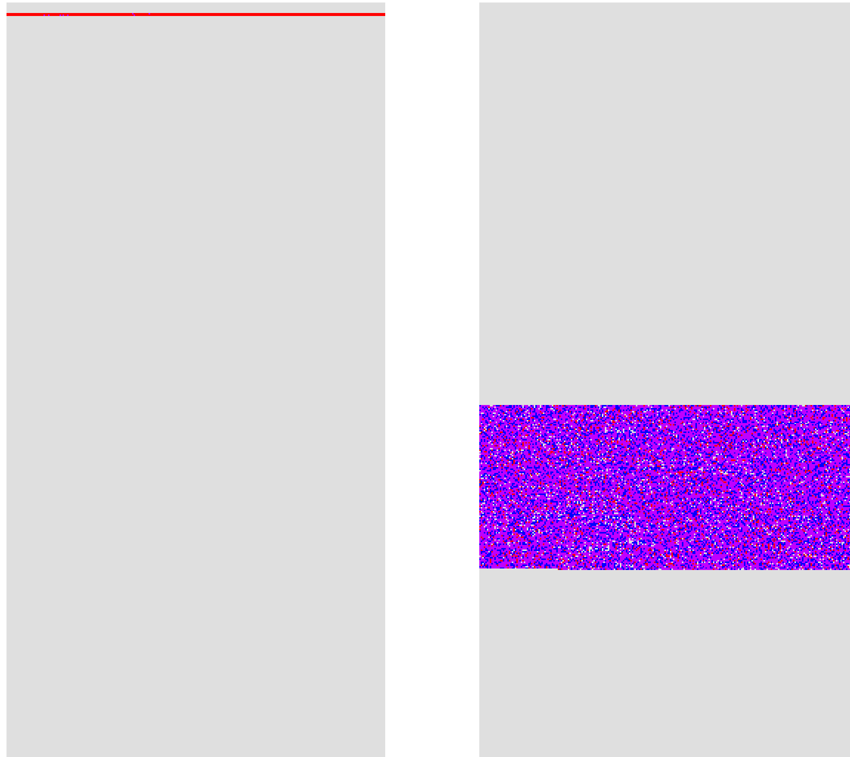

Figure 6-59: Zoomed view of the second and third error map from Figure 6-58

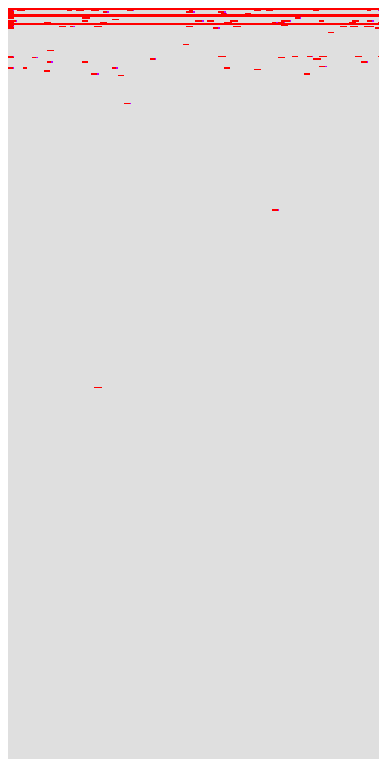

Figure 6-60: Error map, SK Hynix H5TQ4G83MFR-H9CR, unbiased

© Airbus DS GmbH

The error density vs. dose for the operated Micron DUTs is shown in Figure 6-61 (one of the DUTs suffered from a bad contact and is not shown). The first errors appeared around 90 krad. The number of errors quickly increased to the maximum that our test equipment is capable of recording (within 25 krad). This increase is coincident with the current increase. It is suspected that the number of errors is caused by the supply voltage dropping to a value out-side of the specification due to the high current.

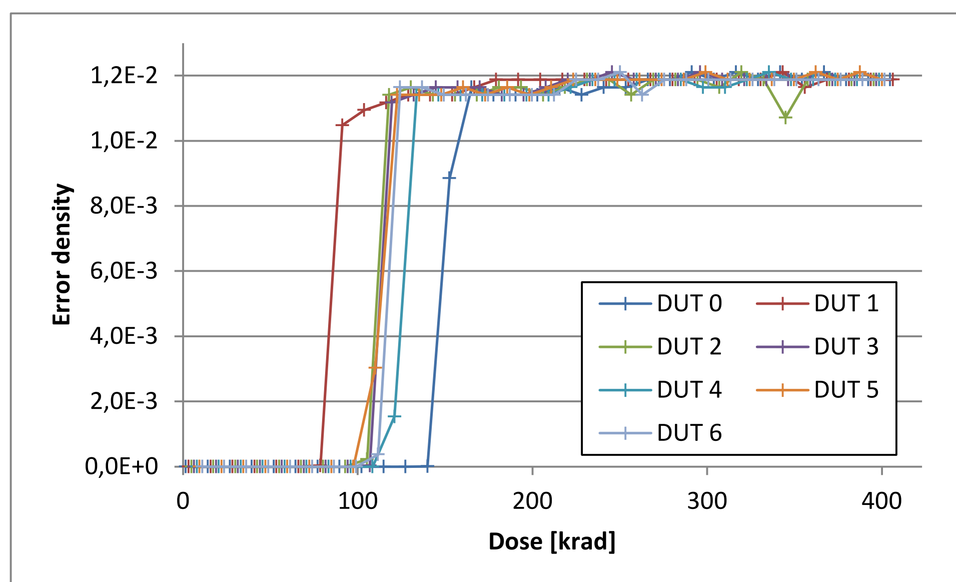

Figure 6-61: Error density vs. dose; Micron MT41J512M8RH-093:E, operated

None of the eight operated Hynix DUTs showed any errors at all, up to the final dose of 423 krad(Si).

All error counts were determined at room temperature

6.3.4 Annealing

The irradiated DUTs were first annealed at room temperature for about one week, and then at 100°C for another week. The measurements were performed at room temperature which was neither controlled nor measured.

The current measurements during annealing are shown in figures 16 to 21. The semi-transparent horizontal lines indicate the baseline values i.e., the values of a pristine part of the same type. The vertical grey lines indicate the start of the high-temperature annealing.

The write and read current are estimated from the graphical display of our test control soft-ware, since our test equipment currently does not support synchronization of the current measurement with DUT operation.

Note that there have been instances where the idle current between initialization and the first set of write and read operations was lower than the later idle current after the device had actually been written to. We therefore wrote and read the whole device before measuring the idle current. Since the

operated Micron device cannot be initialized, this is not possible for this device. The reported value is therefore the current after the failed initialization.

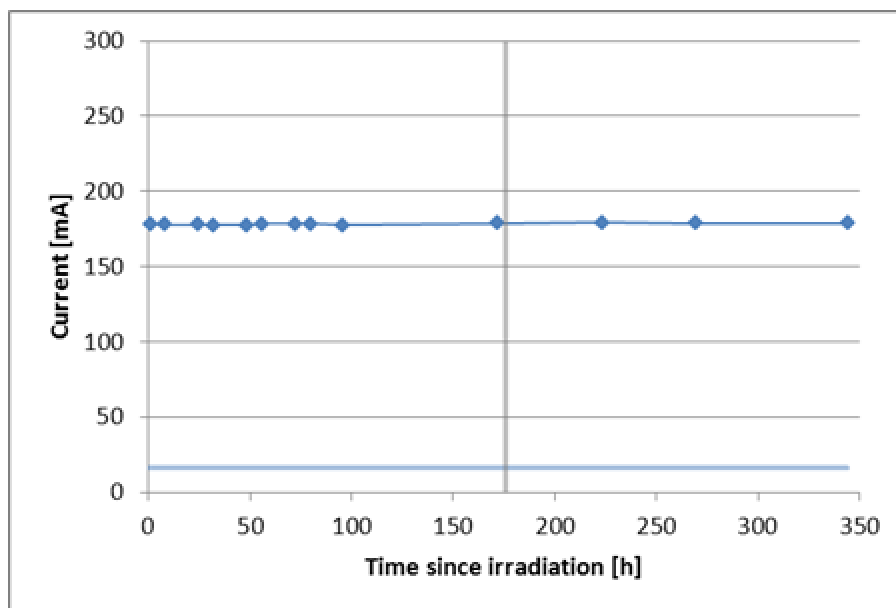

Figure 6-62: Current annealing, Micron MT41J512M8RH-093:E, operated.
The horizontal, semi-transparent line indicates the baseline current value. The vertical, grey line indicates the beginning of high-temperature annealing.

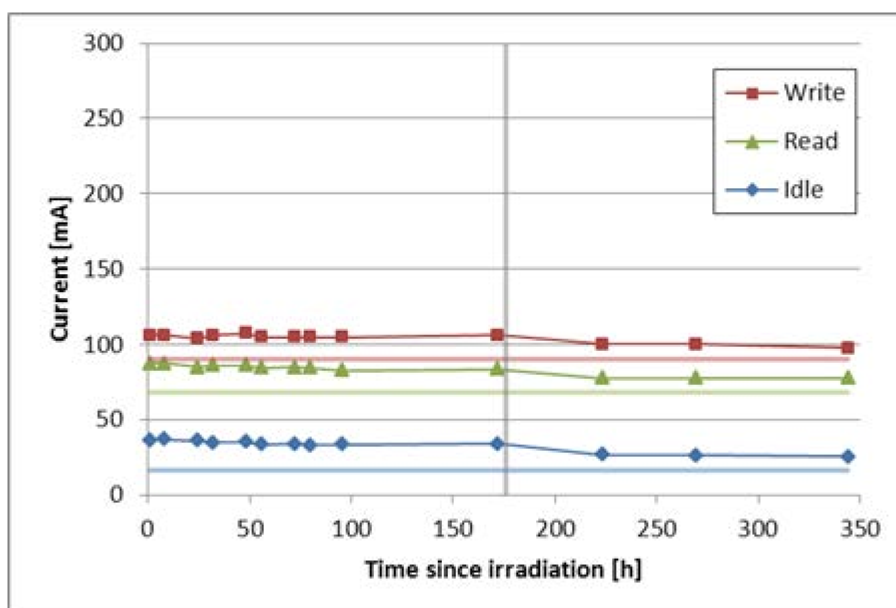

Figure 6-63: current annealing, Micron MT41J512M8RH-093:E, unbiased.
The horizontal, semi-transparent lines indicate the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

© Airbus DS GmbH

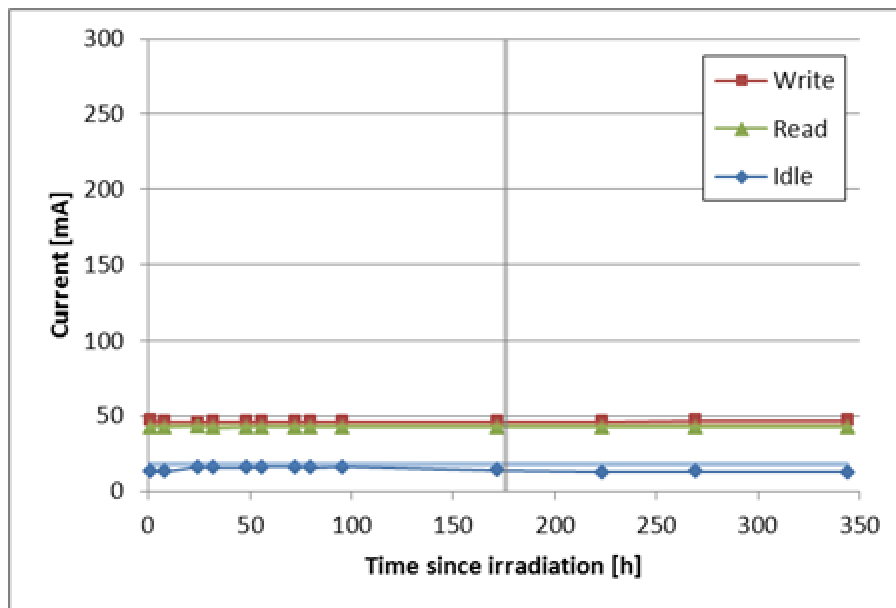

Figure 6-64: current annealing, SK Hynix H5TQ4G83MFR-H9CR, unbiased.
The horizontal, semi-transparent lines indicate the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

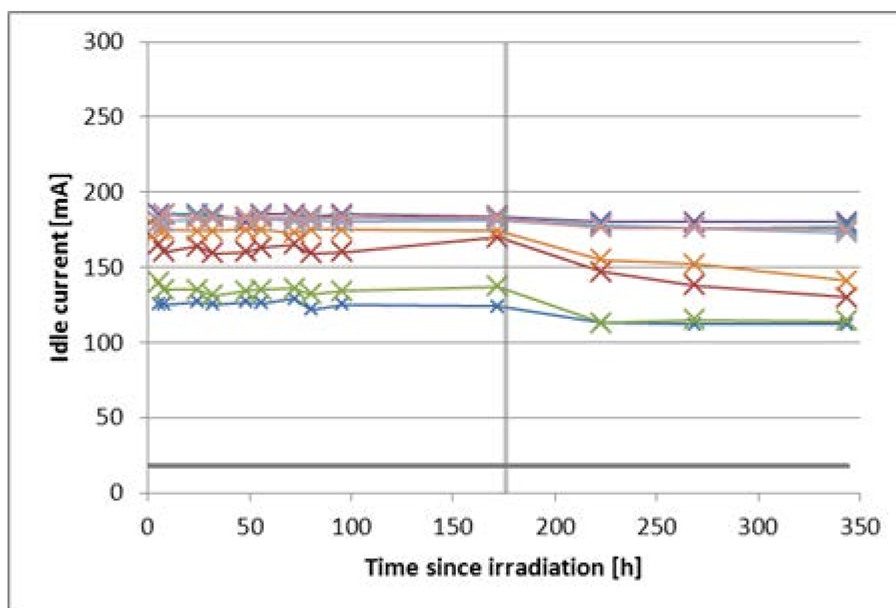

Figure 6-65: Idle current annealing, Nanya NT5CB512M8CN-EK, unbiased.
The horizontal, grey line indicates the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

© Airbus DS GmbH

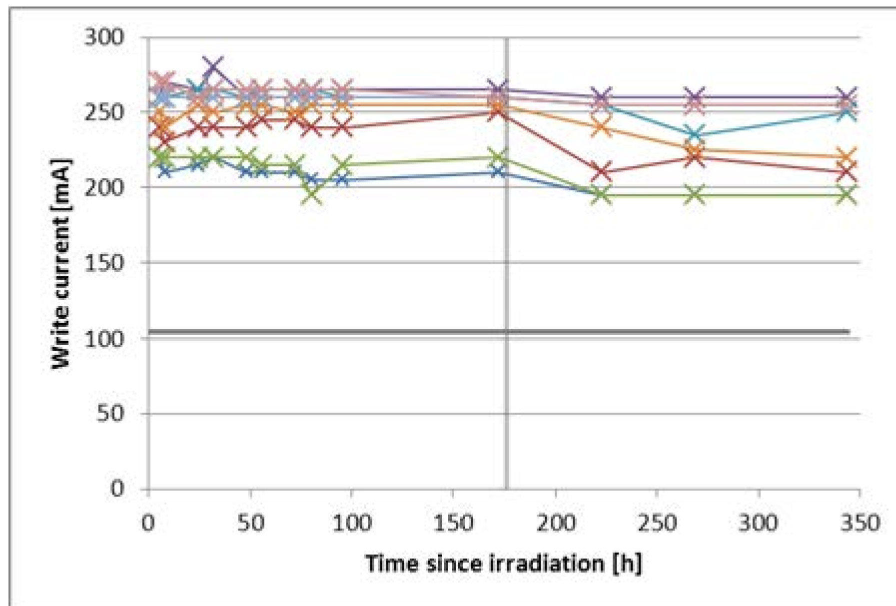

Figure 6-66: Write current annealing, Nanya NT5CB512M8CN-EK, unbiased.
The horizontal, grey line indicates the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

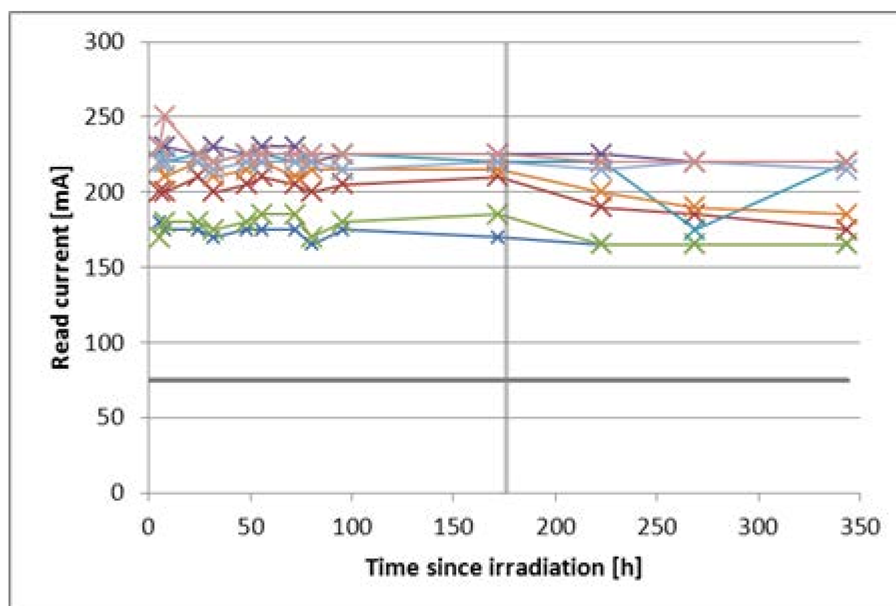

Figure 6-67 Read current annealing, Nanya NT5CB512M8CN-EK, unbiased.
The horizontal, grey line indicates the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

Since the SK Hynix DUTs (H5TQ4G83MFR-H9CR) contained no errors, no error annealing could be observed. The same is true for the unbiased Micron DUTs. The operated Micron DUTs and the unbiased Nanya DUTs both contained too many errors to make useful error annealing measurements.

6.4 Conclusions on DDR3 TID Test Campaigns

Different DUTs of all of the parts had been tested by unbiased irradiation before.

The low number of errors in some of the unbiased SK Hynix DUTs is consistent with previous tests [3, 4]. Other SK Hynix DUTs showed an error pattern that had not been observed before.

Both, the unbiased Micron DUTs not having any errors at all and the very high number of errors in the Nanya DUTs are consistent with previous tests.

The SK Hynix device behaves similarly whether unbiased or operating, with respect to both current and errors. This is similar to the Samsung devices, where the difference between unbiased and operating DUTs was also small.

The Micron device, on the other hand, is totally different. While the unbiased DUTs had no errors at all (which is the best result of all parts tested so far), the operated DUTs showed the highest current increase of all parts so far, and also the highest number of errors. Although the number of errors may be caused by insufficient power supply for the high current, the high current alone may make such a device unsuitable for space applications.

Regarding these outcome, the SK Hynix H5TQ4G83MFR-H9CR is most suitable for use in JUIC mission. But also the Samsung K4B4G0846B-HCH9 device might be an option. The Nanya NT5CB512M8CN-EK needs in-situ testing to judge its applicability for harsh space radiation environments like in JUICE mission.

7 Conclusions

In the frame of ESA Rad Hard Memory study latest technology and heritage SLC NAND Flash and a wide spread of DDR3 SDRAM devices have been characterized regarding their radiation sensitivity. Exhaustive SEE tests with heavy ions as well as with protons were performed. In Four campaigns, the TID sensitivities were investigated.

With respect to the envisaged JUICE (Laplace) mission, the TID sensitivity is the main driver for part selection. For mission to Jovian system TID levels of more than 300 krad inside equipments are expected. Even behind significant amount of shielding, predicted TID level are still in the range of 50 - 100 krad.

TID:

Heritage SLC NAND Flash i.e., Samsung K9WBG08U1M, confirmed their outstanding radiation performance. They remained functional up to the final dose of > 90krad, first data errors occurred not before 70krad.

High scaled SLC NAND Flash technology i.e., Micron devices in 25nm feature size, is more sensitive to radiation effects than former generations. Nevertheless, they are still well suitable for applications with TID levels up to about 25krad. For use in JUICE mission further shielding is mandatory.

The radiation behaviour of modern DDR3 SDRAM is very promising. One candidate, SK Hynix H5TQ4G83MFR was almost insensitive to TID levels > 400krad, also the Samsung K4B4G0846B kept functional up to 400krad(Si), the onset threshold for data errors is > 150krad(Si).

SEE:

Modern DDR3 SDRAM devices are less sensitive to SEU than latest SLC NAND Flash devices. Nevertheless, DDR3 SDRAM devices are quite sensitive to SEFI. Due to their volatility of stored data, special measures have to be taken for mitigation. In contrary, tested SLC NAND Flash devices showed a comparable (Micron 25nm) or even better SEFI behaviour. Furthermore, SEFI can be easily mitigated by power cycling of the devices without data loss. The predicted SEU and SEFI rates for JUICE mission are provided in Table 7-1 and Table 7-2.

One clear trend is the increased sensitivity to protons with scaling for both technologies. At feature sizes < 40nm increased SEE sensitivities at low energies were observed. These devices are susceptible to direct ionisation by protons. Further investigations with low energy protons are recommended.

None of the tested devices exhibit any Single Event Latch-up, even at elevated temperatures of >80°C and LET ≥ 60 MeV $cm^2 mg^{-1}$.

However, SLC NAND flash has been confirmed to be sensitive to destructive events. With scaling, the onset LET for such events is reduced from about 30 MeV $cm^2 mg^{-1}$ for heritage technology devices (Samsung 51nm SLC, K9WBG08U1M) to about 10…15 MeV $cm^2 mg^{-1}$.(Micron 25nm SLC , MT29F16G08ABACAWP-IT:C). Nevertheless, the resulting rates are still acceptable - even more, when they are mitigated by the applied error correction. Up to now, no in-orbit failure due to SEE has been observed for the Samsung heritage devices. In Table 7-3 the predicted rates for JUICE mission are provided.

Table 7-1: Predicted SEU rates (per bit and day) for JUICE mission.

SEU [bit^{-1}day^{-1}]*	Quiet (JUICE)		Solar Flare (CREME96, WW)	
	HI	Protons	HI	Protons
NAND Flash				
K9WBG08U1M	8.8E-12	5.2E-14	7.9E-10	4.4E-10
	∑ = 8.9E-12		**∑ = 1.2E-09**	
MT29F16G08ABACAWP-IT:C/	5.7E-10	8.1E-10	3.6E-08	1.3E-06
MT29F32G08ABAAAWP-IT:A	**∑ = 1.4E-09**		**∑ = 1.3E-06**	
DDR3 SDRAM				
H5TQ4G83MFR	1.0E-14	1.6E-12	9.0E-13	4.1E-09
	∑ = 1.6E-12		**∑ = 4.1E-09**	
K4B4G0846B	5.03E-13	4.1E-13	4.5E-11	1.09E-09
	∑ = 9.1E-13		**∑ = 1.0E-09**	

Table 7-2: Predicted SEFI rates (per die and day) for JUICE mission.

SEFI [day^{-1}]†	Quiet (JUICE)		Solar Flare (CREME96, WW)	
	HI	Protons	HI	Protons
NAND Flash				
K9WBG08U1M	1.3E-05	7.9E-07	1.4E-03	6.1E-03
	∑ = 1.4E-05		**∑ = 7.5E-03**	
MT29F16G08ABACAWP-IT:C/	4.1E-04	4.5E-04	1.8E-01	1.3
MT29F32G08ABAAAWP-IT:A	**∑ = 8.6E-04**		**∑ = 1.5**	
DDR3 SDRAM				
H5TQ4G83MFR	6.6E-04	6.5E-05	4.8E-01	2.1E-01
	∑ = 7.3E-04		**∑ = 6.9E-01**	
K4B4G0846B	7.9E-05	7.2E-07	2.9E-02	3.6E-02
	∑ = 8.6E-05		**∑ = 6.5E-02**	

* SEU rates have been calculated assuming z=1µm for DDR3, and z=0.1µm for flash (FG).

† SEFI rates have been calculated assuming z=1µm.

© Airbus DS GmbH

Table 7-3: Predicted rates of destructive failures (per die and day) for JUICE mission.

Destructive Failure [day^{-1}]‡	Quiet (JUICE)		Solar Flare (CREME96, WW)	
	HI	Protons	HI	Protons
NAND Flash				
K9WBG08U1M	2.5E-09	-	2.2E-07	-
	∑ = 2.5E-09 (0.1 FIT)		**∑ = 2.2E-07**	
MT29F16G08ABACAWP-IT:C	1.0E-07	-	9.6E-06	-
	∑ = 1.0E-7 (4.3 FIT)		**∑ = 9.6E-06**	

To summarize, both commercial technologies are well suited for space applications. Regarding the very harsh TID requirements, DDR3 SDRAMs might be the preferred technology for JUICE mission. However, their outstanding TID performance has to be traded against their sensitivity to SEFI and the needed mitigation measures like sophisticated error correction as well as the needed high-speed low voltage periphery.

SLC NAND flash devices are much more convenient for application in space due to their non-volatility and good SEE behaviour. However, they are more sensitive to TID degradation. Measures to mitigate destructive failures have to be implemented.

‡ DF rates have been calculated assuming 1000 sensitive nodes, z=1µm. The intrinsic failure rate $\lambda_{intrinsic}$ for both devices is in the order of < 10 FIT.

© Airbus DS GmbH

Appendix A. Performed Test Campaigns

Campaign	Date	Facility	Descriptions
SEE_HI_1	May 23-27, 2011	RADEF, JYFL	1st SEE test of 2Gb DDR3 SDRAMs & further tests on the angular dependency of static SEU for Samsung 4x8 Gb and Micron 8 Gb SLC NAND Flash memories [DD-01], [DD-02]
SEE_HI_2	Jan. 9-13, 2012	RADEF, JYFL	SEE characterisation of Micron 16 Gb/32 Gb SLC NAND Flash memories & 2Gb/4 Gb DDR3 SDRAM [DD-03], [DD-04], [DD-05], [DD-06]
SEE_HI_3	Apr. 16-20, 2012	RADEF, JYFL	Further SEE characterisation of Micron 16 Gb/32 Gb SLC NAND Flash memories & 2Gb/4 Gb DDR3 SDRAM [DD-03], [DD-04], [DD-05], [DD-06]
SEE_HI_4	Dec. 4-7, 2012	TAMU	High range SEE testing of DDR3 SDRAM and 1st angular characterisation of Micron 16 Gb SLC NAND Flash memories [DD-07], [DD-09], [DD-10]
SEE_P_1	Mar. 22-23, 2014	PIF, PSI	Protons SEE test on 4 Gb DDR3 SDRAM [DD-18], [DD-20]
SEE_P_2	Apr. 4-6, 2014	PIF, PSI	Protons SEE test on Micron 16 Gb/32 Gb SLC NAND Flash memories [DD-17], [DD-19]
TID_1	Oct. 22-26, 2012	ESTEC Co-60	1st in-situ TID testing of 4 Gb DDR3 SDRAM [DD-08], [DD-11]
TID_2	Mar. 11-18, 2013	ESTEC Co-60	Unbiased preselecting TID tests on DDR3 SDRAM [DD-12].
TID_3	Oct. 18-22, 2013	ESTEC Co-60	Unbiased preselecting TID tests on DDR3 SDRAM [DD-13]
TID_4	Jan. 17-23, 2014	ESTEC Co-60	In-situ TID testing of Micron 16 Gb/32 Gb SLC NAND Flash memories & 4 Gb DDR3 SDRAM [DD-17],

© Airbus DS GmbH

Appendix B. Procured Parts

Table B-1: List of procured parts by Airbus Defence & Space (Astrium)

Type	Function	Vendor	Mask Rev.	Date Code	Manuf. Lot	Quality	Delivery Date	Amn.	Assigned Campaigns
NAND Flash									
K9WBG08U1M-PIB0	SLC NAND Flash 4x8 Gb	SAM K	M / 51nm	0837	FMH030X2	Ind.	23.11.2010	50	SEE_HI_1, SEE_P_2 TID_4
MT29F16G08ABACAWP-IT:C	SLC NAND Flash 16 Gb	MIC U	C / 25nm	1122		Ind.	13.10.2011	50	SEE_HI_2, SEE_HI_3
MT29F16G08ABACAWP-IT:C	SLC NAND Flash 16 Gb	MIC U	C / 25nm	1146		Ind.	19.03.2012	90	SEE_HI_3, SEE_HI_4
MT29F16G08ABACAWP-IT:C	SLC NAND Flash 16 Gb	MIC U	C / 25nm	1218		Ind.	11.07.2012	50	SEE_P_2 TID_4
MT29F32G08ABAAAWP-IT:A	SLC NAND Flash 32 Gb	MIC U	A / 25nm	1130		Ind.	13.10.2011	50	SEE_HI_2, SEE_HI_3, SEE_HI_4
MT29F32G08ABAAAWP-IT:A	SLC NAND Flash 32 Gb	MIC U	A / 25nm	1134		Ind.	19.03.2012	50	SEE_P_2 TID_4
DDR3 SDRAM									
EDJ4208BASE-DJ-F	DDR3 SDRAM 4 Gb	ELP J	A / 4xnm	1044	OWPEY00	Com.	06.07.2011	72	SEE_HI_2, SEE_HI_3, TID_2
H5TQ2G83BFR-H9CR	DDR3 SDRAM 2 Gb	SKH K	B / ?		DTK89426H3	Com.	06.07.2011	50	
H5TQ2G83BFR-H9CR	DDR3 SDRAM 2 Gb	SKH K	B / ?	1223	DTKBA778H1	Com.	11.07.2012	50	TID_2
H5TQ4G83MFR-H9C	DDR3 SDRAM 4 Gb	SKH K	M / 44nm	1223		Com.	11.07.2012	46	SEE_HI_4; TID_1, TID_2
H5TQ4G83MFR-H9C	DDR3 SDRAM 4 Gb	SKH K	M / 44nm	144A		Com.	23.05.2013	50	SEE_P_1, TID_2, TID_4
MT41J256M8HX-15E:D	DDR3 SDRAM 2 Gb	MIC U	D / 50nm	1116	BY8F416.21	Com.	01.06.2011	50	TID_2

© Airbus DS GmbH

Type	Function	Vendor	Mask Rev.	Date Code	Manuf. Lot	Quality	Delivery Date	Amn.	Assigned Campaigns
MT41J512M8RH-093:E	DDR3 SDRAM 4 Gb	MIC U	E / 30nm	1324	DRRKDNB.11	Com.	06.08.2013	150	SEE_P_1, TID_3, TID_4
NT5CB256M8BN-CG	DDR3 SDRAM 2 Gb	NAN TW	B / 50nm	1110	05142700FP L TW	Com.	06.07.2011	50	
NT5CB256M8BN-CG	DDR3 SDRAM 2 Gb	NAN TW	B / 50nm	1145	132154F0FF L TW	Com.	11.07.2012	50	
NT5CB256M8GN-CG	DDR3 SDRAM 2 Gb	NAN TW	G / 35nm	1218	20726200EP 7 TW	Com.	11.07.2012	50	
NT5CB512M8CN-EK	DDR3 SDRAM 4 Gb	NAN TW	C / 3xnm	1238	22755400GP 3 TW	Com.	06.08.2013	150	SEE_P_1, TID_3, TID_4
K4B2G0846D-HCH9	DDR3 SDRAM 2 Gb	SAM K	D / 35nm	1113	GEB701GES	Com.	04.08.2011	21	SEE_HI_3
K4B2G0846D-HCH9	DDR3 SDRAM 2 Gb	SAM K	D / 35nm	1117	GEB66SFFC	Com.	04.08.2011	29	TID_2
K4B2G0846D-HCH9	DDR3 SDRAM 2 Gb	SAM K	D / 35nm	1122	GEDN60GKU	Com.	23.03.2012	50	SEE_HI_4, TID_2
K4B4G0846B-HCH9	DDR3 SDRAM 4 Gb	SAM K	B / 35nm	1125	GMD02390	Com.	04.08.2011	50	SEE_HI_2, SEE_HI_3, SEE_HI_4
K4B4G0846B-HCH9	DDR3 SDRAM 4 Gb	SAM K	B / 35nm	1204	GMK3599Q	Com.	19.03.2012	50	SEE_HI_4, SEE_P_1 TID_1, TID_2
K4B4G0846B-HCH9	DDR3 SDRAM 4 Gb	SAM K	B / 35nm	1216	GMC7679W	Com.	23.05.2013	50	TID_3

Table B-2: List of additional parts provided by IDA

Type	Function	Vendor	Mask Rev.	Date Code	Manuf. Lot	Quality	Delivery Date	Amn.	Assigned Campaigns
NAND Flash									
K9WBG08U1M-PIB0	SLC NAND Flash 4x8 Gb	SAM K	M / 51nm	0816	FFC042X1	Ind.	-	-	SEE_HI_1, TID_4
K9WBG08U1M-PIB0	SLC NAND Flash 4x8 Gb	SAM K	M / 51nm	0925	FME071P2	Ind.	-	-	SEE_HI_1, TID_4
MT29F8G08AAAWP-ET:A	SLC NAND Flash 8 Gb	MIC U	A / 50nm	0846	-	Ind.	-	-	SEE_HI_1
MT29F128G08AJAAAWP-ITZ:A	SLC NAND Flash 4x32 Gb	MIC U	A / 25nm; polyimide coating	1314	-	Ind.	-	-	SEE_P_2
DDR3 SDRAM									
K4B2G0846B-HCH9000	DDR3 SDRAM 2 Gb	SAM K	B / 50nm	0949	GLJ423AC	Com.	-	-	SEE_HI_1, SEE_HI_2, TID_2
MT41J256M8HX-15E:D	DDR3 SDRAM 2 Gb	MIC U	D / 50nm	1006	BYFCM91.21	Com.	-	-	SEE_HI_1, SEE_HI_2, TID_2
NT5CB256M8BN-CG	DDR3 SDRAM 2 Gb	NAN TW	B / 50nm	1026	01340100GP 7 TW	Com.	-	-	SEE_HI_1, SEE_HI_2, SEE_HI_4, TID_2