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Proton SEE Test of 4-Gbit DDR3 SDRAM Devices from Hynix, Micron and Samsung
Test report

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1 Abstract

From March 22 to March 22, 2014, we performed a proton SEE test with DDR3 SDRAM devices at Paul Scherrer Institut, Villigen, Switzerland. This document reports on the findings.

2 Test setup

2.1 DUTs

We tested three part types from Samsung, Hynix, and Micron, as shown in table 1. All tested DUTs were soldered to SODIMM modules. Other than that, none of the DUTs were prepared in any way, such as opening or thinning.

Table 1: tested DUTs

Manufacturer **Part number**	**Lot codes**	**Date code**	**Samples**	**Photos**
Samsung K4B4G0846B-HCH9	GMK3599Q	1204	6	
Hynix H5TQ4G83MFR-H9C	DTLB0241BH DTLB0213HA DWLB1642E2 DWLB151681	Unknown	6	 

				
Micron MT41J512M8RH-093:E	Unknown	Unknown	6	

2.2 Test facility

The tests were performed at the Proton Irradiation Facility (PIF) of Paul Scherrer Institut (PSI) at Villigen, Switzerland. We used proton energies of 21, 33, 42, 60, 100, and 230 MeV.

The primary energies were 230 MeV, 100 MeV and 74 MeV. Energies of 60 MeV and below were obtained by degrading the 74 MeV proton beam with copper degraders.

2.3 Test bench

The test bench, RTMC6 (figures 1 and 2), is capable of operating the DDR3 DUTs at a clock frequency of up to 400 MHz. It is based on a Xilinx ML605 evaluation board, which contains a Xilinx Virtex6 FPGA.

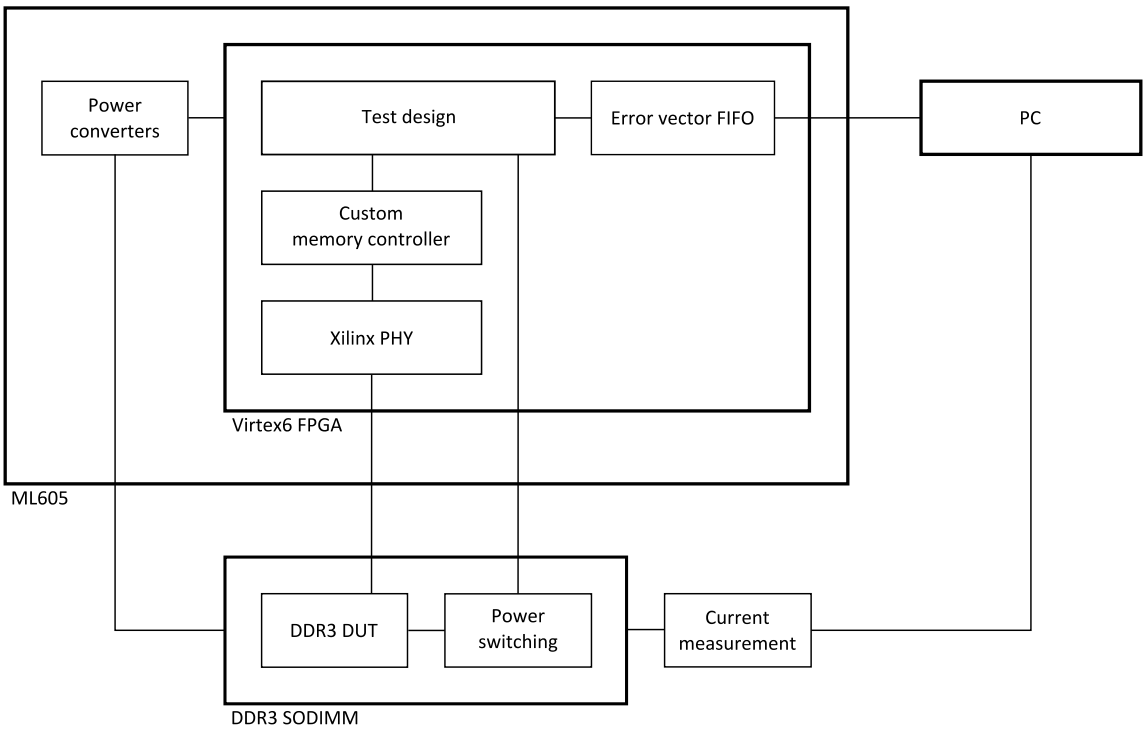

Figure 1: an overview of the RTMC6 test bench (simplified)

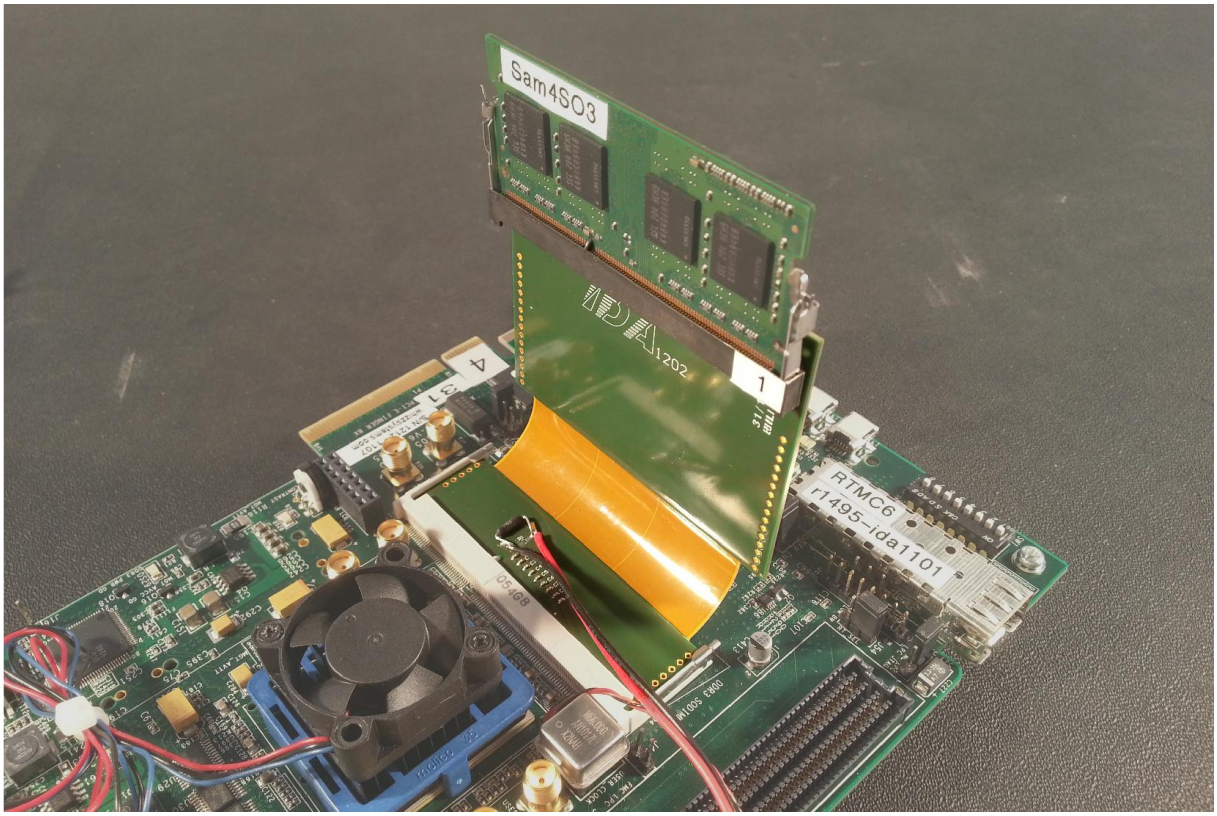

Figure 2: the RTMC6 head station with a DDR3 SODIMM and a flexible extension board

The ML605 is equipped with a small outline dual inline memory module (SODIMM) socket designed for commercially available memory modules. To increase the distance between the DUTs and the FPGA, we developed an extension board consisting of a rigid part and a flexible part. For this test, two of these extension boards were connected in series.

The DUT current is measured at a sampling rate of 1 Hz and is logged by the PC.

The FPGA contains a custom test design which writes a constant, counting or pseudo-random pattern to the DUT, reads the data from the DUT and compares it to the original pattern. If the data is different from the pattern, an error vector is generated and transmitted to a PC via a high speed USB connection. Since the DUT has a higher data transfer rate than the USB connection, error vectors have to be buffered in a FIFO in order to be able to handle large runs of consecutive errors without slowing down the test. If the error record FIFO overflows due to too many errors, error vectors are either discarded or the test is slowed down, at the user's choice.

The DUT is controlled by a custom memory controller. This memory controller provides fine-grained control of the DUT and allows performing operations such as writing the mode registers, resetting the DLL of the DUT or calibrating the termination resistance at arbitrary times. It interfaces with Xilinx' DDR3 PHY (the lowest DUT interface design layer).

On the PC, an error map is displayed for preliminary visual analysis, along with a total error count and various statistics. The error vectors are stored on disk for offline analysis.

2.4 Test sequence

The following test modes are available in order to test the behavior of the device in different situations:

- Storage mode: before irradiation, the pattern is written into the DUT and read in order to determine hard errors. After irradiation, the contents of the device are read and compared to the pattern.
- Read mode: before irradiation, the pattern is written into the DUT and read in order to determine hard errors. During irradiation, the device is continuously read.

2.5 Error classification

Several error classes are distinguished, according to the overview shown in figure 3:

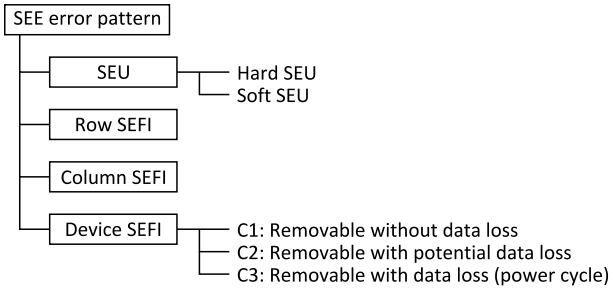

Figure 3: error classification overview

- SEUs are isolated single-bit or multi-bit errors. An SEU is called a *hard SEU* if it cannot be removed by writing the cell again. All other SEUs are called *soft SEUs*. In contrast to soft SEUs, a hard SEU cannot be removed by scrubbing.
- Row SEFIs and column SEFIs are errors that corrupt a single row or column, respectively. The row or column may be corrupted completely or in part.
- Device SEFIs are errors that corrupt a whole device or an extended region of a device. Some device SEFIs can be removed by operations such as rewriting the mode registers of the DUT. These operations do not result in data loss. Other device SEFIs can only be removed by resetting the DUT. The specification does not guarantee data retention in this case. But in practice, no data loss has been observed. Some device SEFIs can only be removed by power cycling the DUT, which always causes data loss.

An example error map, containing SEUs, row SEFIs and column SEFIs is shown in figure 4.

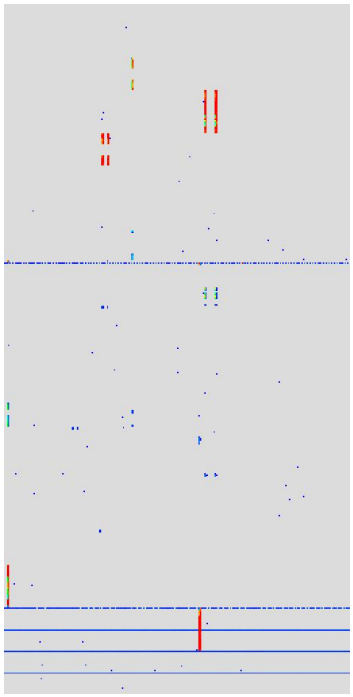

Figure 4: an error map showing row SEFIs, column SEFIs and SEUs

3 Test results

The tests were performed at an operating frequency of 333 MHz with a pseudo-random pattern. Due to the limited available test time, all tests were performed *without* software conditioning.

The total dose received by any DUT was less than 40 krad for the Samsung and Micron parts, even under the pessimistic assumption that all neighboring DUTs in the head station received the same dose as the DUT in the beam path. From our previous TID tests with ^{60}Co, it is known that this dose does not cause any errors. The dose received by the Hynix parts was higher, at around 80 krad, but the Hynix parts have been shown to be even less sensitive to total dose than the other parts.

3.1 Cross sections

The following diagrams show the cross section versus energy for different devices, for a given error class and test mode. Open symbols represent runs where no errors of the respective class were observed. In this case, the value represents an upper limit.

3.1.1 SEUs

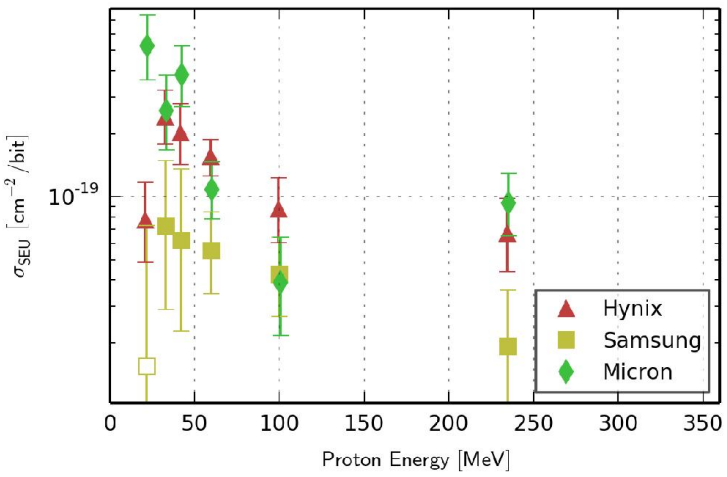

Figure 5: SEU cross section in read mode

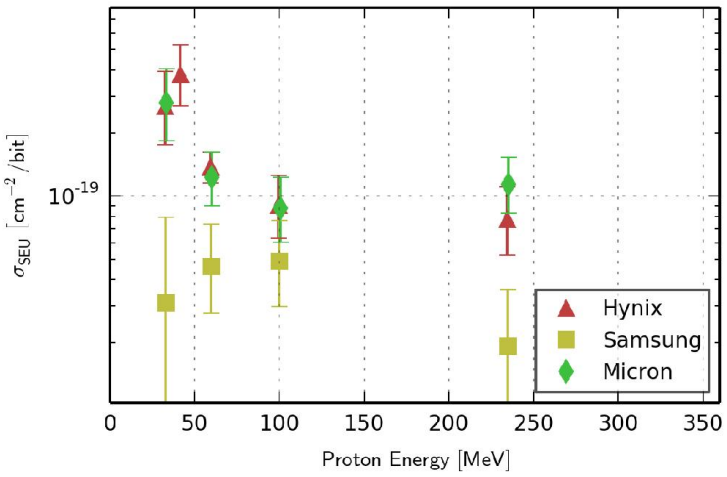

Figure 6: SEU cross section in storage mode

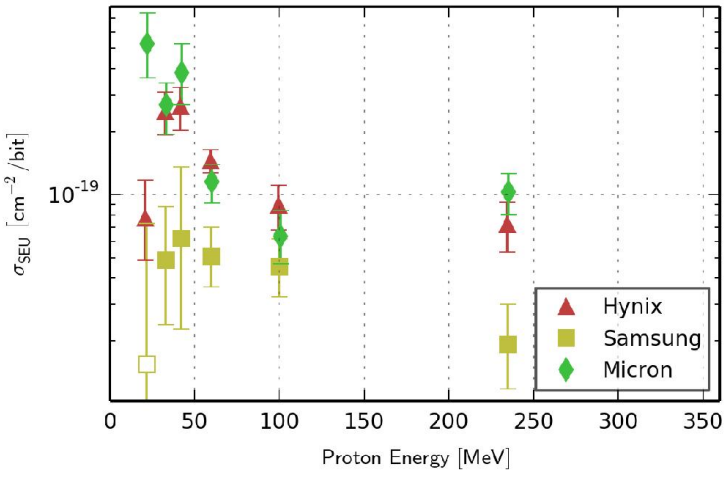

Figure 7: SEU cross section in any mode

3.1.2 Row SEFIs

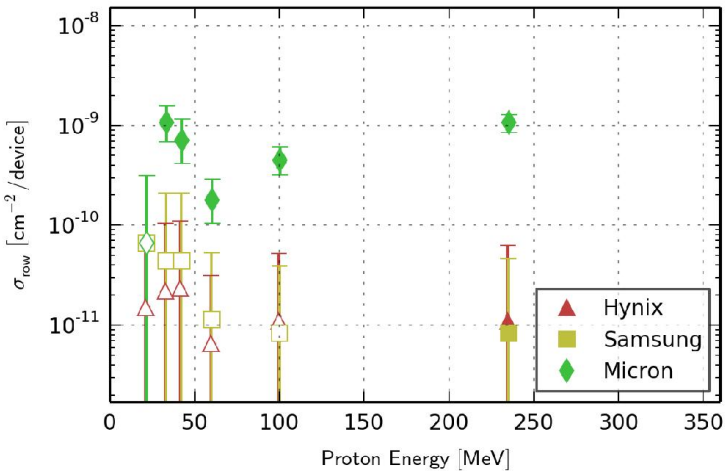

Figure 8: row SEFI cross section in read mode

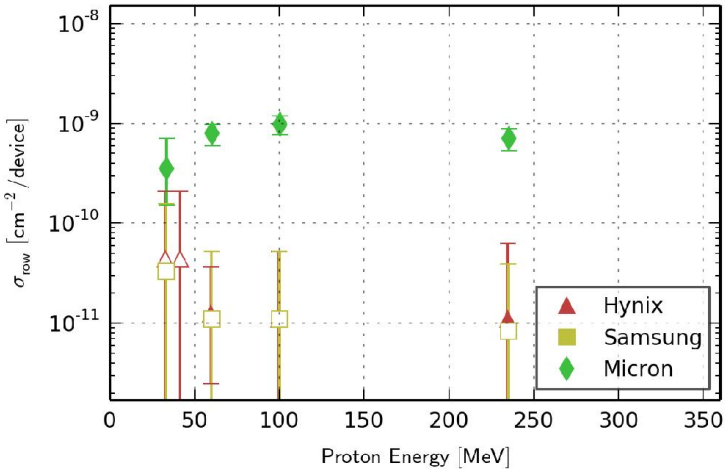

Figure 9: row SEFI cross section in storage mode

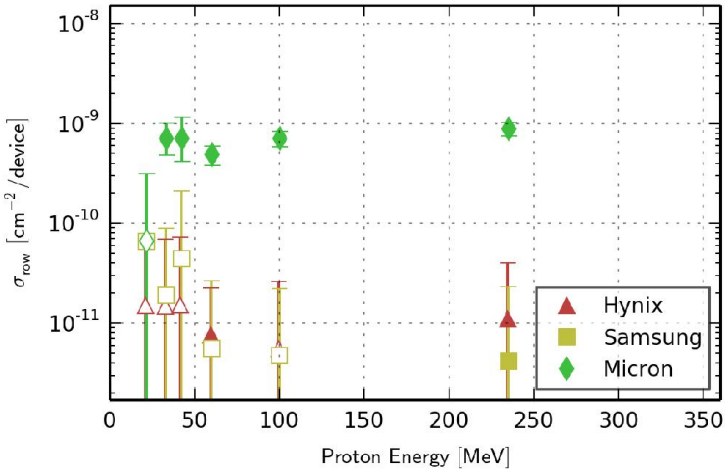

Figure 10: row SEFI cross section in any mode

3.1.3 Column SEFIs

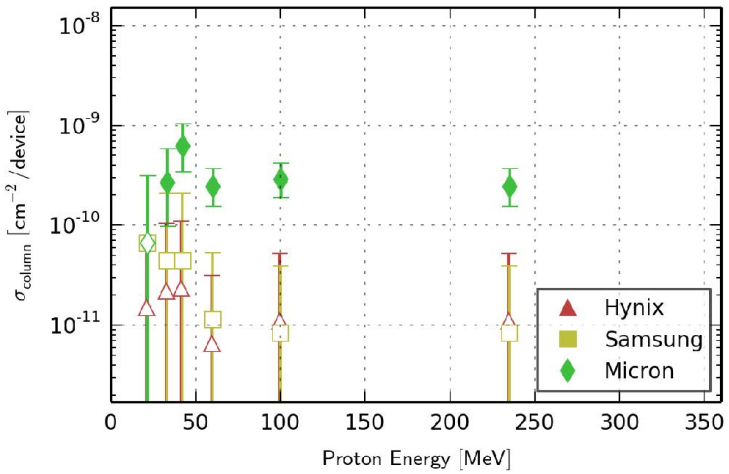

Figure 11: column SEFI cross section in read mode

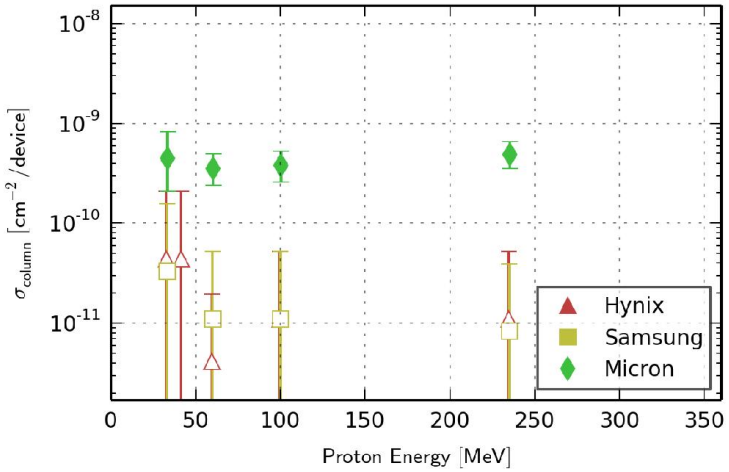

Figure 12: column SEFI cross section in storage mode

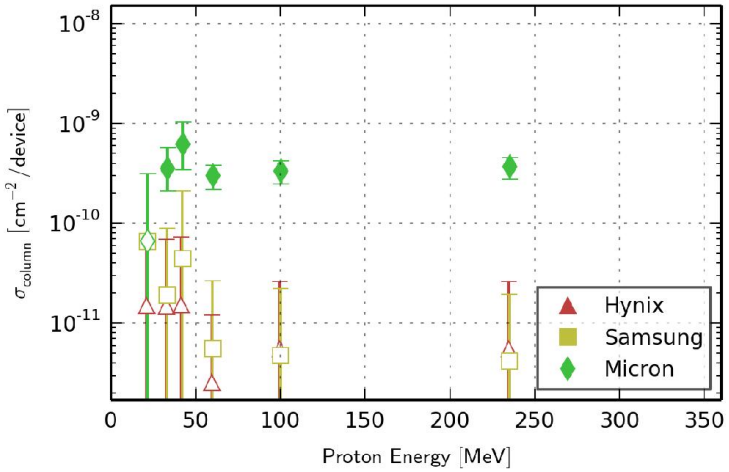

Figure 13: column SEFI cross section in any mode

3.1.4 Device SEFIs

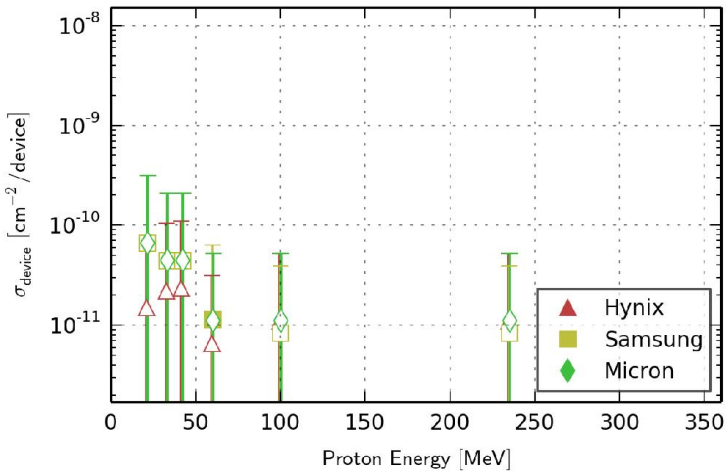

Figure 14: device SEFI cross section in read mode

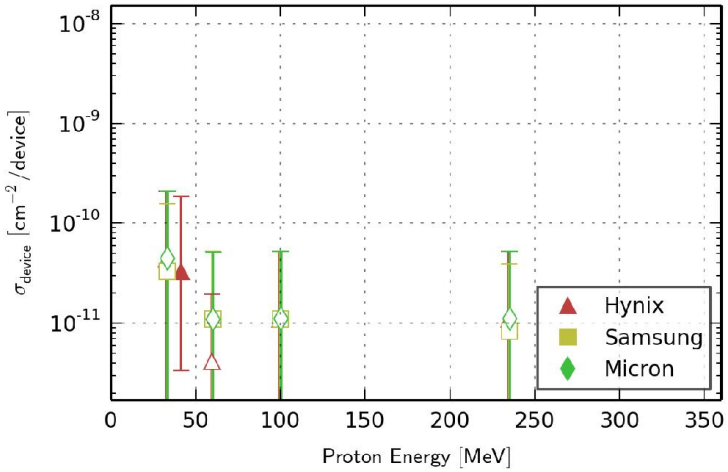

Figure 15: device SEFI cross section in storage mode

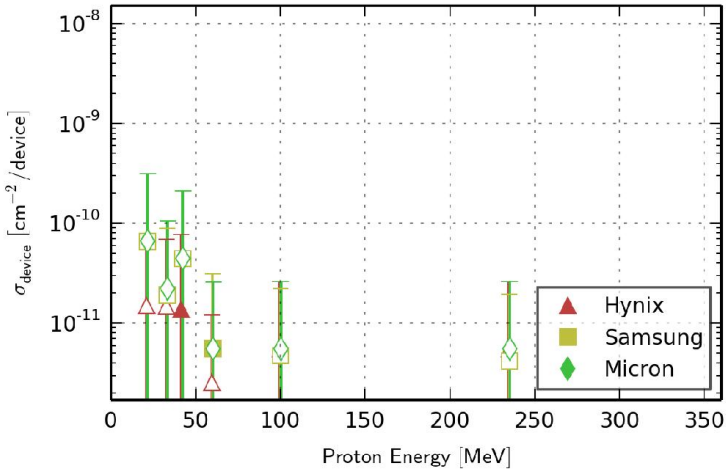

Figure 16: device SEFI cross section in any mode

3.1.5 Discussion

The cross sections are very similar for the two test modes (read mode and storage mode). This is plausible because dynamic memories perform a periodic refresh operation (every 7.8 µs in the case of DDR3) which opens and precharges banks, similar to what happens during a read operation.

The SEU cross section remains well below the die area per bit ($\approx 2 \cdot 10^{-10}$ cm^2) for all devices. This is in contrast to heavy-ion tests, where the SEU cross section was close to the die area per bit for high LET ions.

Column SEFIs were only observed for Micron parts. Samsung and Hynix parts did not show any column SEFIs at all.

Device SEFIs are rare: during 169 irradiation runs, only three device SEFIs were observed:

1. Samsung at 60 MeV in read mode
2. Hynix at 42 MeV in storage mode
3. Micron at 60 MeV; the DUT was in the beam path during several irradiations of another DUT while not being exercised. The fluence that caused the SEFI is therefore not known and the SEFI is not included in the cross section calculation.

All device SEFIs could be removed by applying C1 (non-destructive) measures, i. e. rewrite all mode registers, reset the DLL, and perform a ZQ calibration. Which of these measures removed the SEFI was not examined.

No single-event latch-ups or destructive errors were observed for any device at any energy.

3.2 Error direction

Errors can either be in the 0 → 1 direction (i. e. bits written as 0, but read as 1 after irradiation) or in the 1 → 0 direction. Figure 17 shows the share of 0 → 1 errors (for SEUs only) for the different parts vs. proton energy. The Hynix and Samsung parts have almost only 1 → 0 errors (less than 1% 0 → 1 errors). For the Micron parts, the share of error directions is approximately equal. Very likely, this indicates an equal distribution of logical “1” states to physical “0” and “1” states.

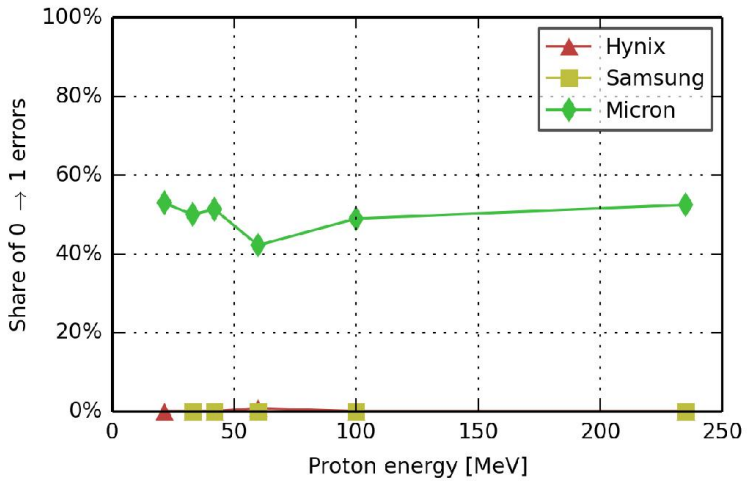

Figure 17: SEU direction

3.3 Error patterns

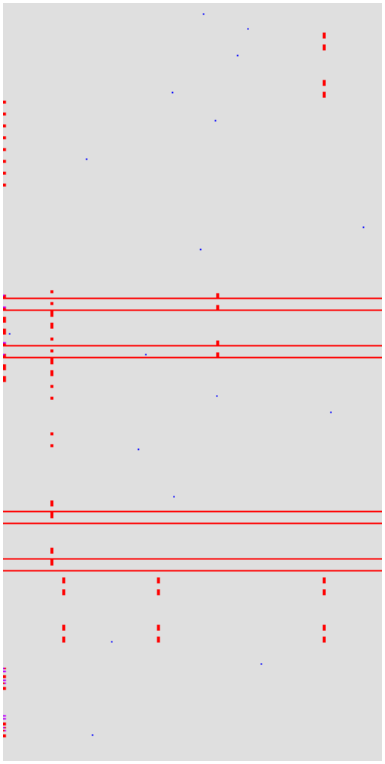

Figure 18: row errors typically occur in patterns. Each horizontal line actually consists of two consecutive rows. Micron DUT in storage mode at 60 MeV.

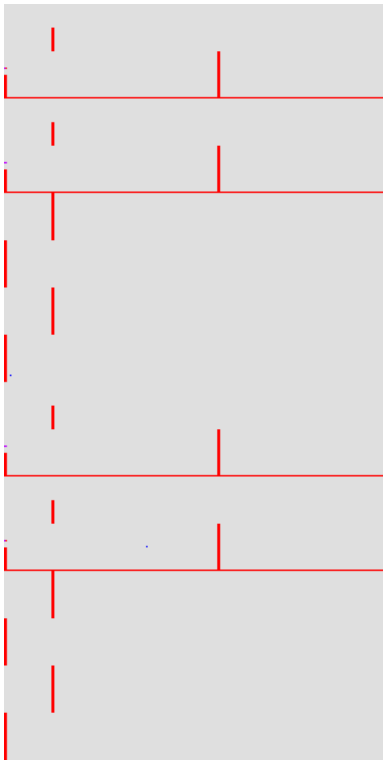

Figure 19: close-up of bank #4 in the same run as shown in figure 18. The column error patterns are linked to the row error patterns.

Column errors typically are non-contiguous and affect whole bursts, i. e. the same consecutive 8 columns are affected in a range of rows.

For Micron devices, row errors often occur in groups, as shown in figure 18. Each horizontal line in this figure actually consists of two consecutive rows of errors. In read mode, groups of four pairs typically appear simultaneously (figure 18 contains two such groups).

Figure 19 shows a close-up of one eighth of the device address space (one bank, specifically bank #4) of the same run as figure 18. The column errors display a periodicity that coincides with the row error periodicity.

Errors in row and column SEFIs do not have a preferred direction, even for Samsung and Hynix devices, where almost all SEUs have the same direction.

3.4 Hard SEUs

The DUTs were written and read before each irradiation to determine the number of hard SEUs. Additionally, the same operation was performed after each set of irradiations with one DUT.

Hard SEUs are created for all part types and at all energies. It is, however, not possible to reliably determine a cross section because (a) the number of hard SEUs is very low and (b) some of the hard SEUs anneal quickly: for some irradiation runs, the number of hard SEUs was lower after the irradiation than before (i. e. the number of hard SEUs that annealed during the irradiation exceeds the number of newly created hard SEUs).

Long-term annealing measurements could not be performed because the DUTs, having been activated by irradiation, had to remain at PSI.

Despite the fact that a proper analysis of hard errors was not possible, some qualitative conclusions can still be reached:

- Generally, the number of hard SEUs seems to increase slightly with proton energy. This is in contrast to the SEU cross section, which decreases with proton energy.
- The Micron parts are the most sensitive parts, with an estimated cross section of $5 \cdot 10^{-20}$ cm^2 per bit at 230 MeV.
- The Samsung parts are the least sensitive parts: no hard SEUs were observed except 2 hard SEUs at 230 MeV, corresponding to a cross section of $2 \cdot 10^{-21}$ cm² per bit. This corresponds to the fact that the Samsung parts are also the least sensitive to SEUs. These 2 hard SEUs annealed within 4 minutes.

4 Appendix A: Raw cross section data

The table in this section contains the number of errors and the corresponding fluence for all parts, test modes, error classes, and energy values (in MeV).

Table 1: Raw cross section data

Part	Test mode	Error class	Energy	Errors	Fluence
4-Gbit Elpida	Read	SEU	21.37	22	6.6e+10
4-Gbit Elpida	Read	SEU	32.88	47	4.5e+10
4-Gbit Elpida	Read	SEU	41.9	37	4.2e+10
4-Gbit Elpida	Read	SEU	59.78	101	1.5e+11
4-Gbit Elpida	Read	SEU	100.0	34	9.0e+10
4-Gbit Elpida	Read	SEU	230.0	26	9.0e+10
4-Gbit Elpida	Read	Row SEFI	21.37	0	6.6e+10
4-Gbit Elpida	Read	Row SEFI	32.88	0	4.5e+10
4-Gbit Elpida	Read	Row SEFI	41.9	0	4.2e+10
4-Gbit Elpida	Read	Row SEFI	59.78	0	1.5e+11
4-Gbit Elpida	Read	Row SEFI	100.0	0	9.0e+10
4-Gbit Elpida	Read	Row SEFI	230.0	1	9.0e+10
4-Gbit Elpida	Read	Column SEFI	21.37	0	6.6e+10
4-Gbit Elpida	Read	Column SEFI	32.88	0	4.5e+10
4-Gbit Elpida	Read	Column SEFI	41.9	0	4.2e+10
4-Gbit Elpida	Read	Column SEFI	59.78	0	1.5e+11
4-Gbit Elpida	Read	Column SEFI	100.0	0	9.0e+10
4-Gbit Elpida	Read	Column SEFI	230.0	0	9.0e+10
4-Gbit Elpida	Read	Device SEFI	21.37	0	6.6e+10
4-Gbit Elpida	Read	Device SEFI	32.88	0	4.5e+10
4-Gbit Elpida	Read	Device SEFI	41.9	0	4.2e+10
4-Gbit Elpida	Read	Device SEFI	59.78	0	1.5e+11
4-Gbit Elpida	Read	Device SEFI	100.0	0	9.0e+10
4-Gbit Elpida	Read	Device SEFI	230.0	0	9.0e+10
4-Gbit Elpida	Storage	SEU	32.88	26	2.2e+10
4-Gbit Elpida	Storage	SEU	41.9	37	2.2e+10

4-Gbit Elpida	Storage	SEU	59.78	143	2.4e+11
4-Gbit Elpida	Storage	SEU	100.0	35	9.0e+10
4-Gbit Elpida	Storage	SEU	230.0	30	9.0e+10
4-Gbit Elpida	Storage	Row SEFI	32.88	0	2.2e+10
4-Gbit Elpida	Storage	Row SEFI	41.9	0	2.2e+10
4-Gbit Elpida	Storage	Row SEFI	59.78	3	2.4e+11
4-Gbit Elpida	Storage	Row SEFI	100.0	0	9.0e+10
4-Gbit Elpida	Storage	Row SEFI	230.0	1	9.0e+10
4-Gbit Elpida	Storage	Column SEFI	32.88	0	2.2e+10
4-Gbit Elpida	Storage	Column SEFI	41.9	0	2.2e+10
4-Gbit Elpida	Storage	Column SEFI	59.78	0	2.4e+11
4-Gbit Elpida	Storage	Column SEFI	100.0	0	9.0e+10
4-Gbit Elpida	Storage	Column SEFI	230.0	0	9.0e+10
4-Gbit Elpida	Storage	Device SEFI	32.88	0	2.2e+10
4-Gbit Elpida	Storage	Device SEFI	41.9	1	3.0e+10
4-Gbit Elpida	Storage	Device SEFI	59.78	0	2.4e+11
4-Gbit Elpida	Storage	Device SEFI	100.0	0	9.0e+10
4-Gbit Elpida	Storage	Device SEFI	230.0	0	9.0e+10
4-Gbit Micron	Read	SEU	21.37	34	1.5e+10
4-Gbit Micron	Read	SEU	32.88	25	2.2e+10
4-Gbit Micron	Read	SEU	41.9	37	2.2e+10
4-Gbit Micron	Read	SEU	59.78	42	9.0e+10
4-Gbit Micron	Read	SEU	100.0	15	9.0e+10
4-Gbit Micron	Read	SEU	230.0	36	9.0e+10
4-Gbit Micron	Read	Row SEFI	21.37	0	1.5e+10
4-Gbit Micron	Read	Row SEFI	32.88	24	2.2e+10
4-Gbit Micron	Read	Row SEFI	41.9	16	2.2e+10
4-Gbit Micron	Read	Row SEFI	59.78	16	9.0e+10
4-Gbit Micron	Read	Row SEFI	100.0	40	9.0e+10
4-Gbit Micron	Read	Row SEFI	230.0	96	9.0e+10
4-Gbit Micron	Read	Column SEFI	21.37	0	1.5e+10
4-Gbit Micron	Read	Column SEFI	32.88	6	2.2e+10
4-Gbit Micron	Read	Column SEFI	41.9	14	2.2e+10
4-Gbit Micron	Read	Column SEFI	59.78	22	9.0e+10
4-Gbit Micron	Read	Column SEFI	100.0	26	9.0e+10
4-Gbit Micron	Read	Column SEFI	230.0	22	9.0e+10
4-Gbit Micron	Read	Device SEFI	21.37	0	1.5e+10
4-Gbit Micron	Read	Device SEFI	32.88	0	2.2e+10
4-Gbit Micron	Read	Device SEFI	41.9	0	2.2e+10
4-Gbit Micron	Read	Device SEFI	59.78	0	9.0e+10
4-Gbit Micron	Read	Device SEFI	100.0	0	9.0e+10
4-Gbit Micron	Read	Device SEFI	230.0	0	9.0e+10
4-Gbit Micron	Storage	SEU	32.88	27	2.2e+10
4-Gbit Micron	Storage	SEU	59.78	48	9.1e+10
4-Gbit Micron	Storage	SEU	100.0	34	9.0e+10
4-Gbit Micron	Storage	SEU	230.0	44	9.0e+10

4-Gbit Micron	Storage	Row SEFI	32.88	8	2.2e+10
4-Gbit Micron	Storage	Row SEFI	59.78	72	9.1e+10
4-Gbit Micron	Storage	Row SEFI	100.0	88	9.0e+10
4-Gbit Micron	Storage	Row SEFI	230.0	64	9.0e+10
4-Gbit Micron	Storage	Column SEFI	32.88	10	2.2e+10
4-Gbit Micron	Storage	Column SEFI	59.78	32	9.1e+10
4-Gbit Micron	Storage	Column SEFI	100.0	34	9.0e+10
4-Gbit Micron	Storage	Column SEFI	230.0	44	9.0e+10
4-Gbit Micron	Storage	Device SEFI	32.88	0	2.2e+10
4-Gbit Micron	Storage	Device SEFI	59.78	0	9.1e+10
4-Gbit Micron	Storage	Device SEFI	100.0	0	9.0e+10
4-Gbit Micron	Storage	Device SEFI	230.0	0	9.0e+10
4-Gbit Samsung	Read	SEU	21.37	0	1.5e+10
4-Gbit Samsung	Read	SEU	32.88	7	2.2e+10
4-Gbit Samsung	Read	SEU	41.9	6	2.2e+10
4-Gbit Samsung	Read	SEU	59.78	21	8.8e+10
4-Gbit Samsung	Read	SEU	100.0	22	1.2e+11
4-Gbit Samsung	Read	SEU	230.0	10	1.2e+11
4-Gbit Samsung	Read	Row SEFI	21.37	0	1.5e+10
4-Gbit Samsung	Read	Row SEFI	32.88	0	2.2e+10
4-Gbit Samsung	Read	Row SEFI	41.9	0	2.2e+10
4-Gbit Samsung	Read	Row SEFI	59.78	0	8.8e+10
4-Gbit Samsung	Read	Row SEFI	100.0	0	1.2e+11
4-Gbit Samsung	Read	Row SEFI	230.0	1	1.2e+11
4-Gbit Samsung	Read	Column SEFI	21.37	0	1.5e+10
4-Gbit Samsung	Read	Column SEFI	32.88	0	2.2e+10
4-Gbit Samsung	Read	Column SEFI	41.9	0	2.2e+10
4-Gbit Samsung	Read	Column SEFI	59.78	0	8.8e+10
4-Gbit Samsung	Read	Column SEFI	100.0	0	1.2e+11
4-Gbit Samsung	Read	Column SEFI	230.0	0	1.2e+11
4-Gbit Samsung	Read	Device SEFI	21.37	0	1.5e+10
4-Gbit Samsung	Read	Device SEFI	32.88	0	2.2e+10
4-Gbit Samsung	Read	Device SEFI	41.9	0	2.2e+10
4-Gbit Samsung	Read	Device SEFI	59.78	1	8.8e+10
4-Gbit Samsung	Read	Device SEFI	100.0	0	1.2e+11
4-Gbit Samsung	Read	Device SEFI	230.0	0	1.2e+11
4-Gbit Samsung	Storage	SEU	32.88	4	3.0e+10
4-Gbit Samsung	Storage	SEU	59.78	18	9.0e+10
4-Gbit Samsung	Storage	SEU	100.0	19	9.0e+10
4-Gbit Samsung	Storage	SEU	230.0	10	1.2e+11
4-Gbit Samsung	Storage	Row SEFI	32.88	0	3.0e+10
4-Gbit Samsung	Storage	Row SEFI	59.78	0	9.0e+10
4-Gbit Samsung	Storage	Row SEFI	100.0	0	9.0e+10
4-Gbit Samsung	Storage	Row SEFI	230.0	0	1.2e+11
4-Gbit Samsung	Storage	Column SEFI	32.88	0	3.0e+10
4-Gbit Samsung	Storage	Column SEFI	59.78	0	9.0e+10

4-Gbit Samsung	Storage	Column SEFI	100.0	0	9.0e+10
4-Gbit Samsung	Storage	Column SEFI	230.0	0	1.2e+11
4-Gbit Samsung	Storage	Device SEFI	32.88	0	3.0e+10
4-Gbit Samsung	Storage	Device SEFI	59.78	0	9.0e+10
4-Gbit Samsung	Storage	Device SEFI	100.0	0	9.0e+10
4-Gbit Samsung	Storage	Device SEFI	230.0	0	1.2e+11
4-Gbit Nanya	Read	SEU	21.37	21	1.5e+10
4-Gbit Nanya	Read	SEU	32.88	22	2.2e+10
4-Gbit Nanya	Read	SEU	41.9	28	2.3e+10
4-Gbit Nanya	Read	SEU	59.78	29	9.0e+10
4-Gbit Nanya	Read	SEU	100.0	26	9.0e+10
4-Gbit Nanya	Read	SEU	230.0	31	9.0e+10
4-Gbit Nanya	Read	Row SEFI	21.37	0	1.5e+10
4-Gbit Nanya	Read	Row SEFI	32.88	16	2.2e+10
4-Gbit Nanya	Read	Row SEFI	41.9	8	2.3e+10
4-Gbit Nanya	Read	Row SEFI	59.78	88	9.0e+10
4-Gbit Nanya	Read	Row SEFI	100.0	104	9.0e+10
4-Gbit Nanya	Read	Row SEFI	230.0	144	9.0e+10
4-Gbit Nanya	Read	Column SEFI	21.37	2	1.5e+10
4-Gbit Nanya	Read	Column SEFI	32.88	10	2.2e+10
4-Gbit Nanya	Read	Column SEFI	41.9	12	2.3e+10
4-Gbit Nanya	Read	Column SEFI	59.78	58	9.0e+10
4-Gbit Nanya	Read	Column SEFI	100.0	36	9.0e+10
4-Gbit Nanya	Read	Column SEFI	230.0	32	9.0e+10
4-Gbit Nanya	Read	Device SEFI	21.37	0	1.5e+10
4-Gbit Nanya	Read	Device SEFI	32.88	0	2.2e+10
4-Gbit Nanya	Read	Device SEFI	41.9	0	2.3e+10
4-Gbit Nanya	Read	Device SEFI	59.78	0	9.0e+10
4-Gbit Nanya	Read	Device SEFI	100.0	0	9.0e+10
4-Gbit Nanya	Read	Device SEFI	230.0	0	9.0e+10
4-Gbit Nanya	Storage	SEU	32.88	20	2.2e+10
4-Gbit Nanya	Storage	SEU	59.78	46	9.0e+10
4-Gbit Nanya	Storage	SEU	100.0	22	9.0e+10
4-Gbit Nanya	Storage	SEU	230.0	33	9.0e+10
4-Gbit Nanya	Storage	Row SEFI	32.88	8	2.2e+10
4-Gbit Nanya	Storage	Row SEFI	59.78	160	9.0e+10
4-Gbit Nanya	Storage	Row SEFI	100.0	104	9.0e+10
4-Gbit Nanya	Storage	Row SEFI	230.0	120	9.0e+10
4-Gbit Nanya	Storage	Column SEFI	32.88	14	2.2e+10
4-Gbit Nanya	Storage	Column SEFI	59.78	34	9.0e+10
4-Gbit Nanya	Storage	Column SEFI	100.0	54	9.0e+10
4-Gbit Nanya	Storage	Column SEFI	230.0	60	9.0e+10
4-Gbit Nanya	Storage	Device SEFI	32.88	0	2.2e+10
4-Gbit Nanya	Storage	Device SEFI	59.78	0	9.0e+10
4-Gbit Nanya	Storage	Device SEFI	100.0	0	9.0e+10
4-Gbit Nanya	Storage	Device SEFI	230.0	0	9.0e+10