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Unbiased TID Test of 2-Gbit and 4-Gbit DDR3 SDRAM Devices

Test report
Proposal for Revision of the Test Strategy

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1 Abstract

From March 11 to March 18, 2013, a TID test campaign with DDR3 SDRAM was performed at ESTEC, Noordwijk, Netherlands. Preparatory work and analysis was performed by IDA. The irradiation was performed by Michele Muschitiello, ESTEC. This document reports on the findings.

The goal of the test campaign was to supplement the data gathered in our previous in-situ test campaign of 4-Gbit Samsung devices in October, 2012 [3] by testing more unbiased devices from a larger spectrum of manufacturers. Specifically, we examined these devices for the band error pattern described in [3].

2 Test setup

2.1 Test facility

The tests were performed at ESTEC's ^{60}Co source in Noordwijk, Netherlands.

2.2 DUTs

We tested 9 devices from 5 manufacturers, as described in tables 1 and 2. Some of the Hynix devices were soldered to SODIMM [2] modules. Other than that, none of the devices were prepared in any way, such as opening or thinning. For the Samsung 2-Gbit parts, two die revisions were tested: die revision D is produced in 35 nm feature size, while die revision B is produced in the previous generation technology (≈50 nm feature size). For the Nanya 2-Gbit parts, two die revisions were tested: die revision G is produced in 42 nm feature size, while die revision B is produced in 50 nm feature size.

Table 1: tested devices

Manufacturer	and part number	Capacity	Lot codes	Samples	Notes
Samsung	K4B4G0846B-HCH9	4 Gbit	GMK3599Q	3	
Hynix	H5TQ4G83MFR-H9C	4 Gbit	DTLB1237AM	1	
			DTLB1254BM	1	
			DTLB1284AM	2	
			DTLB1088DM	1	
			DTLB1591AM	1	
			DTLB0241BH	8	SODIMM – front
			DTLB0213HA	8	SODIMM – back
Hynix	H5TQ2G83BFR-H9C	2 Gbit	DTKBA778H1	6	
Samsung	K4B2G0846B-HCH9	2 Gbit	GLJ423AC	6	Revision B
Samsung	K4B2G0846D-HCH9	2 Gbit	GEDN60GKU	6	Revision D
			GEB66SFFC	6	
Elpida	J4208BASE-DJ-F	4 Gbit	OWPEYOO	6	
Micron	MT41J256M8HX-15E:D	2 Gbit	BYFCM91.21	6	
			BY8F416.21	6	
Nanya	NT5CB256M8BN-CG	2 Gbit	01340100GP 7 TW	6	

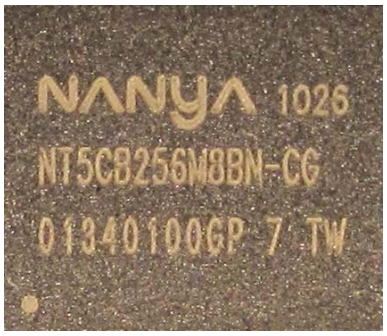
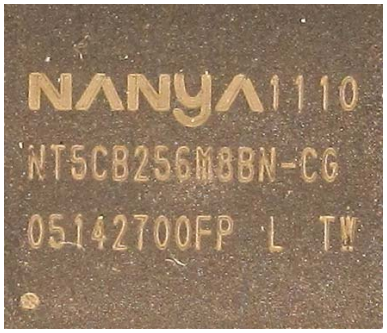
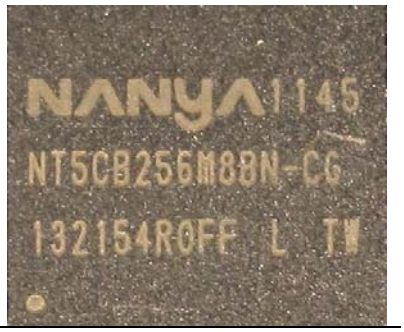
			05142700FP L TW	6	
			132154F0FF L TW	6	Revision B
Nanya	NT5CB256M8GN-CG	2 Gbit	20726200EP 7 TW	6	Revision G

Table 2: part photos

Part	Lot code	Photo
4-Gbit Samsung	GMK3599Q	
4-Gbit Hynix	DTLB1237AM	
4-Gbit Hynix	DTLB1254BM	
4-Gbit Hynix	DTLB1284AM	

4-Gbit Hynix	DTLB1088DM	
4-Gbit Hynix	DTLB1591AM	
4-Gbit Hynix	DTLB0241BH	
4-Gbit Hynix	DTLB0213HA	
2-Gbit Hynix	DTKBA778H1	

2-Gbit Samsung (rev. B)	GLJ423AC	
2-Gbit Samsung (rev. D)	GEDN60GKU	
2-Gbit Samsung (rev. D)	GEB665FFC	
4-Gbit Elpida	0WPEY00	
2-Gbit Micron	BYFCM91.21	 

2-Gbit Micron	BY8F416.21	
2-Gbit Nanya (rev. B)	01340100GP 7 TW	
2-Gbit Nanya (rev. B)	05142700FP L TW	
2-Gbit Nanya (rev. B)	132154R0FF L TW	
		

2-Gbit Nanya (rev. G)	20726200EP 7 TW	

Additionally, an SODIMM that had been irradiated in our 10/2012 test campaign [3] was examined again. This SODIMM contains the same Hynix 4-Gbit devices (lot codes DTLB0241BH and DTLB0213HA) as the SODIMM used in this test campaign.

2.3 Test equipment

The devices were mounted in a plastic frame with the balls of the devices placed on conductive foam (figure 1). They were shielded against electrons with a 3 mm sheet of acrylic glass and a 3 mm aluminum foil.

Figure 1: the DUTs in the plastic frame with an acrylic glass cover (without the aluminium foil)

The test bed used to operate the devices after the irradiation is the same as described in [3]. We have 4 – theoretically identical – copies of the head station. The DDR3 SODIMM extension board contains a 0.1 Ω shunt in the supply voltage line for current measurement. This shunt can be shorted by a jumper.

For some of the test runs, the DUTs were heated using a heat gun or a temperature chamber. In the latter case, the head station was cooled using air flow from a water heat exchanger.

A limitation of the head station is that for an SODIMM, only the first rank (rank 0) can be operated. Since the SODIMM we tested is arranged in two ranks, only 8 of the 16 DUTs on the SODIMM could be tested. 4 of these DUTs are located on the front side and 4 on the back side.

Additionally, we used a PC running the Memtest86+ software [4], version 4.20. This setup can operate an SODIMM at a higher clock frequency (533 Mhz, compared to 333 MHz with our test bed) and performs more thorough tests of all ranks, but does not allow detailed analy-

sis of errors in the device. Furthermore, the PC was too large to be placed in the temperature chamber.

When the device is idle, the memory controller performs a read operation every microsecond (*periodic read*), as required by the Xilinx PHY. This causes the last page that was accessed before to be activated again. The test bed can be configured to precharge the page immediately after the read operation. This is called *precharge after periodic read* and reduces the additional page open time to a minimum. More details about *periodic read* and *precharge after periodic read* can be found in [3].

3 Test procedures and test results

The devices were irradiated with approximately 376 krad (silicon) at a dose rate of approximately 2.3 krad (silicon) per hour. The devices were unbiased during irradiation. The balls of the devices were connected to each other through conductive foam.

After the devices had been shipped back after the end of the irradiation, various tests were performed. We particularly focused on the band error pattern described in detail in [3].

In regular operation, the memory device is read continuously and rows are kept active for a short time only. The band error pattern is believed to be triggered by keeping a DRAM row active for an extended time (within the maximum time allowed by the specification, $t_{RAS} = 9 \cdot t_{REF\,I} \approx 70\ \mu s$ [1]). In order to cause rows to be kept active for an extended time, the test bed can be configured to perform *intermittent operation*. This is similar to read operation, but includes additional pauses which keep the current row active. Subsequently reading the data from the DUT in continuous operation (without rewriting) typically results in a higher number of errors. More details are described in [3].

3.1 At room temperature

First, a subset of the irradiated devices (typically 3 out of 6 available samples for each device type and lot) were tested at room temperature:

- The band error pattern was observed for 4-Gbit Samsung as in the October 2012 in-situ test and also for the 2-Gbit Samsung (revision D) devices. In the "worst" affected rows, about 5% of all cells contained the wrong value.
- There were no errors for 2-Gbit Micron and 2-Gbit Nanya devices, with the exception of one single error each in one Micron device (out of the 6 devices tested) and one Nanya device (out of the 12 devices tested). These errors were 1-to-0 transitions in the second to last page (page address 0x7fffe), suggesting that it constitutes a very weak band error pattern.
- There were no errors at all for 4-Gbit Hynix, 4-Gbit Elpida, 2-Gbit Samsung (revision B), 2-Gbit Micron, and 2-Gbit Nanya devices.

The 4-Gbit Samsung devices had a consistent number of bit errors, as shown in table 3 (note that only devices from one lot were available for testing, so the lot-to-lot variation remains unknown). The 2-Gbit Samsung devices, on the other hand, showed considerable device-to-device and lot-to-lot variation (table 4).

Table 3: total bit errors at room temperature, 4-Gbit Samsung devices

DUT code	Number of bit errors
Sam4.a1	$7.8 \cdot 10^2$
Sam4.a2	$8.0 \cdot 10^2$

Sam4.a3	$3.8 \cdot 10^2$

Table 4: total bit errors at room temperature, 2-Gbit Samsung devices (revision D)

DUT code	Lot code	Number of bit errors
Sam2d.a3	GEDN60GKU	$4.6 \cdot 10^3$
Sam2d.a4	GEDN60GKU	$1.2 \cdot 10^2$
Sam2d.a5	GEDN60GKU	$1.5 \cdot 10^3$
Sam2d.a6	GEDN60GKU	$1.8 \cdot 10^3$
Sam2d.b1	GEB66SFFC	$2.3 \cdot 10^2$
Sam2d.b2	GEB66SFFC	$2.3 \cdot 10^1$
Sam2d.b3	GEB66SFFC	$6.0 \cdot 10^0$
Sam2d.b4	GEB66SFFC	$1.9 \cdot 10^1$
Sam2d.b5	GEB66SFFC	$6.0 \cdot 10^0$
Sam2d.b6	GEB66SFFC	$1.9 \cdot 10^1$

3.2 At elevated temperature

Since errors are more pronounced at higher temperature [3], the devices were operated at elevated temperature.

As a first test, the Hynix SODIMM was heated to approximately 80°C using a heat gun while being operated in the PC (timing parameters, as given by Memtest86+: 6-7-7-18) and exhibited some single bit errors, in contrast to operation at room temperature[1]. For a cross-check, an unirradiated SODIMM with the same devices was operated under the same conditions and showed no errors.

After that, at least 3 samples of each device type were operated at 85°C, the maximum allowed temperature for most of the devices, in our test bed. First, several write and read operations were performed without and, in case of errors, with precharge after periodic read. After that, intermittent operation was performed on the first half of the device and the whole device was read again (an example where intermittent operation has a strong effect is shown in figure 2).

At 85°C, many devices showed the band error pattern, in contrast to room temperature. The band error pattern includes several error regions with different error intensity, as described in detail in [3]. For a *weak* band error pattern, all but the most intense error regions (the second and fourth pages from the end) are not present. A *very weak* band error pattern consists of very few isolated errors in these two pages.

The results of the tests are summarized in table 5. Examples for the error intensities are shown in figures 3 to 5. A blue symbol indicates a 32-bit word with a single-bit error. A purple symbol indicates a word with 2 or 3 bit errors, and a red symbol indicates a word with 4 or more bit errors.

[1] Note that the SPD (*serial presence detect*) EEPROM on the SODIMM still worked, despite the high received dose.

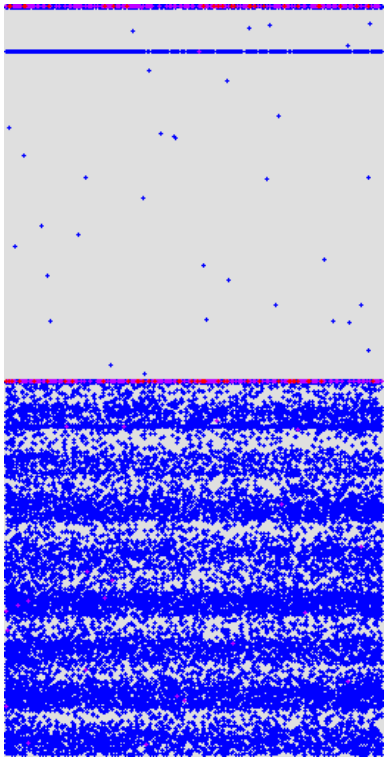


Figure 2: after intermittent operation (2 Gbit Samsung, revision D, 85°C)

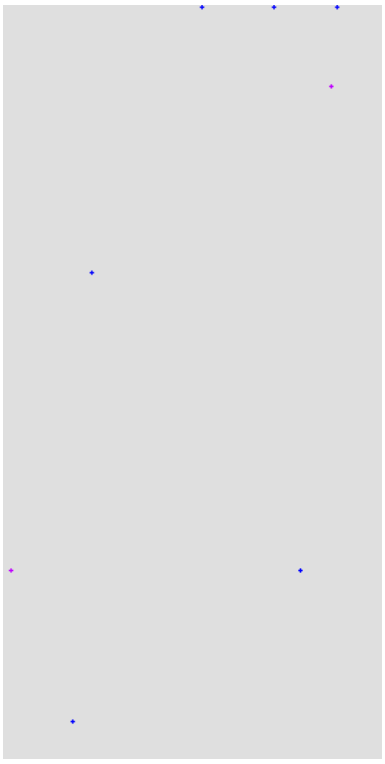


Figure 3: *few* random errors and *very weak* band error pattern (4 Gbit Hynix, 95°C)

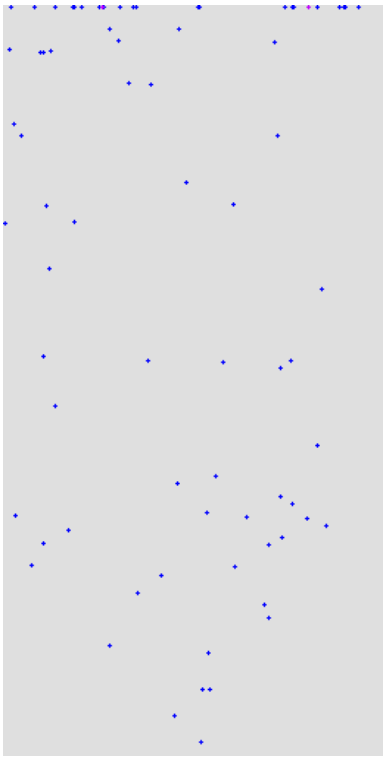


Figure 4: *significant* random errors and *weak* band error pattern (2 Gbit Micron, 85°C)

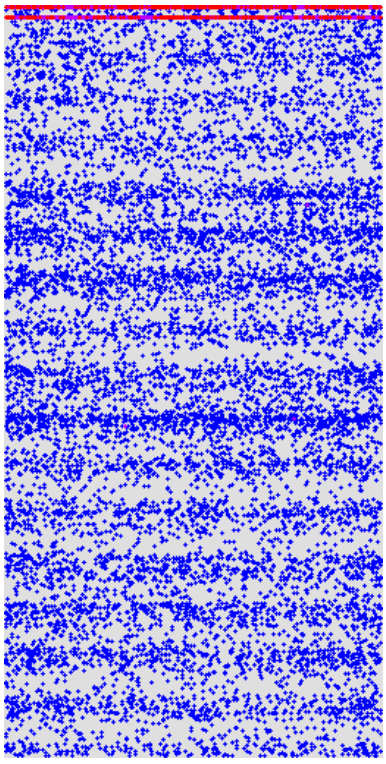


Figure 5: *severe* random errors and *strong* band error pattern (4 Gbit Samsung, 85°C)

Precharge after periodic read typically reduces the band error pattern significantly. If the band error pattern is weak in the first place, it may be reduced to the point of disappearing completely. An effect on the random errors could not be observed.

Table 5: Test results at 85°C (ordered by band error pattern severity)

Device DUTs tested	**Random errors**	**Band error pattern (BEP)**	**Precharge after periodic read**	**Intermittent operation**	**Comments**
4 Gbit Samsung 8 (1 lot)	Severe	Strong	Reduces BEP	More errors	cf. [3]
2 Gbit Samsung (D) 4 (2 lots)	Severe	Strong	Reduces BEP	More errors	
2 Gbit Micron 4 (2 lots)	Significant/ severe	Weak	Removes BEP	No effect	
2 Gbit Hynix 3 (1 lot)	Few	Weak/very weak	Removes BEP	No effect	
2 Gbit Nanya (B) 3 (3 lots)	Significant	Very weak	No effect	No effect	
2 Gbit Nanya (G) 3 (1 lots)	Few	None	No effect	No effect	
4 Gbit Hynix 19 (3 lots)	Few	None	No effect	No effect	
4 Gbit Elpida 3 (1 lot)	Few	None	No effect	No effect	Device still procurable?
2 Gbit Samsung (B) 3 (1 lot)	None	None	No effect	No effect	

Note that all three 2-Gbit Samsung (revision B) devices did not show any errors at all, even after intermittent operation at 85°C, in very contrast to the 4-Gbit and 2-Gbit (revision D) devices from the same manufacturer.

In an additional test, of the tested 2-Gbit Micron devices, one contained more random errors and the other showed a stronger band error pattern. Another 2-Gbit Micron device showed random errors in a pronounced gradient pattern (figure 6).

3.3 Hynix device row errors

With only one of the 4 copies of the head station (head station #2), we observed severe row errors in 2 of the 22 tested 4-Gbit Hynix devices, starting at 65°C (figure 7). These devices also showed clusters of errors in the first column. This error pattern has not been observed for any other devices.

Note that this error pattern only appears with one of the 4 copies of the head station. With the other copies, the 4-Gbit Hynix devices behave as described in table 5. Furthermore, the error pattern only appears when the shunt is shorted. This is surprising, as the operating voltage should be closer to its nominal value in this case.

The operating voltage (V_{DD}) and the reference voltages for the address/command bus ($V_{ref,CA}$) and the data bus ($V_{ref,DQ}$), respectively, were confirmed to be practically identical across the head station copies with an SODIMM containing 4 Micron x16 1-Gbit devices (table 6).

The effect was not further investigated. It may be due to small differences of the line impedance between the boards. All of the tests described above were performed with head station #3, where these errors did not occur.

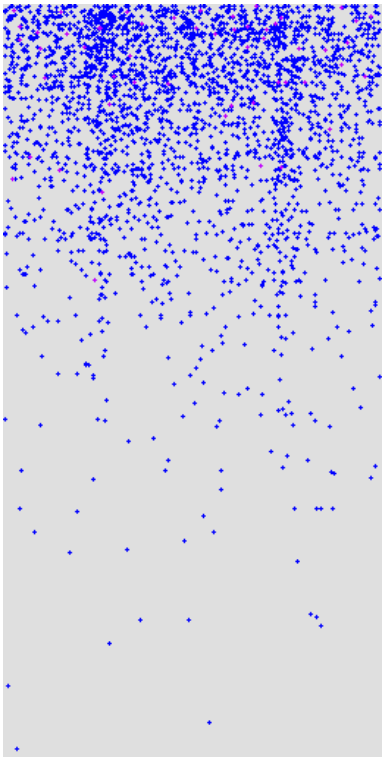


Figure 6: gradient pattern (2 Gbit Micron, 85°C)

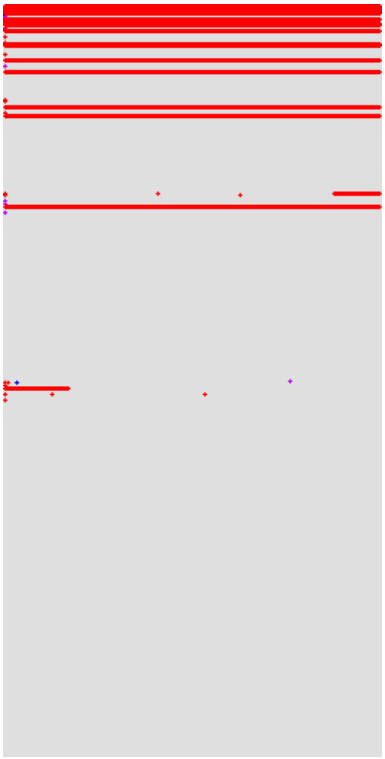


Figure 7: row errors and first column cluster (4 Gbit Hynix, 85°C)

Table 6: DDR3 voltage measurements

Head station number	V_{DD} [V]	$V_{ref,CA}$ [V]	$V_{ref,DQ}$ [V]
1	1.535	0.768	0.767
2	1.539	0.769	0.770
3	1.532	0.765	0.767
4	1.532	0.765	0.767

3.4 Current

To be done – idle/write/read currents of irradiated vs. unirradiated device

4 Discussion

The 4-Gbit Samsung device behaves very similarly to the 2-Gbit Samsung (revision D) device, which is manufactured with the same feature size. In particular, the band error pattern is almost identical. The 2-Gbit Samsung (revision B) device, manufactured with a larger feature size, behaves different from the revision D device: it seems much less susceptible to errors.

The band error pattern is also exhibited by several other devices at high temperature (in contrast to room temperature), although typically much weaker than for the 4-Gbit Samsung device. Some 4-Gbit Samsung samples started showing the band error pattern at a relatively low dose (as low as 200 krad) [3].

It has been shown that the band error pattern can be reduced significantly by operational measures; however, this may not be possible with a stock memory controller but may require a tailored controller design.

Significant lot-to-lot and device-to-device variation have been observed, depending on the device type.

None of the devices tested so far can be unconditionally recommended for a high TID application: 4-Gbit Elpida and 2-Gbit Samsung (revision B) parts are no longer available. 4-Gbit Hynix parts have shown severe row errors in some devices. 2-Gbit Micron, 4-Gbit Samsung and 2-Gbit Samsung (revision D) parts have severe random errors and/or strong band error pattern. Of the only remaining part, 2-Gbit Hynix, only one lot was available for testing.

5 Future work

The band error pattern constitutes a very severe performance degradation. It is difficult, if not impossible, to cope with this error pattern using even sophisticated error correction measures and/or a tailored controller design.

In our assessment, this is an absolute verdict against the 4-Gbit Samsung device, which, after 400 krad, already shows the band error pattern at room temperature.

Another point is that it makes no sense to test 2-Gbit devices which are already obsolete.

This means that **the test strategy should be revised**. A more extensive survey by unbiased irradiation of other 4-Gbit devices (Micron, Nanya, Elpida?, others?) should be done first.

The more effort-consuming in-situ TID test (and also the proton test) should be focused on the best suited device determined by that survey.

For devices with no band error pattern (BEP) at room temperature and the band error pattern at 85°C, the BEP onset temperature should be determined. Parts with a BEP onset temperature of >50°C, >60°C, >70°C after 400 krad could potentially be of interest.

The first step of the revised test strategy would be to procure a reasonable number (100 per type each of Micron, Nanya, Elpida?, others?) for unbiased irradiation to 400 krad.

A decision about the further test strategy is urgently needed.

6 References

[1] JEDEC standard 79-3E: *DDR3 SDRAM Specification*

[2] JEDEC standard 21C: *204-Pin DDR3 SDRAM Unbuffered SO-DIMM Design Specification*

[3] M. Herrmann, K. Grürmann, and F. Gliem: *TID Test of 4 Gbit DDR3 SDRAM Devices*, TN-IDA-RAD-13/4

[4] http://www.memtest.org/