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In-situ and unbiased TID Test of 4-Gbit DDR3 SDRAM Devices Test report

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candidate memory devices for Laplace mission

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1 Abstract

From January 17 to January 23, 2014, we performed a TID test campaign with DDR3 SDRAM at ESTEC, Noordwijk, Netherlands. This document reports on the findings.

2 Preliminary notes

Unless specified otherwise, all dose and dose rate values in this document refer to absorbed dose in silicon (D_{Si}). Absorbed dose in silicon is calculated from absorbed does in water (as reported by ESTEC dosimetry) by $D_{Si} = D_{H2O} / 1.12$.

Unless specified otherwise, the terms “unbiased DUT” and “operated DUT” refer to DUTs that were unbiased or operated, respectively, during irradiation. The terms “unbiased TID test” and “in-situ TID test” refer to TID tests when the DUTs are unbiased or operated, respectively, during irradiation.

3 Test procedure

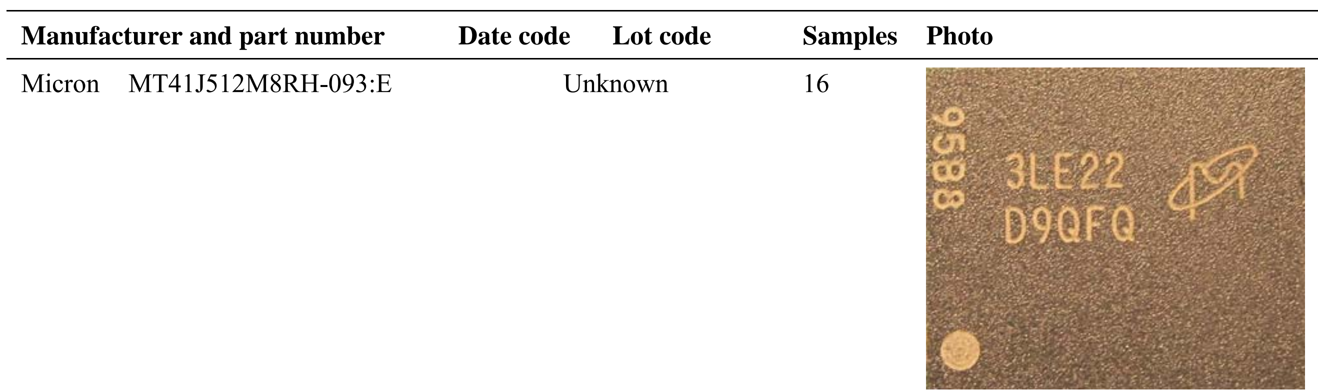
3.1 Test facility

The tests were performed at ESTEC’s ^{60}Co source in Noordwijk, Netherlands.

3.2 DUTs

We tested four 4-Gbit parts from Micron, Hynix and Nanya, described in table 1. Some of the devices were soldered to SODIMM modules, as shown in table 2. Other than that, none of the devices were prepared in any way, such as opening or thinning.

Table 1: tested parts (all 4 Gbit). For Hynix, there were two lots. Half of the tested DUTs were from each lot.

Manufacturer and part number		Date code	Lot code	Samples	Photo
Micron	MT41J512M8RH-093:E	Unknown		16	

Hynix	H5TQ4G83MFR-H9C	144A	DTLB0241BH	8	
Hynix	H5TQ4G83MFR-H9C	144A	DTLB0213HA	8	

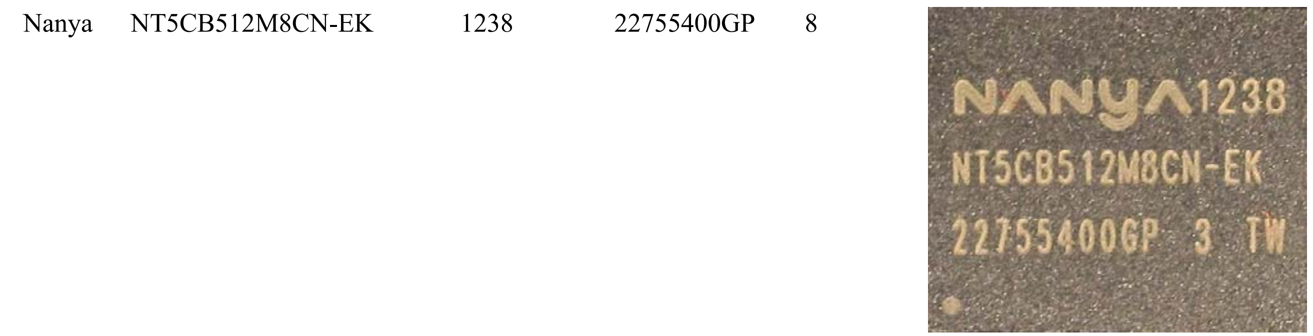
Nanya	NT5CB512M8CN-EK	1238	22755400GP	8	

Table 2: tested samples (all 4 Gbit)

Name	**Type**	**Manufacturer**	**DUTs**	**Dose**	**Irradiation**
Mic4SO4	SODIMM	Micron	8	407	In-situ
Mic4SO3	SODIMM	Micron	8	407	Unbiased
Hyn4SO4	SODIMM	Hynix	8	423	In-situ
Hyn4SO3	SODIMM	Hynix	8	407	Unbiased
Nan4.a[11-18]	Single	Nanya	8	407	Unbiased

3.3 Test bed

The test bed, RTMC6 (figure 1), is capable of operating the first rank of one SODIMM with 8 DUTs in ×8 configuration, at a clock frequency of up to 333 MHz. It is based on a Xilinx ML605 evaluation board, which contains a Xilinx Virtex6 FPGA.

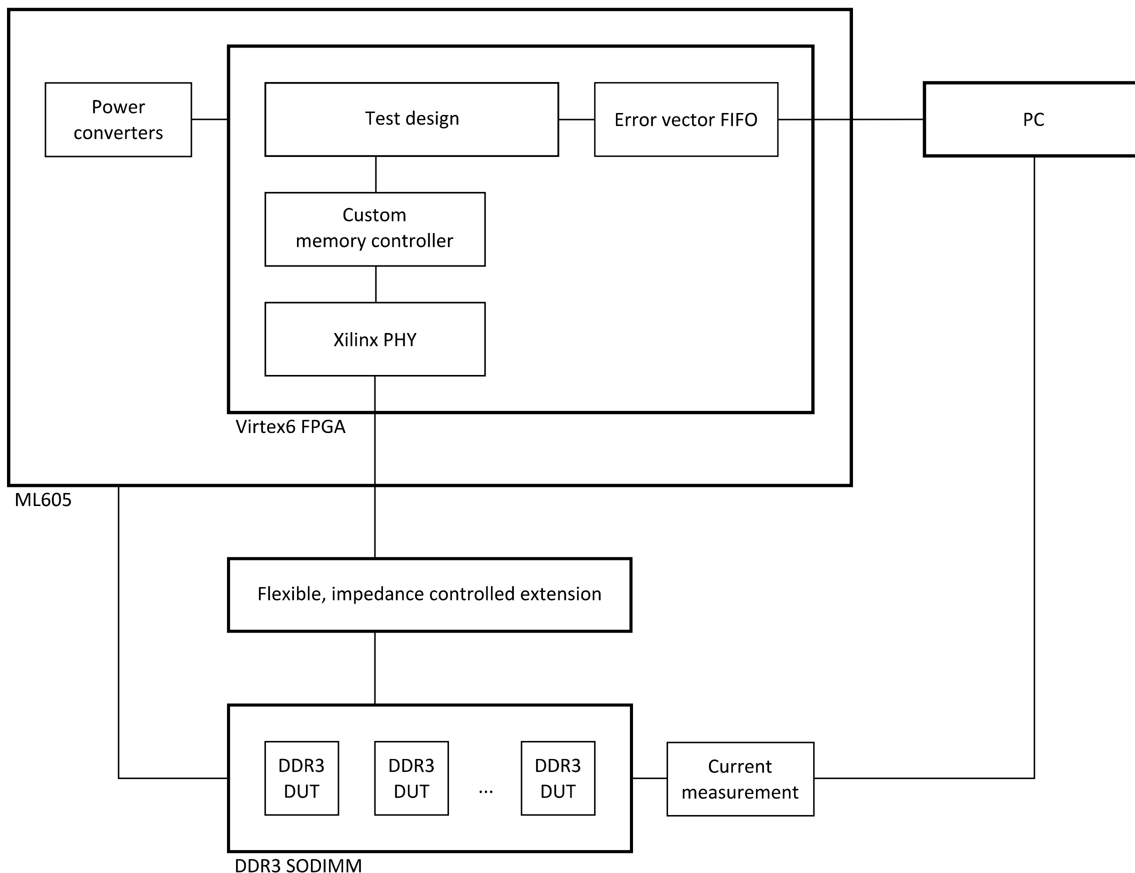


Figure 1: an overview of the RTMC6 test bench (simplified)

The FPGA contains a custom test design which writes a constant, counting or pseudo-random pattern to one of the DUTs, reads the data from the DUTs and compares it to the original pattern. If the data is different from the pattern, an error vector is generated and transmitted to a PC via a high speed USB connection. Since the DUTs have a higher data transfer rate than the USB connection, error vectors are buffered in an on-FIFO in order to be able to handle large runs of consecutive errors without slowing down the test. If the error record FIFO runs full due to too many errors, error vectors are either discarded or the test is slowed down, at the user's choice. In the latter case, when the FIFO runs full, the test is stalled until enough error vectors have been transmitted to make sufficient space in the buffer, and then resumed.

On the PC, an error map is displayed for each DUT for preliminary visual analysis, along with a total error count and various statistics. The error vectors are stored for offline analysis.

Due to the common command bus for all devices on an SODIMM, all commands are issued to all DUTs simultaneously and the DUTs generally operate in unison. Writing to one DUT selectively is achieved by using the *data mask* (DM) signal individual to each DUT. The associated activate and precharge commands are still performed by all DUTs simultaneously. Reading from one DUT selectively is not possible, apart from discarding the data from the other DUTs.

The total supply current for the whole SODIMM is measured at a sampling rate of 16 Hz and is logged by the PC. The supply current for individual DUTs cannot easily be measured as this would require a modification of the SODIMM.

3.3.1 Memory controller

An SDRAM controller consists of two parts (see figure 2): the memory controller proper (MC), which interfaces with the user logic, and the physical interface (PHY), which interfaces with the SDRAM device. The MC is responsible for tracking the state of the DDR3 device and high-level timing. The PHY is responsible, among others, for low level (sub-clock-period) timing, data capturing and DDR translation. MC and PHY are connected via the DDR PHY interface (DFI).

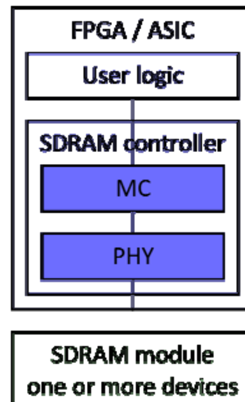


Figure 2: a typical design involving an SDRAM controller

Our test device uses a custom memory controller that has been developed specifically for memory tests. It provides fine-grained control over the DUT and allows performing operations such as writing the mode registers, resetting the DLL of the DUT or calibrating the termination resistance at arbitrary times. Our controller implements an open page policy, which means that a row of the DRAM is kept open as long as possible after an access. In addition to simplifying the design, this policy has been shown to significantly increase DRAM performance [2]. It is particularly efficient for highly localized access patterns, as is the case with our memory test.

Our memory controller interfaces with the PHY developed by Xilinx and included in their Memory Interface Generator (MIG) package [1]. A peculiarity of the Xilinx DDR3 PHY is that it requires a read access (to no particular location) at least every microsecond in order to maintain internal timing parameters. If the user logic does not perform enough read operations, a read operation called “periodic read”, or PRD, is initiated by the MC. The controller uses the address that currently happens to be applied to its inputs, which is typically the last address accessed by the user logic.

3.3.2 Cooling

The FPGA and the power regulators dissipate several watts of heat. We devised a water cooler consisting of copper block placed above the board (see figure 3). The block is equipped with several threaded bolts to match the different heights of the various components to be cooled. Water cooling is used to also be prepared for heavy-ion tests in vacuum.

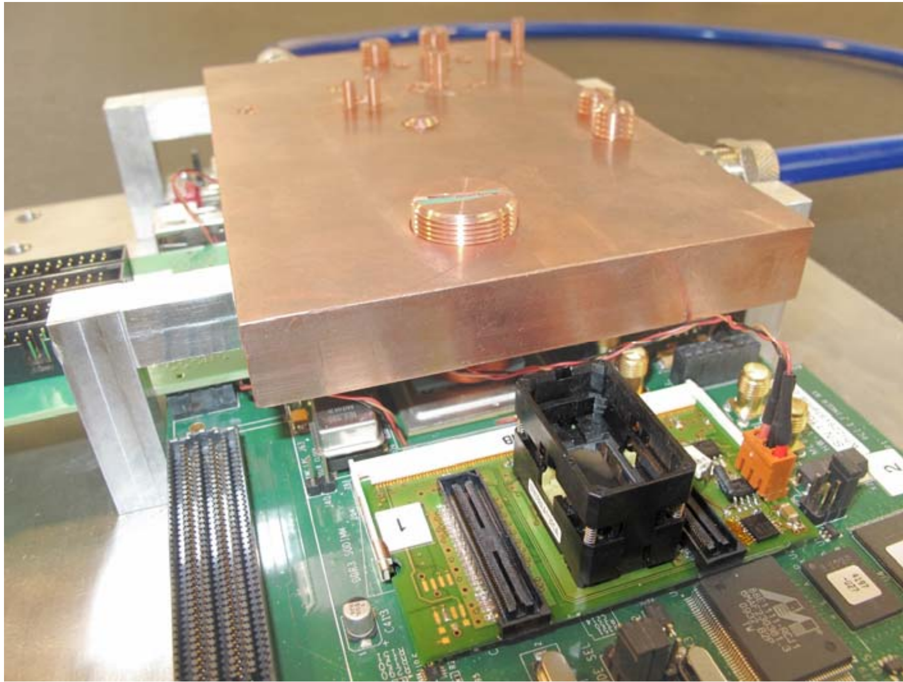


Figure 3: the water cooler is the same as in this SEE test setup

3.3.3 Shielding

In order to perform irradiation tests with a high total dose, all sensitive parts except the DUTs must be shielded from the radiation. For this purpose, we had developed a shielding box made of lead (where space is critical) and steel [3].

For this test, the shielding box (figures 4and 5) was revised. It is now possible to place the DUTs closer to the source, yielding a higher dose rate. Furthermore, the top side of the box used previously had sharp edges. The top side is now flat and covered with a 6-mm sheet of acrylic glass. The DUTs are shielded against electrons by a box made of acrylic glass with 6-mm walls (figure 6).

The revised shielding box is shown in figures 4 and 5. It weighs about 1000 kg and is assembled on-site from individual parts of about 10 kg to 20 kg each. It has several curved channels for feeding electrical wires and water tubes for the cooling system into the box.

Figure 4: the shielding box with water tubes (blue) and electrical wires

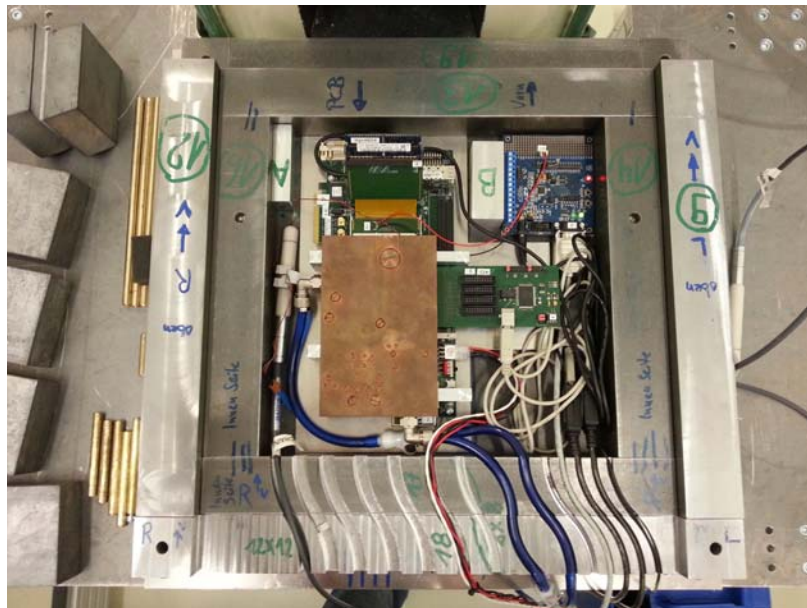


Figure 5: the test equipment head station inside the shielding box

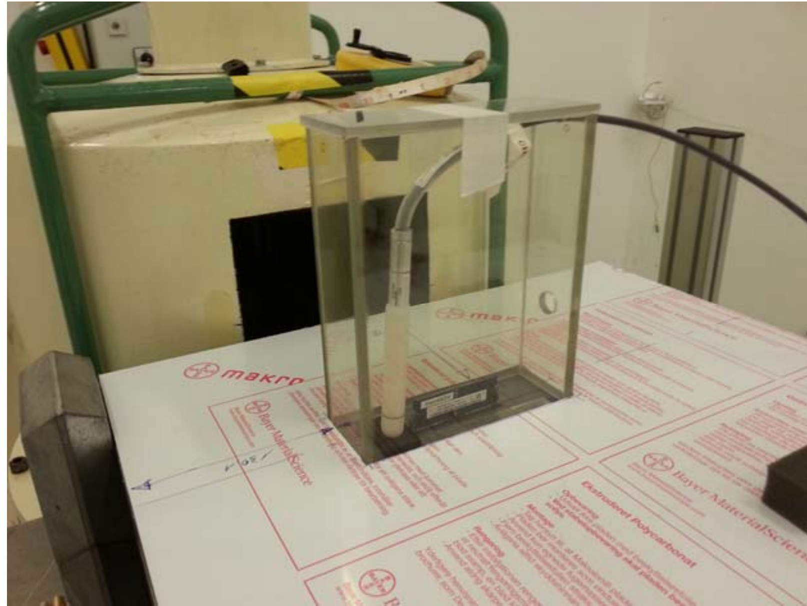


Figure 6: acrylic glass box

We used the same flexible, impedance controlled extension for the DUTs as in the previous test [3].

Figure 7: the flexible extension with an SODIMM in the ML605 (with a fan on the FPGA instead of the water cooler)

A dosimeter placed inside the shielding box indicated a dose that was lower than the dose outside the box by a factor of about 70. This is in contrast to the factor of $5 \cdot 10^3$ that had been determined in the previous test [3], which was implausibly large and probably caused by a poor position of the dosimeter inside the box. Nevertheless, none of the devices inside the box failed during the entire irradiation with a total dose (outside the box) of more than 400 krad, despite already having been used in the last test with more than 420 krad.

3.4 Test operation

At the beginning of the test, a pseudo-random pattern was written to all DUTs. After that, the DUTs were tested in a round-robin fashion. Each DUT was first read. After a pause of 15

minutes, the DUT was written with the original pattern and the sequence repeated with the next DUT. This results in a total period of 120 minutes (2 hours) for each DUT, with 105 minutes between a write operation and the following read operation.

DDR3 devices experience significant self-heating during operation. Since all DUTs are operated in unison (as described in section 3.3), accessing any device has an influence on the temperature of other devices. The staggered operation of the DUTs serves to minimize the influence of this effect: were all DUTs to be read one after another, the last DUT would be read immediately following 7 other read operations, and therefore at a higher temperature than the first.

3.5 Irradiation

The irradiation was performed at a dose rate of ≈ 100 rad per minute, or 6 krad per hour. At this rate, a dose of 400 krad is reached in 67 hours, or more than two and a half days.

4 Test results

4.1 Current

During each loop, the idle current was measured and logged automatically for the operated DUTs. This measurement was performed as the first action after the 15 minute wait time, in order to avoid the warming caused by the write operation to affect the idle current.

As described in section 3.3, the individual current for each DUT could not be measured. The measured current is the total current for the whole SODIMM. Dividing the current by the number of DUTs on the SODIMM yields the average current per DUT.

The current vs. dose for the Micron and Hynix DUTs is shown in figures 8 and 9. For the Micron DUTs, over the course of 407 krad, the average idle current increased by a factor of more than 12, from 9 mA per DUT to 116 mA per DUT. For the Hynix DUTs, the current did not increase at all over the whole 423 krad.

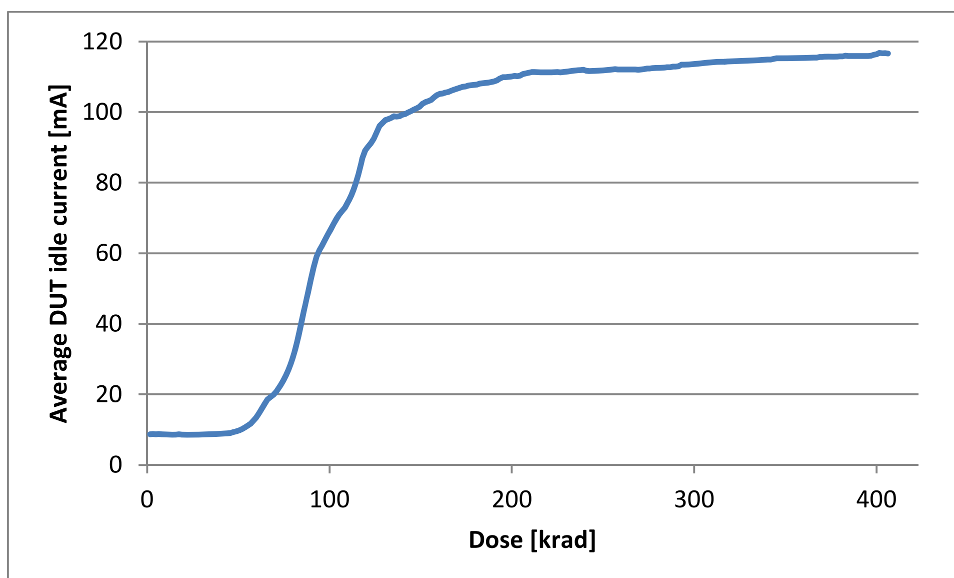


Figure 8: idle current vs. dose, 4-Gbit Micron, operated

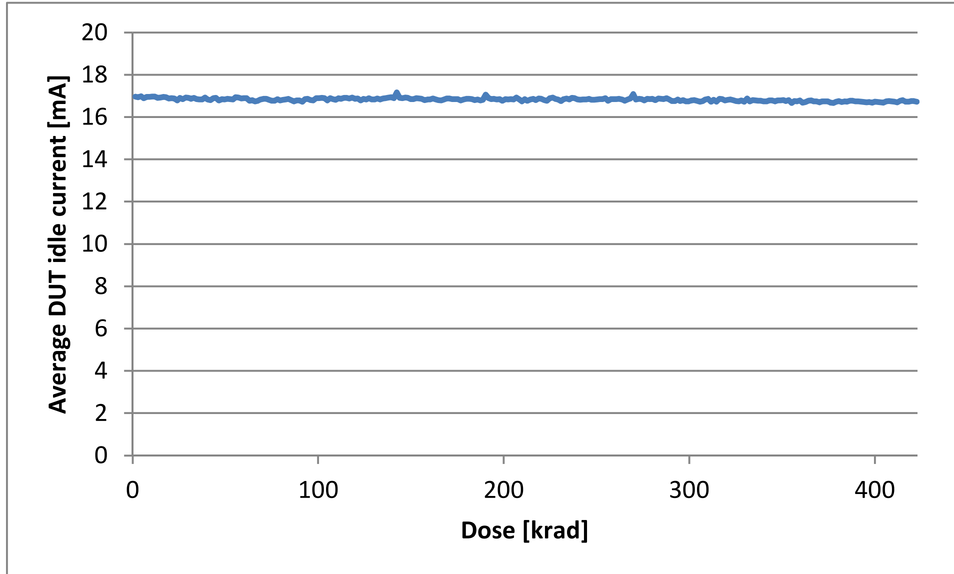


Figure 9: idle current vs. dose, 4-Gbit Hynix, operated

After the test, the supply voltage in idle state was measured at approximately 1.35 V, which is lower than the specified minimum of 1.425 V. The reference voltage $V_{REF,DQ}$ was verified to be within the specified limits. On startup, the controller attempts to initialize the DUT. This includes writing to and reading from the device in order to calibrate the line delays. The initialization procedure does not complete, indicating that writing and reading is not possible.

The current during a write and read operation for the unbiased Hynix DUTs is shown in figure 10. During read operation, the current has a slight periodicity with 8 periods, which may or may not coincide with the 8 banks of the DUT. This periodicity is not present in an unirradiated device of the same type (figure 11).

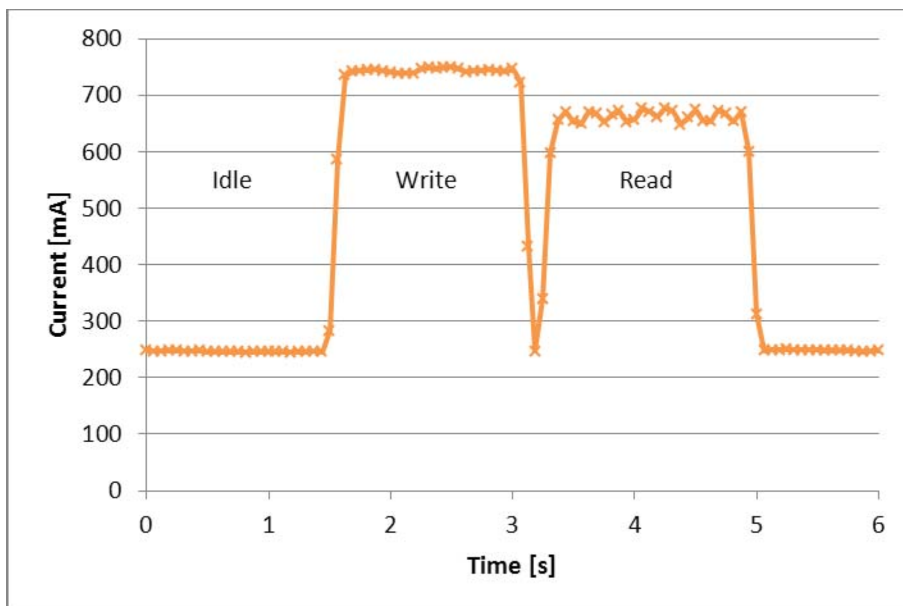


Figure 10: current during write and read operation. 4-Gbit Hynix, unbiased

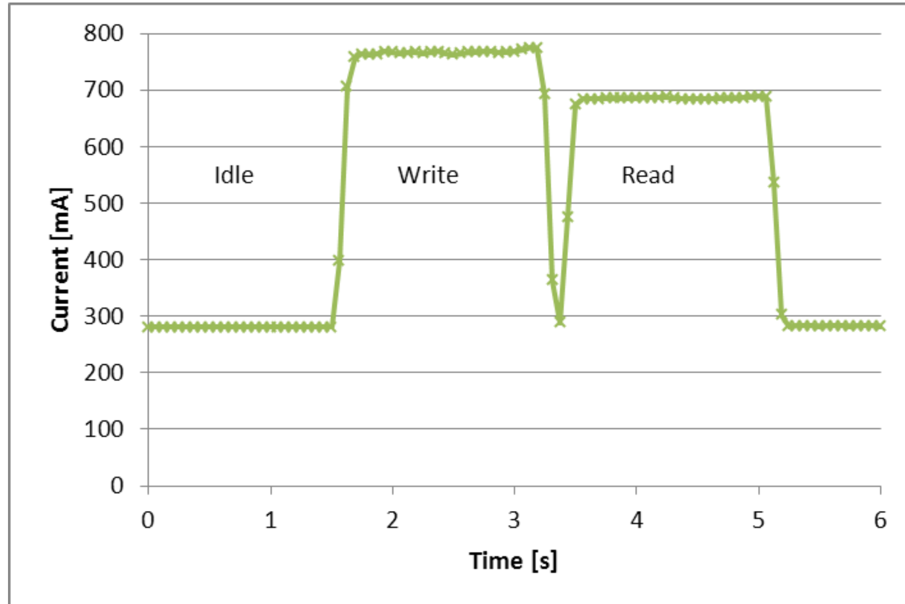


Figure 11: current during write and read operation. 4-Gbit Hynix, unirradiated

4.2 Error count

None of the eight unbiased Micron DUTs showed any errors.

Of the eight unbiased Hynix DUTs:

- Four showed no errors at room temperature.
- One showed very few randomly distributed errors, which disappeared after a few days.
- Two showed a substantial number of errors, including some row errors. The error maps are shown in figure 12. Zooming in on the errors in the second and third case reveals that the former consists of two adjacent error pages, while the latter consists of a contiguous error region (see figure 13).
- One showed a substantial number of errors, including some row errors and many short row segment errors. The error map is shown in figure 14. The pattern is different for each readout, indicating that the errors do not originate from the array.

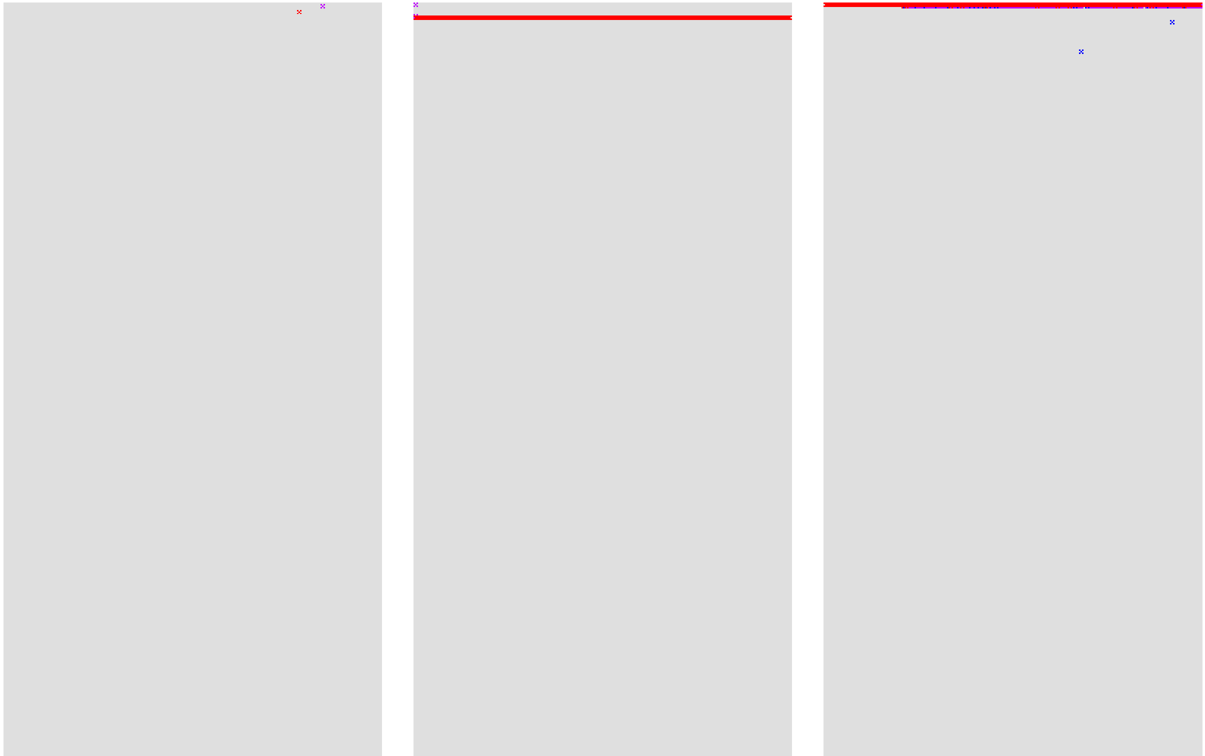


Figure 12: Error maps of three DUTs; 4-Gbit Hynix, unbiased

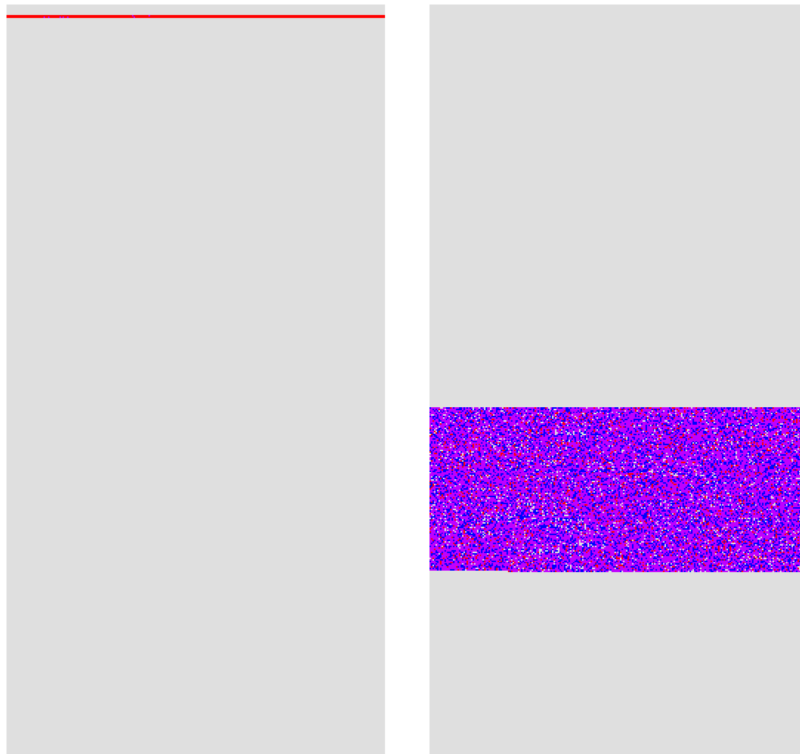


Figure 13: zoomed view of the second and third error map from figure 12

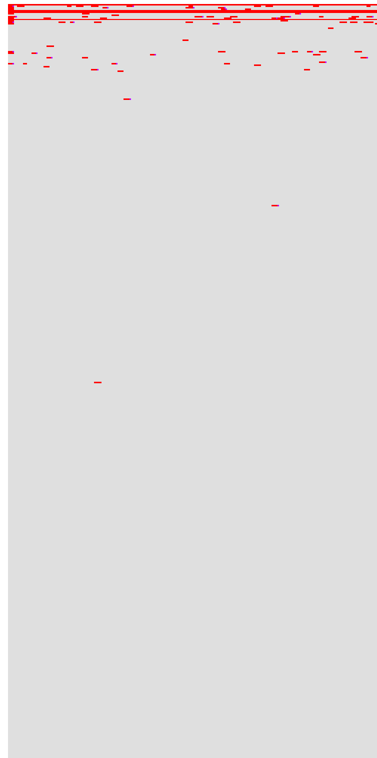


Figure 14: error map, 4-Gbit Hynix, unbiased

The error density vs. dose for the operated Micron DUTs is shown in figure 15 (one of the DUTs suffered from a bad contact and is not shown). The first errors appeared around 90 krad. The number of errors quickly increased to the maximum that our test equipment is capable of recording (within 25 krad). This increase is coincident with the current increase. It is suspected that the number of errors is caused by the supply voltage dropping to a value outside of the specification due to the high current.

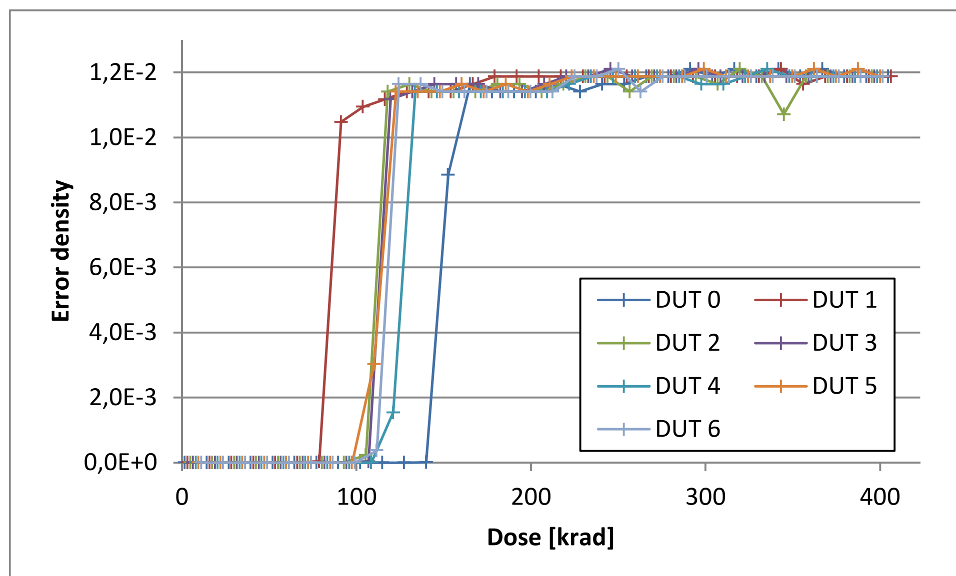


Figure 15: Error density vs. dose; 4-Gbit Micron

None of the eight operated Hynix DUTs showed any errors at all, up to the final dose of 423 krad.

All error counts were determined at room temperature.

4.3 Annealing

The irradiated DUTs were first annealed at room temperature for about one week, and then at 100°C for another week. The measurements were performed at room temperature which was neither controlled nor measured.

4.3.1 Current

The current measurements during annealing are shown in figures 16 to 21. The semi-transparent horizontal lines indicate the baseline values, i. e. the values of an unirradiated part of the same type. The vertical grey lines indicate the start of the high-temperature annealing.

The write and read current are estimated from the graphical display of our test control software, since our test equipment currently does not support synchronization of the current measurement with DUT operation.

Note that there have been instances where the idle current between initialization and the first set of write and read operations was lower than the later idle current after the device had actually been written to. We therefore wrote and read the whole device before measuring the idle current. Since the operated Micron device cannot be initialized, this is not possible for this device. The reported value is therefore the current after the failed initialization.

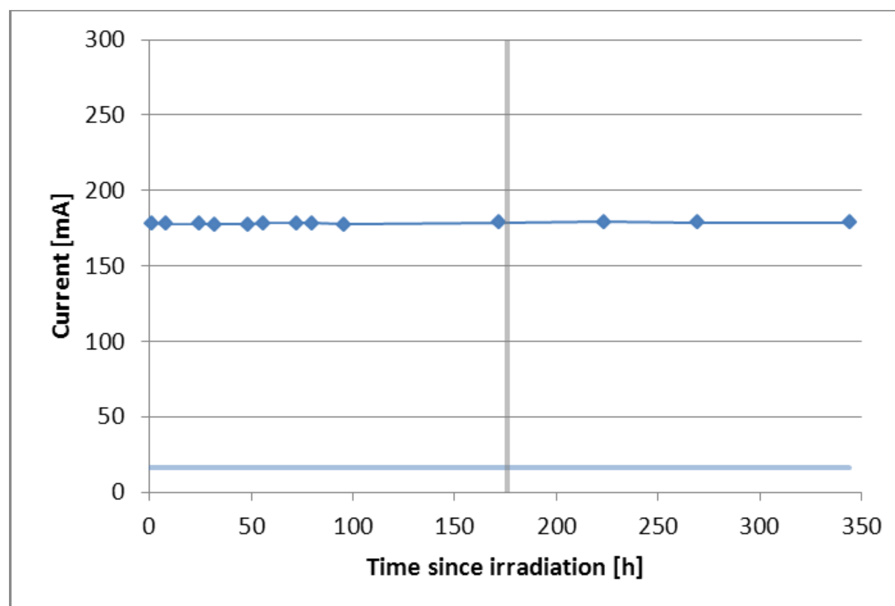


Figure 16: current annealing, 4-Gbit Micron, operated. The horizontal, semi-transparent line indicates the baseline current value. The vertical, grey line indicates the beginning of high-temperature annealing.

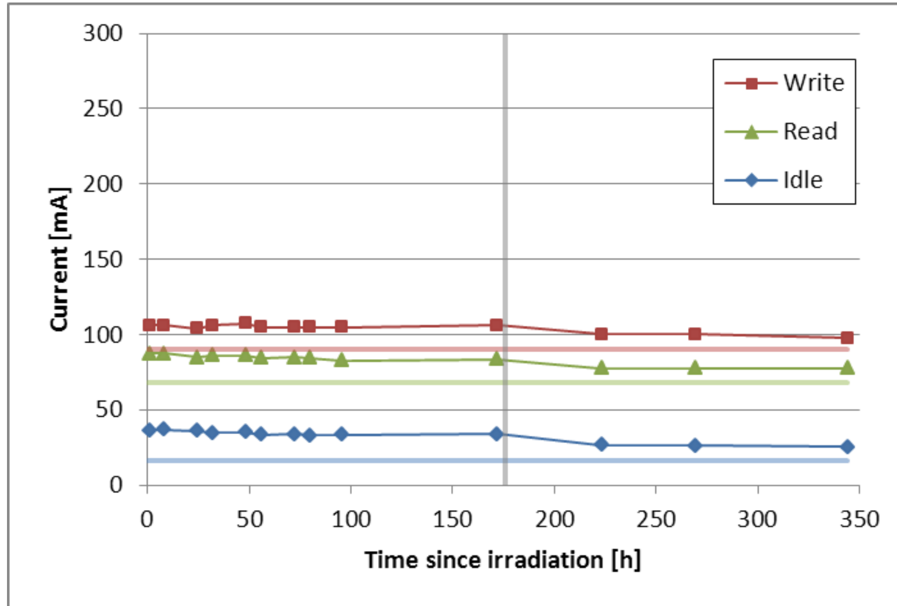


Figure 17: current annealing, 4-Gbit Micron, unbiased. The horizontal, semi-transparent lines indicate the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

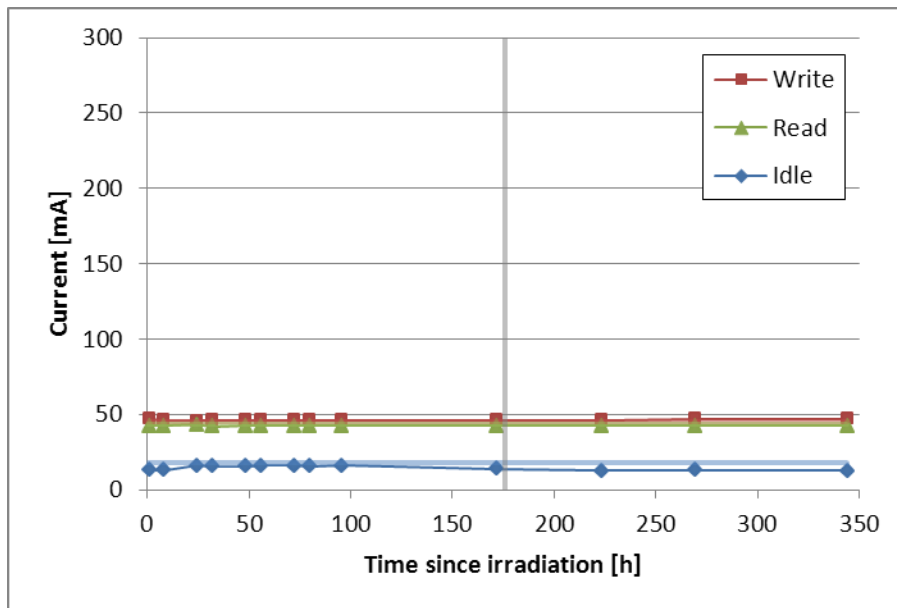


Figure 18: current annealing, 4-Gbit Hynix, unbiased. The horizontal, semi-transparent lines indicate the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

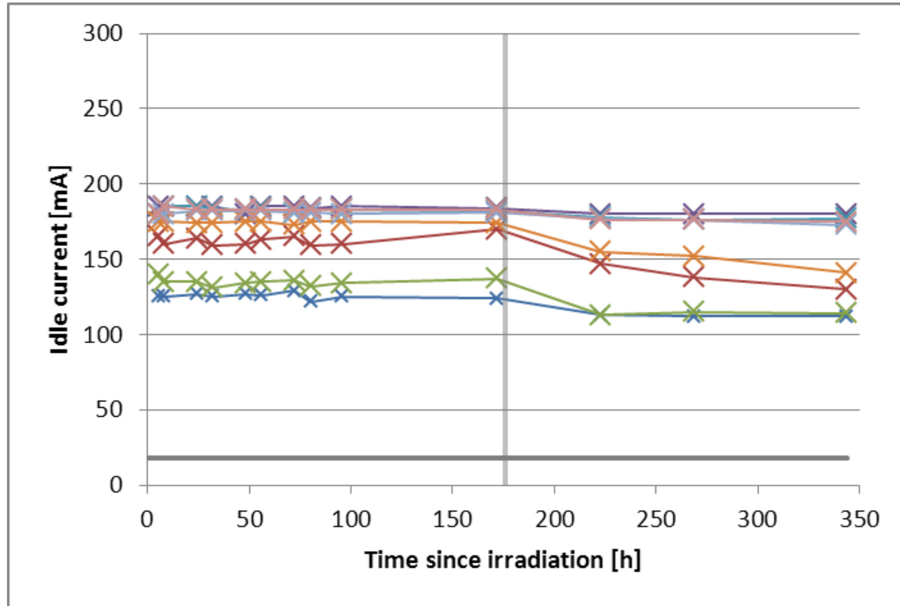


Figure 19: idle current annealing, 4-Gbit Nanya, unbiased. The horizontal, grey line indicate the base-line current values. The vertical, grey line indicates the beginning of high-temperature annealing.

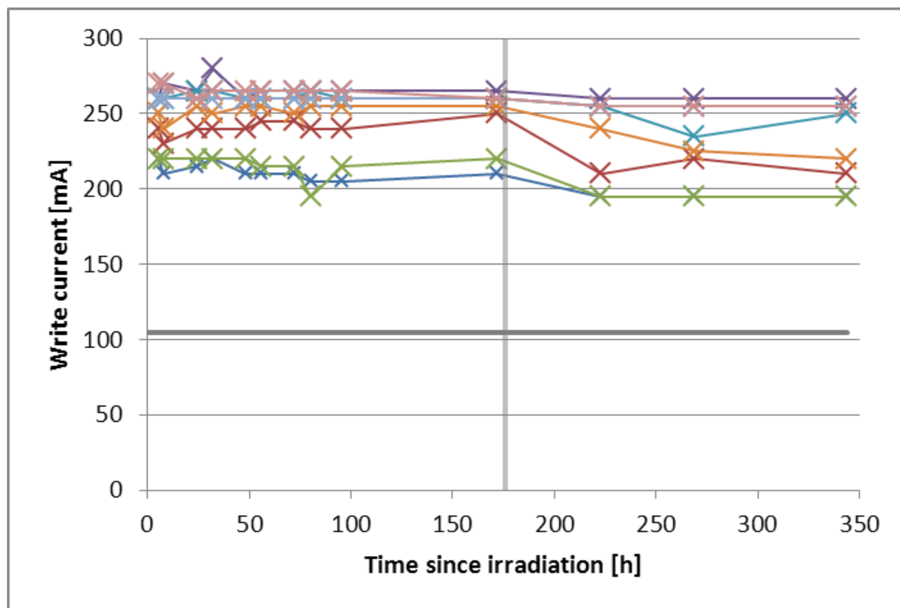


Figure 20: write current annealing, 4-Gbit Nanya, unbiased. The horizontal, grey line indicate the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

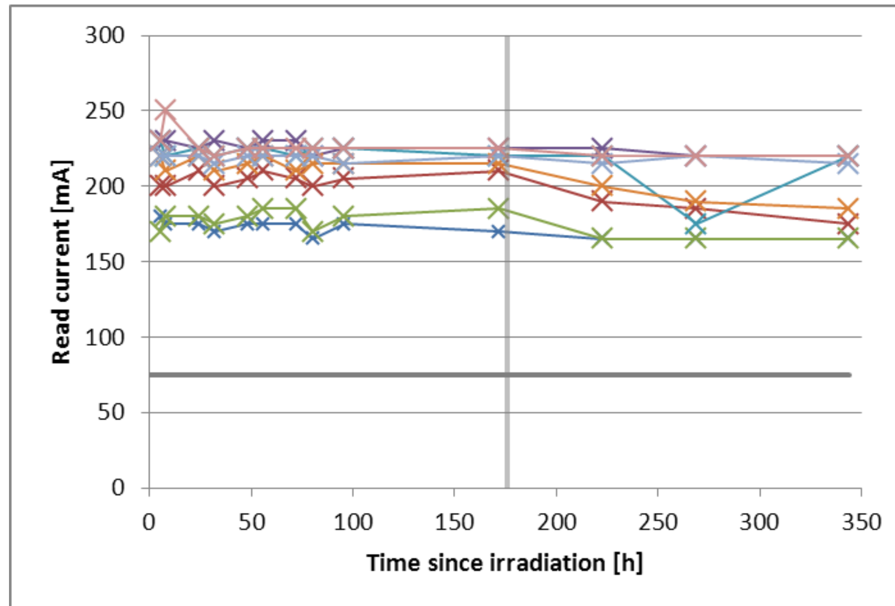


Figure 21: read current annealing, 4-Gbit Nanya, unbiased. The horizontal, grey line indicate the baseline current values. The vertical, grey line indicates the beginning of high-temperature annealing.

4.3.2 Errors

Since the Hynix DUTs contained no errors, no error annealing could be observed. The same is true for the unbiased Micron DUTs. The operated Micron DUTs and the unbiased Nanya DUTs both contained too many errors to make useful error annealing measurements.

4.4 Comparison with previous tests

Different DUTs of all of the parts had been tested by unbiased irradiation before.

The low number of errors in some of the unbiased Hynix DUTs is consistent with previous tests [3, 4]. Other Hynix DUTs showed an error pattern that had not been observed before.

Both the unbiased Micron DUTs not having any errors at all and the very high number of errors in the Nanya DUTs is consistent with a previous test [5].

4.5 Discussion

The Hynix device behaves similarly whether unbiased or operating, with respect to both current and errors. This is similar to the Samsung devices, where the difference between unbiased and operating DUTs was also small.

The Micron device, on the other hand, is totally different. While the unbiased DUTs had no errors at all (which is the best result of all parts tested so far), the operated DUTs showed the highest current increase of all parts so far, and also the highest number of errors. Although the number of errors may be caused by insufficient power supply for the high current, the high current alone may make such a device unsuitable for a space application.

5 References

[1] Xilinx, UG406 – Virtex-6 FPGA Memory Interface Solutions User Guide

[2] J. A. a. J. Niittylahti, *A Comparison of Precharge Policies with Modern DRAM*, in *9th International Conference on Electronics, Circuits and Systems*, 2002

[3] M. Herrmann, K. Grürmann, and F. Gliem: TN-IDA-RAD-13/4, TID Test of 4 Gbit DDR3 SDRAM Devices

[4] M. Herrmann, K. Grürmann, and F. Gliem: TN-IDA-RAD-13/9B, Unbiased TID Test of 2-Gbit and 4-Gbit DDR3 SDRAM Devices

[5] M. Herrmann, K. Grürmann, and F. Gliem: TN-IDA-RAD-13/12, Unbiased pre-selection TID Test of 4-Gbit DDR3 SDRAM Devices