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Unbiased preselection TID Test of 4-Gbit DDR3 SDRAM Devices

Test report
Approach for in-situ test

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1 Abstract

From October 18 to October 22, 2013, a TID test with DDR3 SDRAM was performed at ESTEC, Noordwijk, Netherlands. Preparatory work and analysis was performed by IDA. The irradiation was performed by Michele Muschitiello, ESTEC. This document reports on the findings.

The goal of the test campaign was to supplement the data gathered in our previous tests of 2-Gbit and 4-Gbit devices (October, 2012, in-situ [3] and March, 2013, unbiased [4]) by testing more devices from a larger spectrum of manufacturers. Specifically, we examined these devices for the band error pattern described in [3].

2 Test setup

2.1 Test facility

The tests were performed at ESTEC's ^{60}Co source in Noordwijk, Netherlands.

2.2 DUTs

4-Gbit devices from three manufacturers were irradiated, as described in table 1. None of the devices were prepared in any way, such as opening or thinning.

Devices from different lots of the Samsung part have been irradiated in 10/2012 (biased and unbiased) and 3/2013 (unbiased). For the Micron and Nanya parts, the corresponding 2-Gbit parts have been irradiated in 3/2013 (unbiased). The previously irradiated parts are described in table 2.

Table 1: tested parts (all 4 Gbit)

Manufacturer and part number		Lot code	Date code	Samples	Photo
Samsung	K4B4G0846B-HCH9	GMC7679W	1216	10	
Micron	MT41J512M8RH-093:E	DRRKDNB.11	1324	10	

Nanya	NT5CB512M8CN-EK	22755400GP	1238	10	

Table 2: previously tested parts

Manufacturer and part number		Capacity	Lot code	Date code	Samples
Samsung	K4B4G0846B-HCH9	4 Gbit	GMK3599Q	1204	3
Micron	MT41J256M8HX-15E:D	2 Gbit	BYFCM91.21	1006	6
			BY8F416.21	1116	6
Nanya	NT5CB256M8BN-CG	2 Gbit	01340100GP 7 TW	1026	6
			05142700FP L TW	1110	6
			132154F0FF L TW	1145	6
Nanya	NT5CB256M8GN-CG	2 Gbit	20726200EP 7 TW	1218	6

2.3 Test equipment

The devices were mounted in a plastic frame with the balls of the devices placed on conductive foam (figure 1). They were shielded against electrons with a 3 mm sheet of acrylic glass and a 3 mm aluminum sheet.

Figure 1: the DUTs in the plastic frame (without the acrylic glass and aluminium sheets)

The test bed used to operate the devices after the irradiation is the same as described in [3].

For some of the test runs, the DUTs were heated using a heat gun.

3 Test procedures and test results

The devices were irradiated with approximately 393 krad (silicon) at a dose rate of approximately 2.4 krad (silicon) per hour. The devices were unbiased during irradiation. The balls of the devices were connected to each other through conductive foam.

After the devices had been shipped back after the end of the irradiation, they were tested for errors. The first tests were performed approximately 3 days after the end of the irradiation.

3.1 At room temperature

First, all devices were tested at room temperature:

- The Samsung devices showed the band error pattern, very similarly to the previously tested devices of the same part number. In particular, all errors were in the 1 → 0 direction again. The error density in the rows affected by the band error pattern was about 1%.
- The Micron devices showed no errors at all.

- The Nanya devices showed a very high number of errors (up to an error density of 50%) in both directions. No pattern has been identified so far.

3.2 At elevated temperature

Since errors are more pronounced at higher temperature [3], the Micron devices were tested at 80°C. The Samsung devices were not tested at elevated temperature because they appear to behave similarly to the previously tested DUTs of the same type, which have been thoroughly examined. The Nanya devices were not tested at elevated temperature because they already contain a high number of errors at room temperature.

All 10 Micron devices were tested at 80°C. They only contained between zero and nine single-bit errors each, in both directions, randomly distributed throughout the devices address space.

4 Discussion

The Samsung part is similar to previously tested devices of the same part number.

The Micron part has no errors at room temperature, and very few (<10) errors at 80°C. This is in contrast to the previously tested 2-Gbit Micron parts, which had a significant number of errors (up to 10^5 errors).

The Nanya part has an extremely high error density (up to 0.5) even at room temperature, in contrast to previously tested 2-Gbit Nanya parts, which had no errors at room temperature and an error density of less than 10^{-6} even at 95°C.

5 Selection for in-situ test

The tested samples of the Micron part have very few errors after 393 krad, which makes the part interesting for space applications. It should be examined in the planned in-situ test.

6 Preliminary Test Schedule

General goal is to perform an in-situ test of the selected Micron 4-Gbit DDR3 device up to at least 400 krad (Si) and an in-situ test of the Micron 16/32-Gbit NAND-Flash device up to 200 krad.
In comparison to the previous DDR3 in-situ test the rack of the shielding box has been modified in order to situate the DUTs closer to the Co60 source. This should result in an increased dose rate of roughly 85 rad / min = 5.1 krad / h.
To attain 400 krad the DUTs have to be irradiated over 400 krad / 5.1 krad / h = 79 h. Taking into account 6h installation and de-installation time the target dose of 400 / 500 krad can be reached at best in 3.6 / 4.1 days
Accordingly the duration of the 20 krad NAND-Flash test is assessed to at least another 2 days.

Both tests needs personal attendance in their initial phase and in their expected critical phase, namely for DDR3 from 350 – 400 krad and for NAND-Flash around 100 krad. Apparently, all time personal attendance would be preferable, but is not compliant with the ESTEC access regulation. Most of the irradiation time personal attendance is not possible.

The selected Micron 4-Gbit DDR3 device showed after irradiation to 400 krad in the unbiased

pretest nearly no errors at the test few days later. Accordingly it seems possible that the device survives a significant larger dose in the in-situ test. Therefore we propose to spend one test day more than the minimum of 6 days, namely from Friday morning to Friday afternoon of the next week in order to achieve a dose of roughly 600 krad.

The proposed irradiation schedule is outlined in the following table.

DDR3, Dose rate 85 rad / min = 5.1 krad/h

Irradiation Time	Duration	Dose In-crement [krad]	Total Dose [krad	Remarks
Fr. 9h – 13h	4			Equipment unloading, DDR3 installation
13h – 18h	5	25.5	25.5	Attended irradiation
Fr. 18h – Mo. 9h	63	321	347	Non-attended
Mo 9h – **20**h	11	56	403	Attended
Mo. 20h – Di. 9h	13	66	469	Non-attended
Tue. 9h – 18h	9	46	515	Attended
Tue. 18h – Wed. 9h	15	76	591	Non-attended
Wed. 9h – 14h	5	25	616	Attended

NAND-Flash, Dose rate 85 rad / min = 5.1 krad/h

Irradiation Time	Duration	Dose In-crement [krad]	Total Dose [krad	Remarks
Wed. 14h – 16h	2			DDR3 de-installation, NAND-Flash installation
16h – 18h	2	10.2	10.2	Attended
Wed. 18h – Thur. 9h	15	76	86	Non-attended
Thur. 9h – 18h	9	46	132	Attended
Thur. 18h – Fri. 9h	15	76	208	Non-Attended
9h – 13h	4			NAND-Flash de-installation Equipment loading

7 References

[1] JEDEC standard 79-3E: *DDR3 SDRAM Specification*

[2] JEDEC standard 21C: *204-Pin DDR3 SDRAM Unbuffered SO-DIMM Design Specification*

[3] M. Herrmann, K. Grürmann, and F. Gliem: *TID Test of 4 Gbit DDR3 SDRAM Devices*, TN-IDA-RAD-13/4

[4] M. Herrmann, K. Grürmann, and F. Gliem: Unbiased *TID Test of 2-Gbit and 4-Gbit DDR3 SDRAM Devices*, TN-IDA-RAD-13/9B

[5] *TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD, ESCC Basic Specification No. 22900*