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TN-IDA-RAD-11/5B

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Heavy Ion SEE Test of 2-Gbit DDR3 SDRAM Devices and of 8-Gbit NAND-Flash Memory Devices

RADEF Jyväskylä, May 23 – 27, 2011

Test Report

Contract number: ESTEC Contract No. 4000101358/10/NL/AF
Contract title: Radiation hard memory, Radiation testing of candidate memory devices for Laplace mission
Technical officer: V. Ferlet-Cavrois
Date of first writing: June, 12, 2011
Date of final issue: January, 8, 2015

Contents

1. Heavy Ion Test of 2-Gbit DDR3 3
1. Heavy Ion Test of 2-Gbit DDR3 3
2.Heavy Ion Test of 8-Gbit NAND-Flash 5
2.1 Differences in the SEU Cross Section of Samsung Lots 5
2.2 Asymmetry of Angular Cross Section Diagrams 8
2.2.1 Improvement of the Beam – Die Alignment 8
2.2.2 Angular Dependence of the Micron SEU Cross Section at Argon 10
2.2.3 Angular Dependence of the Samsung SEU Cross Section at Argon 17
2.3 Fluence / Dose Dependency of the SEU Cross Section at Argon 22

1. Heavy Ion Test of 2-Gbit DDR3

The primary test goal was to check out the functionality of the new DDR3 test bed under real conditions. The test bed operates a single DDR3 DUT in DLL ON mode at a clock frequency of 330 MHz.

Manu-facturer	Density [Gbit]	Part Number	Date Code	Lot Code	Count	IDA Marking
Samsung	2	K4B2G0846B-HCH9	0949	GLJ423AC	3	Sam1b, Sam1c, Sam1e
Micron	2	MT41J256M8HX-15E:D	1006	BYFCM91.21	3	Mic1c, Mic1d, Mic1e
Nanya	2	NT5CB256M8BN-CG	1026	01340100GP	3	Nan1b, Nan1c, Nan1d

Tab. 1: List of thinned DDR3 DUTs

Due to this high clock frequency the DUT Test Adapter (DTA, Xilinx Virtex FPGA, local power converter, etc, Fig. 1) dissipates a lot of heat, which in the vacuum chamber can be removed only by water cooling.
All DDR3 tests were performed with the DTA in vacuum. The prepared cooling system worked perfectly. At the hottest spot of the DTA the temperature stabilized below 60°C.

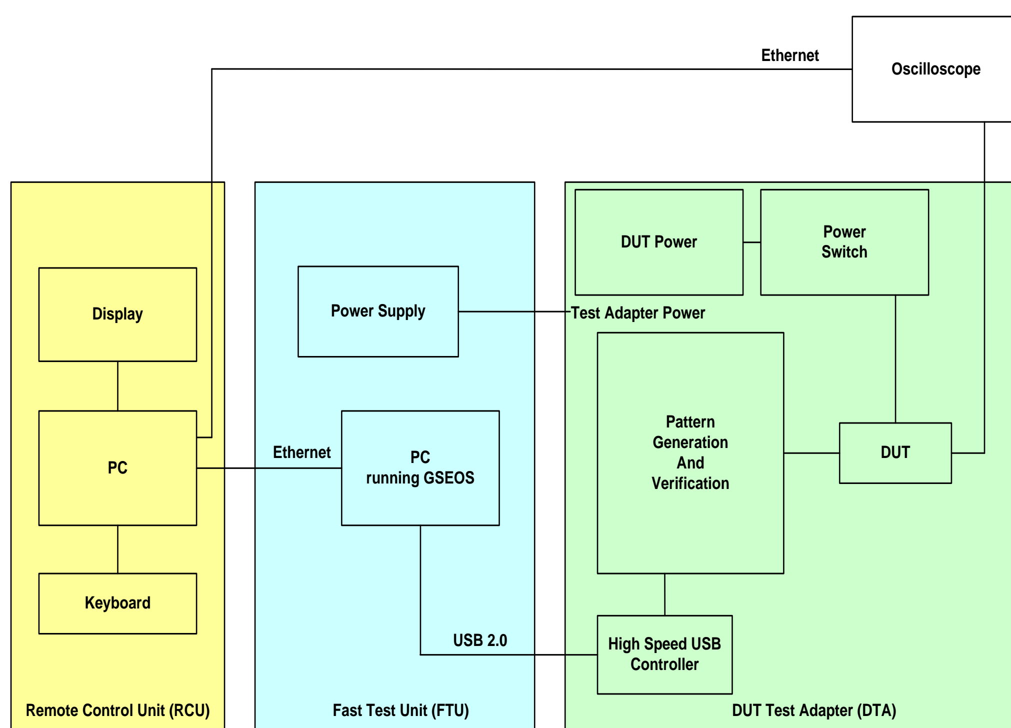

Fig. 1: RTMC6 Test Bed

The operational test unveiled a spurious failure in the USB data / address path between FTU

and DTA. The data / address information is structured into 4-byte blocks, which are transferred serially byte by byte. Two specific byte portions were always correct, and the two other byte portions were corrupted spuriously.

The failure could be masked by comparing of only the two always undisturbed bytes of the USB 4-byte package. In consequence the test was restricted to only one half of the DUT capacity.

Three Samsung, three Micron and three Nanya dies were thinned and showed full functionality after the thinning process. But at RADEF one of the three thinned Micron DUTs could not be operated properly. Accordingly three Samsung, two Micron and three Nanya DUTs were tested in three test modes:

M3a Biased Storage
M1 Marching
M2 Read

at Argon, Neon, Nitrogen, Iron and Krypton

The Argon test showed no significant differences between the DUTs of the same manufacturer, and also no substantial differences from manufacturer to manufacturer.
In consequence, for time saving reasons the tests at other ions were restricted to two or to only one DUT of each manufacturer.

SEFIs produced much more errors than the random SEUs at all ions.

Even Nitrogen, LET = 1.8 MeV $cm^2 mg^{-1}$ delivered SEFIs.

To summarize, the check out of the DDR3 test bed showed no principal deficiencies. The FPGA and the DUT work together properly at 330 MHz clock rate, i.e. at 660 MHz data byte rate. The detected spurious failure will have to be traced and fixed.

The thorough evaluation of the test data files has been started.

The insertion of a short initialization after a given number of accesses and / or after a given time period has been proven to be an efficient countermeasure against SEFI-induced data errors of DDR2 devices. We expect that this will be also the case for DDR3 devices.

In the present test bed the Xilinx Memory Controller S/W is running on the Xilinx FPGA. Since intermittent short initialization is not used in commercial applications, the Xilinx S/W provides no means for intermittent short initialization.

Two options are regarded for the implementation of intermittent short initialization:

(1) Respective modification of the Xilinx S/W

(2) Implementation of a proprietary simplified memory management S/W, which includes intermittent short initialization.

Arguments against option (1) are:

a) No documentation of the Xilinx S/W is available.

b) The Xilinx S/W is overloaded with respect to our intended application.
For example the sequence of specific data transfer operations is rearranged in favour of an improved average data rate. But, this makes the interpretation of error coupling mechanisms more difficult.

c) In the course of future tests other modifications might become desirable, too. Their implementation in a well-known proprietary design should be much easier compared to the implementation in a non-documented overloaded design.

Therefore, at this time we are in favour of option (2). A decision will be taken until end of June, in order to have a DDR3 test bed with intermittent short initialization ready for the next DDR3 test campaign in early November of this year.

The main tasks of the next DDR3 campaign will be:

(A) To extend the DDR3 characterization to Hyunday and Elpida devices

(B) To study the efficiency of intermittent short initialization.

(C) To study the SEL tolerance at Xe at room temperature
DDR3 SEL tests at elevated temperature are intended
for spring of next year.

2.Heavy Ion Test of 8-Gbit NAND-Flash

2.1 Differences in the SEU Cross Section of Samsung Lots

In the January 2011 test campaign the Samsung DUT of lot code FMH030X2, date code 0837 showed at Ar substantially less error counts than the Samsung DUT of lot code FFC042X1, date code 0837 as before, which was previously tested in the course of the joint ESTEC-Astrium France test campaign, and also in earlier campaigns.

It remained open, whether this different behaviour is a property of the tested lots or caused by a non-sufficient removal of the alpha-protection layer or by something else.
For clarification the test was repeated with the following DUTs (Tab. 2):

No	IDA Identifier	Date Code	Lot Code	Comments
1	SA1	0837	FMH030X2	very few SEUs in the previous test
2	SI4	0837	FFC042X1	comparatively many SEUs in the previous test
3	SA20	0837	FMH030X2	alpha protection layer completely removed
4	SI26	0925	FME071P2	alpha protection layer completely removed
5	SA27	0837	FMH030X2	alpha protection layer completely removed,

				plastic rim thinned (originally intended for tilting with slant ion incidence)

Tab. 2: DUT used for the “Lot Difference” investigation

The DUTs were operated in Mode M3a (biased Storage) with normal incidence, such as in the previous tests. Tab. 3 reports the test outcome.

Ion	LET	Test Mode	DUT ID	Number of blocks	Fluence [cm^{-2}]	Appr. Flux [$cm^{-2}s^{-1}$]	SEU Count	Remarks
Ar	10.1	M3a	SA1	64	1.0E6	1.0E4	4 1 3 average 2.7	σ = 4.0E-14 cm^2/bit
			SI4	64	1.0E6	1.0E4	166 187 179 average 177	σ = 2.6E-12 cm^2/bit
			SA20	64	1.0E6	1.0E4	2 4 4 average 3.3	σ = 4.9E-14 cm^2/bit
			SI26	64	1.0E6	1.0E4	4 4 5 average 4.3	
				64	1.0E7	1.0E4	17	17+0+0+0, SEUs only in the upper die
				16k	n.a.	n.a.	1549	No new exposure Read of all four dies delivers 1549 SEUs within the 4k blocks of the upper die, equivalent to 24 SEUs in 64 blocks σ = 3.3E-14 cm^2/bit
Ne	3.6	M3a	SI4	64	1.0E6	1.0E4	0	σ = 2.7E-15 cm^2/bit
				64	1.0E7	1.0E5	2	
			SA27	64	1.0E8	3.0E5	2	σ = 5.0E-16 cm^2/bit
				64	2.0E8	3.0E5	8	

Tab. 3: Outcome of the “Lot Difference” investigation

The DUT (1) delivered the same SEU cross section as measured previously.

The DUTs (2 – 4) delivered a SEU cross section smaller by a factor of about 50, such as in the January test campaign.

Protection layer removed or not removed makes nearly no difference, such as expected.

Further it could be shown,
(i) that at high LET the saturation values of both cross section approach each other, and
(ii) that at low LET the cross section curve of the lot FFC042X1 shows a lower LET threshold than the cross section curve of both lots FMH030X2 and FME071P2.

It remains open whether this significant difference in the SEU cross section is due to a change in the device design, to a general change in the fabrication process or to a non-intended deviation between different fabrication lines.

The cross section per bit is calculated according to

$$\sigma = \frac{SEU\ Count * 64}{F * 8Gbit} * 2 = \frac{SEU\ Count}{F} * 1.49E-8 \left[\frac{cm^2}{bit}\right]$$

The factor 64 takes into account that only 1/64 of the blocks per die are operated.
The factor 2 takes into account that nearly all SEU disturbance are in 0 → 1 direction.
The chosen data pattern implies an equal count of zeros and ones. An all zero pattern would deliver twice the measured count of SEUs.

"New" Samsung (lots FMH030X2 and FME071P2), "Previous" Samsung (lot FFC042X1) and Micron DUTs differ substantially in their SEU cross section. Rough figures are:

"New" Samsung: 4E-14 cm^2/bit
"Previous" Samsung: 3E-12 cm^2/bit = "New" Samsung x 75
Micron: 2E-11 cm^2/bit = "New" Samsung" x 500 (see Tab. 5-Tab. 7)

Manufacturer	Density	Part Number	Date Code	Lot Code	Count	Marking	Comment
Samsung	4x8Gbit	K9WBG08U1M-PIB0	0837	FMH030X2	5	SA20 – SA24	α-Layer removed
Samsung	4x8Gbit	K9WBG08U1M-PIB0	0837	FMH030X2	4	SA25 – SA28	α-Layer removed, rim thinned
Samsung	4x8Gbit	K9WBG08U1M-PIB0	0837	FMH030X2	8	SA1-SA6, SA9, SA10	prev. Test, nearly no errors
Samsung	4x8Gbit	K9WBG08U1M-PIB0	0816	FFC042X1	1	SI4	prev. Test, 63 krad
Samsung	4x8Gbit	K9WBG08U1M-PIB0	0816	FFC042X1	1	SI10	prev. Test, 37 krad
Samsung	4x8Gbit	K9WBG08U1M-PIB0	0925	FME071P2	6	SI20 – SI25	from Projekt

							MORE
Samsung	4x8Gbit	K9WBG08U1M-PIB0	0925	FME071P2	4	SI26 – SI29	from Projekt MORE, α-Layer removed
Micron	8Gbit	MT29F8G08AAAWP-A	0842	unknown	1	MC1	prev. Test, 17 krad
Micron	8Gbit	MT29F8G08AAAWP-A	0842	unknown	1	MC2	prev. Test, 7 krad
Micron	8Gbit	MT29F8G08AAAWP-A	0842	unknown	1	MC5	prev. Test, 70 krad
Micron	8Gbit	MT29F8G08AAAWP-A	0842	unknown	1	MC6	prev. Test, 7 krad
Micron	8Gbit	MT29F8G08AAAWP-A	0842	unknown	5	MC9-MC11, MC14, MC15	prev. Test, fresh

Tab. 4: List of opened DUTs

2.2 Asymmetry of Angular Cross Section Diagrams

2.2.1 Improvement of the Beam – Die Alignment

In the January 2011 campaign the angular cross section diagrams at Ar, Fe and Kr were measured. In particular at very slant incidence, 82.5° and 85.0°, the diagrams showed some asymmetry. This raised the suspicion of a non-perfect alignment of the die surface with respect to the beam axes.
Meanwhile, two improvements of the tilting set up were introduced:

a. To avoid bending of the turn table it was strengthened by a metal rim (Fig. 2)

b. A tube (length 10 cm, diameter 5 mm) could be attached to the turn table with its axes identical to the z-axes (Fig. 3).
   A LED situated at the back end of the tube is monitored by the camera inside the beam line (Fig. 4).
   Correct alignment is reached if the camera sees a round shape of the LED during rotation over all azimuth angles Θ. Then the z–axis is an extension of the beam axes.

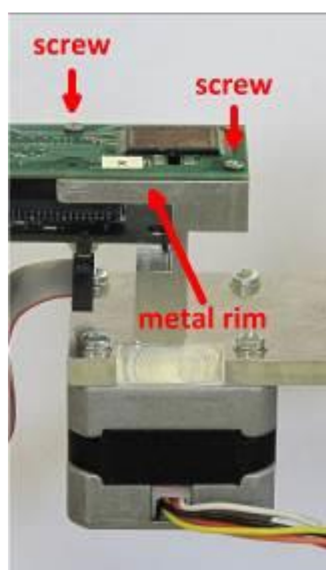

Fig. 2: Improved turn table of the tilting set up

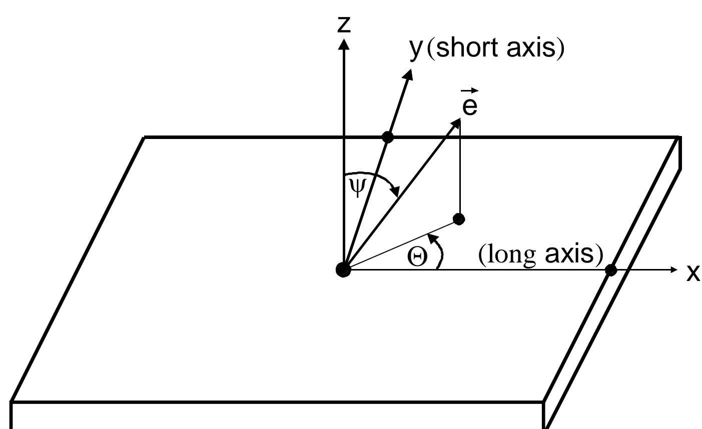

Fig. 3: Definition of the Azimuth Angle Θ and the Elevation Angle ψ vector e in parallel to the ion incidence

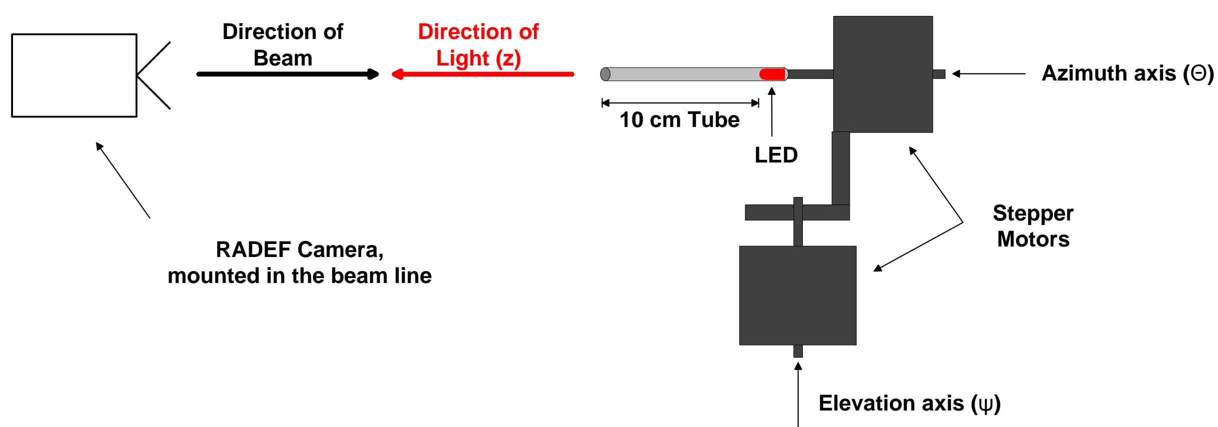

Fig. 4: Alignment tube

Both measures delivered a much better symmetry of the polar SEU cross section diagram.

Assuming an overlayer thickness of 10 µm, the range of the ion should be larger than 115 µm at elevation angle $\psi = 85°$. The range of the used argon ions is 118 µm.

2.2.2 Angular Dependence of the Micron SEU Cross Section at Argon

The comparison of the previous and the new SEU Cross Section diagram of the Micron 8-Gbit NAND-Flash for the elevation angles $\psi = 75°$, 82.5° and 85.0° illustrates the improvement in symmetry (Fig. 5 to Fig. 7, Tab. 5 to Tab. 7). The cross section is normalized by its value for normal incidence. At $\psi = 75°$ the previous and the new angular diagram are in good agreement. At the larger elevation angles of $\psi = 82.5°$ and 85.0° the previous diagrams show a substantial distortion due to an angular misalignment between the axes of the beam and the turn table. This distortion is gone after the improved alignment.
At $\psi \leq 60°$ the misalignment effective in the previous test caused an only negligible distortion. Fig. 8 gained by the previous test and Fig. 9 gained by the new test give a valid description of the angular dependence of the SEU cross section.

At $\psi = 82.5°$ and 85.0° the ion incidence exactly in parallel to the long die axis ($\Theta = 0°$ and 180°) produced many 2-bit errors, in contrast to all other azimuth angles Θ.

At $\psi \leq 60°$, i.e. for one half of the hemisphere, the cross section remains for all azimuth angles Θ below its value for normal incidence.
With the increase of the elevation angle from $\psi = 0$ to $\psi = 60°$ the cross section for incidence in parallel to the long die axis ($\Theta = 0$) remains nearly unchanged.
In contrast the cross section for incidence along the short die axis drops with increasing elevation angle ψ to about 30% of its value at normal incidence. The polar diagram is shaped similar to that of a dipole antenna.

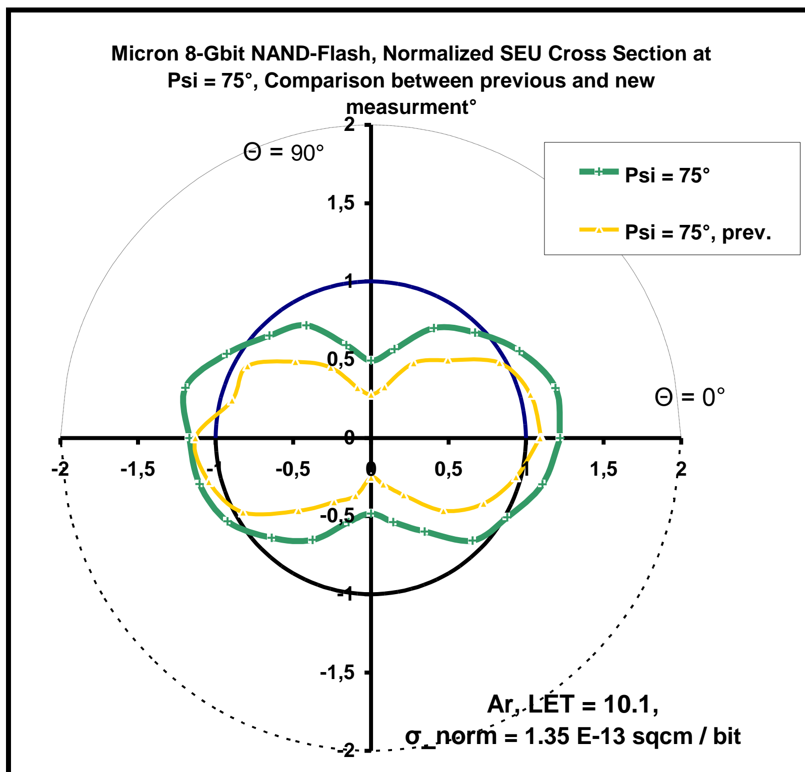

Fig. 5: Comparison between previous and new cross section diagram, Psi = 75°

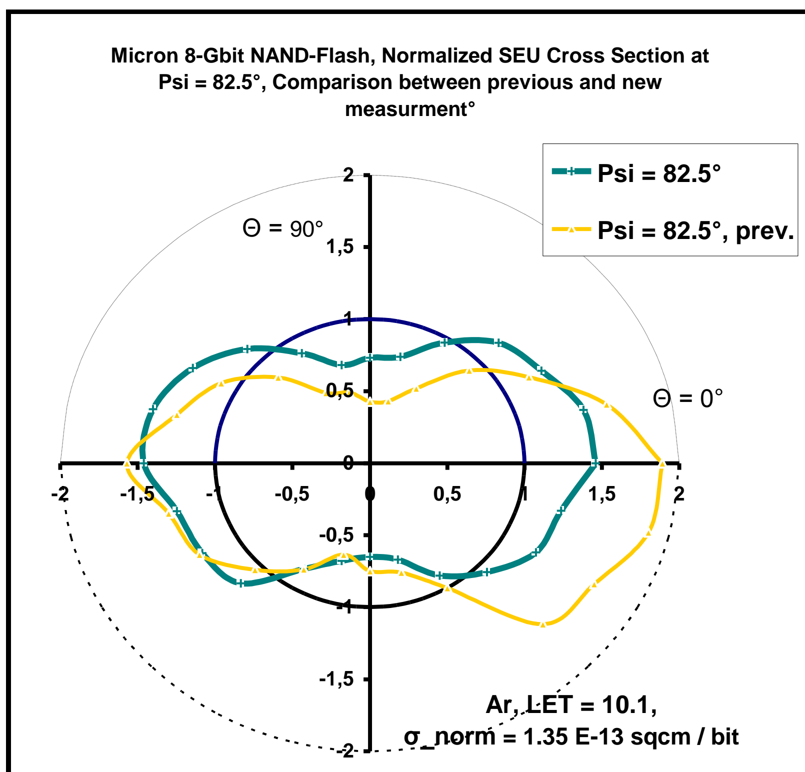

Fig. 6: Comparison between previous and new cross section diagram, Psi = 82.5°

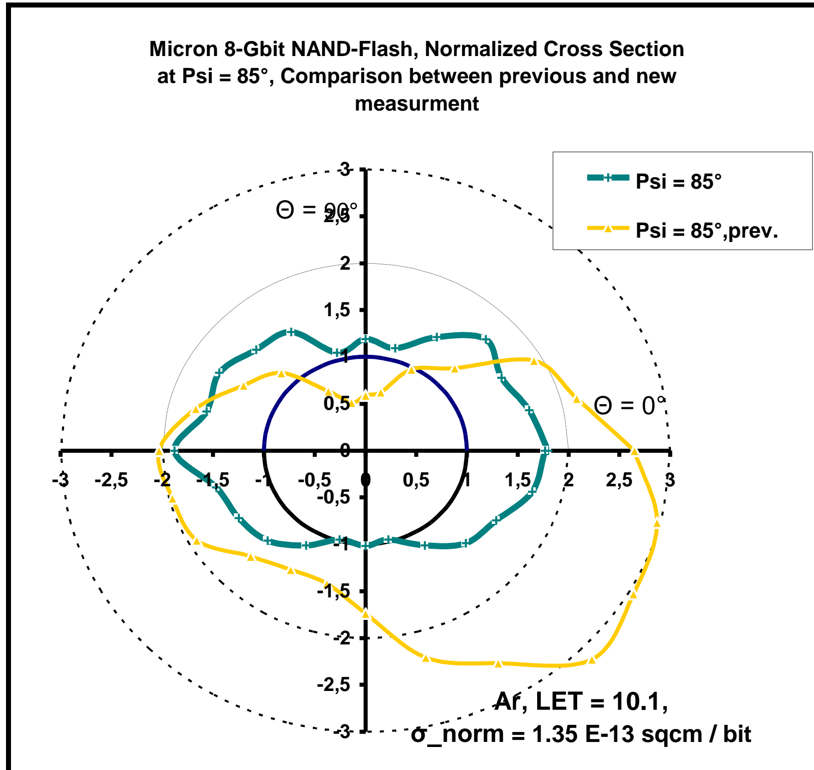

Fig. 7: Comparison between previous and new cross section diagram, Psi = 82.5°

Micron 8-Gbit NAND-Flash, Normalized Cross Section
at Psi ≤ 60°

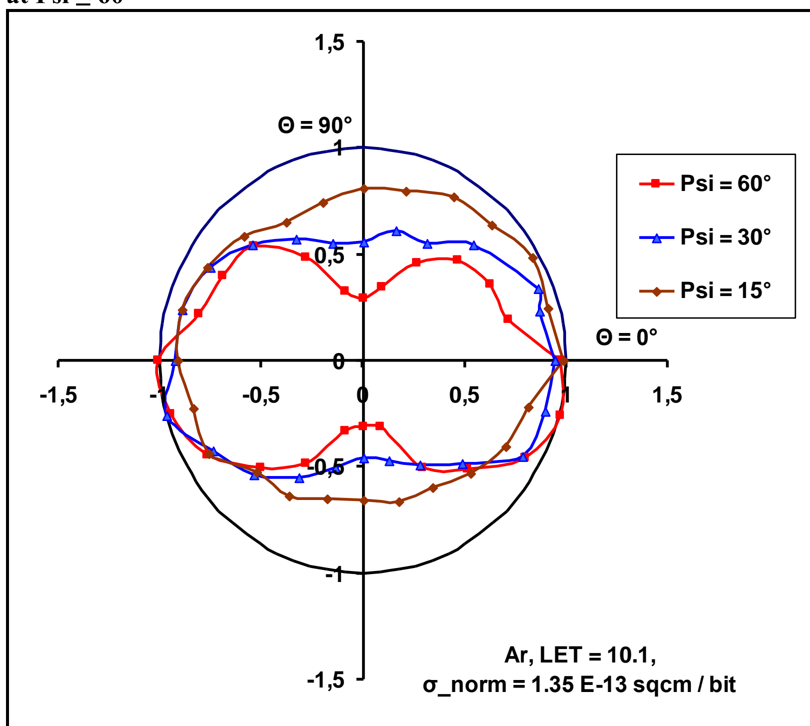

Fig. 8: Valid SEU cross section diagram, elevation angles Psi ≤ 60°

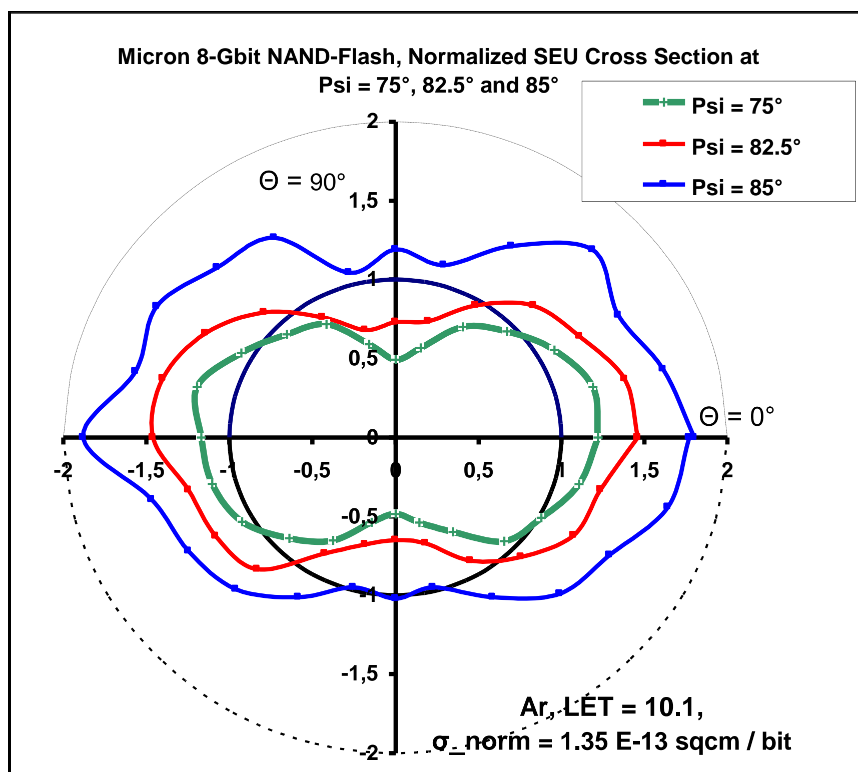

Fig. 9: Valid SEU cross section diagram, elevation angle Psi = 75°, 82.5° and 85°

At larger elevation angles (ψ = 75°, 82.5°, 85°) the diagram expands. It remains its elongation for incidence in parallel to the long die axis.

At ψ =85° the cross section exceeds at all azimuth angles its value for normal incidence, but for all azimuth angles Θ by less than a factor of two. As we will see later on, this makes a significant difference between the Micron and the Samsung device.

40Ar+12, LET = 10.1 MeV cm²mg⁻¹, Micron 8 Gbit NAND-Flash, 64 blocks operated

DUT	Test Mode	Elevation Angle ψ [°]	Azimuth Angle θ [°]	Fluence cm^{-2}	Flux $cm^{-2}\ s^{-1}$	Error Counts,	$\sigma_{\psi,\Theta}$ / $\sigma_{0,0}$	σ [cm^2/bit]	
9.3 MeV / amu									
m/q = 3.33, 40Ar+12, E = 372 MeV, LET = 10.1 / 12.6 MeV cm^2mg^{-1} @ surface / 50 µm, range 118 µm									
MC2	M3b	0	0	1.0E6	1.0 E4	1068 1065 998 average 1044		1.6E-11	DUT of previous test, already exposed to 7.3 krad
MC9	M3b			1.0E6	1.0E4	1251 1208 1244 average 1234		1.8E-11	New DUT

MC9	M3b	75.0	0			1558	1.263		
			+15			1521	1.233		
			+30			1367	1.08		
			+45			1173	0.951		
			+60			1000	0.810		
			+75			724	0.587		
			+90			609	0.494		
			105			756	0.613		
			120			1024	0.830		
			135			1140	0.924		
			150			1323	1.072		
			165			1526	1.237		
			180			1443	1.169		
			195			1410	1.143		
			210			1316	1.066		
			225			1115	0.904		
			240			928	0.752		
			255			687	0.558		
			270			598	0.485		
			285			688	0.558		
			300			853	0.691		
			315			1147	0.929		
			330			1253	1015		
			345			1414	1.146		
			0			1386	1.123		
			180			1562	1.266		

Tab. 5: Tilting of Micron 8-Gbit NAND-Flash, Storage Mode M3, ψ = 75.0°

40Ar+12, LET = 10.1 MeV cm^{2}mg^{-1}, Micron 8 Gbit NAND-Flash, 64 blocks operated

DUT	Test Mode	Elevation Angle	Azimuth Angle	Fluence cm^{-2}	Flux cm^{-2} s^{-1}	Error Counts,	$\sigma_{\psi,\Theta}$ / $\sigma_{0,0}$	σ [cm^2/bit]	

		ψ [°]	θ [°]						
9.3 MeV / amu									
m/q = 3.33, 40Ar+12, E = 372 MeV, LET = 10.1 / 12.6 MeV cm^{2}mg^{-1} @ surface / 50 µm, range 118 µm									
MC9	M3b	0	0	1.0E6	2.5E4	1166 1156 1151 average 1158		1.7E-11	
MC9	M3b	82.5	0			1761 1756 1691 average 1736	1.50	Many 2-bit errors	
			+15			1653	1.43		
			+30			1478	1.28		
			+45			1364	1.18		
			+60			1118	0.965		
			+75			884	0.763		
			+90			846	0.731		
			105			816	0.705		
			120			1018	0.880		
			135			1294	1.12		
			150			1524	1.32		
			165			1683	1.45		
			180			1675 1705 average 1680	1.46	Many 2-bit errors	
			195			1495	1.29		
			210			1447	1.25		
			225			1372	1.18		
			240			983	0.849		
			255			813	0.702		
			270			754	0.651		
			285			805	0.695		
			300			1045	0.902		
			315			1241	1.07		

			330			1438	1.24		
			345			1481	1.28		
			0			1540 1674 1730 average 1648	1.42	Many 2-bit errors	
			180			1505	1.30		

Tab. 6: Tilting of Micron 8-Gbit NAND-Flash, Storage Mode M3, ψ = 82.5°

40Ar+12, LET = 10.1 MeV cm^{2}mg^{-1}, Micron 8 Gbit NAND-Flash, 64 blocks operated

DUT	Test Mode	Elevation Angle ψ [°]	Azimuth Angle θ [°]	Fluence cm^{-2}	Flux cm^{-2} s^{-1}	Error Counts,	$\sigma_{\psi,\Theta}$ / $\sigma_{0,0}$, new		
9.3 MeV / amu									
m/q = 3.33, 40Ar+12, E = 372 MeV, LET = 10.1 / 12.6 MeV cm^{2}mg^{-1} @ surface / 50 µm, range 118 µm									
MC9	M3b	0	0	1.0E6	2.5E4	1036 962 984 average 994			
MC9	M3b	85.0	0			1939 1660 1766 average 1788	1.80	Many 2-bit errors, also 3-bit errors	
			+15			1660	1.67		
			+30			1542	1.55		
			+45			1667	1.68		
			+60			1394	1.40		
			+75			1123	1.13		
MC9	M3b	82.5	+90			1178	1.19		
			105			1081	1.088		
			120			1447	1.46		
			135			1515	1.52		
			150			1647	1.66		
			165			1606	1.62	One 2-bit error	
			180			1871	1.88		

								Many 2-bit errors	
			195			1509	1.52		
			210			1428	1.44		
			225			1350	1.36	1 stuck bit	
			240			1163	1.17		
			255			978	0.984		
			270			1009	1.02		
			285			867	0.872		
			300			1166	1.17		
			315			1393	1.40		
			330			1485	1.49		
			345			1688	1.70		
			0			1971 1747 1566 average 1761	1.77	Many 2-bit errors	
			180			1807	1.82		
		0	0			910 822 923 average 885			

Tab. 7: Tilting of Micron 8-Gbit NAND-Flash, Storage Mode M3b, $\psi = 85.0°$

2.2.3 Angular Dependence of the Samsung SEU Cross Section at Argon

Fig. 10 shows the angular dependence of the SEU cross section of the Samsung device at Argon and $\psi \leq 60°$. This diagram is derived from small error counts gained during the previous test. Therefore, the shape of the diagrams is somewhat fluctuating. But it becomes apparent that the cross section remains restricted to values roughly equal or even less than the value for normal incidence. This is in agreement to the Micron device.

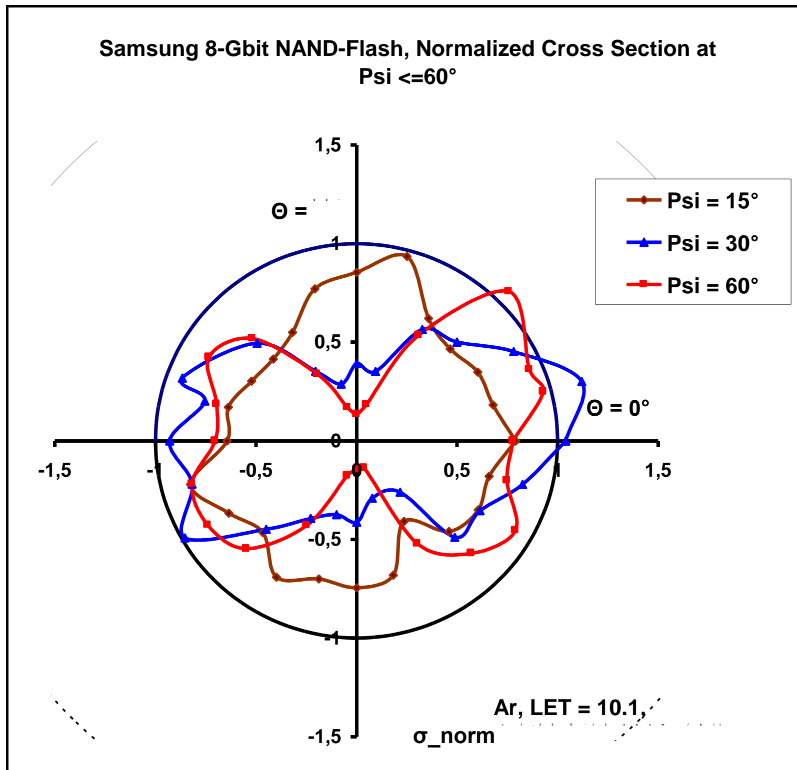

Fig. 10: SEU cross section diagram, elevation angles Psi ≤ 60°

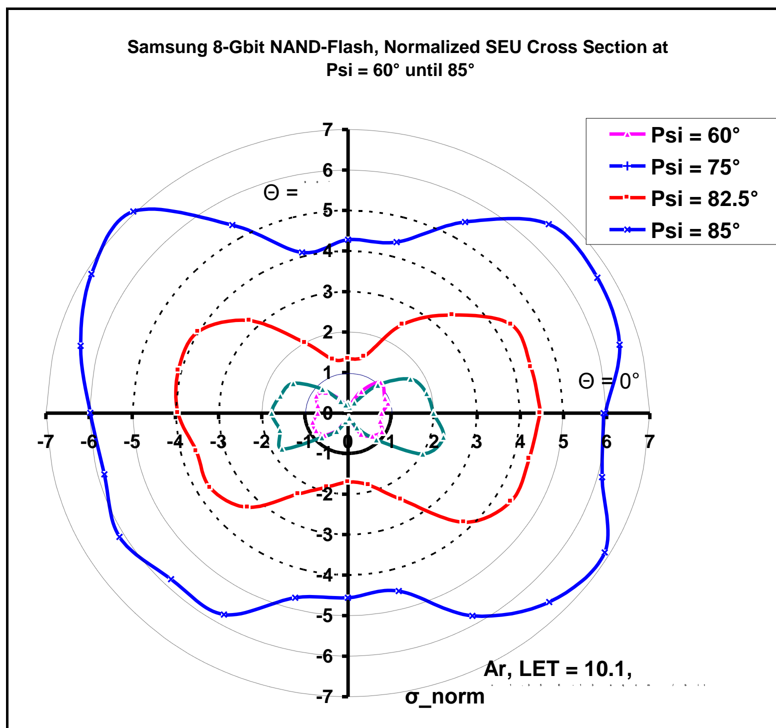

Fig. 11: SEU cross section diagram, elevation angles Psi ≥ 60°

Fig. 11 shows the cross section diagram for elevation angles $\psi \geq 60°$. The test data are compiled in Tab. 8 and Tab. 9.

Such as for the Micron device the diagrams develop a “dipole” shape with the major

extension for incidence in parallel to the long die axis (Θ = 0). But the expansion of the diagrams from ψ = 60° until ψ = 85° exceeds that of the Micron device by far. For the Micron device we got a maximum expansion factor of about two, but for the Samsung device of up to seven. Maximum sensitivity is reached between the long die axis and the Θ= + - 45° diagonals, and minimum sensitivity for the short die axis.
The diagrams for ψ = 60° and ψ = 75° are gained in the January test campaign, and the diagrams for ψ = 82.5° and ψ = 85° in the May campaign.
At ψ = 75° two azimuth positions were measured again for comparison. The previous values are in a fair agreement with the new values (Θ = 0°: previously 1.99 ↔1.56; Θ = 90°: 0.22 ↔0.22).

Again we see a rather good symmetry of the diagrams due to the improved alignment procedure.

40Ar+12, LET = 10.1 MeV cm^{2}mg^{-1}, Samsung 8 Gbit NAND-Flash, 64 blocks operated

DUT	Test Mode	Elevation Angle ψ [°]	Azimuth Angle θ [°]	Fluence cm^{-2}	Flux cm^{-2} s^{-1}	Error Counts,	$\sigma_{\psi,\Theta}$ / $\sigma_{0,0}$, new	σ [cm^2/bit]	
9.3 MeV / amu									
m/q = 3.33, 40Ar+12, E = 372 MeV, LET = 10.1 / 12.6 MeV cm^{2}mg^{-1} @ surface / 50 µm, range 118 µm									
SI10	M3b	0	0	1.0E6	2.0E4	283 356 295 average 311	1.0	4.6E-12	
SI10	M3b	85.0	0			1897 1929 1744 average 1857	5.97	2-Bit Errors as for Micron?	
			+15			2028	6.52		
			+30			2078	6.68		
			+45			2050	6.59		
			+60			1692	5.44		
			+75			1358	4.37		
			+90			1330	4.28		
			105			1276	4.10		
			120			1666	5.36		
			135			2187	7.03		
			150			2134	6.86		

			165			1994	6.41		
			180			1857	5.97	? Many 2-bit errors ?	
			195			1818	5.85		
			210			1901	6.11		
			225			1803	5.80	1 stuck bit	
			240			1787	5.75		
			255			1468	4.72		
			270			11418	4.56		
			285			1414	4.55		
			300			1798	5.78		
			315			2053	4.67		
			330			2139	6.88		
			345			1898	6.10		
			0			1760 1819 1954 average 1844	5.93	Many 2-bit errors	
								In between Psi = 82.5° Run	
		85	5	1.0E6	2.0E4	1872	6.02	Many 2-bit errors ?	
			10			1864	5.99	Many 2-bit errors ?	
			355			1786	5.74	Many 2-bit errors ?	
			350			1887	6.06	Many 2-bit errors ?	

Tab. 8: Tilting of Samsung 8-Gbit NAND-Flash, Storage Mode M3b, ψ = 85.0°

40Ar+12, LET = 10.1 MeV cm^{2}mg^{-1}, Samsung 8 Gbit NAND-Flash, 64 blocks operated

DUT	Test Mode	Elevation Angle ψ [°]	Azimuth Angle θ [°]	Fluence cm^{-2}	Flux cm^{-2} s^{-1}	Error Counts,	$\sigma_{\psi,\Theta}$ / $\sigma_{0,0}$, new	σ [cm^2/bit]	
9.3 MeV / amu									
m/q = 3.33, 40Ar+12, E = 372 MeV, LET = 10.1 / 12.6 MeV cm^{2}mg^{-1} @ surface / 50 µm, range 118 µm									
SI10	M3b	0	0	1.0E6	2.0E4	288 281 295 average	0.926		

						288			
SI10	M3b	85.0	0			1264 1220 1384 average 1289	4.14		
			+15			1265	4.07		
			+30			1259	4.05		
			+45			987	3.17		
			+60			727	2.34		
			+75			416	1.34		
			+90			386	1.24		
			105			395	1.27		
			120			576	1.85		
			135			930	2.99		
			150			1155	3.71		
			165			1171	3.77		
			180			1134	3.65	? Many 2-bit errors ?	
			195			1047	3.37		
			210			1062	3.41		
			225			947	3.05		
			240			664	2.14		
			255			544	1.75		
			270			490	1.58		
			285			529	1.70		
			300			708	2.28		
			315			1097	3.53		
			330			1256	4.04		
			345			1253	4.03		
			0			1246 1264 1341 average 11284	4.13	Many 2-bit errors ?	

Tab. 9: Tilting of Samsung 8-Gbit NAND-Flash, Storage Mode M3b, $\psi = 82.5°$

2.3 Fluence / Dose Dependency of the SEU Cross Section at Argon

In previous campaigns it was observed that the SEU cross section of the Micron device shrinks substantially with increasing fluence / dose.

This was again the case for both, the Micron and the Samsung DUT (Fig. 12).

The SEU count of a virgin Micron DUT at normal incidence (average of three exposures) decreased from initially

1234	@ Argon fluence of F = 0 to	
1158	@ $\Delta F = 42 \times 1.0E6\ cm^{-2} = 4.2\ E7\ cm^{-2}$	$\rightarrow$ D = 6.8 krad
994	@ $\Delta F = 35 \times 1.0E6\ cm^{-2} = 3.5\ E7\ cm^{-2}$	$\rightarrow$ D = 12.4 krad
885	@ $\Delta F = 7.0\ E7\ cm^{-2}$	$\rightarrow$ D = 23.8 krad

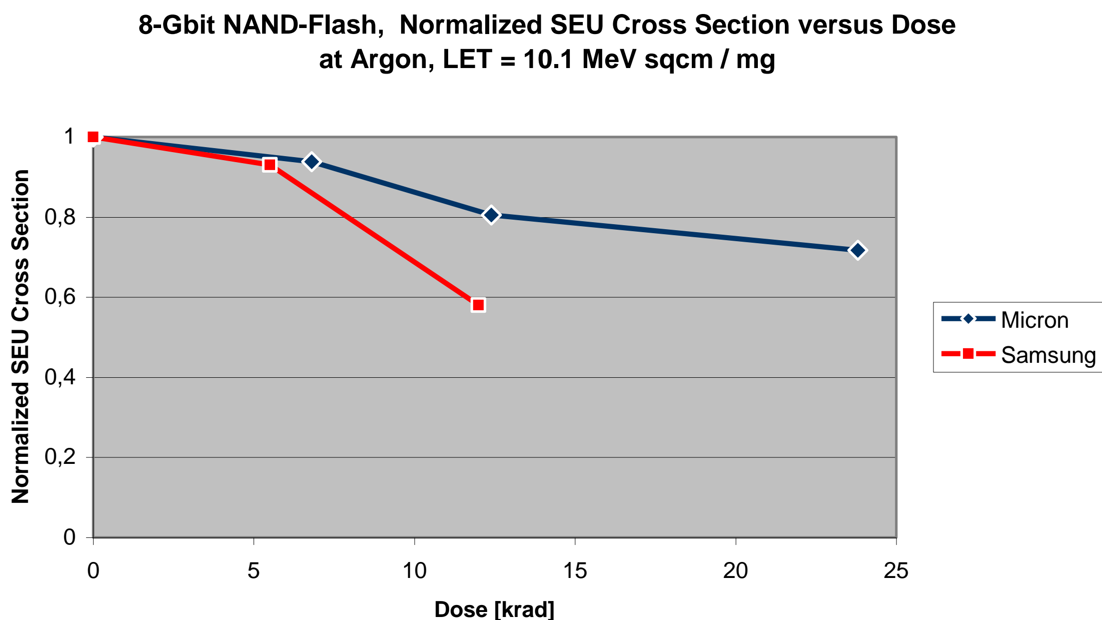

Fig. 12: Micron 8-Gbit NAND-Flash, Normalized SEU Cross Section versus Dose at Argon

The respective values of the Samsung DUT are:

311	@ Argon fluence of F = 0 to	
288	@ $\Delta F = 34 \times 1.0E6\ cm^{-2} = 3.4\ E7\ cm^{-2}$	$\rightarrow$ D = 5.5 krad
181	@ $\Delta F = 40 \times 1.0E6\ cm^{-2} = 4.0\ E7\ cm^{-2}$	$\rightarrow$ D = 12.0.2 krad.

Whether this effect is reversible by annealing ore permanent is an open question.
In the first case measured cross sections would be too optimistic, in particular those, which have been measured at the end of a test series due to the accumulated and still not annealed dose.

In the second case the measured SEU cross section measured at a particular dose would be too optimistic at the beginning of a mission, until the mission reaches the respective dose.

To study this effect DUTs should be irradiated with Argon until e.g. 25 krad at the first day of the campaign. After 5 krad each the cross section at normal incidence should be measured. Then, every following day the cross section should be determined again.

Another open question is whether this effect appears in the same way at other ions?

3. DDR3 SDRAM package pictures

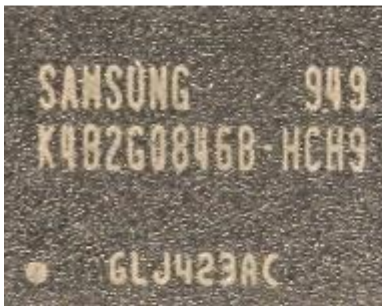

Fig. 13: Samsung K4B2G0846B-HCH9 DDR3 SDRAM

Fig. 14: Micron MT41J256M8HX-15E:D DDR3 SDRAM

Fig. 15: Nanya NT5CB256M8BN-CG DDR3 SDRAM

4. NAND-Flash package pictures

Fig. 16: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 17: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 18: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 19: Micron MT29F8G08AAA-WP