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Heavy Ion SEE Test
of
16-Gbit/32-Gbit Micron
SLC NAND-Flash Memory Devices

RADEF Jyväskylä, Jan. 9 – 13, 2012
RADEF Jyväskylä, April 16 – 20, 2012

Test Report

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1 Introduction

Overall goal is the SEE heavy ion response of 25 nm Micron 16-Gbit and 32-Gbit Single Level Cell (SLC) NAND-Flash memory devices. In this context, two radiation test campaigns were performed by IDA under contract with Astrium, Astrium being under contract with ESTEC:

1. Heavy ion test at the Radiation Effects Facility (RADEF) of the University of Jyväskylä, Jyväskylä, Finland, January 9 – 13, 2012

2. Heavy ion test at the Radiation Effects Facility (RADEF) of the University of Jyväskylä, Jyväskylä, Finland, April 16 – 20, 2012

Both test campaigns were combined tests of NAND-Flash and DDR3 SDRAM devices. In this test report, only the NAND-Flash test results are presented.

The focus of the first test campaign was to determine SEU and SEFI cross sections and to address the annealing behaviour.

The focus of the second test campaign was to study Destructive Failures (DF) and annealing of hard and soft SEUs.

2 Test Facility

Beam time at the RADEF facility of the University of Jyväskylä, Finland, was provided by ESTEC to perform these Heavy Ion tests. The RADEF facility is described in [1].

The ion cocktail shown in Tab. 1 was used with the exception of Silicon. The MEAS and SRIM simulated LET values differ somewhat in detail. For the test data evaluation, the SRIM simulated LET values are used.

Tab. 1: RADEF 9.3 MeV/amu Ion Cocktail

Ion	Energy	LET, Surface, MEAS	LET, Surface, SRIM	Range
	[MeV]	[MeV cm^2 mg^{-1}]	[MeV cm^2 mg^{-1}]	[µm]
$^{15}N^{4+}$	139	1.87	1.83	202
$^{20}Ne^{6+}$	186	3.68	3.63	146
$^{30}Si^{8+}$	278	6.74	6.40	130
$^{40}Ar^{12+}$	372	10.08	10.2	118
$^{56}Fe^{15+}$	523	18.84	18.5	97
$^{82}Kr^{22+}$	768	30.44	32.2	94
$^{131}Xe^{35+}$	1217	54.95	60.0	89

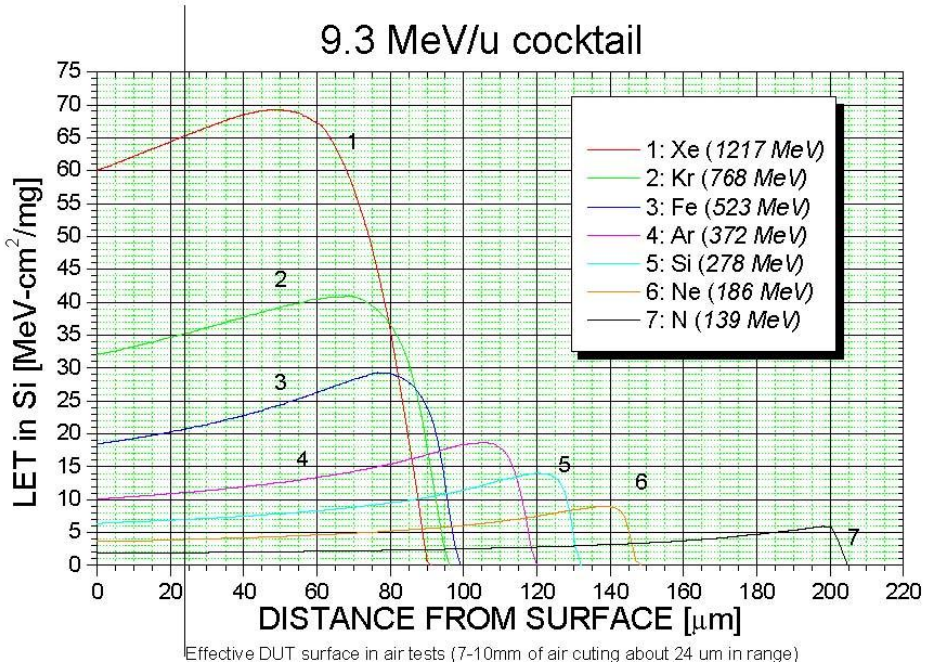

Fig. 1: RADEF 9.3 MeV/amu ion cocktail, LET versus range [2]

Fig. 1 shows the LET versus range for DUTs in vacuum.

Most of the tests were performed with the DUT in air. The ions penetrate a kapton foil of about 25 µm thickness at the end of the beam tube and additionally an air gap of about 1 cm. In comparison to irradiation in vacuum, the ion range in Si/SiO_2 is shortened, and the LET value in the active layer below the surface is shifted toward the Bragg peak and thereby it is increased.

3 DUT Type and Organization

The tested DUTs [3] [4] are described in Tab. 2. Tab. 3 presents the DUTs used for comparison. All parts are single die packages (SDP), except the Samsung 4x8-Gbit part which is a quad die package (QDP).

Manufacturer	Capacity [Gbit]	Package	Part Number	Date Code	Lot Code	Samples	IDA ID
Micron	16	SDP	MT29F16G08ABACAWP-IT:C	1122	unknown	7	M305-M311
				1146	unknown	34	M312-M345
Micron	32	SDP	MT29F32G08ABAAAWP-IT:A	1130	unknown	14	M403-M416

Tab. 2: Tested DUTs

Manufacturer	Capacity [Gbit]	Package	Part Number	Date Code	Lot Code
Micron	8	SDP	MT29F8G08AAAWP-A	0842	unknown
Samsung	8	SDP	K9F8G08U0M	0725	FFE006XX IDA Lot E
Samsung	4x8	QDP	K9WBG08U1M-PIB0	0816	FFC042X1, IDA Lot D
Samsung	4x8	QDP	K9WBG08U1M-PIB0	0837	FMH030X2 IDA Lot F
Samsung	4x8	QDP	K9WBG08U1M-PIB0	0925	FME071P2, IDA Lot G

Tab. 3: DUTs for comparison

Die capacity	Number of blocks	Number of pages per block	Number of bytes per page+spare area
8-Gbit	4096	64, (64)	4096+128, (4224)
16-Gbit	4096	128, (64)	4096+224, (4224)
32-Gbit	4096	128, (64)	8192+448, (4224)

Tab. 4: Organization of SLC NAND-Flash devices. The tested subset is given in parentheses.

In the existing NAND-Flash test bed the write operation is hardware controlled by the head station and covers the full address space.

In contrast, the read and compare operation is software controlled by the GSEOS S/W of the remote control PC.

This software could not be adapted in time to the changed count of pages and bytes of the 16-Gbit and 32-Gbit NAND-Flash devices.

Therefore, the read operation always covers only 64 pages per block and always only 4k bytes per page, such as shown by the figures in parentheses in Tab. 4.

Erase and write operations are performed over all pages and all bytes of the accessed blocks.

4 DUT Preparation

First, all DUTs were marked with an individual ID and were checked for factory marked bad blocks. The ID and the bad block table were programmed into block 0, which is guaranteed to be valid by the manufacturer for every DUT. These bad blocks were not accessed by erase or program operations any more.

All tested Micron 25 nm SLC NAND-Flash devices showed factory marked bad blocks at the block addresses 90 and 91. Only a few devices showed additional bad blocks which are listed in Tab. 5. These four devices were not used during these SEE test campaigns.

IDA ID	bad block 1	bad block 2	bad block 3	bad block 4
M360	90	91	3794	
M361	90	91	1550	
M362	90	91	2562	
M363	90	91	3613	3615

Tab. 5: DUTs with more than two factory marked bad blocks

The 48-pin TSOP1 packages were opened for direct access of the ion beam to the surface of the die. The opening is done by drop etching with fuming nitric acid. The device is placed on a mounting plate and is covered with Teflon tape. A window is cut into this tape. Then the device is heated to about 70°C, and an acid drop is given into the window. Thereafter the device is rinsed with water and then with acetone. This process of etching and rinsing is repeated many times until the die surface is free of plastic cover. After the opening procedure the functionality check is repeated.

The opening yield of both Micron devices is extremely low. For the 16-Gbit DUTs a yield of 40% of fully opened dies was achieved. This is in line with the older 50 nm 8-Gbit Micron devices. In contrast to the old 51 nm 8-Gbit Samsung devices, there is only a small time window to get a fully opened die surface and a functional device. For the 32-Gbit devices a yield of 0% of fully opened dies was achieved because in contrast to the previous 51 nm Samsung and 50 nm Micron NAND-Flash generations, the new 25 nm NAND-Flash from Micron is packaged differently (Fig. 2 and Fig. 3 compared to Fig. 4 and Fig. 5). The complete opening of the 32-Gbit Micron DUTs is extremely delicate because there is nearly no space between the die edges and the package rim on three of the four sides (Fig. 3). Because of the insufficient yield the Destructive Failure investigations were gained from the 16-Gbit Micron device.

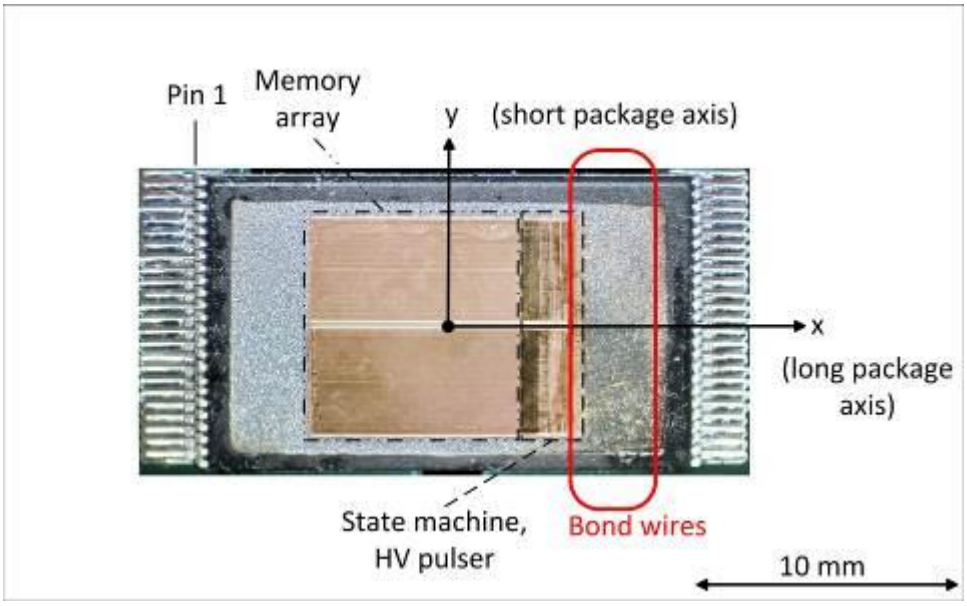

Fig. 2: Opened package of the Micron 25 nm 16-Gbit NAND-Flash

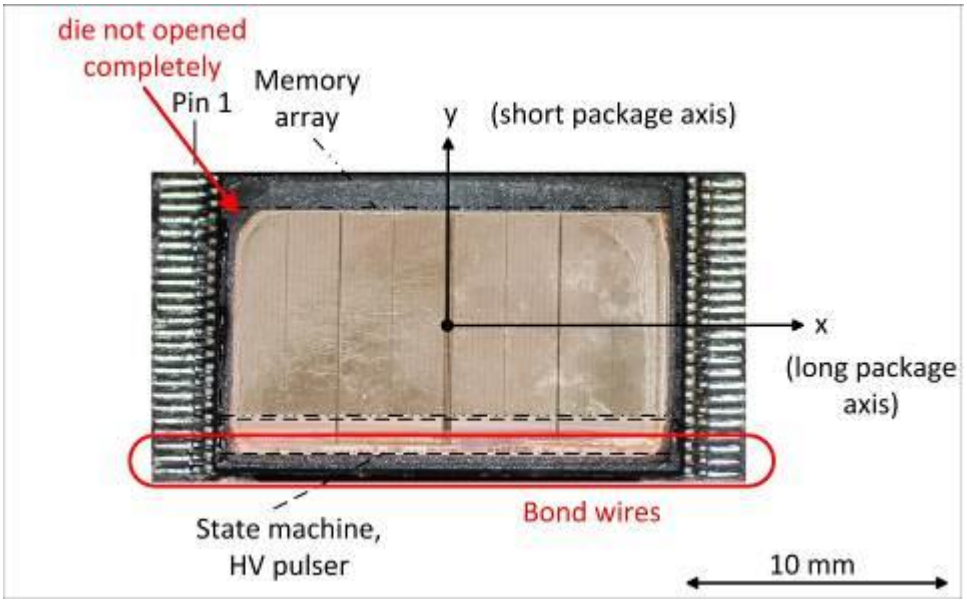

Fig. 3: Opened package of the Micron 25 nm 32-Gbit NAND-Flash

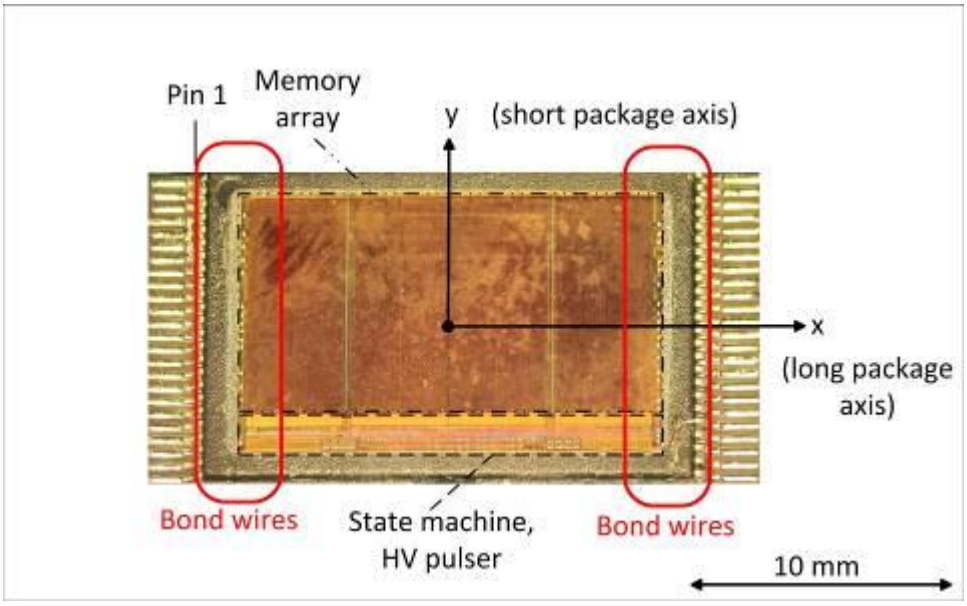

Fig. 4: Opened package of the Samsung 51 nm 4x8-Gbit NAND-Flash with bond wires on the small sides of the TSOP1 package

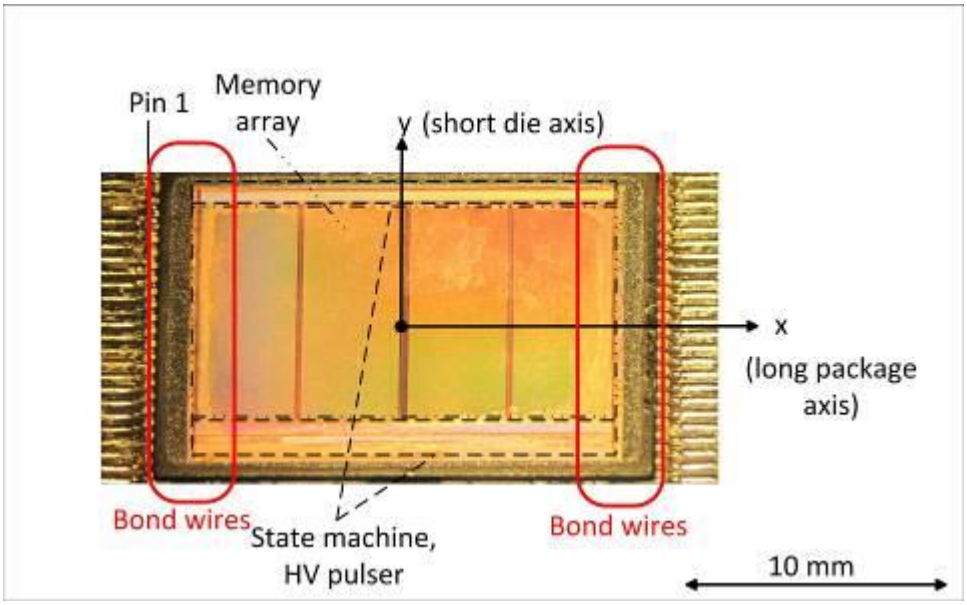

Fig. 5: Opened package of the Micron 50 nm 8-Gbit NAND-Flash with bond wires on the small sides of the TSOP1 package

5 Test procedure

5.1 Test mode and error classification

Due to the complex device structure, comprising state machines, large address, status, command and data registers, a high voltage pulser, etc. a large number of different error conditions can occur. These error conditions are classified into four main classes and several subclasses according to Fig. 6.

Static errors appear again at repeated read in contrast to dynamic errors. The transient dynamic errors are differentiated further into those which are distributed randomly over the address space and those which are clustered.

Static errors originate from the array and dynamic errors from the peripheral data path. Both kinds of spurious data errors can be handled easily with a conventional error correction scheme (Hamming, Reed-Solomon).

More challenging for the error correction are SEFIs. SEFIs are caused by hits in the control circuitry as in the state machine or in the S/P Register. Transient SEFIs disappear without the need of a device reset, unlike persistent SEFIs.

In particular the transient SEFIs are differentiated further into (i) row errors corrupting more than 100 bytes per page, (ii) block errors corrupting a series of 3…64 device pages up to the end of the respective device block and (iii) column errors corrupting the same byte position of subsequent device pages. Again, the column errors are split into those restricted or not restricted to one block.

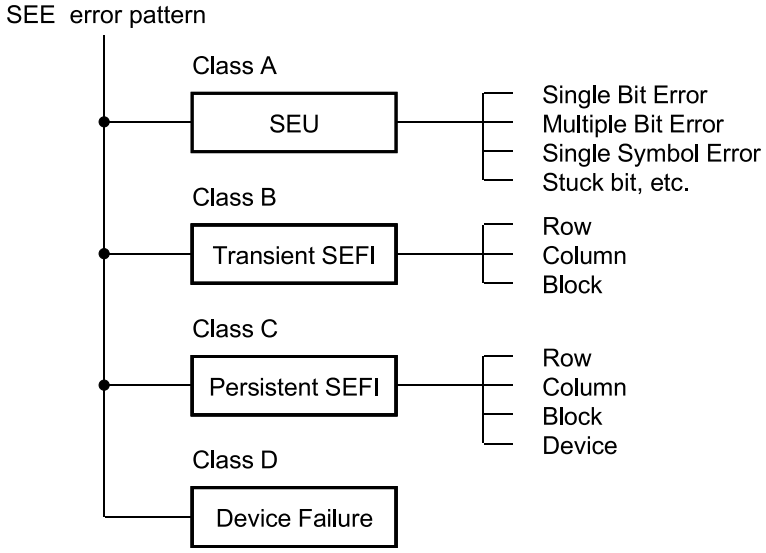

Fig. 6: Error classification scheme

For the purpose of later detailed error analysis and classification, all test vectors are stored. A quick look of the error distribution over the complete address space is displayed in real time. Fig. 7 shows an example quick look error image. Horizontal lines represent page errors, vertical lines column errors and the horizontal bar a series of block errors, which were stopped by manual power cycling.

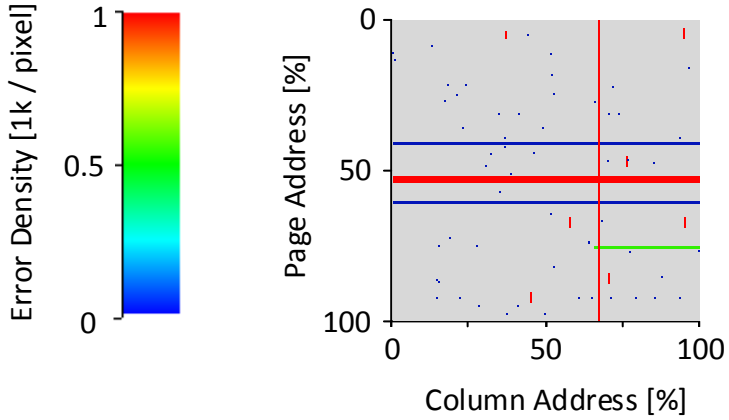

Fig. 7: Example quick look error image

6 Test Results

6.1 SEU cross section for normal ion incidence

Tab. 6 and Fig. 8 show the static random SEU cross section of the Micron 16-Gbit and 32-Gbit device with 25 nm feature size. For comparison in Fig. 8, the values for the Micron 50 nm 8-Gbit device are shown also.

Stuck bits from previous runs are subtracted from the error count.

Run IDA	Run RADEF	Run TAMU	Ion	LET	Device					Mode	Fluence	Time	Average Flux	Dose [rad]	Class A Errors			
				[MeV cm^2mg^{-1}]	Marking	Tested Blocks	Type	Date Code	Lot Code		F [cm^{-2}]	[s]	[$cm^{-2}s^{-1}$]		Stuck bits	Stuck bit source	SEU	σSEU [cm^2bit^{-1}]
3	251		N	1.8	M305	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	1.00E+07	226	4.42E+04	288			2938	4.25E-12
9	157		N	1.8	M306	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	1.01E+07	252	4.01E+04	291			4665	6.67E-12
Σ						**64**					**2.01E+07**						**7603**	**5.47E-12**
13	261		N	1.8	M412	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	1.00E+07	259	3.86E+04	288			3439	4.97E-12
17	165		N	1.8	M413	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	1.01E+07	273	3.70E+04	291			3498	5.00E-12
Σ						**64**					**2.01E+07**						**6937**	**4.99E-12**
96.a	408		Ne	3.6	M310	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	5.05E+06	174	2.90E+04	1132	71	Ar	4731	1.35E-11
100.a	412		Ne	3.6	M311	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	5.06E+06	190	2.66E+04	999	7	Ar	5036	1.44E-11
Σ						**64**					**1.01E+07**						**9767**	**1.40E-11**
88.a	400		Ne	3.6	M415	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	5.02E+06	175	2.87E+04	809	332	Ar	4748	1.37E-11
92.a	404		Ne	3.6	M414	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	5.02E+06	179	2.80E+04	3340	51	Ar	4705	1.35E-11
Σ						**64**					**1.00E+07**						**9453**	**1.36E-11**
68.a	379		Ar	10.1	M310	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	1.01E+06	169	5.98E+03	356	286	Xe	2815	4.03E-11
72.a	383		Ar	10.1	M311	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	1.01E+06	168	6.01E+03	163			3026	4.33E-11
77.a	388		Ar	10.1	M308	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	1.01E+06	151	6.69E+03	163			2809	4.02E-11
Σ						**64**					**3.03E+06**						**8650**	**4.13E-11**
78.a	389		Ar	10.1	M414	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	1.01E+06	160	6.31E+03	2388	463	Xe	2730	3.91E-11
84.a	395		Ar	10.1	M415	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	1.01E+06	143	7.06E+03	2313	1051	Xe	2715	3.88E-11
Σ						**64**					**2.02E+06**						**5445**	**3.89E-11**
33.a	280		Fe	18.5	M305	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	1.01E+06	171	5.91E+03	1467			5753	8.23E-11
37.a	284		Fe	18.5	M306	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	1.01E+06	133	7.59E+03	1460			6210	8.88E-11
Σ						**64**					**2.02E+06**						**11963**	**8.56E-11**
22.a	270		Fe	18.5	M413	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	1.01E+07	191	5.29E+04	7110			60038	8.59E-11
23.a	271		Fe	18.5	M414	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	1.00E+06	206	4.85E+03	296			5570	8.05E-11
28.a	276		Fe	18.5	M415	64	MT29F32G08ABAAAWP-IT:A	1131	BYZT5C7.21	M3a	1.00E+06	157	6.37E+03	296	170		6317	9.13E-11
Σ						**64**					**1.21E+07**						**71925**	**8.59E-11**
41.a	288		Kr	32.1	M306	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	5.01E+05	185	2.71E+03	2495	364	Fe	5641	1.63E-10
45.a	292		Kr	32.1	M305	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	5.03E+05	176	2.86E+03	2354	227	Fe	5220	1.50E-10
57.a	304		Kr	32.1	M307	64	MT29F16G08ABACAWP-IT:C	1123	BYV7W87.21	M3a	5.05E+05	192	2.63E+03				5363	1.53E-10
Σ						**64**					**1.51E+06**						**16224**	**1.55E-10**
139		266	Kr	21.8	M356	32	MT29F16G08ABACAWP-IT:C	1146	BYP5ZT9.21	M3a	1.02E+06	19	5.37E+04				3011	8.53E-11
167		293	Kr	21.8	M357	32	MT29F16G08ABACAWP-IT:C	1146	BYP5ZT9.21	M3a	1.01E+05	27	3.74E+03				281	8.04E-11
Σ						**32**					**1.12E+06**						**3292**	**8.49E-11**
53.a	300		Kr	32.1	M415	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	5.05E+05	202	2.50E+03	1181	222	Fe	5353	1.53E-10
Σ						**64**					**5.05E+05**						**5353**	**1.53E-10**
58.a	305		Xe	60	M305	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	2.01E+05	204	9.85E+02	3154	965	Kr	3821	2.75E-10
60.a	307		Xe	60	M306	64	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M3a	1.01E+05	219	4.61E+02	3148	1215	Fe	2216	3.17E-10
62.a	309		Xe	60	M310	64	MT29F16G08ABACAWP-IT:C	1123	BYV7W87.22	M3a	1.01E+05	246	4.11E+02	97			1939	2.77E-10
Σ						**64**					**4.03E+05**						**7976**	**2.86E-10**
64.a	311		Xe	60	M414	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	1.00E+05	240	4.17E+02	2129	467	Kr	1877	2.71E-10
66.a	313		Xe	60	M415	64	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M3a	1.01E+05	240	4.21E+02	2054	1141	Kr	1948	2.79E-10
Σ						**64**					**2.01E+05**						**3825**	**2.75E-10**

Tab. 6: Storage Mode M3 Test Data

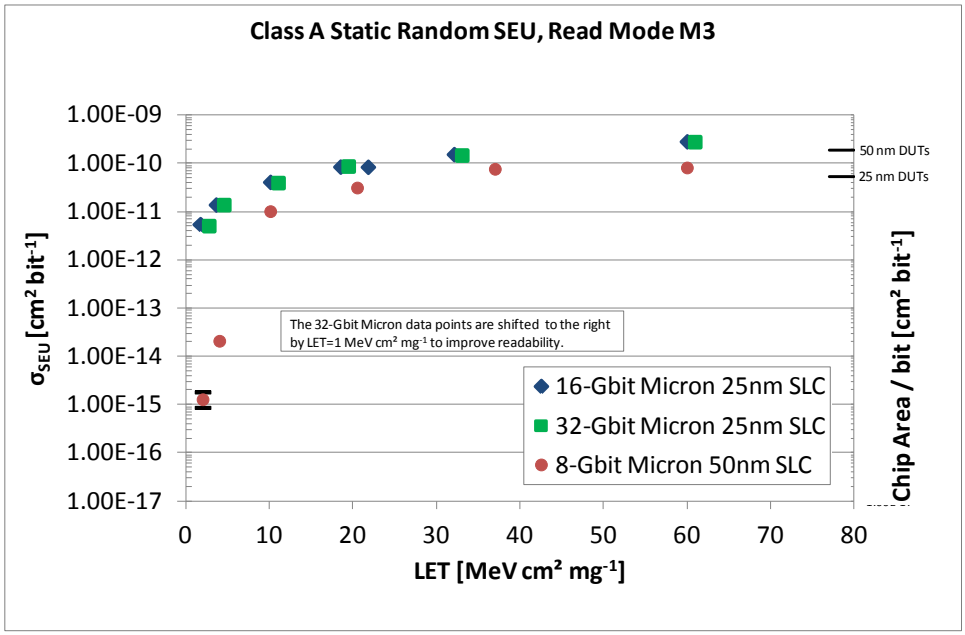

Fig. 8: Static random SEU cross section of 8-Gbit, 16-Gbit and 32-Gbit SLC NAND-Flash devices

These static random SEU results differ at low LET from the results presented by F. Irom, JPL [5], Fig. 9. The devices tested by F. Irom are of the same part number (MT29F32G08ABAAA), but of a different date code (1106).

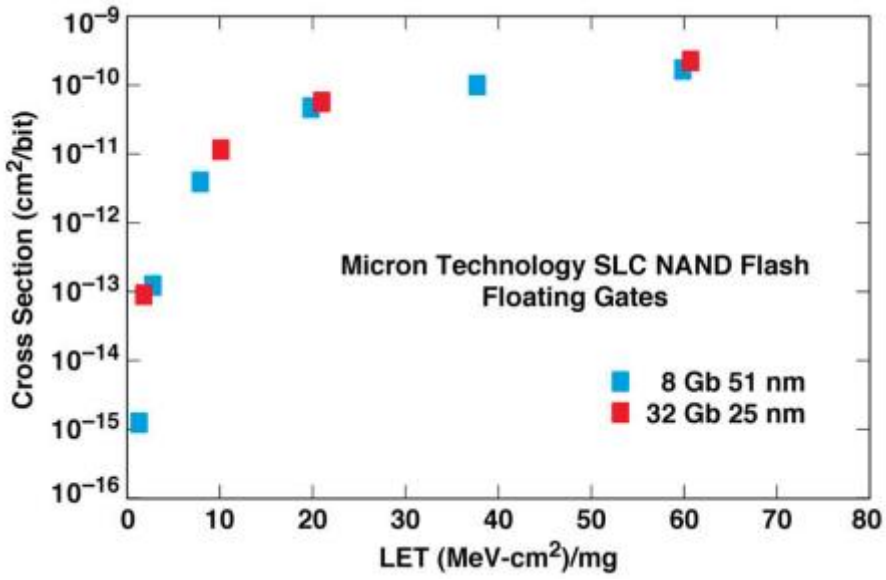

Fig. 9: SEU cross section for Micron 32-Gb SLC NAND flash memory. Measurements were performed at RADEF. SEU cross section for Micron Technology 8-Gb SLC is shown for comparison. [5, Fig. 1]

Fig. 10 compares the SEU cross sections gained by JPL and IDA. For unknown reasons, the cross section differs by nearly two orders of magnitude at low LET. The SLC cross section measured by IDA is nearly congruent with the MLC cross section measured by JPL.

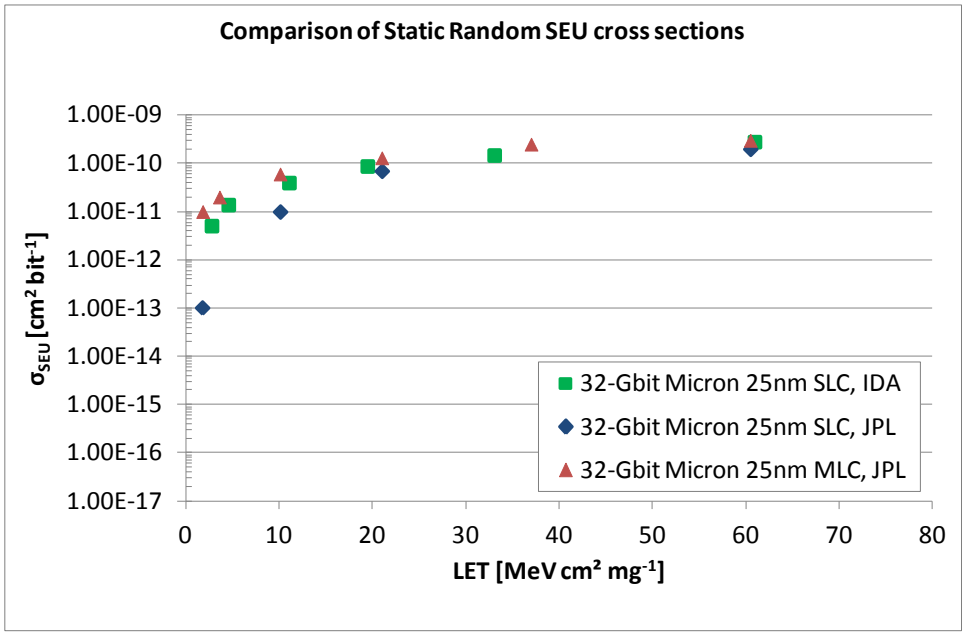

Fig. 10: Comparison of SEU cross sections for Micron 32-Gbit SLC and MLC parts tested by JPL[5] and IDA

The static SEU cross sections of the 16-Gbit and the 32-Gbit NAND-Flash derived by IDA are nearly identical (Fig. 8). At low LET, they exceed the SEU cross-section of the Micron 8-Gbit NAND-Flash by several orders of magnitude. In particular, the IDA cross section curve results in a threshold LET substantially lower than the lowest LET of the available RADEF ion cocktail (nitrogen, 1.8 MeV cm^2/mg). At high LET, the difference between cross sections is reduced to less than one order of magnitude. The area of the 16-Gbit chip is 0.9 cm^2, i.e., 5.24×10^{-11} cm^2/bit = (72 nm)^2/bit. The measured random SEU cross section exceeds this value, even at LET = 10 MeV cm^2/mg. This indicates that single hits induce multiple random SEUs. The inspection of the error records revealed that, in most cases, the same bit in the same byte of adjacent rows is corrupted. Multi-bit errors in the same byte are rare. Fig. 11 shows the increase of the share of those adjacent row SEUs with LET.

Stuck bits are noted in increasing number at higher LET – about 20% of the random SEUs at xenon.

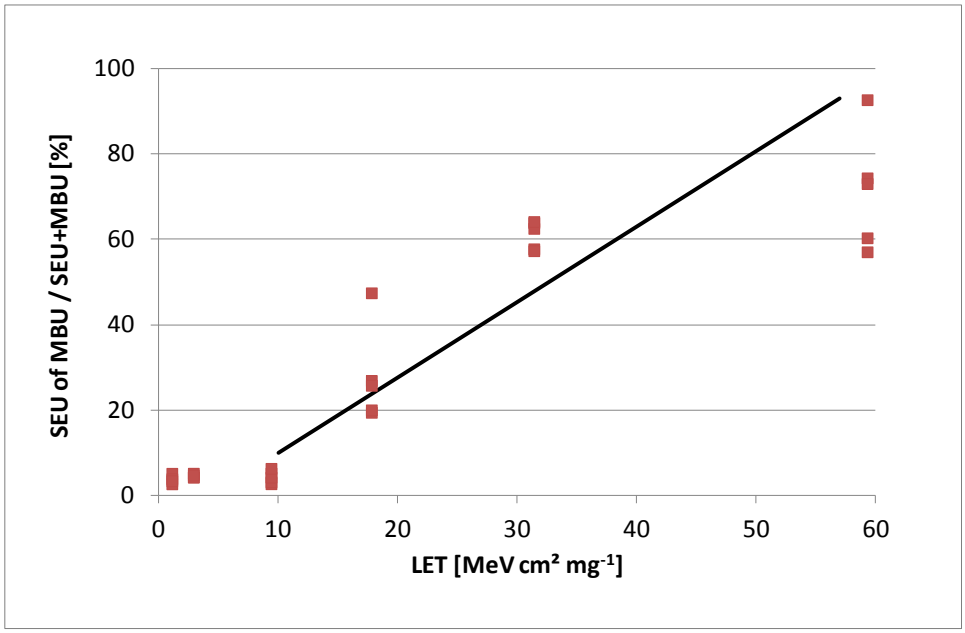

Fig. 11: Share of adjacent row SEUs

6.2 SEFI cross section

The SEFI cross sections have been measured individually for each mode. As the following section shows the influence of the respective mode is rather minor. Mode 5 delivers nearly the same cross section than Mode 1 in contrast to early NAND-Flash generations.

6.2.1 Read Mode M2R

Both, Transient (Class B) SEFIs and Persistent (Class C) SEFIs occurred in Read Mode.

The respective test data are shown in Tab. 7.

The SEFIs are classified into Column Errors, Row Errors and Block Errors.

Fig. 12, Fig. 13 and Fig. 14 show the Class B column error (CE), Class B row error (RE) and Class B block error (BE) cross section versus LET, Fig. 15 the combined Class B cross section of all three SEFI types.

Fig. 16, Fig. 17 and Fig. 18 show the Class C CE, Class C RE and Class C BE cross section versus LET, Fig. 19 the combined Class C cross section of all three SEFI types.

Fig. 20 shows the combined Class B+C cross section of all three SEFI types.

All row errors are transient (Fig. 13, Fig. 17) and all column errors are persistent (Fig. 12, Fig. 16).

As Fig. 16 shows one out of 2000 xenon ions generates a Class C Persistent SEFI.

Run IDA	Run RADEF	Ion	LET [MeV cm²mg⁻¹]	Device: Marking	Tested Blocks	Type	Date Code	Lot Code	Mode	Fluence F [cm⁻²]	Time [s]	Average Flux [cm⁻²s⁻¹]	Dose [rad]	Class B Errors: CE	RE	BE	σCE [cm²die⁻¹]	σRE [cm²die⁻¹]	σBE [cm²die⁻¹]	σClassB [cm²die⁻¹]	Class C Errors: CE	RE	BE	σCE [cm²die⁻¹]	σRE [cm²die⁻¹]	σBE [cm²die⁻¹]	σClassC [cm²die⁻¹]	σClassB+C [cm²die⁻¹]
5	253	N	1.8	M305	777	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	1.01E+07	231	4.37E+04	589				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08
12	260	N	1.8	M306	770	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	1.01E+07	231	4.37E+04	1161				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08
Σ					**773.5**					**2.02E+07**				**0**	**0**	**0**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**	**0**	**0**	**0**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**
16	264	N	1.8	M412	905	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	1.00E+07	275	3.64E+04	1155				< 1.00E-07	< 1.00E-07	< 1.00E-07	< 1.00E-07				< 1.00E-07	< 1.00E-07	< 1.00E-07	< 1.00E-07	< 1.00E-07
20	268	N	1.8	M413	601	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	1.01E+07	175	5.77E+04	1161				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08
Σ					**753**					**2.01E+07**				**0**	**0**	**0**	**< 4.98E-08**	**< 4.98E-08**	**< 4.98E-08**	**< 4.98E-08**	**0**	**0**	**0**	**< 4.98E-08**	**< 4.98E-08**	**< 4.98E-08**	**< 4.98E-08**	**< 4.98E-08**
99	411	Ne	3.6	M310	629	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	5.04E+06	186	2.71E+04	2003				< 1.98E-07	< 1.98E-07	< 1.98E-07	< 1.98E-07			2	< 1.98E-07	< 1.98E-07	3.97E-07	3.97E-07	3.97E-07
103	415	Ne	3.6	M311	645	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	5.02E+06	188	2.67E+04	1867				< 1.99E-07	< 1.99E-07	< 1.99E-07	< 1.99E-07			3	< 1.99E-07	< 1.99E-07	5.98E-07	5.98E-07	5.98E-07
Σ					**637**					**1.01E+07**				**0**	**0**	**0**	**< 9.94E-08**	**< 9.94E-08**	**< 9.94E-08**	**< 9.94E-08**	**0**	**0**	**5**	**< 9.94E-08**	**< 9.94E-08**	**4.97E-07**	**4.97E-07**	**4.97E-07**
91	403	Ne	3.6	M415	605	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	5.04E+06	176	2.86E+04	454				< 1.98E-07	< 1.98E-07	< 1.98E-07	< 1.98E-07			3	< 1.98E-07	< 1.98E-07	5.95E-07	5.95E-07	5.95E-07
95	407	Ne	3.6	M414	606	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	5.06E+06	177	2.86E+04	4211				< 1.98E-07	< 1.98E-07	< 1.98E-07	< 1.98E-07			2	< 1.98E-07	< 1.98E-07	3.95E-07	3.95E-07	3.95E-07
Σ					**605.5**					**1.01E+07**				**0**	**0**	**0**	**< 9.90E-08**	**< 9.90E-08**	**< 9.90E-08**	**< 9.90E-08**	**0**	**0**	**5**	**< 9.90E-08**	**< 9.90E-08**	**4.95E-07**	**4.95E-07**	**4.95E-07**
71	382	Ar	10.1	M310	556	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	1.00E+06	170	5.88E+03	841		1	1	< 1.00E-06	1.00E-06	1.00E-06	2.00E-06	37		3	3.70E-05	< 1.00E-06	3.00E-06	4.00E-05	4.20E-05
76	387	Ar	10.1	M311	547	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	1.01E+06	157	6.43E+03	708		2	2	< 9.90E-07	1.98E-06	1.98E-06	3.96E-06	33		2	3.27E-05	< 9.90E-07	1.98E-06	3.47E-05	3.86E-05
Σ					**551.5**					**2.01E+06**				**0**	**3**	**3**	**< 4.98E-07**	**1.49E-06**	**1.49E-06**	**2.99E-06**	**70**	**0**	**5**	**3.48E-05**	**< 4.98E-07**	**2.49E-06**	**3.73E-05**	**4.03E-05**
83	194	Ar	10.1	M414	606	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	1.01E+06	177	5.71E+03	3051		5		< 9.90E-07	4.95E-06	< 9.90E-07	4.95E-06	25		1	2.48E-05	< 9.90E-07	9.90E-07	2.57E-05	3.07E-05
87	398	Ar	10.1	M415	492	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	1.00E+06	140	7.14E+03	355		2	1	< 1.00E-06	2.00E-06	1.00E-06	3.00E-06	36		1	3.60E-05	< 1.00E-06	1.00E-06	3.70E-05	4.00E-05
Σ					**549**					**2.01E+06**				**0**	**7**	**1**	**< 4.98E-07**	**3.48E-06**	**4.98E-07**	**3.98E-06**	**61**	**0**	**2**	**3.03E-05**	**< 4.98E-07**	**9.95E-07**	**3.13E-05**	**3.53E-05**
36	283	Fe	18.5	M305	505	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	1.02E+06	132	7.73E+03	2095		4	1	< 9.80E-07	3.92E-06	9.80E-07	4.90E-06	80		2	7.84E-05	< 9.80E-07	1.96E-06	8.04E-05	8.53E-05
40	287	Fe	18.5	M306	577	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	1.00E+06	165	6.06E+03	2237		14		< 1.00E-06	1.40E-05	< 1.00E-06	1.40E-05	80			8.00E-05	< 1.00E-06	< 1.00E-06	8.00E-05	9.40E-05
Σ					**541**					**2.02E+06**				**0**	**18**	**1**	**< 4.95E-07**	**8.91E-06**	**4.95E-07**	**9.41E-06**	**160**	**0**	**2**	**7.92E-05**	**< 4.95E-07**	**9.90E-07**	**8.02E-05**	**8.96E-05**
27	275	Fe	18.5	M414	489	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	1.01E+06	121	8.35E+03	1170		2	1	< 9.90E-07	1.98E-06	9.90E-07	2.97E-06	56		2	5.54E-05	< 9.90E-07	1.98E-06	5.74E-05	6.04E-05
32	279	Fe	18.5	M415	606	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	1.01E+06	177	5.71E+03	922		12	2	< 9.90E-07	1.19E-05	1.98E-06	1.39E-05	60		2	5.94E-05	< 9.90E-07	1.98E-06	6.14E-05	7.52E-05
Σ					**547.5**					**2.02E+06**				**0**	**14**	**3**	**< 4.95E-07**	**6.93E-06**	**1.49E-06**	**8.42E-06**	**116**	**0**	**4**	**5.74E-05**	**< 4.95E-07**	**1.98E-06**	**5.94E-05**	**6.78E-05**
44	291	Kr	32.1	M306	661	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	5.03E+05	194	2.59E+03	3051		5		< 1.99E-06	9.94E-06	< 1.99E-06	9.94E-06	101			2.01E-04	< 1.99E-06	< 1.99E-06	2.01E-04	2.11E-04
48	295	Kr	32.1	M305	633	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	5.03E+05	186	2.70E+03	2961		2		< 1.99E-06	3.98E-06	< 1.99E-06	3.98E-06	73		2	1.45E-04	< 1.99E-06	3.98E-06	1.49E-04	1.53E-04
Σ					**647**					**1.01E+06**				**0**	**7**	**0**	**< 9.94E-07**	**6.96E-06**	**< 9.94E-07**	**6.96E-06**	**174**	**0**	**2**	**1.73E-04**	**< 9.94E-07**	**1.99E-06**	**1.75E-04**	**1.82E-04**
52	299	Kr	32.1	M414	715	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	5.02E+05	212	2.37E+03	2033		9		< 1.99E-06	1.79E-05	< 1.99E-06	1.79E-05	96			1.91E-04	< 1.99E-06	< 1.99E-06	1.91E-04	2.09E-04
56	303	Kr	32.1	M415	708	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	5.05E+05	209	2.42E+03	1957		7	1	< 1.98E-06	1.39E-05	1.98E-06	1.58E-05	83		4	1.64E-04	< 1.98E-06	7.92E-06	1.72E-04	1.88E-04
Σ					**711.5**					**1.01E+06**				**0**	**16**	**1**	**< 9.93E-07**	**1.59E-05**	**9.93E-07**	**1.69E-05**	**179**	**0**	**4**	**1.78E-04**	**< 9.93E-07**	**3.97E-06**	**1.82E-04**	**1.99E-04**
63	310	Xe	60	M310	818	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M2R	1.00E+05	244	4.10E+02	193		1		< 1.00E-05	1.00E-05	< 1.00E-05	1.00E-05	46		2	4.60E-04	< 1.00E-05	2.00E-05	4.80E-04	4.90E-04
65	312	Xe	60	M414	854	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	1.00E+05	260	3.85E+02	2225		1	2	< 1.00E-05	1.00E-05	2.00E-05	3.00E-05	29		1	2.90E-04	< 1.00E-05	1.00E-05	3.00E-04	3.30E-04
67	314	Xe	60	M415	830	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M2R	1.00E+05	249	4.02E+02	2150				< 1.00E-05	< 1.00E-05	< 1.00E-05	< 1.00E-05	33			3.30E-04	< 1.00E-05	< 1.00E-05	3.30E-04	3.30E-04
Σ										**2.00E+05**				**0**	**1**	**2**	**< 5.00E-06**	**5.00E-06**	**1.00E-05**	**1.50E-05**	**62**	**0**	**1**	**3.10E-04**	**< 5.00E-06**	**5.00E-06**	**3.15E-04**	**3.30E-04**

Tab. 7: Read Mode M2R Test Data

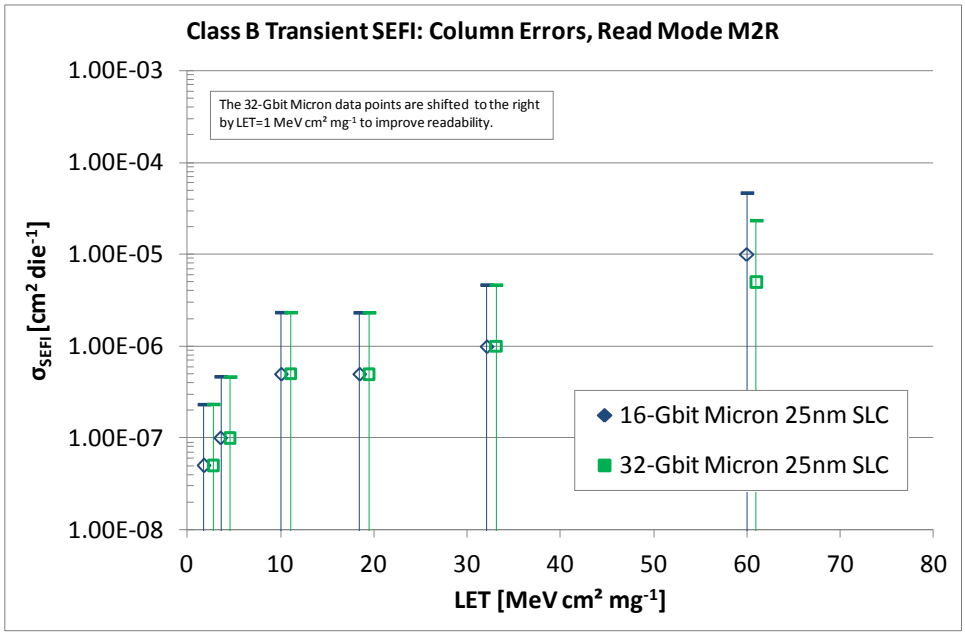

Fig. 12: Class B Transient SEFI cross section in read mode M2R, Column Errors, open symbols indicate "no DF until the applied fluence"
Please note: no column errors where observed.

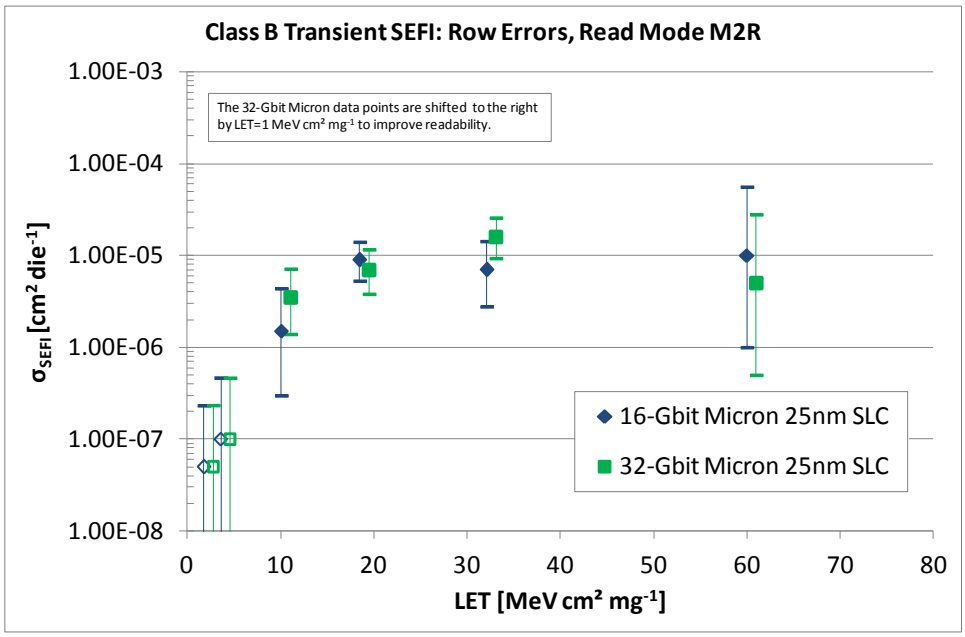

Fig. 13: Class B Transient SEFI cross section in read mode M2R, Row Errors

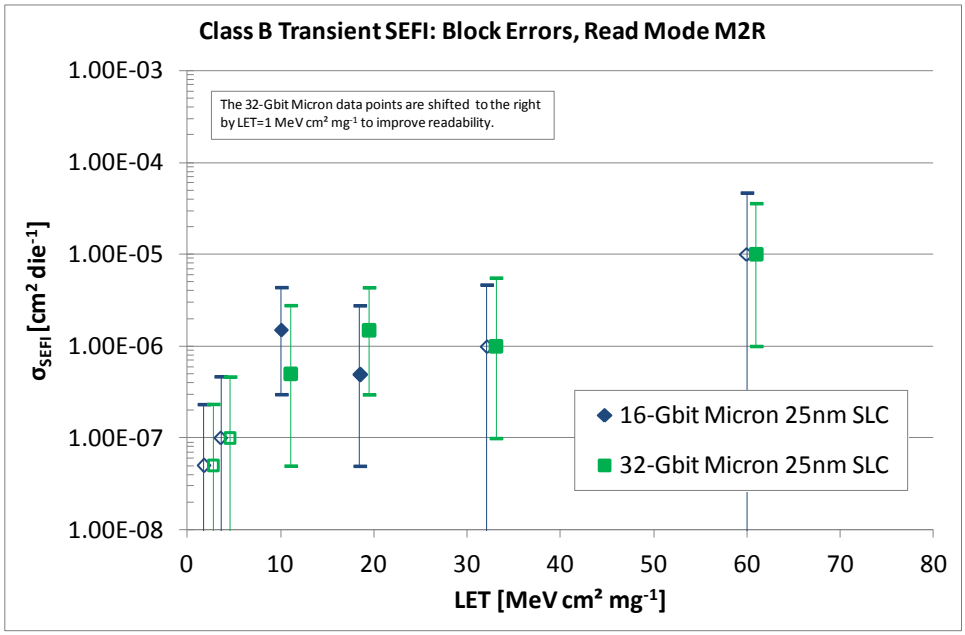

Fig. 14: Class B Transient SEFI cross section in read mode M2R, Block Errors

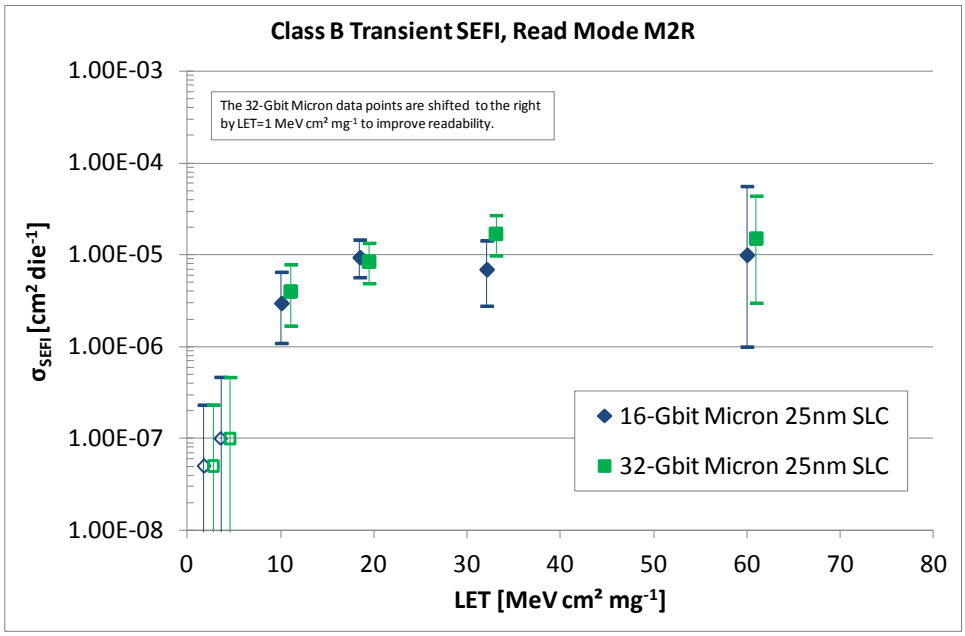

Fig. 15: Class B Transient SEFI cross section in read mode M2R, all Errors

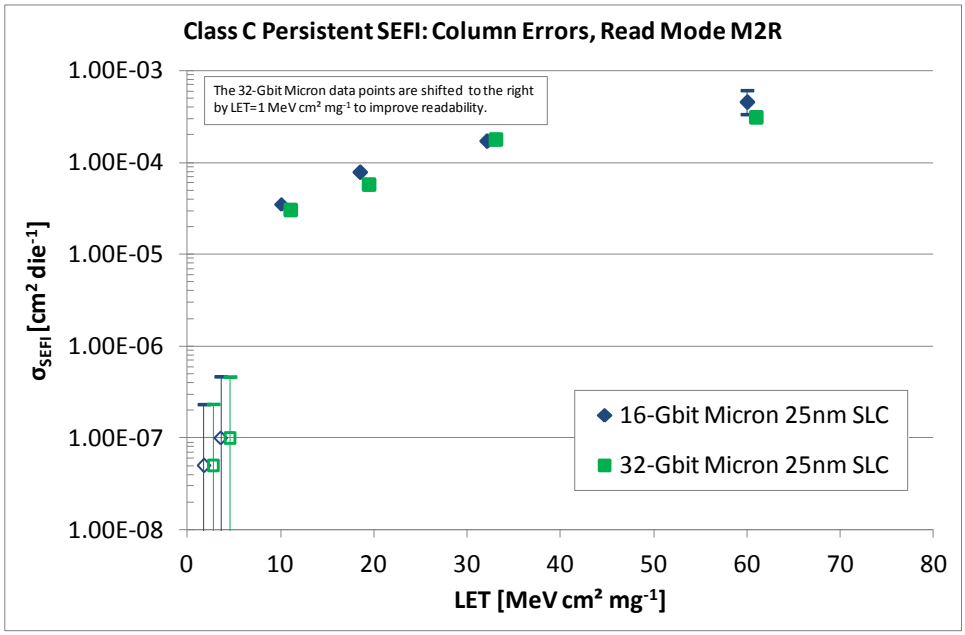

Fig. 16: Class C Persistent SEFI cross section in read mode M2R, Column Errors

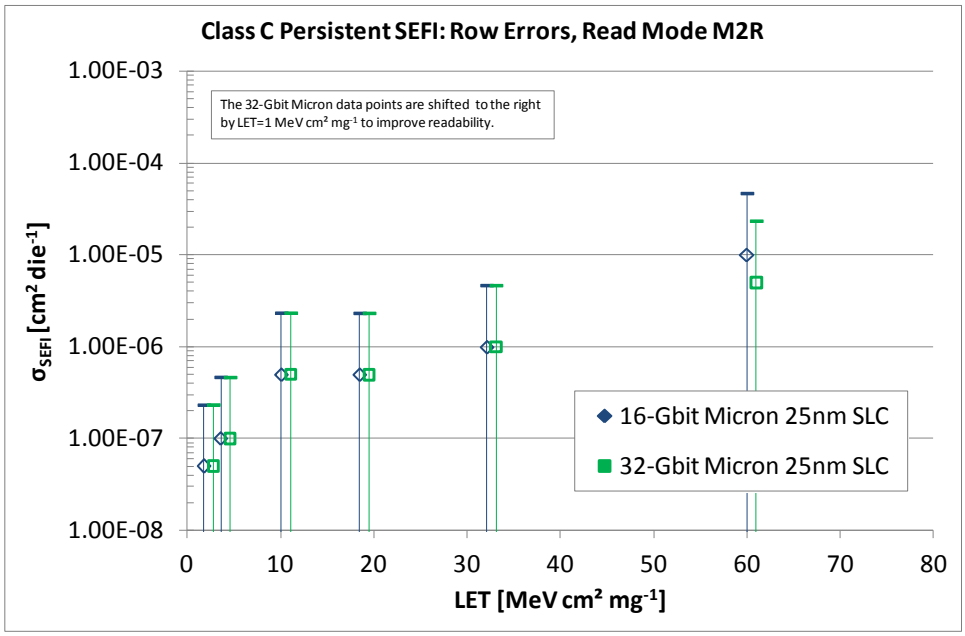

Fig. 17: Class C Persistent SEFI cross section in read mode M2R, Row Errors
Please note: no row errors where observed.

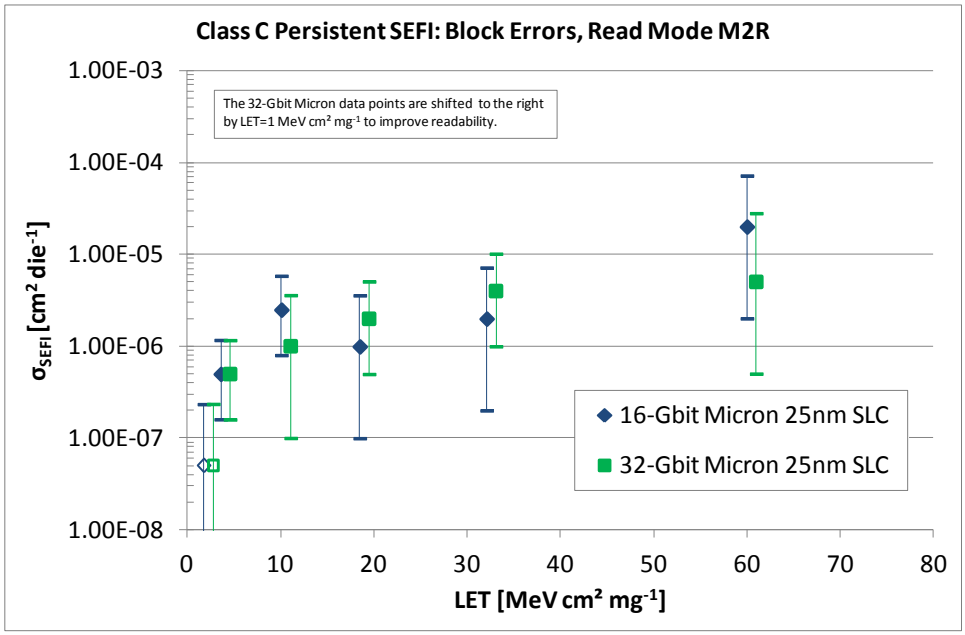

Fig. 18: Class C Persistent SEFI cross section in read mode M2R, Block Errors

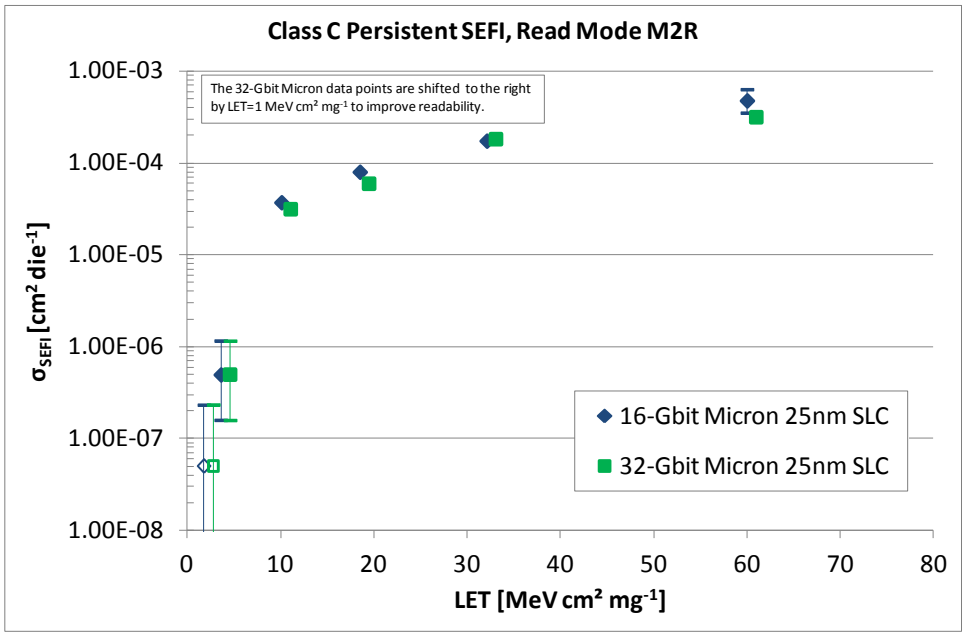

Fig. 19: Class C Persistent SEFI cross section in read mode M2R, all Errors

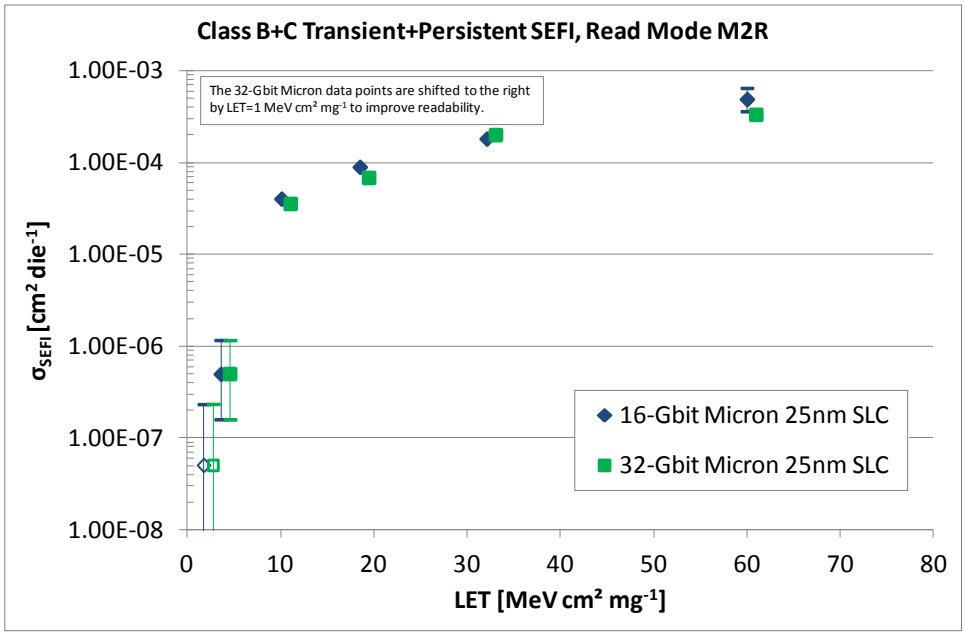

Fig. 20: Class B+C Transient+Persistent SEFI cross section in read mode M2R, all Errors

6.2.2 Marching Mode with Power Cycle M5

In contrast to Read Mode Marching Mode implies Write and Erase operations, i.e. operations with activated high voltage generator.

Both, Transient (Class B) SEFIs and Persistent (Class C) SEFIs occurred in Marching Mode with power cycle (M5).

The respective test data are shown in Tab. 8.

The SEFIs are classified into Column Errors, Row Errors and Block Errors.

Fig. 21, Fig. 22 and Fig. 23 show the Class B+C column error (CE), row error (RE) and block error (BE) cross section versus LET, Fig. 24 the combined Class B+C cross section of all three SEFI types.

Each Marching step takes more time than a write or read step and therefore an only shorter address range could be tested. Due to the limited SEFI count both classes were accumulated.

Run IDA	Run RADEF	Ion	LET [MeV cm^{2}mg^{-1}]	Device Marking	Tested Blocks	Type	Date Code	Lot Code	Mode	Fluence F [cm^{-2}]	Time [s]	Average Flux [cm^{-2}s^{-1}]	Dose [rad]	Class B+C Errors CE	RE	BE	σ_{CE} [cm^{2}die^{-1}]	σ_{RE} [cm^{2}die^{-1}]	σ_{BE} [cm^{2}die^{-1}]	$\sigma_{ClassB+C}$ [cm^{2}die^{-1}]
7	255	N	1.8	M305	117	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	1.00E+07	245	4.08E+04	1168	2			2.00E-07	< 1.00E-07	< 1.00E-07	2.00E-07
11	259	N	1.8	M306	116	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	1.00E+07	259	3.86E+04	870				< 1.00E-07	< 1.00E-07	< 1.00E-07	< 1.00E-07
Σ					**116.5**					**2.00E+07**				**2**	**0**	**0**	**1.00E-07**	**< 5.00E-08**	**< 5.00E-08**	**1.00E-07**
15	263	N	1.8	M412	126	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	1.01E+07	264	3.83E+04	867				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08
19	267	N	1.8	M413	97	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	1.01E+07	204	4.95E+04	870				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08
Σ					**111.5**					**2.02E+07**				**0**	**0**	**0**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**
98	410	Ne	3.6	M310	85	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	5.02E+06	178	2.82E+04	1712				< 1.99E-07	< 1.99E-07	< 1.99E-07	< 1.99E-07
102	414	Ne	3.6	M311	87	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	5.03E+06	184	2.73E+04	1578				< 1.99E-07	< 1.99E-07	< 1.99E-07	< 1.99E-07
Σ					**86**					**1.01E+07**				**0**	**0**	**0**	**< 9.95E-08**	**< 9.95E-08**	**< 9.95E-08**	**< 9.95E-08**
90	402	Ne	3.6	M415	82	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	5.05E+06	175	2.89E+04	1132				< 1.98E-07	< 1.98E-07	< 1.98E-07	< 1.98E-07
94	406	Ne	3.6	M414	84	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	5.03E+06	178	2.83E+04	3920				< 1.99E-07	< 1.99E-07	< 1.99E-07	< 1.99E-07
Σ					**83**					**1.01E+07**				**0**	**0**	**0**	**< 9.92E-08**	**< 9.92E-08**	**< 9.92E-08**	**< 9.92E-08**
70	381	Ar	10.1	M310	79	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	9.93E+05	181	5.49E+03	680	21	1		2.11E-05	1.01E-06	< 1.01E-06	2.22E-05
75	386	Ar	10.1	M311	83	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	1.00E+06	190	5.26E+03	545	19	2		1.90E-05	2.00E-06	< 1.00E-06	2.10E-05
Σ					**81**					**1.99E+06**				**40**	**3**	**0**	**2.01E-05**	**1.51E-06**	**< 5.02E-07**	**2.16E-05**
82	393	Ar	10.1	M414	75	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	1.01E+06	158	6.39E+03	2888	23	1		2.28E-05	9.90E-07	< 9.90E-07	2.38E-05
86	397	Ar	10.1	M415	68	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	1.01E+06	141	7.16E+03	356	11	1		1.09E-05	9.90E-07	< 9.90E-07	1.19E-05
Σ					**71.5**					**2.02E+06**				**34**	**2**	**0**	**1.68E-05**	**9.90E-07**	**< 4.95E-07**	**1.78E-05**
35	282	Fe	18.5	M305	41	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	6.70E+05	86	7.79E+03	1793	41	1		6.12E-05	1.49E-06	< 1.49E-06	6.27E-05
39	286	Fe	18.5	M306	63	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	1.01E+06	138	7.32E+03	1941	45	2		4.46E-05	1.98E-06	< 9.90E-07	4.65E-05
Σ					**52**					**1.68E+06**				**86**	**3**	**0**	**5.12E-05**	**1.79E-06**	**< 5.95E-07**	**5.30E-05**
26	274	Fe	18.5	M414	83	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	1.00E+06	187	5.35E+03	871	53	7		5.30E-05	7.00E-06	< 1.00E-06	6.00E-05
31	278	Fe	18.5	M415	65	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	7.61E+05	144	5.28E+03	623	31	2		4.07E-05	2.63E-06	< 1.31E-06	4.34E-05
Σ					**74**					**1.76E+06**				**84**	**9**	**0**	**4.77E-05**	**5.11E-06**	**< 5.68E-07**	**5.28E-05**
43	290	Kr	32.1	M306	87	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	5.03E+05	183	2.75E+03	2793	84	6		1.67E-04	1.19E-05	< 1.99E-06	1.79E-04
47	294	Kr	32.1	M305	95	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	5.02E+05	199	2.52E+03	2702	74	7	1	1.47E-04	1.39E-05	1.99E-06	1.63E-04
Σ					**91**					**1.01E+06**				**158**	**13**	**1**	**1.57E-04**	**1.29E-05**	**9.95E-07**	**1.71E-04**
51	298	Kr	32.1	M414	66	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	3.85E+05	141	2.73E+03	1775	50	4		1.30E-04	1.04E-05	< 2.60E-06	1.40E-04
55	302	Kr	32.1	M415	105	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M5	5.04E+05	221	2.28E+03	1697	55	5		1.09E-04	9.92E-06	< 1.98E-06	1.19E-04
Σ					**85.5**					**8.89E+05**				**105**	**9**	**0**	**1.18E-04**	**1.01E-05**	**< 1.12E-06**	**1.28E-04**
61*	308	Xe	60	M306	47	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M5	4.34E+04	98	4.43E+02	3190	14	4		3.23E-04	9.22E-05	< 2.30E-05	4.15E-04

* Destructive Failure @ F = 4.3E4 cm-2

Tab. 8: Marching Mode with Power Cycle M5 Test Data

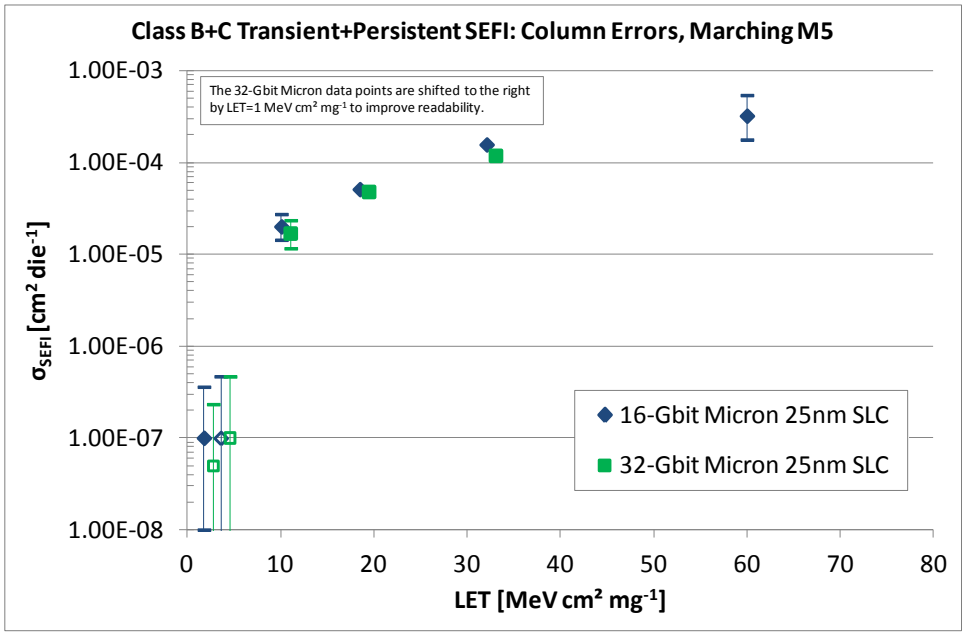

Fig. 21: Class B+C Transient+Persistent SEFI cross section in marching mode M5, Column Errors

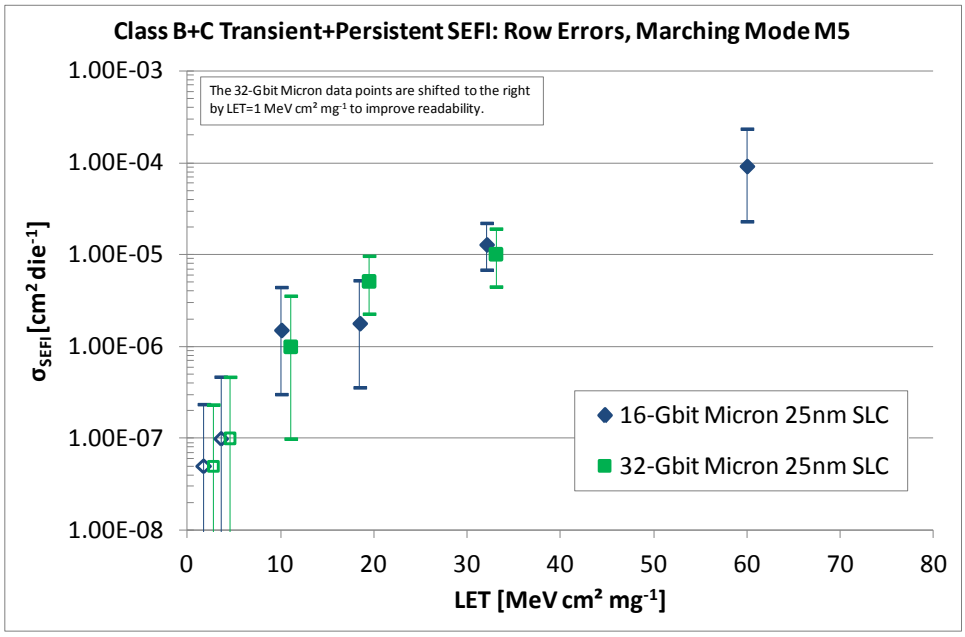

Fig. 22: Class B+C Transient+Persistent SEFI cross section in marching mode M5, Row Errors

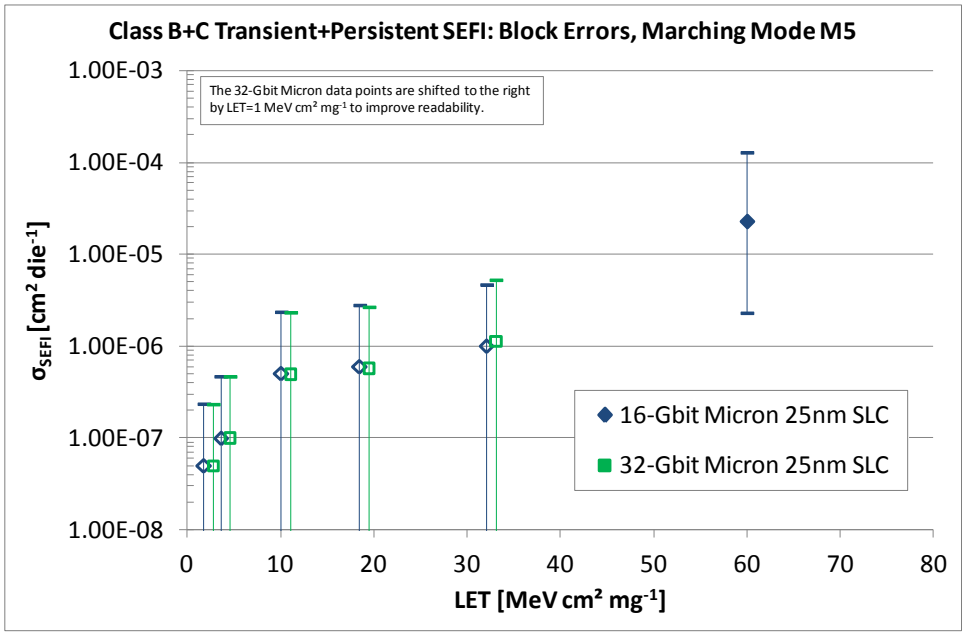

Fig. 23: Class B+C Transient+Persistent SEFI cross section in marching mode M5, Block Errors

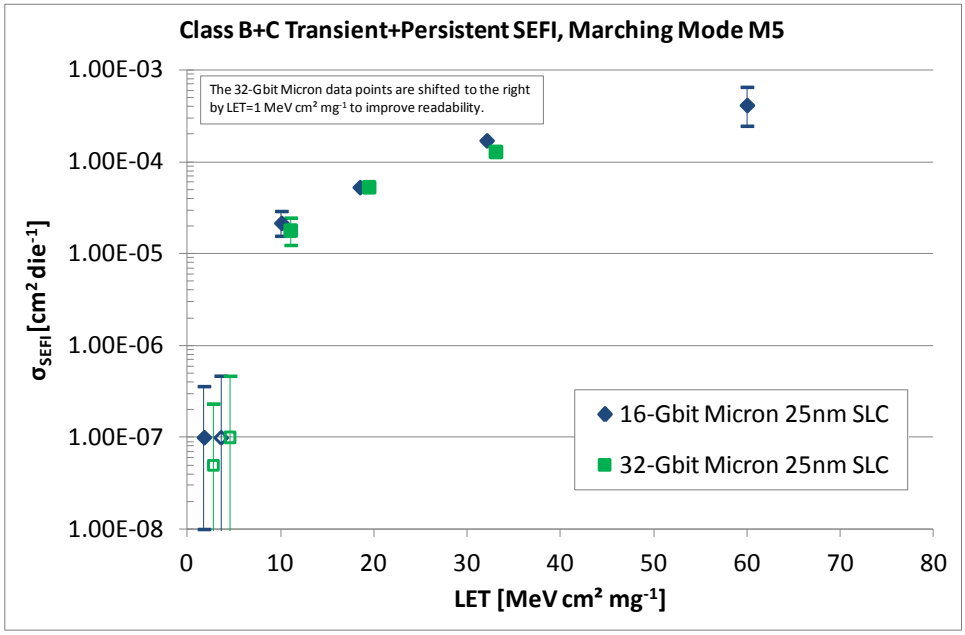

Fig. 24: Class B+C Transient+Persistent SEFI cross section in marching mode M5, all Errors

6.2.3 Marching Mode without Power Cycle M1

Both, Transient (Class B) SEFIs and Persistent (Class C) SEFIs occurred in Marching Mode without power cycle (M1).

The respective test data are shown in Tab. 9.

The SEFIs are classified into Column Errors, Row Errors and Block Errors.

Fig. 25, Fig. 26 and Fig. 27 show the Class B+C column error (CE), row error (RE) and block error (BE) cross section versus LET, Fig. 28 the combined Class B+C cross section of all three SEFI types.

Run IDA	Run RADEF	Ion	LET [MeV cm²mg⁻¹]	Device: Marking	Tested Blocks	Type	Date Code	Lot Code	Mode	Fluence F [cm⁻²]	Time [s]	Average Flux [cm⁻²s⁻¹]	Dose [rad]	Class B+C Errors: CE	RE	BE	σ_{CE} [cm²die⁻¹]	σ_{RE} [cm²die⁻¹]	σ_{BE} [cm²die⁻¹]	$\sigma_{ClassB+C}$ [cm²die⁻¹]
6	254	N	1.8	M305	167	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	1.01E+07	233	4.33E+04	880				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08
10	258	N	1.8	M306	163	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	1.01E+07	235	4.30E+04	582				< 9.90E-08	< 9.90E-08	< 9.90E-08	< 9.90E-08
Σ					**165**					**2.02E+07**				**0**	**0**	**0**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**	**< 4.95E-08**
14	262	N	1.8	M412	187	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	1.00E+07	283	3.53E+04	576				< 1.00E-07	< 1.00E-07	< 1.00E-07	< 1.00E-07
18	266	N	1.8	M413	205	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	1.00E+07	291	3.44E+04	579				< 1.00E-07	< 1.00E-07	< 1.00E-07	< 1.00E-07
Σ					**196**					**2.00E+07**				**0**	**0**	**0**	**< 5.00E-08**	**< 5.00E-08**	**< 5.00E-08**	**< 5.00E-08**
97	409	Ne	3.6	M310	123	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	5.05E+06	173	2.92E+04	1423				< 1.98E-07	< 1.98E-07	< 1.98E-07	< 1.98E-07
101	413	Ne	3.6	M311	131	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	5.02E+06	186	2.70E+04	1288				< 1.99E-07	< 1.99E-07	< 1.99E-07	< 1.99E-07
Σ					**127**					**1.01E+07**				**0**	**0**	**0**	**< 9.93E-08**	**< 9.93E-08**	**< 9.93E-08**	**< 9.93E-08**
89	401	Ne	3.6	M415	122	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	5.05E+06	174	2.90E+04	1132				< 1.98E-07	< 1.98E-07	< 1.98E-07	< 1.98E-07
93	405	Ne	3.6	M414	123	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	5.03E+06	177	2.84E+04	3630				< 1.99E-07	< 1.99E-07	< 1.99E-07	< 1.99E-07
Σ					**122.5**					**1.01E+07**				**0**	**0**	**0**	**< 9.92E-08**	**< 9.92E-08**	**< 9.92E-08**	**< 9.92E-08**
69	380	Ar	10.1	M310	120	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	1.01E+06	171	5.91E+03	519	29	3		2.87E-05	2.97E-06	< 9.90E-07	3.17E-05
74	385	Ar	10.1	M311	105	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	1.01E+06	145	6.97E+03	383	25	4		2.48E-05	3.96E-06	< 9.90E-07	2.87E-05
Σ					**112.5**					**2.02E+06**				**54**	**7**	**0**	**2.67E-05**	**3.47E-06**	**< 4.95E-07**	**3.02E-05**
79	390	Ar	10.1	M414	146	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	9.28E+05	219	4.24E+03	2538	5			5.39E-06	< 1.08E-06	< 1.08E-06	5.39E-06
85	396	Ar	10.1	M415	94	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	9.71E+05	136	7.14E+03	157	16			1.65E-05	< 1.03E-06	< 1.03E-06	1.65E-05
Σ					**120**					**1.90E+06**				**21**	**0**	**0**	**1.11E-05**	**< 5.27E-07**	**< 5.27E-07**	**1.11E-05**
34	281	Fe	18.5	M305	38	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	4.34E+05	54	8.04E+03	1595	21			4.84E-05	< 2.30E-06	< 2.30E-06	4.84E-05
38	285	Fe	18.5	M306	56	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	6.17E+05	79	7.81E+03	1642	39	2		6.32E-05	3.24E-06	< 1.62E-06	6.65E-05
Σ					**47**					**1.05E+06**				**60**	**2**	**0**	**5.71E-05**	**1.90E-06**	**< 9.51E-07**	**5.90E-05**
24	272	Fe	18.5	M414	29	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	2.29E+05	40	5.73E+03	364	6			2.62E-05	< 4.37E-06	< 4.37E-06	2.62E-05
29	277	Fe	18.5	M415	41	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	3.43E+05	58	5.91E+03	398	11			3.21E-05	< 2.92E-06	< 2.92E-06	3.21E-05
Σ					**35**					**5.72E+05**				**17**	**0**	**0**	**2.97E-05**	**< 1.75E-06**	**< 1.75E-06**	**2.97E-05**
42	289	Kr	32.1	M306	22	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	7.80E+04	26	3.00E+03	2535	5			6.41E-05	< 1.28E-05	< 1.28E-05	6.41E-05
46	293	Kr	32.1	M305	54	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	1.77E+05	74	2.39E+03	2445	16	2		9.04E-05	1.13E-05	< 5.65E-06	1.02E-04
Σ					**38**					**2.55E+05**				**21**	**2**	**0**	**8.24E-05**	**7.84E-06**	**< 3.92E-06**	**9.02E-05**
50	297	Kr	32.1	M414	78	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	2.90E+05	114	2.54E+03	1577	16	2		5.52E-05	6.90E-06	< 3.45E-06	6.21E-05
54	301	Kr	32.1	M415	137	MT29F32G08ABAAAWP-IT:A	1130	BYZT5C7.21	M1	5.01E+05	193	2.60E+03	1438	65	5		1.30E-04	9.98E-06	< 2.00E-06	1.40E-04
Σ					**107.5**					**7.91E+05**				**81**	**7**	**0**	**1.02E-04**	**8.85E-06**	**< 1.26E-06**	**1.11E-04**
59*	306	Xe	60	M305	57	MT29F16G08ABACAWP-IT:C	1122	BYV7W87.21	M1	8.51E+04	83	1.03E+03	3235	3	3		3.53E-05	3.53E-05	< 1.18E-05	7.05E-05

* Destructive Failure @ F = 8.5E4 cm-2

Tab. 9: Marching Mode without Power Cycle M1 Test Data

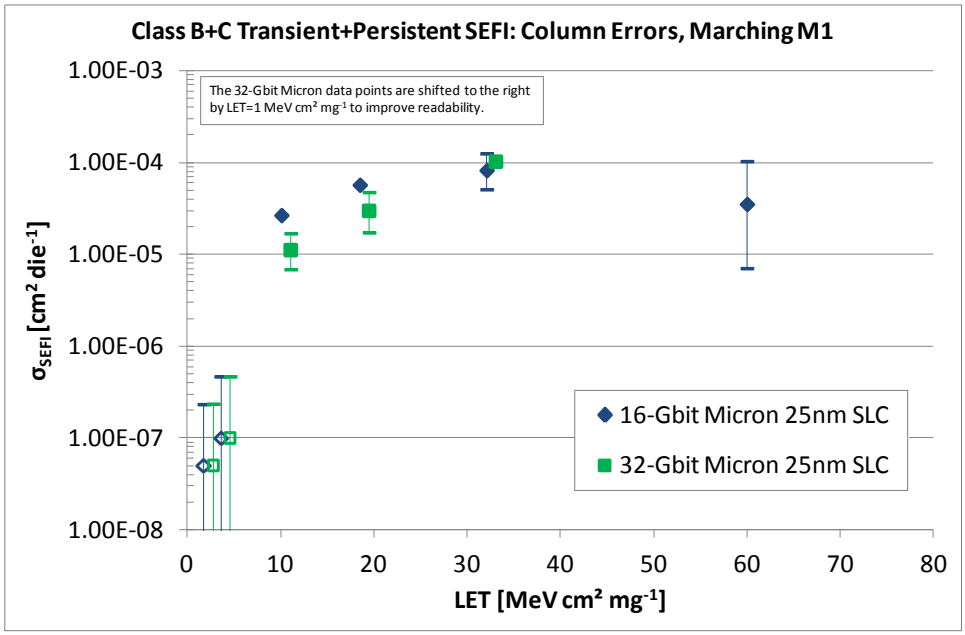

Fig. 25: Class B+C Transient+Persistent SEFI cross section in marching mode M1, Column Errors

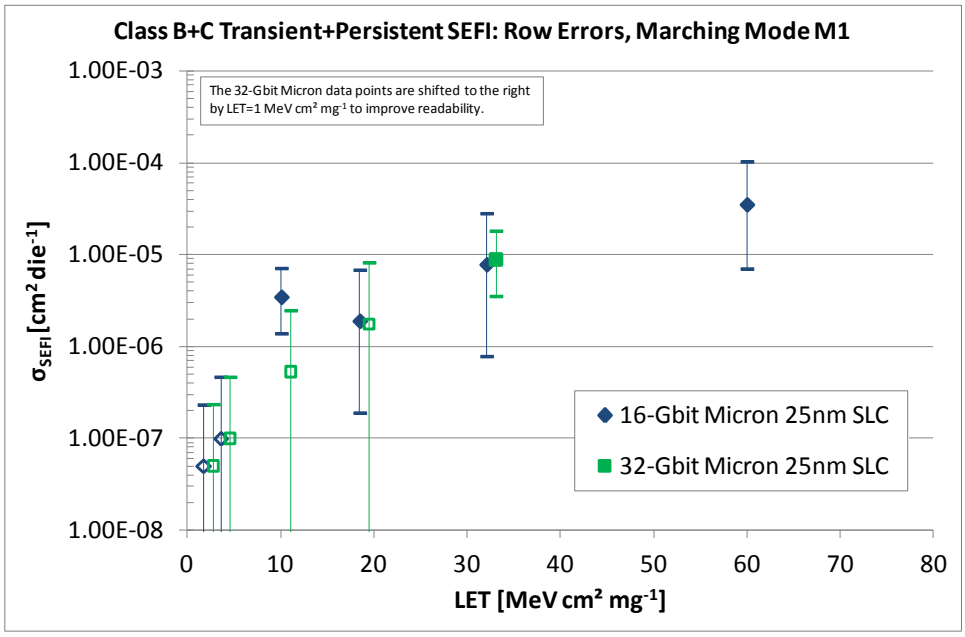

Fig. 26: Class B+C Transient+Persistent SEFI cross section in marching mode M1, Row Errors

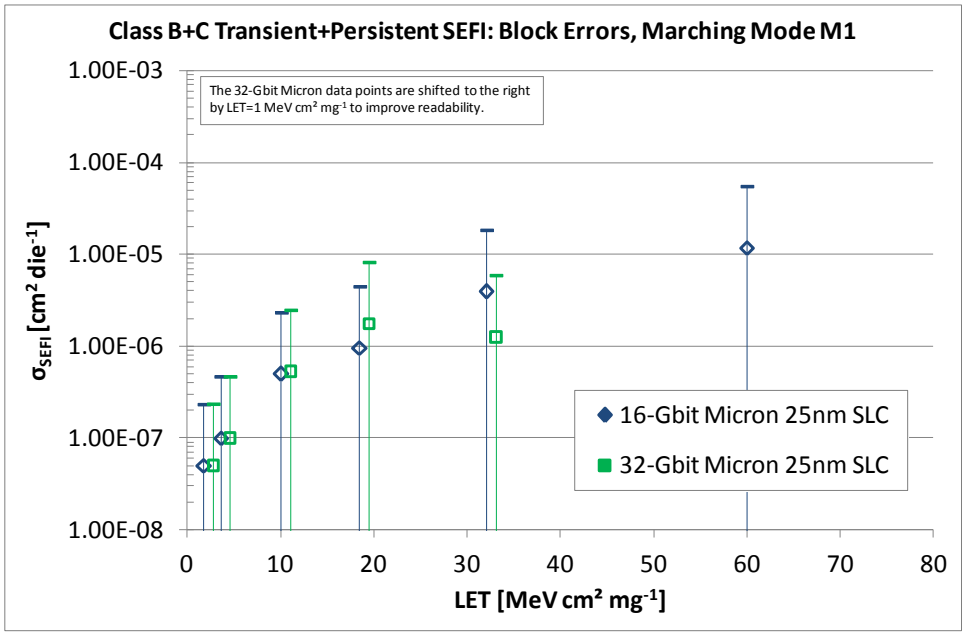

Fig. 27: Class B+C Transient+Persistent SEFI cross section in marching mode M1, Block Errors

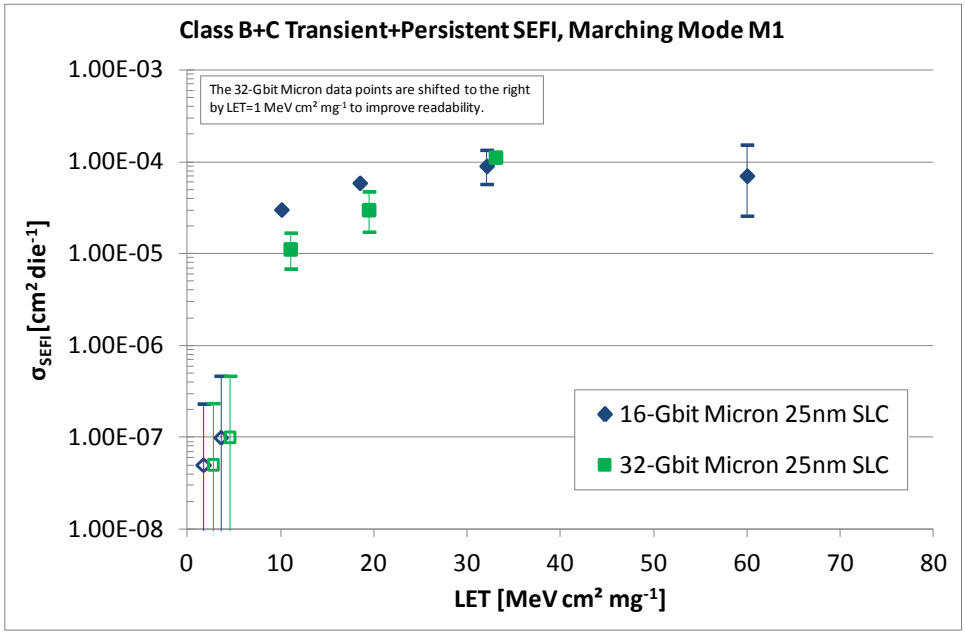

Fig. 28: Class B+C Transient+Persistent SEFI cross section in marching mode M1, all Errors

6.3 Destructive Failures

Under heavy ion irradiation, NAND-Flash is prone to destructive failures (DF). Typically, erase and write are no longer operable, but read is still functional. In contrast to SEL, the DF is not accompanied by an excessive persistent rise of the supply current, but in many cases by a moderate step (factor of 4) of the supply current. The DF event is of statistical nature, just as the SEU and the SEFI events. Fig. 29 shows DF cross section curves from several test campaigns. Open symbols indicate “no DF until the applied fluence”. The state of the art 16-Gbit

device delivers $\sigma_{sat} \approx 1.0 \times 10^{-5}$ cm^2 and $LET_{th} \approx 15$ MeV cm^2/mg. The threshold LET of this 25 nm Micron device is lowered in comparison to the 50 nm 8-Gbit Samsung device.

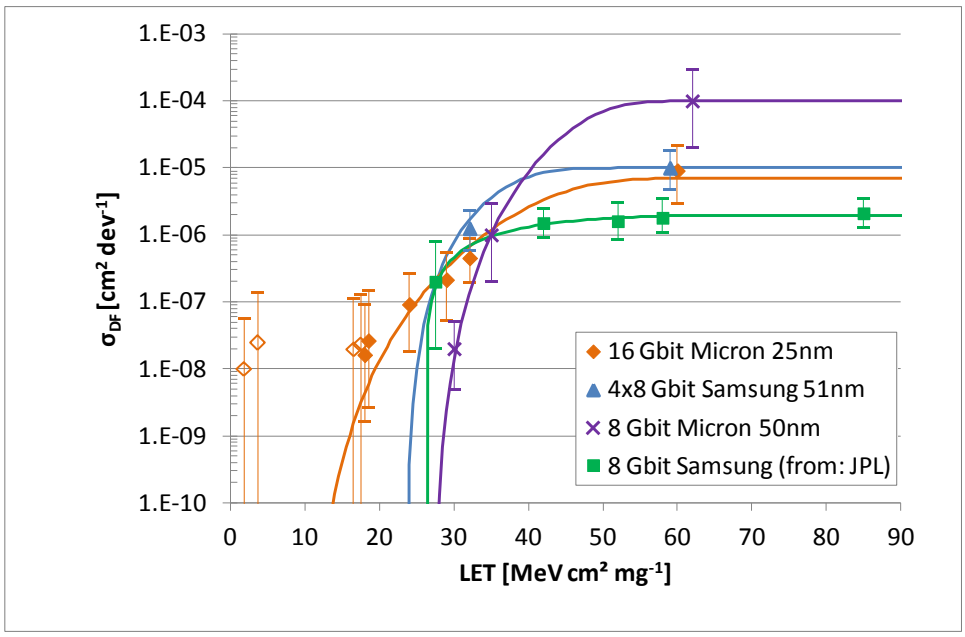

Fig. 29: DF cross section curves, open symbols indicate "no DF until the applied fluence"

The saturation cross section of 1.0×10^{-5}cm^2 describes a sensitive area of 30×30 µm^2. By masking of the chip surface and also by IR hot spot sensing [6], [7], the sensitive area has been located to be the capacitor-switch cascade of the HV generator and its surroundings. Furthermore, it has been demonstrated that in the DF case, the high voltage drops to a significantly lower value [6]. Presumably, the hit of a high LET ion induces a SEGR of the comparatively thick oxide of the HV switching transistors.

We examined the flux dependence (flux between 30 and 8000 cm^{-2} s^{-1}) of Samsung 8-Gbit NAND-Flash DFs. From the negative outcome, we conclude that the DF is triggered by a single hit and not by the coincidence of several hits.

Ions of normal incidence - namely those travelling in parallel to the electric field - should be most dangerous with respect to SEGR. The worst case simplification that ions of all directions are as dangerous as those of normal incidence delivers estimates of the mean time until DF occurrence for 1AU, GCR, 3.7mm Al: between $1.4 \times 10^{+6}$ years (8-Gbit and 16-Gbit Micron) and $2.5 \times 10^{+5}$ years (8-Gbit Samsung). For comparison, the failure rates of commercial memory devices are in the order of 1 FIT, which is equivalent to an average time to failure of $1 \times 10^{+9}$ h = $1.2 \times 10^{+5}$ years. Accordingly, ion induced DFs increase the overall device failure rate by less than a factor of two. To give a concrete example, in a large space mass memory of e.g. 1000 memory devices, a DF can be expected after more than two hundred and fifty years on average.

At DF occurrence, the program current of the 8-Gbit Samsung device jumps from its plateau amplitude of 40 mA maximum to a continuous current of 80 mA. The DF occurrence is independent of the irregularities of the supply current such as occasional current spikes of several 100 mA or the stepping of the erase / program current pulse. Presumably, these spikes are caused by bus contentions in consequence of a hit induced disturbance of the controlling state machine.

Fig. 30 shows the supply current waveform during the programming of a page. The current rises to a pulse plateau with superimposed needles. These needles reflect the sequence of HV program pulses. Under irradiation, the plateau widens and its amplitude grows, step by step.

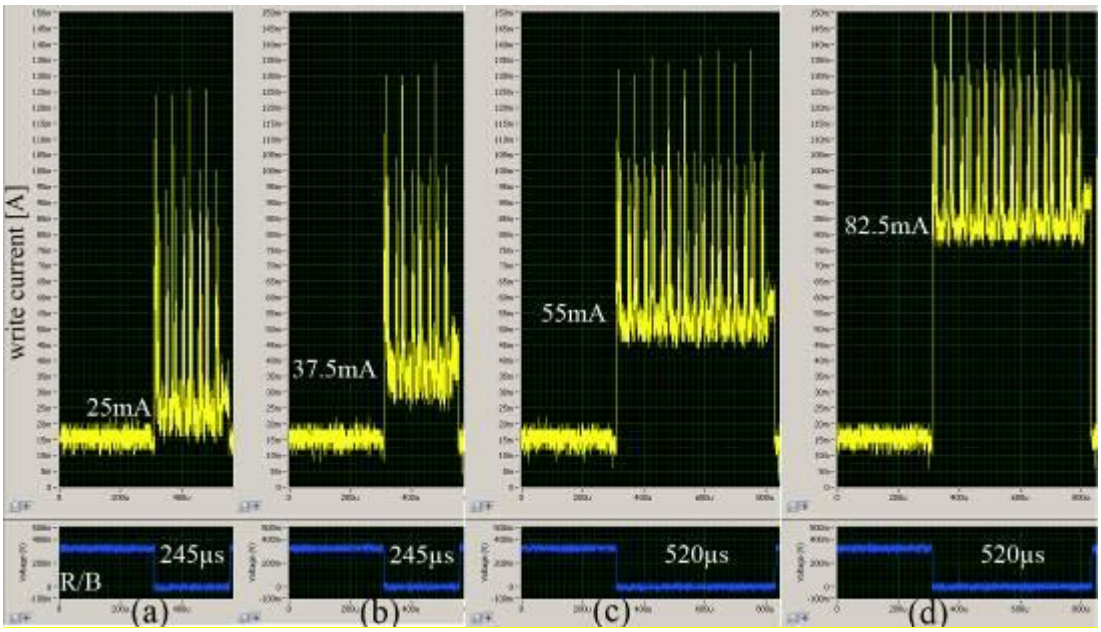

Fig. 30: Development of the program current window until DF occurrence, (a) soon after irradiation start, (b) midway to the final saturation waveform, (c) the final saturation waveform and (d) after DF occurrence, Samsung 8-Gbit NAND-Flash

At the begin of this work we got the impression that the stepping of the supply current leads finally to a DF but a more detailed analysis of the respective waveforms of later test campaigns delivered clearly that such a connection does not exist. DFs occurred as well after stepts (b) and (c) as directly after step (a).

6.4 Soft SEU Annealing

All soft and all hard SEUs are falsifications in 0 → 1 direction. They indicate or fake a loss of FG electrons. Fig. 31 shows the SEU annealing of an earlier 4-Gbit ST NAND-Flash device. SEUs induced by ions of LET between 10 and 32.1 (Ar, Fe, Kr) show significant annealing. For low LET ions, the annealing is more intensive than for high LET ions.

They originate from two effects: a) loss of the negative floating gate charge and b) positive charge trapping near the floating gate. Charge loss is irreversible, trapping is reversible with time.

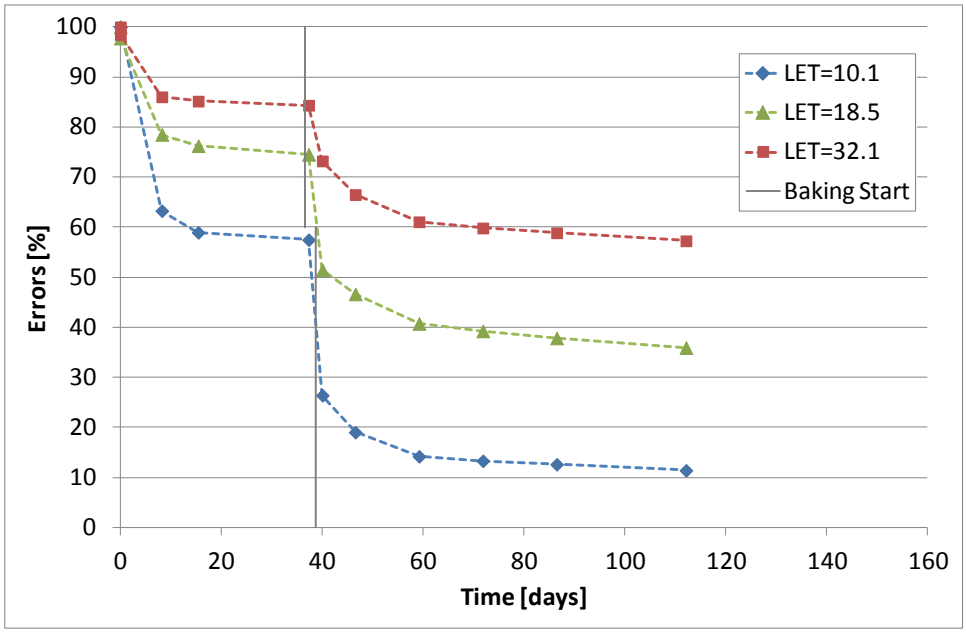

Fig. 31: Annealing of SEUs, baking at 100°C started after 40 days, ST 4-Gbit NAND-Flash [8]

In case of annealing, charge trapping is the error creating effect. In case of the earlier 4-Gbit device, even at argon about 90% of the SEUs are due to charge trapping and only the remaining 10% are due to charge loss from the FG. At krypton, still about 40% of the SEUs are due to charge trapping.

The actual test of the 25nm 16-Gbit Micron devices shows significant annealing only for SEUs induced by very low LET ions (nitrogen, LET = 1.8 MeV cm^2/mg, Fig. 32). SEU generation by charge trapping is restricted to very low LET. Even at neon, nearly all SEUs are due to charge loss.

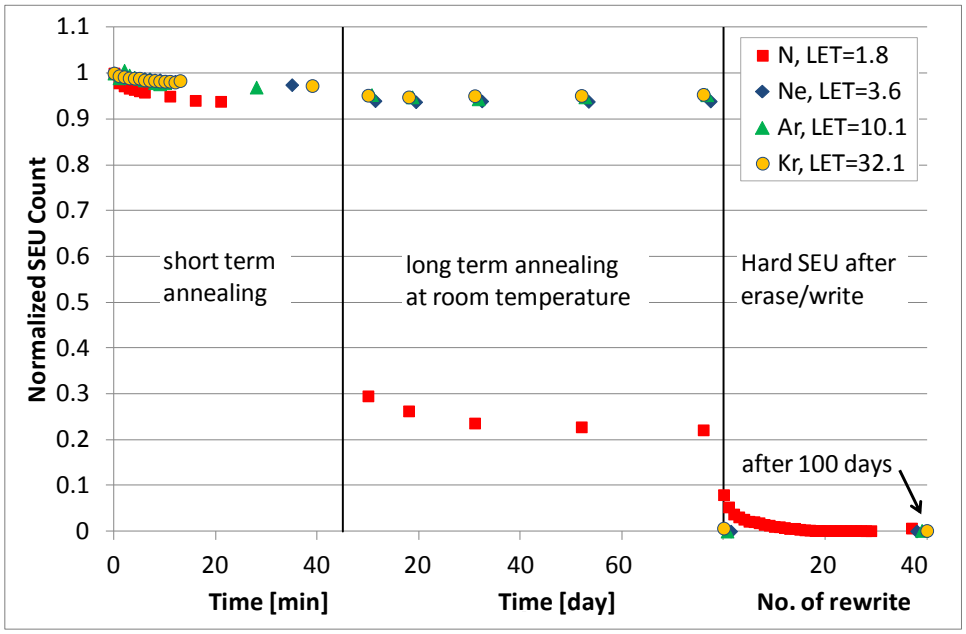

Fig. 32: Annealing of SEUs, Micron 16/32-Gbit NAND-Flash

Fig. 33 illustrates the trend that with scaling of the feature size, charge loss becomes dominating over charge trapping. The trapped charge domain is restricted more and more to lower LET. Remarkably devices of the same type but different lot code differed substantially with respect to the annealing behaviour.

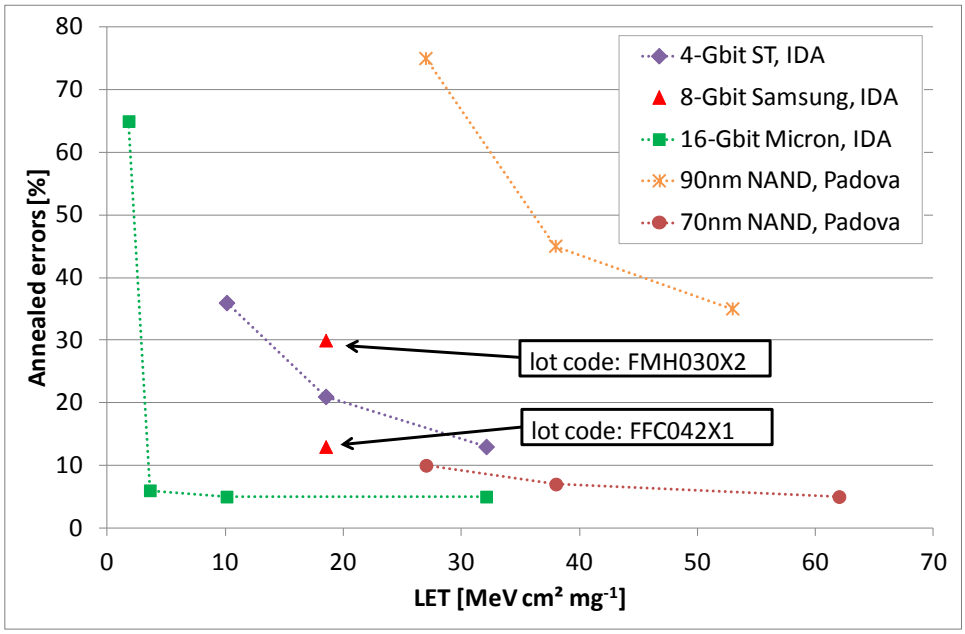

Fig. 33: Percentage of annealed SEUs, 120 hours after irradiation as a function of ion LET

6.5 Hard SEU Annealing

Hard SEUs survive a reversal of the cell status by erase-write immediately after beam stop and error verification. We observed annealing of hard SEUs for 16-Gbit NAND-Flash (Fig. 34). The logarithmically scaled bar graph shows the cross section of (i) the total of soft and hard SEUs, (ii) the share of hard SEUs directly after exposure, (iii) the annealing of soft SEUs after 20 days and (iv) the annealing of hard SEUs after 20 days.

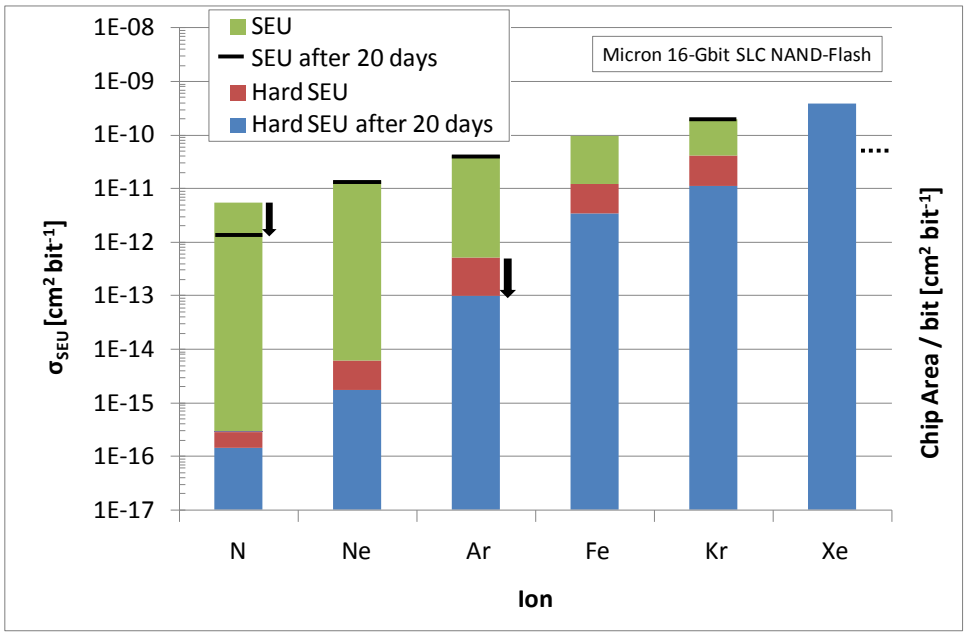

Fig. 34: Total of soft and hard SEUs, share of hard SEUs directly after exposure and 20 days later, 16-Gbit Micron SLC NAND-Flash

The share of hard SEUs (Fig. 34, blue part of the bar) increases steadily with LET from 3 × 10^{-3} % at nitrogen to nearly 100% at xenon. Significant annealing of soft SEUs exists only at nitrogen. In contrast the soft SEUs, typically more than one half of the hard SEUs anneal within 20 days.

Fig. 35 shows the respective cross sections over the linear LET scale. Starting with iron, the cross section per bit exceeds the chip area per bit of 6 × 10^{-11} cm^2, which indicates an increasing count of multi-bit SEUs.

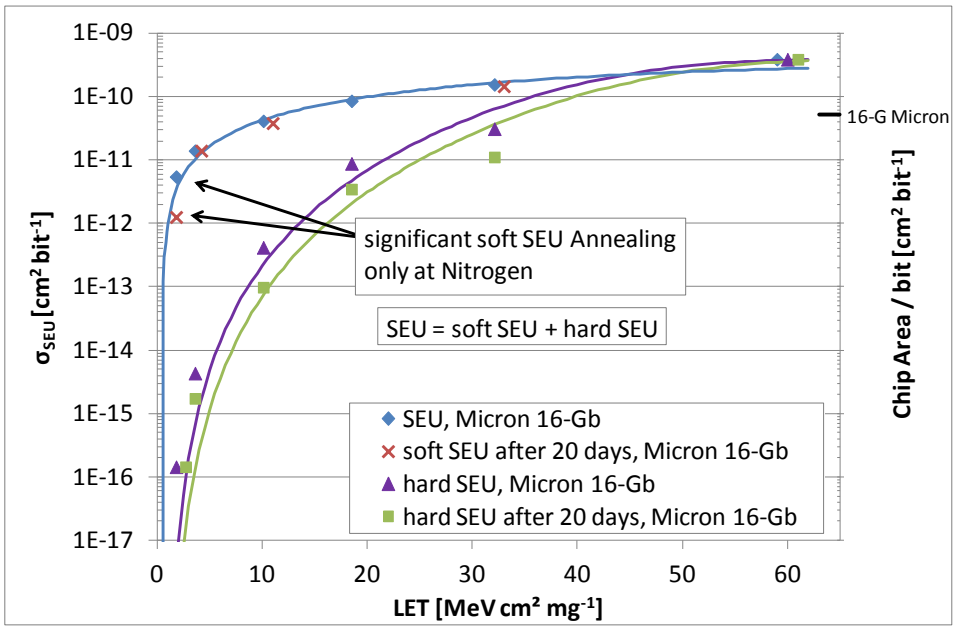

Fig. 35: Cross section of SEUs, share of hard SEUs directly after exposure and 20 days later, 16-Gbit Micron SLC NAND-Flash

All multi-SEUs extend in column direction. Fig. 36 illustrates this for the 25nm Micron 16-Gbit device under normal incidence of xenon ions (LET ≈ 60 MeV cm^2/mg). Soft SEUs are indicated by small diamonds and hard SEUs by large horizontal bars. In many cases, one or several hard SEUs are accompanied by soft SEUs on one or on both sides.

In our interpretation the hard SEUs indicate the hit position, the soft SEUs the charge deposition in the neighbourhood.

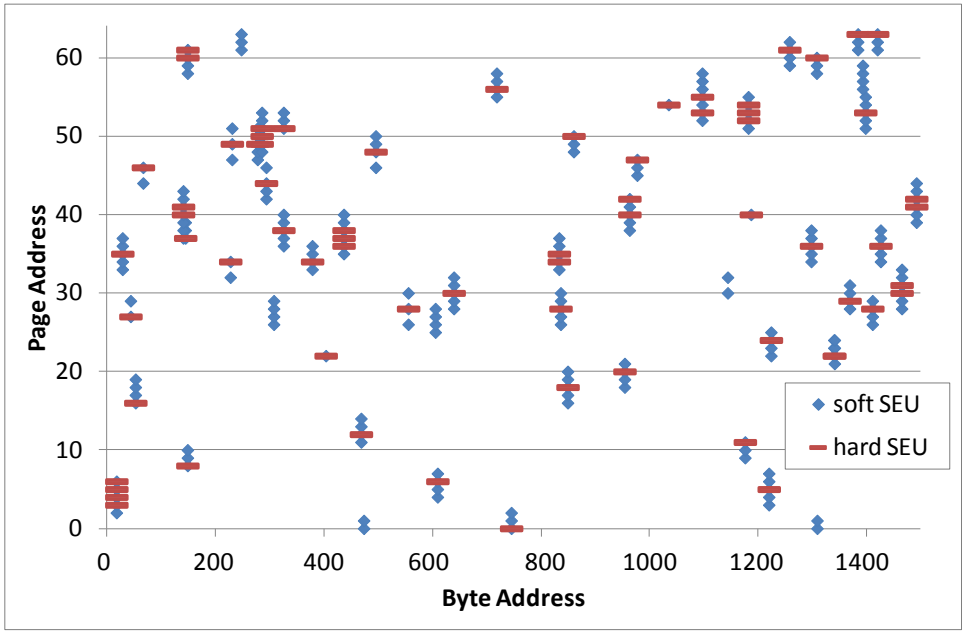

Fig. 36: Micron 16-Gbit SLC NAND-Flash, MBUs at normal incidence, Xe, LET = 60

Fig. 37 shows the annealing of hard SEUs versus time. For all ion species except xenon we get substantial annealing, more pronounced for lower LET ions.

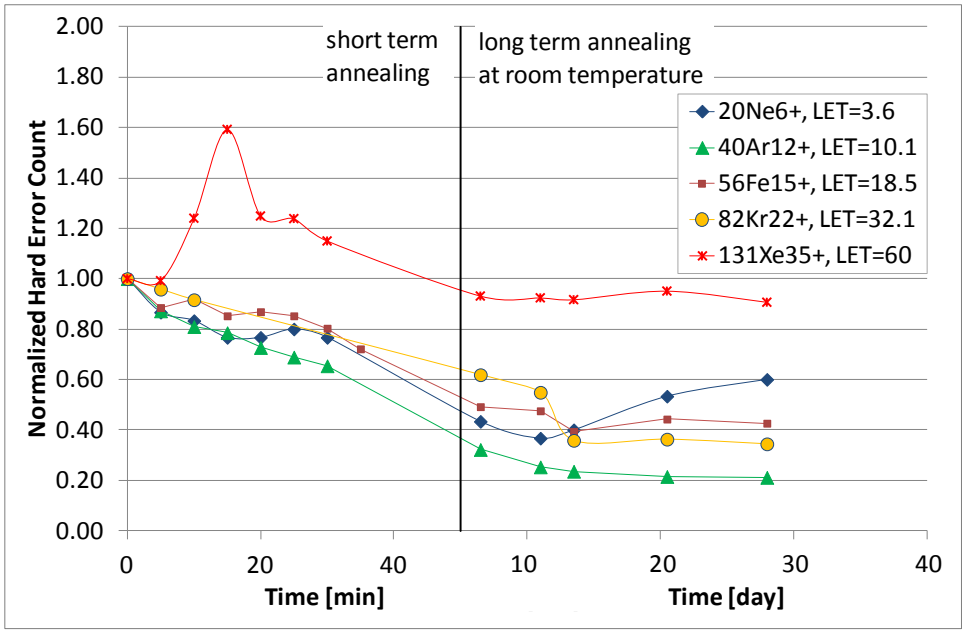

Fig. 37: Short term and long term hard error annealing, Micron 16/32-Gbit NAND-Flash DUTs unbiased

Xenon, iron and neon induced hard SEUs show some reverse annealing for some ten minutes after exposure.

An erase-write operation after 100 days (Fig. 32) delivered a complete annealing of the heavy ion induced hard SEUs. Only a fraction of the nitrogen induced hard SEUs survived, but disappeared within the following 30 erase/write cycles.

One hundred days after irradiation, the read of the xenon exposed DUT delivered 95% of the initial count of hard SEUs. An erase-write-read reduced this count to 55%. But then, the count of hard errors increased again with time as depicted in Fig. 38.

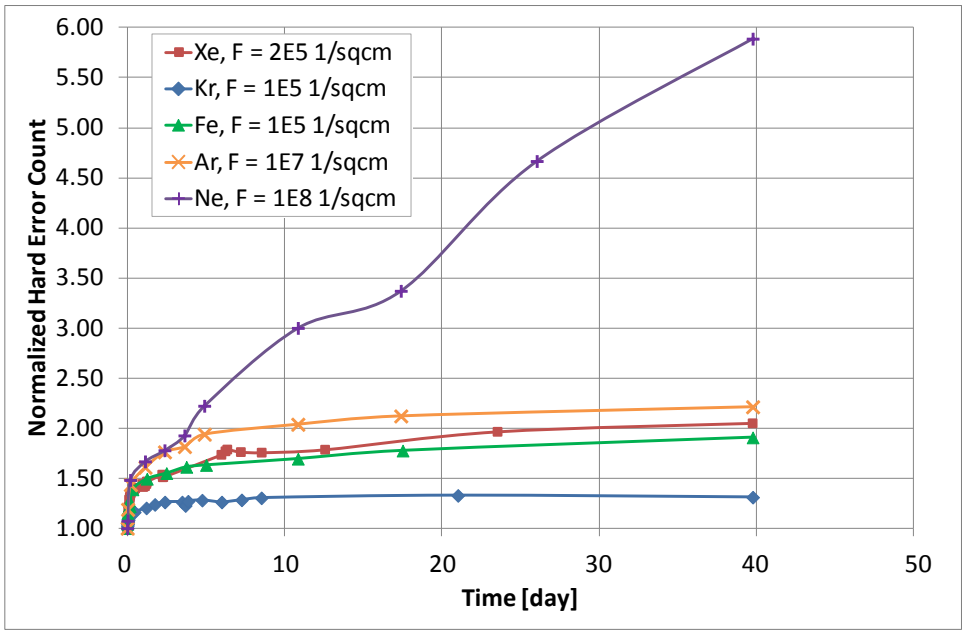

Fig. 38: Development of the hard SEU count after repeated erase-write-read cycles

6.6 Discussion

The stepping of the program current (Fig. 30) reflects a closed loop controlled adaptation of the count of high voltage pulses. We assume that the HV leakage current increases by ion induced defects, possibly by micro latch ups [7]. The associated reduction of the pulse tunnel current is compensated by more programming pulses.

The pulse tunnel current is the program current which appears between FG and channel induced by the high voltage pulses generated by the program charge pump. Every high voltage pulse induces a current spike at the supply rail. These spikes were measured and shown in Fig. 30.

After a given number of compensation steps, this process comes to an end, mostly before DF occurrence, but the converse situation happens as well. The mean time until DF is larger than the mean time until the freeze of the adaptation of the program pulse sequence.

The fact that a further degradation of the program pulse voltage cannot be compensated any more by an increased count of program pulses raises some concern about the long term data retention. The decreasing amount of injected FG charge should result in a reduced data reten-

tion time. In consequence, for applications with large data storage time, the usability of the device should be determined by the freezing of the program pulse window rather than by the DF occurrence. This issue requires further investigation.

Presumably, the center of the hard error pattern given in Fig. 36 reflects the shortest distance between the transistor string and the ion track. The SEUs always affect the same bit position of the same byte of subsequent pages. Physically, in the string of concatenated transistors, the channels of adjacent transistors cannot be depleted by the lowered word line voltage.

This seems to indicate that the hard SEUs are caused by a large trapped charge, which cannot be compensated by the negative charge of a single write cycle, and which anneals over time.

The write operation charges all FGs including those with impaired insulation. The starting count of hard SEUs reflects cells which are in erroneous state (i) because of still not sufficiently removed trapped holes, or (ii) because of an immediate loss of FG electrons due to a leakage current of more than some ten electrons per second.

The increasing count of hard SEUs (Fig. 38) reflects the discharge of less impaired FG structures by an even smaller leakage current. If, for example, an additional SEU is created by the loss of a floating gate charge of 360 electrons in one hour, then the leakage amounts to only one electron per second or 1.6×10^{-4} fA.

The “reverse annealing” of the heavier ion curves in Fig. 37 can be explained by the superposition of the increasing count of “resistive” hard SEUs and the decreasing count of “charge trapping” SEUs. The steady loss of FG electrons makes more and more “resistive” hard SEUs visible.

Persistent hard errors accumulate over the mission time. Their detrimental effect on the error rate increases steadily. In contrast, soft SEUs accumulate only over the data storage time, which is only of some days in many cases. in consequence, hard errors survive scrubbing and can therefore be more harmful. Scrubbing is a measure to reduce the storage time.

7 Run Table January Test

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	3	251	226	1.00E+07	4.4E+04	1	2938	
		M2r	4	252	9	3.43E+05	3.8E+04	1		operating error
		M2r	5	253	231	1.01E+07	4.4E+04	11	15730	
		R	5.a				-		2737	
		M1	6	254	233	1.01E+07	4.3E+04	2	2221	
		M5	7	255	245	1.00E+07	4.1E+04	1	4855	

Tab. 10: Run Table of Micron 16-Gbit DUT M305, N, LET = 1.8, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	8	257	242	1.00E+07	4.1E+04	8	0	
		R	8.a				-		0	

Tab. 11: Run Table of Micron 8-Gbit DUT MC14, N, LET = 1.8, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	9	257	252	1.01E+07	4.0E+04	1	4665	
		M1	10	258	235	1.01E+07	4.3E+04	2	3553	
		M5	11	259	245	1.00E+07	4.1E+04	1	6007	
		M2r	12	260	231	1.01E+07	4.4E+04	11	22570	
		R	12.a				-		3963	
		R	12.b				-		3803	

Tab. 12: Run Table of Micron 16-Gbit DUT M306, N, LET = 1.8, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks

		M3a	13	261	259	1.00E+07	3.9E+04	1	3439	
		M1	14	262	267	1.00E+07	3.7E+04	2	2581	
		M5	15	263	264	1.01E+07	3.8E+04	1	4574	
		M2a	16	264	275	1.00E+07	3.6E+04	13	19098	
		R	16.a				-		2863	
		R	16.b				-		2838	

Tab. 13: Run Table of Micron 32-Gbit DUT M412, N, LET = 1.8, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	17	265	273	1.01E+07	3.7E+04	1	3498	
		M1	18	266	291	1.00E+07	3.4E+04	18	2731	
		M5	19	267	204	1.01E+07	5.0E+04	1	4199	
		M2a	20	268	175	1.01E+07	5.8E+04	8	14489	
		R	20.a				-		3357	

Tab. 14: Run Table of Micron 32-Gbit DUT M413, N, LET = 1.8, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	21	269	190	1.00E+07	5.3E+04	1	0	beamline closed
		M3a	22	270	191	1.01E+07	5.3E+04	1	77229	Timeout, MBUs
PC		R	22.a				-	1	60038	
		BG					-		2755	
		R	22.b				-		2629	

Tab. 15: Run Table of Micron 32-Gbit DUT M413, Fe, LET = 18.5, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	23	271	206	1.00E+06	4.9E+03		5605	few 2-

										BEs
		R	23.a				-		5570	
		BG							170	
		M1	24	272	40	2.29E+05	5.7E+03		2131	Timeout
	85	M5	25	273	140	7.13E+05	5.1E+03		63385	Timeout
	143	M5	26	274	187	1.00E+06	5.3E+03		92803	Timeout
	210	M2r	27	275	121	1.01E+06	8.3E+03	6	>>	
	5755						-			many SBs

Tab. 16: Run Table of Micron 32-Gbit DUT M414, Fe, LET = 18.5, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	28	276	157	1.00E+06	6.4E+03		>>	
		R	28.a				-		6487	
	368	M1	29	277	58	3.43E+05	5.9E+03			Timeout
	296	M5	30				-			Tuning
	296	M5	31	278	144	7.61E+05	5.3E+03		37891	Timeout
	325	M2r	32	279	177	1.01E+06	5.7E+03		>>	BE PC+, BE+
PC		R	32.a				-			

Tab. 17: Run Table of Micron 32-Gbit DUT M415, Fe, LET = 18.5, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	32.b				-		>>	BE
	0	M3a	33	280	171	1.01E+06	5.9E+03		22724	stuck bits von N at the next day 0, Timeout
		R	33.a				-		5755	
	266	M1	34	281	54	4.34E+05	8.0E+03			TO PC-

	262	M5	35	282	86	6.70E+05	7.8E+03			PC, TO PC-
	337	M2r	36	283	132	1.02E+06	7.7E+03		>>	BE, BE+, BE same place+, BE PC+
PC		R	36.a				-		5860	

Tab. 18: Run Table of Micron 16-Gbit DUT M305, Fe, LET = 18.5, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	36.b				-		3733	stuck bits of N at the next day
	0	M3a	37	284	133	1.01E+06	7.6E+03		6258	
		R	37.a				-		6210	
	325	M1	38	285	79	6.17E+05	7.8E+03		28637	Timeout, PC-
PC	375	M5	39	286	138	1.01E+06	7.3E+03		41831	Timeout PC-
	499	M2	40	287	165	1.00E+06	6.1E+03		>>	Timeout during BG
PC		R	40.a				-		6367	
		R	40.b				-		6112	after lunch break, (45 min)

Tab. 19: Run Table of Micron 16-Gbit DUT M306, Fe, LET = 18.5, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	364	M3a	41	288	185	5.01E+05	2.7E+03		6034	
		R	41.a				-		6005	
	1135	M1	42	289	26	7.80E+04	3.0E+03		2763	Timeout, PC-

PC	918	M5	43	290	183	5.03E+05	2.7E+03		>>	
	1379	M2	44	291	194	5.03E+05	2.6E+03		>>	
		R	44.a				-		6740	

Tab. 20: Run Table of Micron 16-Gbit DUT M306, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	44.b				-			operating error
		R	44.c				-		5611	
	227	M3a	45	292	176	5.03E+05	2.9E+03		5465	
		R	45.a				-		5447	
	921	M1	46	293	74	1.77E+05	2.4E+03		75635	Timeout, PC-
	820	M5	47	294	199	5.02E+05	2.5E+03			
	1118	M2r	48	295	186	5.03E+05	2.7E+03		>>	first CE, BE PC+
PC		R	48.a				-		5965	

Tab. 21: Run Table of Micron 16-Gbit DUT M305, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	48.b				-		5565	
	94	M3a	49	296	205	5.03E+05	2.5E+03		4888	
		R	49.a				-		4875	
	570	M1	50	297	114	2.90E+05	2.5E+03		34713	Timeout, PC-
	539	M5	51	298	141	3.85E+05	2.7E+03			Timeout, PC-, Controller Reset+
	563	M2r	52	299	212	5.02E+05	2.4E+03		>>	
PC		R	52.a				-		5267	

Tab. 22: Run Table of Micron 32-Gbit DUT M414, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	52.b				-		5530	
	222	M3a	53	300	202	5.05E+05	2.5E+03		5589	
		R	53.a				-		5575	
	1002	M1	54	301	193	5.01E+05	2.6E+03		>>	
	1155	M5	55	302	221	5.04E+05	2.3E+03		>>	
	1402	M2r	56	303	209	5.05E+05	2.4E+03		>>	BE @ 1.6E5, PC+, 3BE remaining
		R	56.a				-		6453	

Tab. 23: Run Table of Micron 32-Gbit DUT M415, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	57	304	192	5.05E+05	2.6E+03		>>	3 BE
		R	57.a				-		5363	

Tab. 24: Run Table of Micron 16-Gbit DUT M307, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	57.p				-		5543	
	965	M3a	58	305	204	2.01E+05	9.9E+02		4819	12 BE
PC		R	58.a				-		4786	
	1757	M1	59	306	83	8.51E+04	1.0E+03		>>	CS, PC-, write op. failed

Tab. 25: Run Table of Micron 16-Gbit DUT M305, Xe, LET = 60, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	1215	M3a	60	307	219	1.01E+05	4.6E+02		3421	
		R	60.a				-		3431	
	1564	M5	61	308	98	4.34E+04	4.4E+02		>>	CS, PC-, write op. failed

Tab. 26: Run Table of Micron 16-Gbit DUT M306, Xe, LET = 60, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	62	309	246	1.01E+05	4.1E+02		1958	
		R	62.a				-		1939	
	363	M2r	63	310	244	1.00E+05	4.1E+02		>>	2 BE
		R	63.a				-			PC for-gotten
PC		R	63.b				-		2345	

Tab. 27: Run Table of Micron 16-Gbit DUT M310, Xe, LET = 60, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	63.c				-		4993	
	467	M3a	64	311	240	1.00E+05	4.2E+02		2354	
PC		R	64.a				-		2344	
	731	R	64.b				-		662	
	662	M2r	65	312	260	1.00E+05	3.8E+02	12	>>	CS @ 2.5E4, PC+, transient BE
PC		R	65.a				-		2376	

Tab. 28: Run Table of Micron 32-Gbit DUT M414, Xe, LET = 60, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	65.b				-		5978	
	1141	M3a	66	313	240	1.01E+05	4.2E+02		>>	
		R	66.a				-		3089	
	1435	M2r	67	314	249	1.00E+05	4.0E+02	11	>>	
PC		R	67.a				-		4248	remaining CE after PC
PC		R	67.b				-		4238	remaining CE after PC

Tab. 29: Run Table of Micron 32-Gbit DUT M415, Xe, LET = 60, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
PC		R	67.a				-			irrelevant
		R	67.b				-		2142	
	286	M3a	68	379	169	1.01E+06	6.0E+03		>>	1 BE
PC		R	68.a				-		3101	
	237	M1	69	380	171	1.01E+06	5.9E+03	1	36676	
	123	M5	70	381	170	9.93E+05	5.8E+03			Timeout @ 9.5E5, PC-, PC+, DUT OK
	78	M2r	71	382	170	1.00E+06	5.9E+03	7	>>	Timeout @ 1.5E5, PC+, BE
PC		R	71.a				-		2804	

Tab. 30: Run Table of Micron 16-Gbit DUT M310, Ar, LET = 10.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M3a	72	383	168	1.01E+06	6.0E+03	1	3035	

		R	72.a				-		3026	
	16	M1	73	384	60	3.50E+05	5.8E+03	0		Timeout @ 3.0E5, PC+
	9	M1	74	385	145	1.01E+06	7.0E+03	1	65800	
	12	M5	75	386	171	1.00E+06	5.8E+03	1	36332	
	21	M2b	76	387	157	1.01E+06	6.4E+03		>>	
		R	76.a				-		>>	
PC		R	76.b				-		3065	

Tab. 31: Run Table of Micron 16-Gbit DUT M311, Ar, LET = 10.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M3a	77	388	151	1.01E+06	6.7E+03	1	2806	
PC		R	77.a				-	1	2809	

Tab. 32: Run Table of Micron 16-Gbit DUT M308, Ar, LET = 10.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	77.m				-	1	2156	
	463	M3a	78	389	160	1.01E+06	6.3E+03	1	3202	
		R	78.a				-	1	3193	
	377	M1	79	390	219	9.28E+05	4.2E+03	?	?	unstable flux, Timeout @ 8.8E5, PC+
	203	M1	80	391	166	1.01E+06	6.1E+03	?	?	
	112	M5	81	392	26	1.46E+05	5.6E+03	?	?	Timeout @ 1.0E5, PC+
	81	M5	82	393	158	1.01E+06	6.4E+03	?	?	
	63	M2r	83	394	177	1.01E+06	5.7E+03	8	>>	2 BE
PC		R	83.a				-		2611	

Tab. 33: Run Table of Micron 32-Gbit DUT M414, Ar, LET = 10.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	1051	M3a	84	395	143	1.01E+06	7.1E+03	1	3779	
		R	84.a				-	1	3766	
	924	M1	85	396	136	9.71E+05	7.1E+03	1	7838	Timeout @ 9.1E5, PC
PC	542	M5	86	397	141	1.01E+06	7.2E+03	1	40522	
PC	395	M2r	87	398	140	1.00E+06	7.1E+03	1	>>	Timeout @ 2.9E5, PC+
PC		R	87.a				-		3134	

Tab. 34: Run Table of Micron 32-Gbit DUT M415, Ar, LET = 10.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	360			399	60	1.92E+05	3.2E+03			flux too low
	332	M3a	88	400	175	5.02E+06	2.9E+04	1	>>	1 BE
PC		R	88.a				-	1	5080	
	313	M1	89	401	174	5.05E+06	2.9E+04	1	4164	
	228	M5	90	402	175	5.05E+06	2.9E+04	1	6645	
	181	M2r	91	403	176	5.04E+06	2.9E+04		>>	
PC		R	91.a				-		4835	

Tab. 35: Run Table of Micron 32-Gbit DUT M415, Ne, LET = 3.6, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	91.b				-	1	2556	
	51	M3a	92	404	179	5.02E+06	2.8E+04	1	>>	4 BE
PC		R	92.a				-	1	4756	

	45	M1	93	405	177	5.03E+06	2.8E+04	1	3894	
PC	31	M5	94	406	178	5.03E+06	2.8E+04	1	6246	
PC	20	M2r	95	407	177	5.06E+06	2.9E+04	8	>>	
PC		R	95.a				-		4765	

Tab. 36: Run Table of Micron 32-Gbit DUT M414, Ne, LET = 3.6, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	71	M3a	96	408	174	5.05E+06	2.9E+04	1		2 BE
		R	96.a				-	1	4802	
	55	M1	97	409	173	5.05E+06	2.9E+04	1	3929	
PC	38	M5	98	410	178	5.02E+06	2.8E+04	1	7100	not only SEUs
	28	M2b	99	411	186	5.04E+06	2.7E+04	8	>>	
PC		R	99.a				-	1	4752	

Tab. 37: Run Table of Micron 16-Gbit DUT M310, Ne, LET = 3.6, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		R	99.b				-		2941	
	7	M3a	100	412	190	5.06E+06	2.7E+04	1	>>	BE
		R	100.a				-		5043	few 2BE
	7	M1	101	413	186	5.02E+06	2.7E+04	2	3937	
PC	3	M5	102	414	184	5.03E+06	2.7E+04	1	6197	
	2	M2r	103	415	188	5.02E+06	2.7E+04	9	>>	
PC		R	103.a				-	1	4930	

Tab. 38: Run Table of Micron 16-Gbit DUT M311, Ne, LET = 3.6, 64 blocks tested

8 Run Table April Test

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
Foil		M1	1	1	47	2.65E+06	5.6E+04	0		
Foil		M1	2	2	129	6.81E+06	5.3E+04	2		Erase failed, Program failed

Tab. 39: Run Table of Micron 16-Gbit DUT M312, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
Foil		M1	3	3	870	4.95E+06	5.7E+03	17		
Foil		M1	4	4	1289	6.97E+06	5.4E+03	25		
Foil		M1	5	5	80	4.20E+05	5.3E+03	3		
Foil		M1	6				-			DF

Tab. 40: Run Table of Micron 16-Gbit DUT M313, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
Foil		M1	7	6	56	5.89E+05	1.1E+04	0		
Foil		M1	8	7	45	4.81E+05	1.1E+04	1		DF

Tab. 41: Run Table of Micron 16-Gbit DUT M314, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
Foil		M3	8.a				-			
Foil		M3b	9	8	83	1.01E+06	1.2E+04	1	1655	
Foil		R	9.a				-	1		PC, 1 SB
Foil		M1	10				-			no beam
Foil		M1	11	9	59	7.16E+05	1.2E+04	1		

Foil		M1	12	10	381	4.55E+06	1.2E+04	7		
Foil		M1	13	11	517	6.28E+06	1.2E+04	10		
Foil	3	M1	14	12	526	6.14E+06	1.2E+04	10		
Foil	3	M1	15	13	37	4.38E+05	1.2E+04	0		
Foil	3	M1	16	14	227	2.63E+06	1.2E+04	4		
Foil	3	M1	17	15	23	2.72E+05	1.2E+04	1		Erase OK, program failes

Tab. 42: Run Table of Micron 16-Gbit DUT M315, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3a	18	16	83	1.02E+06	1.2E+04	1	11775	2BU, 1867 SB

Tab. 43: Run Table of Micron 16-Gbit DUT M316, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	1867	M1	19	17	20	2.30E+05	1.2E+04	0	775	
		M1	20	18	16	1.92E+05	1.2E+04	0		
	757	M1	21	19	40	4.93E+05	1.2E+04	0		
	924	M1	22	20	12	1.39E+05	1.2E+04	0		1 persistent CE
	>>	M1	23	21	40	4.97E+05	1.2E+04	0		CEs
	1101	M1	24	22	82	1.02E+06	1.2E+04			
		M1		23	83	1.01E+06	1.2E+04	3		continuation RADEF Run 22
	1898	M1	25	24	57	7.15E+05	1.3E+04	0		
	1892	M1	26	25	18	2.14E+05	1.2E+04	0		
		M1	27	26	18	2.20E+05	1.2E+04	0		
	1377	M1	28	27	76	9.17E+05	1.2E+04			

	1762	M1	29	28	12	1.45E+05	1.2E+04	0		
	1438	M1	30	29	23	3.02E+05	1.3E+04	0		
	1335	M1	31	30	45	5.67E+05	1.3E+04	0		
	1437	M1	32	31	33	4.20E+05	1.3E+04	0		
	1487	M1	33	32	42	5.53E+05	1.3E+04	0		
	1562	M1	34	33	11	1.40E+05	1.3E+04	0		
	1240	M1	35	34	27	3.70E+05	1.4E+04	0		
	1248	M1	36	35	35	5.18E+05	1.5E+04	0		
		M1	37	36	49	7.29E+05	1.5E+04	0		
	1636	M1	38	37	104	1.52E+06	1.5E+04	1		
	2226	M1	39	38	13	2.06E+05	1.6E+04	0		
	1861	M1	40	39	27	4.14E+05	1.5E+04	0		
	1773	M1	41	40	149	2.23E+06	1.5E+04	2		
	2537	M1	42	41	40	6.04E+05	1.5E+04	0		
	2824	M1	43	42	26	4.02E+05	1.5E+04	0		
	2472	M1	44	43	28	4.31E+05	1.5E+04	0		1 CE stuck
	2349	M1	45	44	55	8.35E+05	1.5E+04	0		
	3284	M1	46	45	11	1.67E+05	1.5E+04	0		
	2323	M1	47	46	33	5.04E+05	1.5E+04	0		1 CE stuck
	2322	M1	48	47	32	4.95E+05	1.5E+04	0		
	2366	M1	49	48	9	1.47E+05	1.6E+04	0		2 CE stuck
	2130	M1	50	49	76	1.17E+06	1.5E+04	0		2 CE stuck, DF

Tab. 44: Run Table of Micron 16-Gbit DUT M316, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M1	51	50	32	4.69E+05	1.5E+04	0		
	348	M1	52	51	12	1.86E+05	1.6E+04	0		
	332	M1	53	52	45	6.56E+05	1.5E+04	0		

	607	M1	54	53	14	2.12E+05	1.5E+04	0		DF

Tab. 45: Run Table of Micron 16-Gbit DUT M317, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M1	55	54	37	6.01E+05	1.6E+04	0		persistent BE, PC-
	433	M1	56	55	31	4.79E+05	1.5E+04	0		
	615	M1	57	56	35	5.59E+05	1.6E+04	0		
	783	M1	58	57	17	2.59E+05	1.5E+04	0		
	726	M1	59	58	91	1.45E+06	1.6E+04	1		
	1358	M1	60	59	28	4.52E+05	1.6E+04	0		erase failed, program failed, read still functional

Tab. 46: Run Table of Micron 16-Gbit DUT M318, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M1	61	60	23	3.66E+05	1.6E+04	0		
	440	M1	62	61	27	4.47E+05	1.7E+04	0		
	1903	M1	63	62	132	2.18E+06	1.7E+04	2		3 stuck CE
	3892	M1	64	63	11	1.80E+05	1.6E+04	0		3 stuck CE
	3359	M1	65	64	11	1.94E+05	1.8E+04	0		3 stuck CE
	3111	M1	66	65	105	1.73E+06	1.6E+04	1		3 stuck CE
	4200	M1	67	66	20	3.25E+05	1.6E+04	0		3 stuck CE
	3678	M1	68	67	48	8.40E+05	1.8E+04	0		3 stuck CE
	3980	M1	69	68	35	5.94E+05	1.7E+04	0		BE, erase

										failed, program functional, read 0xFF

Tab. 47: Run Table of Micron 16-Gbit DUT M319, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M1	70	69	52	8.67E+05	1.7E+04	0		
	892	M1	71	70	10	1.65E+05	1.7E+04	0		
	808	M1	72	71	88	1.44E+06	1.6E+04	1		
	1795	M1	73	72	9	1.45E+05	1.6E+04	0		
	1443	M1	74	73	18	3.12E+05	1.7E+04	0		
	1433	M1	75	74	13	2.06E+05	1.6E+04	0		
	1295	M1	76	75	8	1.29E+05	1.6E+04	0		
	1166	M1	77	76	11	1.89E+05	1.7E+04	0		
	1130	M1	78	77	22	3.78E+05	1.7E+04	0		
	1293	M1	79	78	26	4.48E+05	1.7E+04	0		
	1386	M1	80	79	23	4.32E+05	1.9E+04	0		
	1511	M1	81	80	51	8.93E+05	1.8E+04	0		
		M1		81	19	3.21E+05	1.7E+04	0		continuation
	2176	M1	82	82	15	2.56E+05	1.7E+04	0		
	1992	M1	83	83	17	2.94E+05	1.7E+04	0		
	1879	M1	84	84	9	1.50E+05	1.7E+04	0		
	1652	M1	85	85	18	3.30E+05	1.8E+04	0		erase failed, program failed

Tab. 48: Run Table of Micron 16-Gbit DUT M320, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M1	86	86	56	1.00E+06	1.8E+04	0		

	687	M1	87	87	23	4.27E+05	1.9E+04	0		
	710	M1	88	88	11	2.08E+05	1.9E+04	0		
	596	M1	89	89	10	1.86E+05	1.9E+04	0		
	552	M1	90	90	35	6.56E+05	1.9E+04	0		
	1345	M1	91	91	62	1.15E+06	1.9E+04	0		1 stuck CE
	2367	M1	92	92	23	4.21E+05	1.8E+04	0		2 stuck CE, erase failed, program failed

Tab. 49: Run Table of Micron 16-Gbit DUT M321, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	1	M1	93	93	24	4.65E+05	1.9E+04	0		
	969	M1	94	94	68	3.06E+05	4.5E+03	1		2 stuck CE, beam error
	506	M1	95	95	41	8.24E+05	2.0E+04	0		DF

Tab. 50: Run Table of Micron 16-Gbit DUT M322, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M1	96	96	9	1.79E+05	2.0E+04	0		
	213	M1	97	97	18	3.70E+05	2.1E+04	0		erase failed, program failed, read ok
		R	97.a				-			

Tab. 51: Run Table of Micron 16-Gbit DUT M323, Kr, LET = 32.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks

	0	M3b	98	98	103	1.00E+05	9.7E+02	1	1220	few 2be, no SEFI, 222 stuck bits, all 1 be
		R	99				-		206	@5 min
		R	100				-		197	@10 min

Tab. 52: Run Table of Micron 16-Gbit DUT M324, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	0	M2	101	99	192	1.87E+05	9.7E+02			
		R	101.a				-		295261	
		R	101.b				-		295162	@5 min
		R	101.c				-		295010	@10 min
		R	101.d				-		294781	@46 min
		R	101.e				-		1867	PC, 2be

Tab. 53: Run Table of Micron 16-Gbit DUT M325, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	247	M1	102	100	44	9.23E+05	2.1E+04			
	304	M1	103	101	18	4.12E+05	2.3E+04			
	286	M1	104	102	9	2.01E+05	2.2E+04			
	217	M1	105	103	39	8.46E+05	2.2E+04			
	328	M1	106	104	16	3.34E+05	2.1E+04			
	269	M1	107	105	24	5.31E+05	2.2E+04			
	280	M1	108	106	50	1.12E+06	2.2E+04			
	391	M1	109	107	40	8.69E+05	2.2E+04			
	375	M1	110	108	7	1.64E+05	2.3E+04			
	267	M1	111	109	72	1.54E+06	2.1E+04			

	450	M1	112	110	75	1.58E+06	2.1E+04			
	560	M1	113	111	64	1.35E+06	2.1E+04			
	587	M1	114	112	18	3.79E+05	2.1E+04			
	419	M1	115	113	45	9.75E+05	2.2E+04			
	446	M1	116	114	70	1.55E+06	2.2E+04			
	576	M1	117	115	38	9.62E+05	2.5E+04			
	548	M1	118	116	78	1.69E+06	2.2E+04			
	622	M1	119	117	17	3.58E+05	2.1E+04			
	472	M1	120	118	26	5.63E+05	2.2E+04			
	417	M1	121	119	32	7.71E+05	2.4E+04			
	441	M1	122	120	46	1.05E+06	2.3E+04			
	495	M1	123	121	9	1.86E+05	2.1E+04			
	350	M1	124	122	18	3.95E+05	2.2E+04			
	318	M1	125	123	24	5.14E+05	2.1E+04			
	316	M1	126	124	127	2.79E+06	2.2E+04			
	649	M1	127	125	59	1.34E+06	2.3E+04			
	675	M1	128	126	49	1.07E+06	2.2E+04			
	628	M1	129	127	20	4.36E+05	2.2E+04			
	474	M1	130	128	6	1.36E+05	2.3E+04			
	327	M1	131	129	91	2.16E+06	2.4E+04			
	652	M1	132	130	55	1.25E+06	2.3E+04			
	629	M1	133	131	9	1.94E+05	2.2E+04			
	435	M1	134	132	10	2.30E+05	2.3E+04			
	348	M1	135	133	15	3.54E+05	2.4E+04			
	324	M1	136	134	7	1.46E+05	2.1E+04			
	252	M1	137	135	12	2.48E+05	2.1E+04			
	232	M1	138	136	9	1.81E+05	2.0E+04			
	218	M1	139	137	59	1.30E+06	2.2E+04			
	408	M1	140	138	41	8.67E+05	2.1E+04			

	368	M1	141	139	21	4.40E+05	2.1E+04			
	318	M1	142	140	22	4.62E+05	2.1E+04			
	286	M1	143	141	26	5.81E+05	2.2E+04			
	347	M1	144	142	5	1.05E+05	2.1E+04			
	246	M1	145	143	91	1.99E+06	2.2E+04			
	521	M1	146	144	30	6.57E+05	2.2E+04			
	441	M1	147	145	111	2.38E+06	2.1E+04			
	677	M1	148	146	15	3.18E+05	2.1E+04			
	492	M1	149	147	26	5.63E+05	2.2E+04			
	442	M1	150	148	6	1.41E+05	2.4E+04			
	319	M1	151	149	16	3.86E+05	2.4E+04			
	309	M1	152	150	17	3.53E+05	2.1E+04			
	293	M1	153	151	19	3.76E+05	2.0E+04			
	270	M1	154	152	42	9.30E+05	2.2E+04			
	387	M1	155	153	33	7.82E+05	2.4E+04			
	394	M1	156	154	24	5.21E+05	2.2E+04			

Tab. 54: Run Table of Micron 16-Gbit DUT M325, Fe, LET = 18.5, 32 blocks tested

Pre-paration	**stuck bits**	**Mode**	**Run IDA**	**Run RADEF**	**Time**	**Fluence**	**Flux**	**Loops**	**Errors**	**Remarks**
2Foil		M1	157	155	38	8.17E+05	2.2E+04			
	966	M1	158	156	50	1.07E+06	2.1E+04			
	1790	M1	159	157	15	3.27E+05	2.2E+04			
		M1	160	158	30	6.56E+05	2.2E+04			no stuck bit re-cording from now, id+, program failed, DF

Tab. 55: Run Table of Micron 16-Gbit DUT M326, Fe, LET = 18.5, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
2Foil		M1	161	159	26	5.75E+05	2.2E+04			ID incom-plete, DF

Tab. 56: Run Table of Micron 16-Gbit DUT M327, Fe, LET = 18.5, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
2Foil		M1	162	160	42	9.44E+05	2.2E+04			CS pc-4
		M1	163	161	31	6.89E+05	2.2E+04			perm. CE
		M1	164	162	9	2.14E+05	2.4E+04			
		M1	165	163	16	3.75E+05	2.3E+04			operating error
		M1	166	164	15	3.64E+05	2.4E+04			
		M1	167	165	43	1.07E+06	2.5E+04			
		M1	168	166	9	2.03E+05	2.3E+04			
		M1	169	167	35	9.19E+05	2.6E+04			
		M1	170	168	22	5.23E+05	2.4E+04			
		M1	171	169	16	3.97E+05	2.5E+04			erase failed, program failed

Tab. 57: Run Table of Micron 16-Gbit DUT M328, Fe, LET = 18.5, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
1Foil		M1	172	170	58	1.40E+06	2.4E+04			
		M1	173	171	27	6.51E+05	2.4E+04			
		M1	174	172	45	1.08E+06	2.4E+04			
		M1	175	173	7	1.72E+05	2.5E+04			operating error
		M1	176	174	23	5.63E+05	2.4E+04			

		M1	177	175	7	1.70E+05	2.4E+04			
		M1	178	176	61	1.40E+06	2.3E+04			
		M1	179	177	25	6.12E+05	2.4E+04			
		M1	180	178	15	3.65E+05	2.4E+04			
		M1	181	179	15	3.60E+05	2.4E+04			
	1101	M1	182	180	40	9.63E+05	2.4E+04			
		M1	183	181	16	4.20E+05	2.6E+04			
		M1	184	182	15	3.82E+05	2.5E+04			
		M1	185	183	20	4.89E+05	2.4E+04			
		M1	186	184	11	2.44E+05	2.2E+04			
		M1	187	185	95	2.34E+06	2.5E+04			
		M1	188	186	59	1.48E+06	2.5E+04			
		M1	189	187	62	1.48E+06	2.4E+04			
		M1	190	188	37	8.74E+05	2.4E+04			
		M1	191	189	57	1.37E+06	2.4E+04			program failed
	1864	M1	192	190	10	2.37E+05	2.4E+04			ID incom-plete, DF

Tab. 58: Run Table of Micron 16-Gbit DUT M329, Fe, LET = 18.5, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
1Foil		M1	193	191	11	2.79E+05	2.5E+04			
		M1	194	192	97	2.34E+06	2.4E+04			
		M1	195	193	25	6.09E+05	2.4E+04			
		M1	196	194	8	1.97E+05	2.5E+04			
		M1	197	195	29	6.70E+05	2.3E+04			
		M1	198	196	7	1.82E+05	2.6E+04			
		M1	199	197	42	1.02E+06	2.4E+04			
		M1	200	198	17	3.89E+05	2.3E+04			

		M1	201	199	42	1.00E+06	2.4E+04			
		M1	202	200	41	9.59E+05	2.3E+04			
	497	M1	203	201	9	2.08E+05	2.3E+04			
		M1	204	202	108	2.57E+06	2.4E+04			prog-
		M1	205	203	109	6.94E+05	6.4E+03			
		M1	206	204	73	1.77E+06	2.4E+04			
		M1	207	205	63	1.56E+06	2.5E+04			
		M1	208	206	46	1.11E+06	2.4E+04			
		M1	209	207	36	9.39E+05	2.6E+04			
		M1	210	208	111	2.77E+06	2.5E+04			
		M1	211	209	20	4.78E+05	2.4E+04			
		M1	212	210	77	1.91E+06	2.5E+04			
	691	M1	213	211	14	3.41E+05	2.4E+04			
		M1	214	212	33	8.26E+05	2.5E+04			
		M1	215	213	5	1.27E+05	2.5E+04			
		M1	216	214	25	6.46E+05	2.6E+04			
		M1	217	215	10	2.53E+05	2.5E+04			
		M1	218	216	10	2.58E+05	2.6E+04			
		M1	219	217	6	1.29E+05	2.2E+04			
		M1	220	218	19	4.88E+05	2.6E+04			
		M1	221	219	8	2.14E+05	2.7E+04			
		M1	222	220	7	1.78E+05	2.5E+04			
	259	M1	223	221	13	3.36E+05	2.6E+04			
		M1	224	222	33	8.51E+05	2.6E+04			
		M1	225	223	8	2.13E+05	2.7E+04			
		M1	226	224	57	1.50E+06	2.6E+04			
		M1	227	225	19	5.21E+05	2.7E+04			
		M1	228	226	10	2.56E+05	2.6E+04			
		M1	229	227	8	2.57E+05	3.2E+04			

		M1	230	228	21	6.47E+05	3.1E+04			
		M1	231				-			Tuesday
		M1	232	229	24	5.10E+05	2.1E+04			
		M1	233	230	25	5.32E+05	2.1E+04			
		M1	234	231	36	8.09E+05	2.2E+04			
		M1	235	232	15	3.42E+05	2.3E+04			
		M1	236	233	30	7.72E+05	2.6E+04			
		M1	237	234	18	5.95E+05	3.3E+04			
		M1	238	235	84	2.06E+06	2.5E+04			
		M1	239	236	23	5.19E+05	2.3E+04			
		M1	240	237	10	2.31E+05	2.3E+04			
		M1	241	238	36	8.62E+05	2.4E+04			
		M1	242	239	17	3.96E+05	2.3E+04			RADEF fluence "Inf"
		M1	243	240	17	3.97E+05	2.3E+04			
		M1	244	241	7	1.90E+05	2.7E+04			
		M1	245	242	69	1.68E+06	2.4E+04			
		M1	246	243	8	1.84E+05	2.3E+04			
		M1	247	244	10	2.41E+05	2.4E+04			
		M1	248	245	19	4.67E+05	2.5E+04			
		M1	249	246	38	1.06E+06	2.8E+04			
		M1	250	247	8	2.05E+05	2.6E+04			
		M1	251	248	26	7.67E+05	3.0E+04			
		M1	252	249	42	1.20E+06	2.9E+04			
		M1	253	250	23	5.22E+05	2.3E+04			
		M1	254	251	10	2.70E+05	2.7E+04			
		M1	255	252	37	1.06E+06	2.9E+04			
		M1	256	253	41	1.11E+06	2.7E+04			
		M1	257	254	20	5.61E+05	2.8E+04			

		M1	258	255	20	5.37E+05	2.7E+04			
		M1	259	256	32	8.86E+05	2.8E+04			
		M1	260	257	9	2.58E+05	2.9E+04			
		M1	261	258	36	1.11E+06	3.1E+04			
		M1	262	259	5	1.63E+05	3.3E+04			
2Foil		M1	263	260	58	1.77E+06	3.1E+04			
		M1	264	261	6	1.80E+05	3.0E+04			
		M1	265	262	11	3.28E+05	3.0E+04			
		M1	266	263	38	1.02E+06	2.7E+04			
		M1	267	264	63	1.13E+06	1.8E+04			
		M1	268	265	43	7.36E+05	1.7E+04			
		M1	269	266	61	1.20E+06	2.0E+04			DF

Tab. 59: Run Table of Micron 16-Gbit DUT M330, Fe, LET = 18.5, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
1Foil		M1	270	267	128	2.34E+06	1.8E+04			
		M1	271	268	19	3.61E+05	1.9E+04			
		M1	272	269	7	1.18E+05	1.7E+04			
		M1	273	270	9	1.50E+05	1.7E+04			
		M1	274	271	28	4.69E+05	1.7E+04			
		M1	275	272	15	2.30E+05	1.5E+04			
		M1	276	273	10	1.89E+05	1.9E+04			
		M1	277	274	14	2.34E+05	1.7E+04			
		M1	278	275	26	3.01E+05	1.2E+04			
		M1	279	276	51	5.75E+05	1.1E+04			
		M1	280				-			operating error
		M1	281				-			operating error

		M1	282	277	10	1.43E+05	1.4E+04			DF
		M1	283				-			
		M1	284				-			

Tab. 60: Run Table of Micron 16-Gbit DUT M331, Fe, LET = 18.5, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M1	285	278	236	3.05E+06	1.3E+04			
		M1	286	279	8	1.14E+05	1.4E+04			
		M1	287	280	112	1.33E+06	1.2E+04			
		M1	288	281	77	1.49E+06	1.9E+04			
		M1		282	46	9.26E+05	2.0E+04			
		M1	289	283	6	1.30E+05	2.2E+04			
		M1	290	284	10	2.81E+05	2.8E+04			
		M1	291	285	128	2.91E+06	2.3E+04			
		M1	292	286	14	3.54E+05	2.5E+04			
		M1	293	287	74	1.68E+06	2.3E+04			
		M1	294	288	63	1.73E+06	2.7E+04			
		M1	295	289	64	1.70E+06	2.7E+04			
		M1	296	290	14	3.21E+05	2.3E+04			
		M1	297	291	12	2.83E+05	2.4E+04			
		M1	298	292	12	2.82E+05	2.4E+04			
		M1	299	293	67	1.57E+06	2.3E+04			
		M1	300	294	10	2.82E+05	2.8E+04			
		M1	301	295	22	5.84E+05	2.7E+04			
		M1	302	296	28	5.31E+05	1.9E+04			
		M1	303	297	17	3.88E+05	2.3E+04			
		M1	304	298	27	6.58E+05	2.4E+04			
		M1	305	299	70	1.48E+06	2.1E+04			

		M1	306	300	41	9.58E+05	2.3E+04			
		M1	307	301	17	4.37E+05	2.6E+04			
		M1	308	302	67	1.64E+06	2.4E+04			
		M1	309	303	96	2.01E+06	2.1E+04			
		M1	310	304	28	7.42E+05	2.7E+04			
		M1	311	305	33	7.25E+05	2.2E+04			
		M1	312	306	29	7.16E+05	2.5E+04			
		M1	313	307	32	6.59E+05	2.1E+04			
		M1	314	308	7	1.43E+05	2.0E+04			
		M1	315	309	18	3.48E+05	1.9E+04			
		M1	316	310	27	5.22E+05	1.9E+04			
		M1	317	311	16	3.54E+05	2.2E+04			
		M1	318	312	83	1.69E+06	2.0E+04			
		M1	319	313	15	3.93E+05	2.6E+04			
		M1	320	314	31	7.84E+05	2.5E+04			
		M1	321	315	56	1.34E+06	2.4E+04			
		M1	322	316	70	2.07E+06	3.0E+04			
		M1	323	317	14	3.05E+05	2.2E+04			DF

Tab. 61: Run Table of Micron 16-Gbit DUT M332, Fe, LET = 18.5, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
-		M3b	324	318	242	1.00E+05	4.1E+02		748	no SEFIs
		BG							61	
		R	325				-		54	@5min
		R	326				-		56	@10min
		R	327				-		52	@15min
		R	328				-		53	@20min
		R	329				-		52	@25min

		R	330				-		49	@30min
		R	331				-		44	after lunch

Tab. 62: Run Table of Micron 16-Gbit DUT M333, Fe, LET = 18.5, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M1	332	319	48	7.82E+04	1.6E+03			
		M1	333	320	35	6.52E+04	1.9E+03			program failed, erase functional, read 0xFF
		M1	334				-			

Tab. 63: Run Table of Micron 16-Gbit DUT M334, Xe, LET = 60, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M1	335	321	158	3.72E+04	2.4E+02			
		M1	336	322	524	1.20E+05	2.3E+02			program failed

Tab. 64: Run Table of Micron 16-Gbit DUT M335, Xe, LET = 60, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M1	337	323	1373	3.20E+05	2.3E+02			program failed, read 0xFF

Tab. 65: Run Table of Micron 16-Gbit DUT M336, Xe, LET = 60, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M1	338	324	302	7.19E+04	2.4E+02			program failed

Tab. 66: Run Table of Micron 16-Gbit DUT M337, Xe, LET = 60, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M1	339	325	423	9.39E+04	2.2E+02			
		M1	340				-			program failed, erase failed

Tab. 67: Run Table of Micron 16-Gbit DUT M338, Xe, LET = 60, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M1	341				-			
		M1	342				-			without beam
		M3b	343	326	134	4.02E+04	3.0E+02		1860	1ce
		BG	-				-		1262	1ce
		R	344				-		1252	@5min, 1ce
		R	345				-		1565	@10min, 1ce
		R	346				-		2010	@15min, 1ce
		R	347				-		1576	@20min, 1ce
		R	348				-		1563	@25min,1ce
		R	349				-		1451	@30min,1ce

Tab. 68: Run Table of Micron 16-Gbit DUT M339, Xe, LET = 60, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M1	350	327	3	8.45E+04	2.8E+04			operating error
		M1		328	192	5.91E+06	3.1E+04			still IDA 350,

										increase flux
		M1	351	329	1067	1.00E+08	9.4E+04		17993	no SEFIs

Tab. 69: Run Table of Micron 16-Gbit DUT M340, N, LET = 1.8, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
		M3b	352	330	110	1.02E+07	9.3E+04		4641	
		BG					-		0	
		M3b	353	331	994	1.00E+08	1.0E+05		46396	
		BG	354				-		1	

Tab. 70: Run Table of Micron 16-Gbit DUT M341, N, LET = 1.8, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
-		M1	355	332	83	3.74E+05	4.5E+03			
		M1	356	333	107	4.75E+05	4.4E+03			
		M1	357	334	18	7.12E+04	4.0E+03			
3Foil		M1	358	335	181	7.69E+05	4.2E+03			prog-
		M1	359	336	98	4.19E+05	4.3E+03			
		M1	360	337	181	8.66E+05	4.8E+03			
		M1	361	338	269	1.46E+06	5.4E+03			
		M1	362	339	143	1.43E+06	1.0E+04			
		M1	363	340	94	9.59E+05	1.0E+04			
		M1	364	341	168	1.75E+06	1.0E+04			
		M1	365	342	433	4.88E+06	1.1E+04			
		M1	366	343	32	3.60E+05	1.1E+04			
		M1	367	344	107	2.11E+06	2.0E+04			prog-
		M1	368	345	63	1.28E+06	2.0E+04			
		M1	369	346	37	7.92E+05	2.1E+04			

		M1	370	347	28	5.69E+05	2.0E+04			
		M1	371	348	21	4.25E+05	2.0E+04			
		M1	372	349	118	2.55E+06	2.2E+04			
		M1	373	350	31	6.31E+05	2.0E+04			erase-
		M1	374	351	58	1.20E+06	2.1E+04			
		M1	375	352	56	1.11E+06	2.0E+04			
		M1	376	353	36	7.31E+05	2.0E+04			
		M1	377	354	14	3.10E+05	2.2E+04			
		M1	378	355	113	2.61E+06	2.3E+04			
		M1	379	356	22	9.35E+05	4.3E+04			
		M1	380	357	44	1.85E+06	4.2E+04			
		M1	381	358	12	5.03E+05	4.2E+04			
		M1	382	359	8	2.95E+05	3.7E+04			
		M1	383	360	21	8.23E+05	3.9E+04			
		M1	384	361	31	1.29E+06	4.2E+04			
		M1	385	362	105	4.35E+06	4.1E+04			
		M1	386	363	11	4.33E+05	3.9E+04			
		M1	387	364	122	5.19E+06	4.3E+04			
		M1	388	365	9	3.67E+05	4.1E+04			
		M1	389	366	9	3.82E+05	4.2E+04			
		M1	390	367	24	1.04E+06	4.3E+04			
		M1	391	368	32	1.37E+06	4.3E+04			
		M1	392	369	35	1.41E+06	4.0E+04			
		M1	393	370	57	2.36E+06	4.1E+04			DF

Tab. 71: Run Table of Micron 16-Gbit DUT M340, Ar, LET = 10.1, 32 blocks tested

Pre-paration	**stuck bits**	**Mode**	**Run IDA**	**Run RADEF**	**Time**	**Fluence**	**Flux**	**Loops**	**Errors**	**Remarks**
3Foil		M1	394	371	11	4.81E+05	4.4E+04			prog-

		M1	395	372	17	7.29E+05	4.3E+04			
		M1	396	373	75	3.00E+06	4.0E+04			
		M1	397	374	15	6.29E+05	4.2E+04			
		M1	398	375	39	1.62E+06	4.2E+04			
		M1	399	376	15	5.94E+05	4.0E+04			
		M1	400	377	33	1.39E+06	4.2E+04			
		M1	401	378	7	2.60E+05	3.7E+04			
		M1	402	379	9	4.28E+05	4.8E+04			
		M1	403	380	26	1.12E+06	4.3E+04			
		M1	404	381	7	3.02E+05	4.3E+04			
		M1	405	382	16	6.86E+05	4.3E+04			
		M1	406	383	7	2.91E+05	4.2E+04			
		M1	407	384	47	2.09E+06	4.4E+04			
		M1	408	385	104	5.14E+06	4.9E+04			
		M1	409	386	68	2.47E+06	3.6E+04			
		M1	410	387	25	8.14E+05	3.3E+04			
		M1	411	388	20	6.74E+05	3.4E+04			
		M1	412	389	44	1.50E+06	3.4E+04			
		M1	413	390	11	3.85E+05	3.5E+04			
		M1	414	391	30	1.09E+06	3.6E+04			
		M1	415	392	44	1.55E+06	3.5E+04			
		M1	416	393	7	2.68E+05	3.8E+04			
		M1	417	394	29	9.81E+05	3.4E+04			
		M1	418	395	20	7.38E+05	3.7E+04			
		M1	419	396	28	9.51E+05	3.4E+04			
		M1	420	397	40	1.53E+06	3.8E+04			
		M1	421	398	6	2.20E+05	3.7E+04			
		M1	422	399	11	4.47E+05	4.1E+04			
		M1	423	400	45	1.71E+06	3.8E+04			

		M1	424	401	20	7.78E+05	3.9E+04			
		M1	425	402	15	5.42E+05	3.6E+04			
		M1	426	403	11	4.13E+05	3.8E+04			
		M1	427	404	7	2.60E+05	3.7E+04			
		M1	428	405	164	6.38E+06	3.9E+04			
		M1	429	406	13	4.61E+05	3.5E+04			
		M1	430	407	18	6.75E+05	3.8E+04			
		M1	431	408	12	5.01E+05	4.2E+04			
		M1	432	409	24	8.90E+05	3.7E+04			
		M1	434	410	37	1.44E+06	3.9E+04			
		M1	435	411	10	3.69E+05	3.7E+04			
		M1	436	412	81	3.13E+06	3.9E+04			
		M1	437	413	23	9.20E+05	4.0E+04			
		M1	438	414	23	8.37E+05	3.6E+04			
		M1	439	415	9	3.84E+05	4.3E+04			
		M1	440	416	19	7.45E+05	3.9E+04			
		M1	441	417	19	7.64E+05	4.0E+04			
		M1	442	418	14	5.83E+05	4.2E+04			
		M1	443	419	43	1.82E+06	4.2E+04			
		M1	444	420	31	1.10E+06	3.5E+04			
		M1	445	421	15	5.28E+05	3.5E+04			
		M1	446	422	30	1.15E+06	3.8E+04			
		M1	447	423	36	1.47E+06	4.1E+04			
		M1	448	424	9	3.27E+05	3.6E+04			
		M1	449	425	29	1.17E+06	4.0E+04			
		M1	450		0	0.00E+00	-			DF
		M1	451				-			

Tab. 72: Run Table of Micron 16-Gbit DUT M342, Ar, LET = 10.1, 32 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
-		M3b	452	426	104	1.01E+05	9.7E+02		401	
		BG					-		4	
		M3b	453	427	467	1.00E+07	2.1E+04		36497	
		BG					-		289	
		R	453.a				-		252	@5min
		R	453.b				-		234	@10min
		R	453.c				-		227	@15min
		R	453.d				-		210	@20min
		R	453.e				-		199	@25min
		R	453.f				-		189	@30min

Tab. 73: Run Table of Micron 16-Gbit DUT M343, Ar, LET = 10.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
-		M3b	454	428	484	1.00E+07	2.1E+04		14290	
		BG					-		0	
		M3b	455	429	354	1.00E+08	2.8E+05		140102	
		BG					-		30	
		R	455.a				-		26	@5min
		R	455.b				-		25	@10min
		R	455.c				-		23	@15min
		R	455.d				-		23	@20min
		R	455.e				-		24	@25min
		R	455.f				-		23	@30min

Tab. 74: Run Table of Micron 16-Gbit DUT M344, Ne, LET = 3.6, 64 blocks tested

Pre-	stuck	Mode	Run	Run	Time	Fluence	Flux	Loops	Errors	Remarks

paration	bits		IDA	RADEF						
		M2	456	430	65	2.00E+07	3.1E+05		>>	
		R	456.a				-		26339	PC
		M2	457	431	61	2.05E+07	3.4E+05		>>	
		R	457.a				-			no PC
		R	457.b				-		26510	PC

Tab. 75: Run Table of Micron 16-Gbit DUT M345, Ne, LET = 3.6, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	133	R	458							

Tab. 76: Run Table of Micron 16-Gbit DUT M324, Kr, LET = 32.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	30	R	459							

Tab. 77: Run Table of Micron 16-Gbit DUT M333, Fe, LET = 18.5, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	1175	R	460							

Tab. 78: Run Table of Micron 16-Gbit DUT M339, Xe, LET = 60, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	93	R	461							

Tab. 79: Run Table of Micron 16-Gbit DUT M343, Ar, LET = 10.1, 64 blocks tested

Pre-paration	stuck bits	Mode	Run IDA	Run RADEF	Time	Fluence	Flux	Loops	Errors	Remarks
	13	R	462							

Tab. 80: Run Table of Micron 16-Gbit DUT M344, Ne, LET = 3.6, 64 blocks tested

9 Package pictures

Fig. 39: Micron MT29F16G08ABACAWP-IT:C NAND-Flash

Fig. 40: Micron MT29F16G08ABACAWP-IT:C NAND-Flash

Fig. 41: Micron MT29F32G08ABAAAWP-IT:A NAND-Flash

Fig. 42: Micron MT29F8G08AAA-WP-A

Fig. 43: Samsung K9F8G08U0M-PCB0 NAND-Flash

Fig. 44: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 45: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 46: Samsung K9WBG08U1M-PIB0 NAND-Flash

10 References

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