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Heavy Ion SEE Test

of

4 x 8-Gbit Samsung and 16-Gbit Micron

SLC NAND-Flash Memory Devices

TAMU Texas, December 4 – 7, 2012

Test Report

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Contents

1 Introduction

From December 4th to December 7th 2012, we performed a heavy ion test campaign with NAND-Flash and DDR3 SDRAM devices at Texas A&M University (TAMU). This document reports on the findings for NAND-Flash devices.

Most of the previously published SEU cross sections are for normal ion incidence [1] [2][3].

However, in space the ion flux is omni-directional. In consequence the omni-directional cross section should be used for the calculation of the error rates. The omni-directional cross section can be calculated by ray tracing through the sensitive volume [4], provided the shape and dimensions of the sensitive volume are known. However, detailed knowledge of the device structure is needed to define this sensitive volume. For commercial parts, which are the only available NAND-Flash parts, those design details are typically not disclosed. The other way around, the measurement of the angular dependence of the SEU cross section can provide some indications about the shape of the sensitive volume. Accordingly, an experimental investigation of the angular dependence of the SEU cross section was performed for two types of SLC NAND-Flash devices from Samsung and Micron.

2 Test Facility

The tests were performed at the Cyclotron Institute of the Texas A&M University, College Station, Texas, USA, December 4 – 7, 2012.

The used ion cocktail is the 25MeV/amu ion cocktail described in Tab. 1, Fig. 1.

Tab. 1: TAMU 25 MeV/amu ion cocktail

Ion	Total Energy [MeV]	Range in Silicon [µm]	LET [MeV cm^2 mg^{-1}]	
			Initial (air)	at Bragg Peak
^{84}Kr	2081	332	19.8	41.4

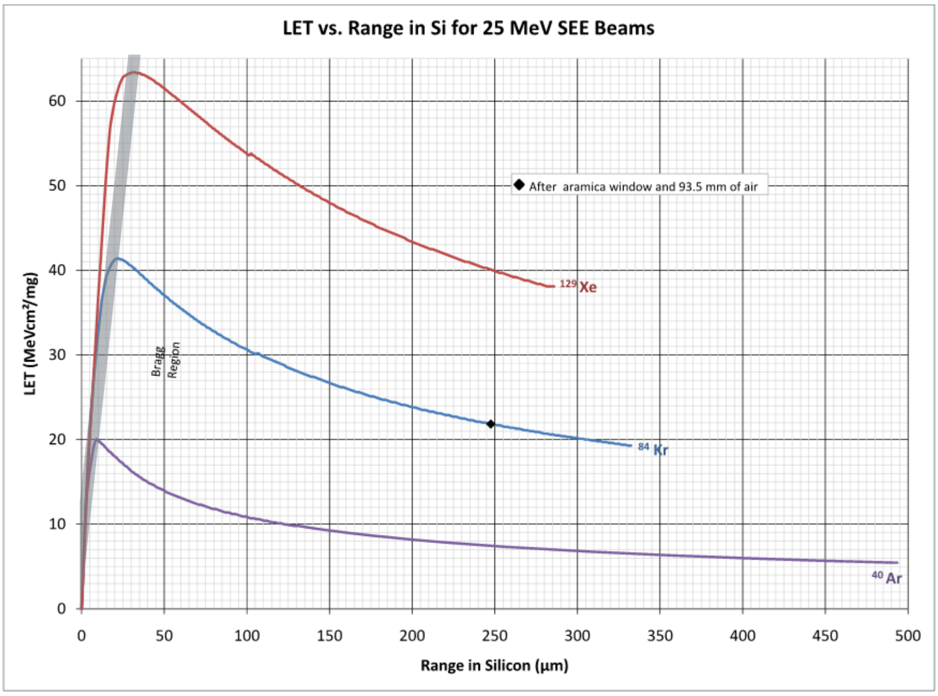

Fig. 1: LET vs. Range in Si for 25 MeV SEE Beams (high LET)

The tilting exercise was performed in air with Kr ions. Because of the tilting setup an airgap of 93.5 mm was needed. Tab. 2 shows the layer stack which was used to calculate the beam parameters (Tab. 3) with the TAMU Single Event Upset System Supervisor (SEUSS).

Tab. 2: Layerstack

material	**thickness**
aramica	1 mil
air gas	93.5 mm
silicon	10 µm

Tab. 3: Beam parameters

Ion	**Beam Energy**	**Beam Energy**	**Nominal LET / Effective LET**	**Nominal Range**
	[MeV / amu]	**[MeV]**	**[MeV cm² mg^{-1}]**	**[µm]**
^{84}Kr	20	1682	21.8	248.6

Assuming at worst 15 µm of overlayer thickness, the range of the ion should be larger than 170 µm at 85deg angle.

The Fluence is counted as for normal incidence independent from the tilting angles. The LET is not corrected with respect to the tilting angles.

3 DUTs

The tested DUTs [5] [6] are described in Tab. 4. Tab. 5 presents the DUTs used for comparison between the TAMU test results and the previous findings at RADEF, Finland. All parts are single die packages (SDP), except the Samsung 4x8-Gbit part which is a quad die package (QDP).

Manu-facturer	Ca-pacity [Gbit]	Package	Part Number	Date Code	Lot Code	Sam-ples	IDA ID
Samsung	4x8	QDP	K9WBG08U1M-PIB0	0925	FME071P2, IDA Lot G	4	SI21, SI22, SI23, SI26
Micron	16	SDP	MT29F16G08ABACAWP-IT:C	1146	unknown	2	M356, M357

Tab. 4: Tested DUTs

Manu-facturer	Ca-pacity [Gbit]	Package	Part Number	Date Code	Lot Code
Samsung	8	SDP	K9F8G08U0M	0725	FFE006XX IDA Lot E
Samsung	4x8	QDP	K9WBG08U1M-PIB0	0816	FFC042X1, IDA Lot D
Samsung	4x8	QDP	K9WBG08U1M-PIB0	0837	FMH030X2 IDA Lot F
Samsung	4x8	QDP	K9WBG08U1M-PIB0	0925	FME071P2, IDA Lot G
Micron	16	SDP	MT29F16G08ABACAWP-IT:C	1146	unknown
Micron	32	SDP	MT29F32G08ABAAAWP-IT:A	1130	unknown

Tab. 5: DUTs for comparison

4 DUT Preparation

First all DUTs were marked by an individual ID and were checked for factory marked bad blocks. The ID and the bad block table were programmed into block 0 which is guaranteed to be valid by the manufacturer for every DUT. These bad blocks were not accessed by erase or program operations anymore.

The 48-pin TSOP1 packages were opened for direct access of the ion beam to the surface of the die. In case of the Samsung device the package consists of 4 dies. During the test only the upper die is directly exposed to the ion beam. Therefore only this die is used for the test.

Fig. 2 and Fig. 3 show the orientation of the die with respect to the TSOP1 package.

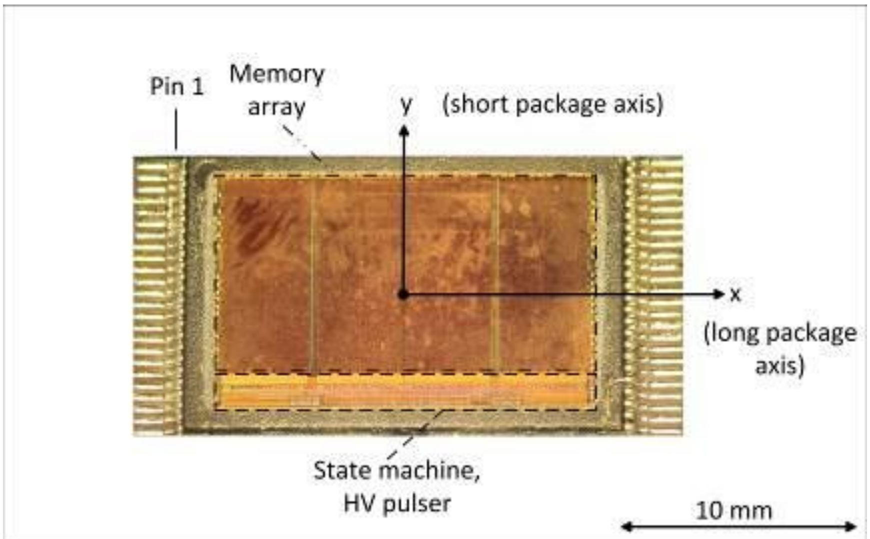

Fig. 2: Die orientation of the Samsung 4x8-Gbit NAND-Flash

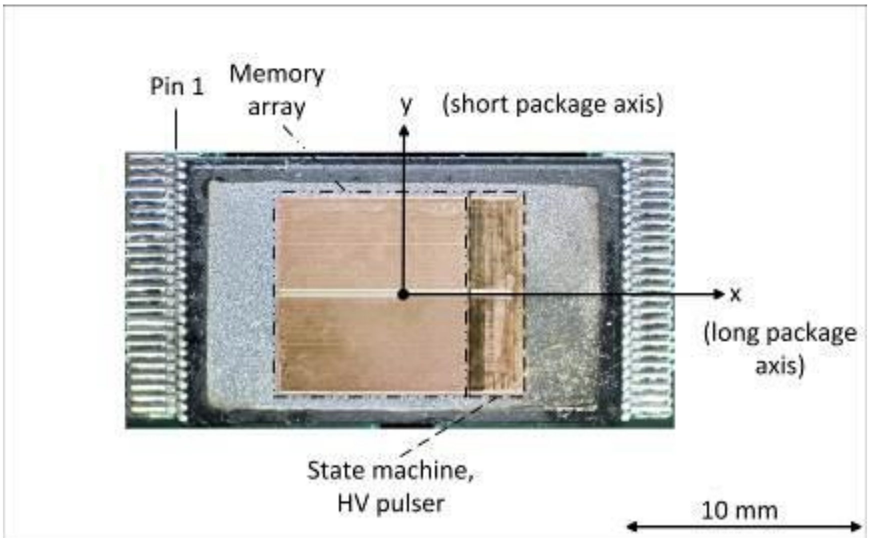

Fig. 3: Die orientation of the Micron 16-Gbit NAND-Flash

The opening is done by drop etching with fuming nitric acid. The device is placed on a mounting plate and is covered with Teflon tape. A window is cut into this tape. Then the device is heated to about 70°C, and an acid drop is given into the window. Thereafter the device is rinsed with water and then with acetone. This process of etching and rinsing is repeated many times until the die surface is free of plastic cover.

After the opening procedure the functionality check was repeated.

5 Test procedure

5.1 Test mode and error classification

The focus of this test is to determine the storage array response to Kr ions for two types of NAND-Flash devices at slant ion incidence with respect to normal ion incidence.

Fig. 4 shows the IDA Error Classification Scheme. Errors originating from the storage array are summarized in Class A.

In order to get rid of all SEFI related error patterns (Class B and C) and Device Failures (Class D), the DUTs were power cycled after each irradiation run and during the evaluation the test data were checked for SEFI related error patterns.

All tests were performed with a checkerboard pattern which is inverted after each page and after each block in biased Storage Mode. Before irradiation, the pattern is written into the DUT and verified. After irradiation, a power cycle of the DUT is performed in order to get rid of SEFI related errors. Then the content of the device is read and compared to the pattern.

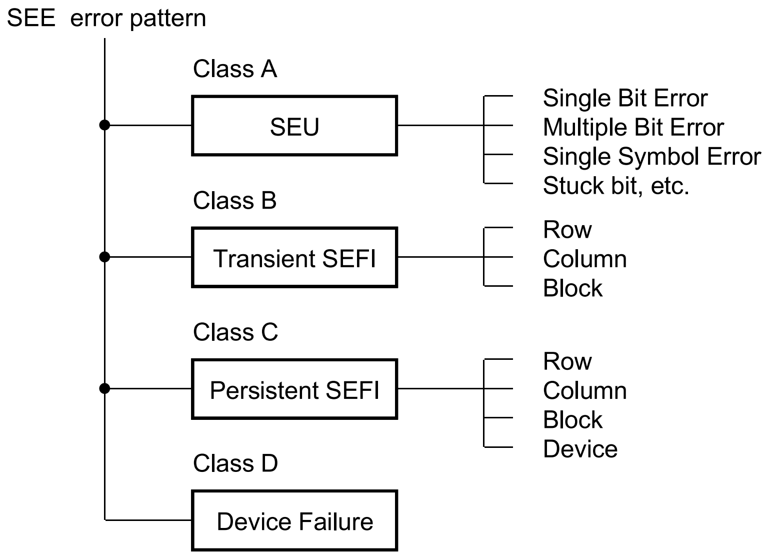

Fig. 4: Error Classification Scheme

5.2 Tilting setup

For fast and efficient tilting of the DUT, the IDA NAND-Flash test bench is equipped with our auxiliary tilting equipment (Fig. 5).

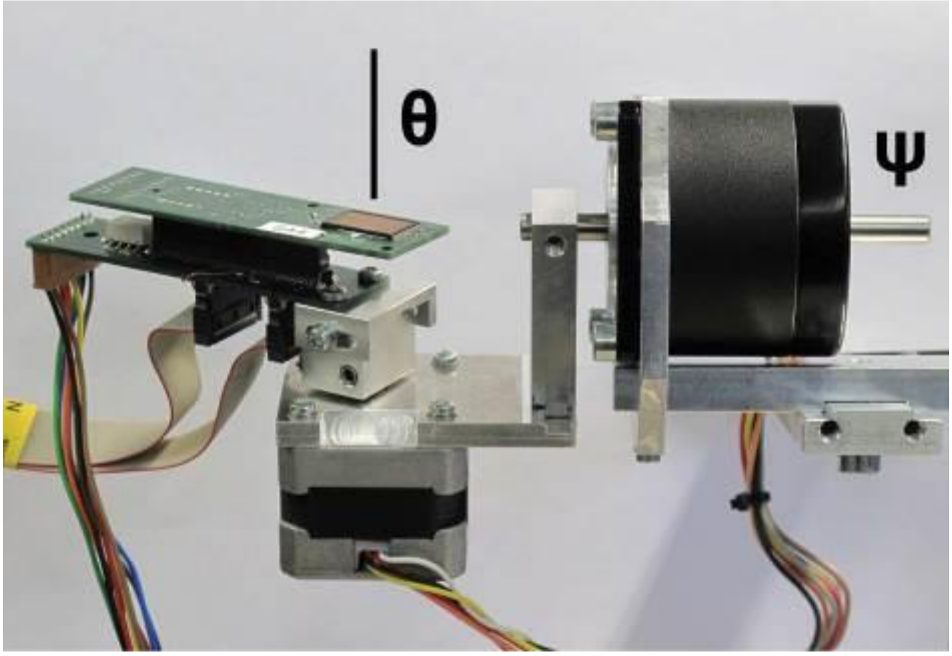

Fig. 5: Tilting setup

The DUT was rotated by the azimuth angle Θ and tilted by the elevation angle ψ (Fig. 6).

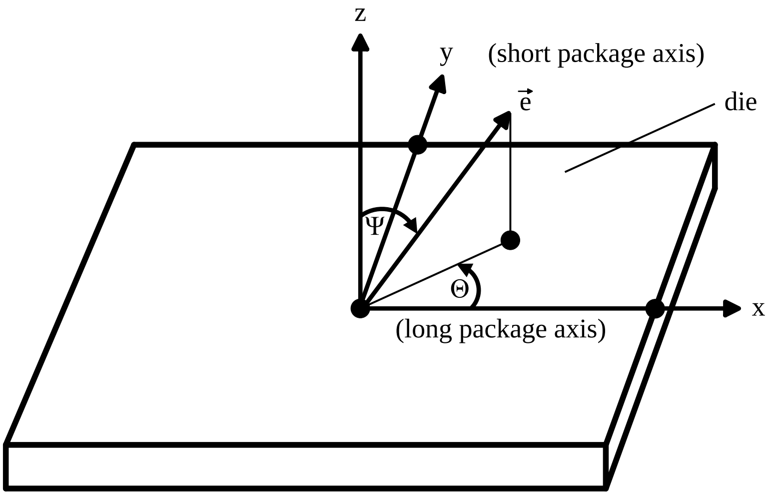

Fig. 6: Definition of Azimuth Angle Θ and Elevation Angle ψ, vector e parallel to the direction of ion incidence

6 Test Results

6.1 SEU cross section for normal ion incidence

First the cross section value for Kr ions at TAMU is plotted into the complete cross section diagram determined at RADEF, Finland (Fig. 7). The cross section points for Kr from TAMU fit well into the complete cross sections determined at RADEF. All values derived from TAMU remain little below the Weibull approximation of the RADEF values.

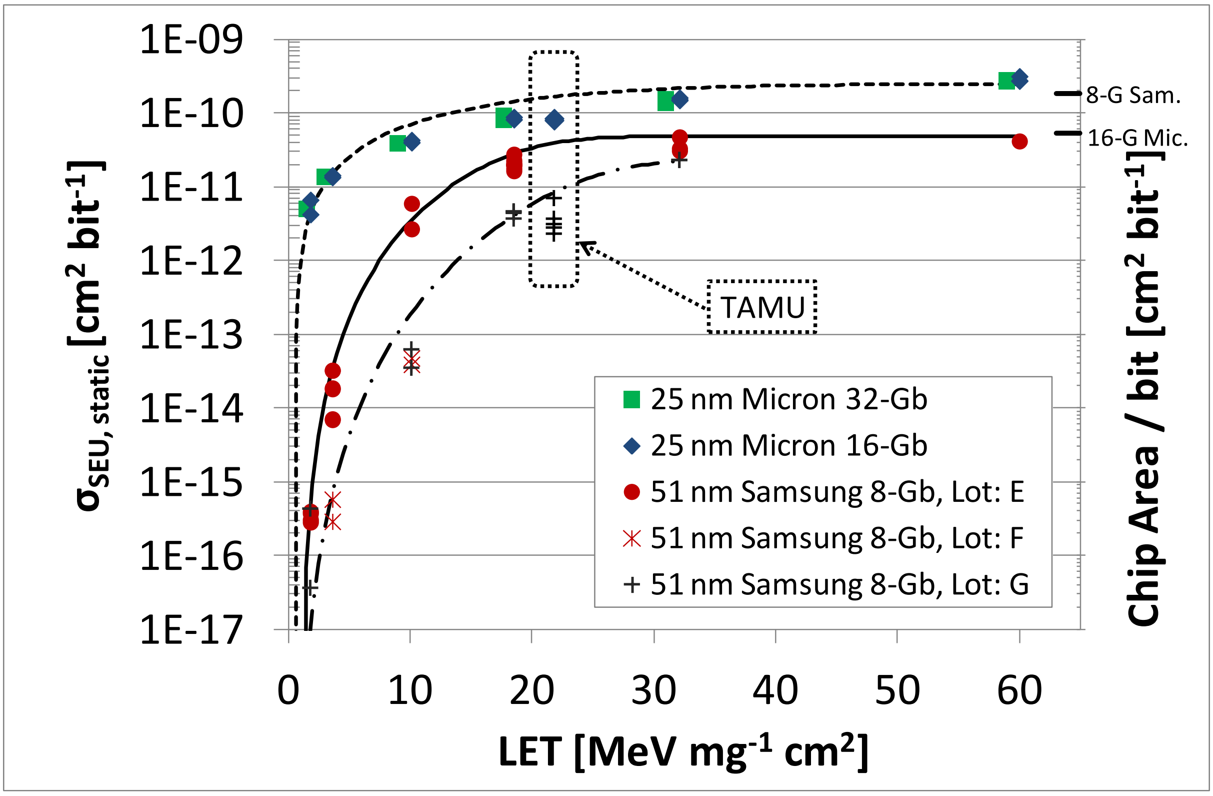

Fig. 7: Cross section at normal incidence, comparison between RADEF and TAMU values

6.2 Omnidirectional SEU cross section of Samsung 4x8-Gbit NAND-Flash

The polar diagrams of Fig. 8 and Fig. 9 show the SEU cross section of the Samsung device, normalized by the value at normal ion incidence ($\psi = 0°$), represented by the circle of radius 1. The polar diagrams show a dipole shape with the main dipole axis in parallel to the long die axis.

For $\psi \leq 75°$, the cross section remains within this circle for all azimuth angles Θ (Fig. 8).

For $\psi \geq 75°$, (Fig. 9), the dipole shape grows along the long axis of the die ($\Theta = 0°$ and $\Theta = 180°$), and exceeds the normal incidence circle up to a factor of four at $\psi = 85°$.

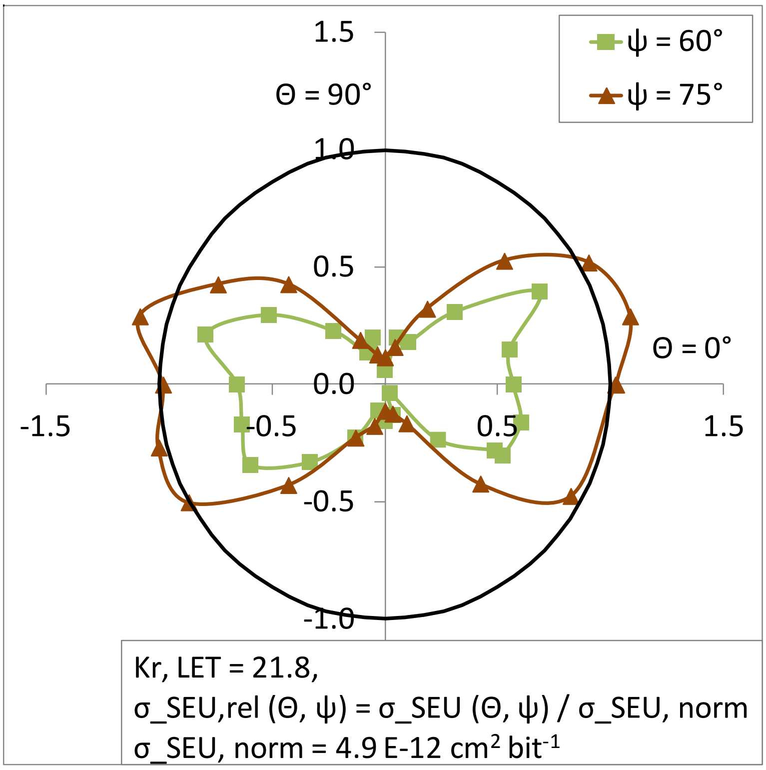

Fig. 8: Normalized SEU cross section, ψ ≤ 75°, Samsung 4x8-Gbit NAND-Flash

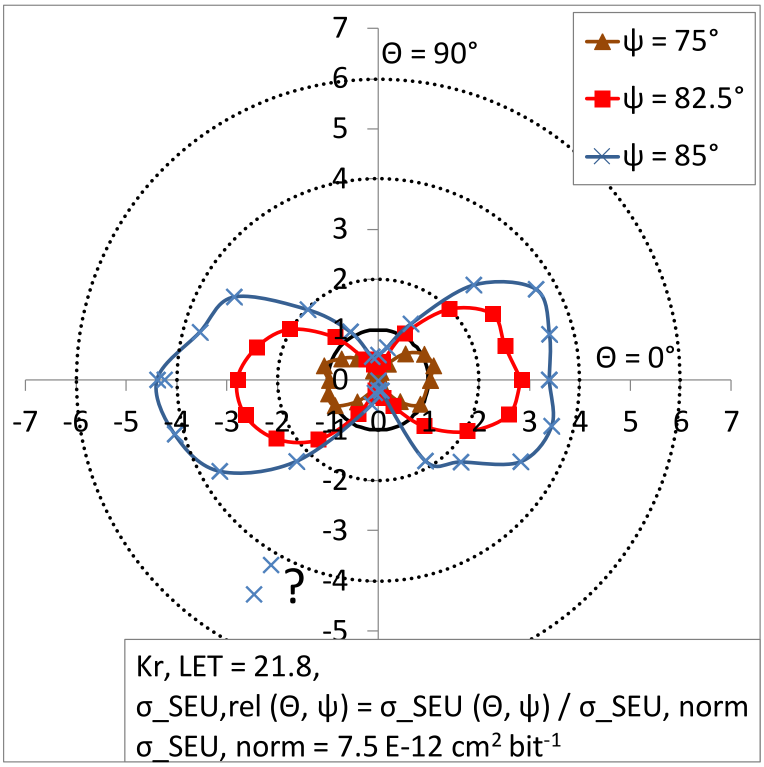

Fig. 9: Normalized SEU cross section, 75° ≤ ψ ≤ 85°, Samsung 4x8-Gbit NAND-Flash

6.3 Omnidirectional SEU cross section of Micron 16-Gbit NAND-Flash

Fig. 10 and Fig. 11 show the respective diagrams for the Micron device. In contrast to Samsung, the effect of tilting is less significant. Also at slant ion incidence (ψ = 82.5°, Fig. 11), the SEU cross section remains near the normal incidence circle.

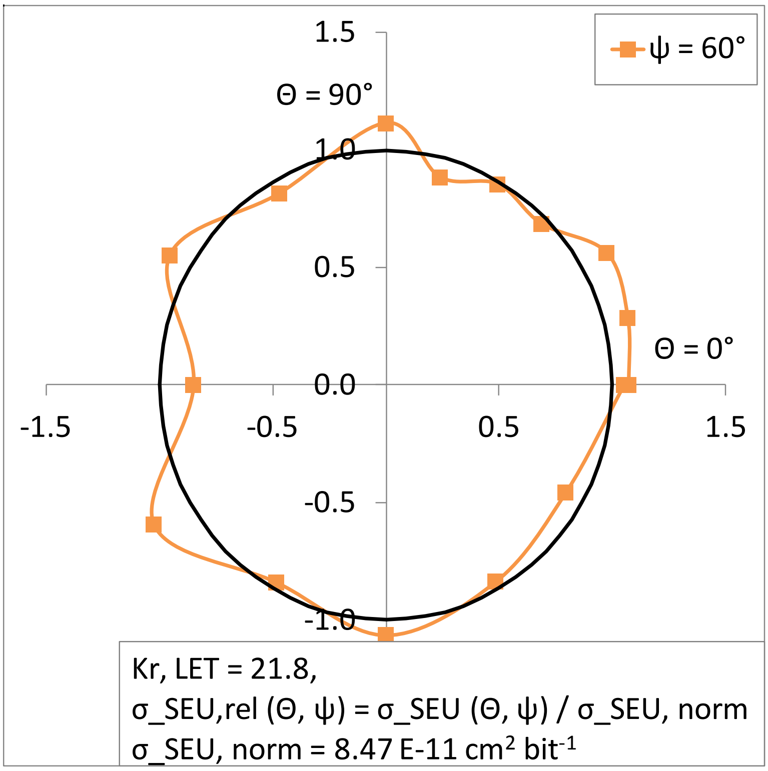

Fig. 10: Normalized SEU cross section, ψ = 60°, Micron 16-Gbit NAND-Flash

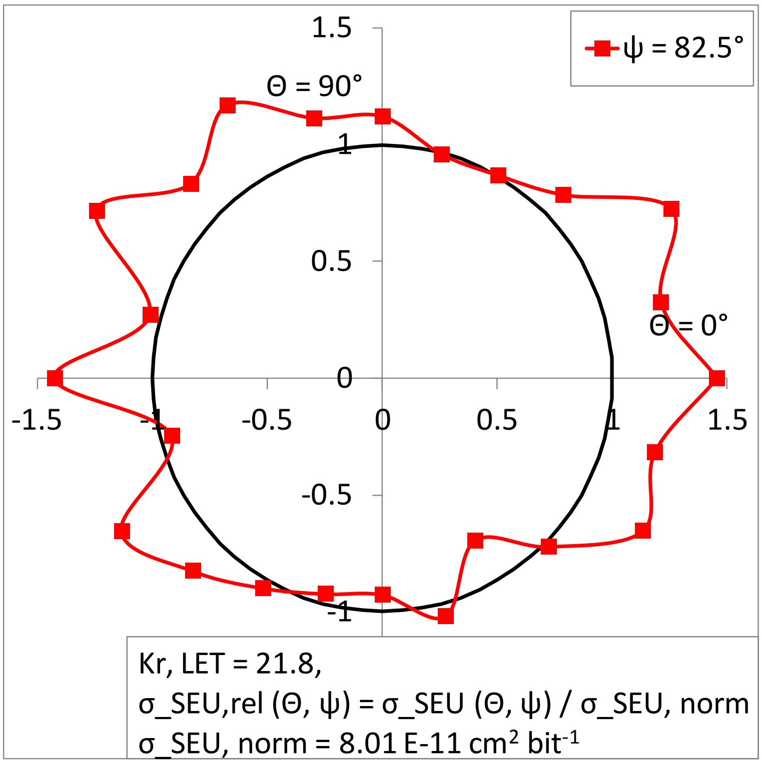

Fig. 11: Normalized SEU cross section, ψ = 82.5°, Micron 16-Gbit NAND-Flash

6.4 Interpretation

6.4.1 Samsung

Fig. 12 shows the normalized SEU cross section derived at RADEF with Argon, LET = 10.1.

The butterfly shape of the omnidirectional cross section remains at Kr but for example at ψ = 85° the growth at Ar (up to factor 7, Fig. 12) is more pronounced compared to Kr (up to factor 4, Fig. 9).

Possible explanations could be (i) the different Lot Code which also caused different cross sections at normal ion incidence or (ii) the different ion range (?).

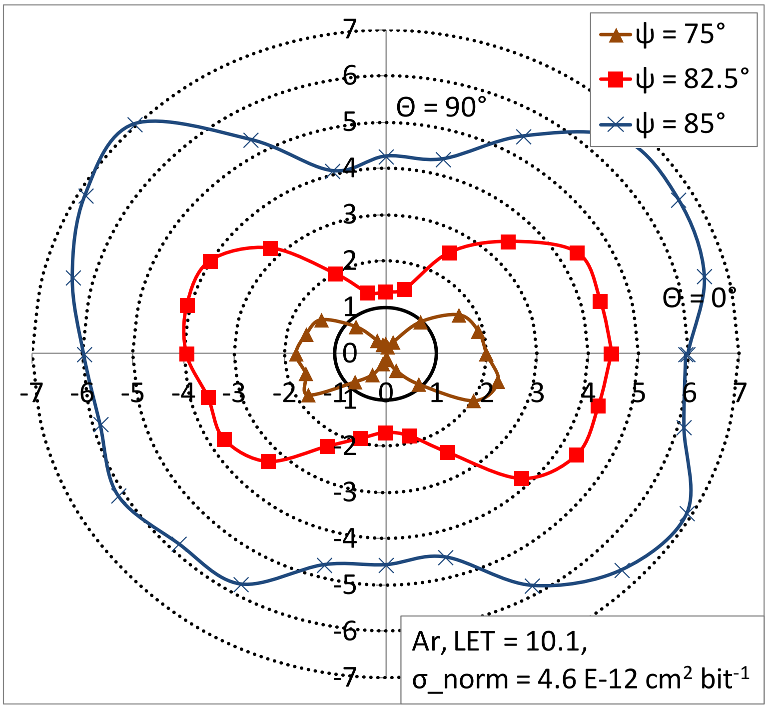

Fig. 12: For comparison: normalized SEU cross section, 75° ≤ ψ ≤ 85°, Samsung 4x8-Gbit NAND-Flash, RADEF, Finland

6.4.2 Micron

In contrast to the Samsung device the Micron device shows MBUs also at normal ion incidence (Fig. 13). At slant ion incidence (ψ = 82.5°) there are different and new effects.

For example at Θ = 0° we get MBUs with errors in the same byte address and different page addresses with a mean length of 10 errors (Fig. 14).

For Θ = 90° we get only a small amount of MBUs up to a length of 4 but we see errors clusters with up to 4 errors inside the same byte (Fig. 15).

Nevertheless the SEU cross section remains near the normal incidence circle.

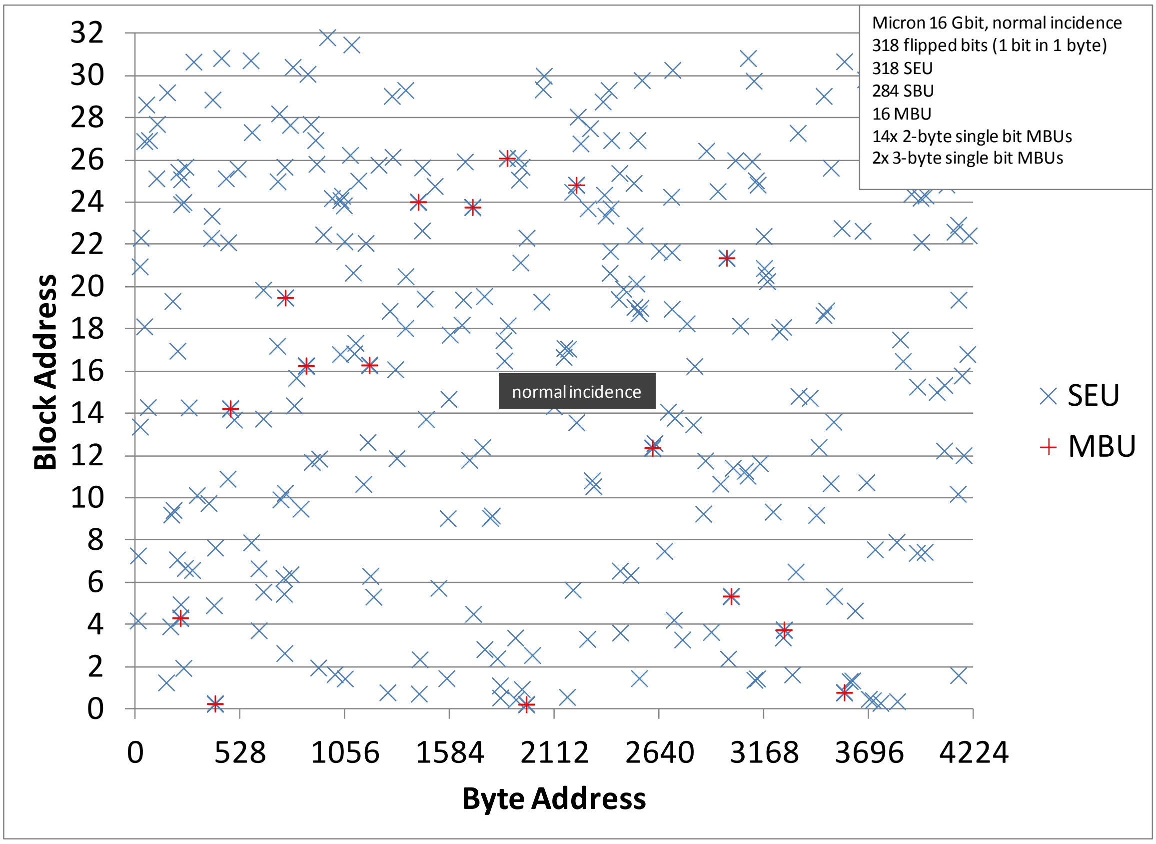

Fig. 13: Error map, normal ion incidence, Micron 16-Gbit NAND-Flash, fluence: 1× 10^5 cm^{-2}

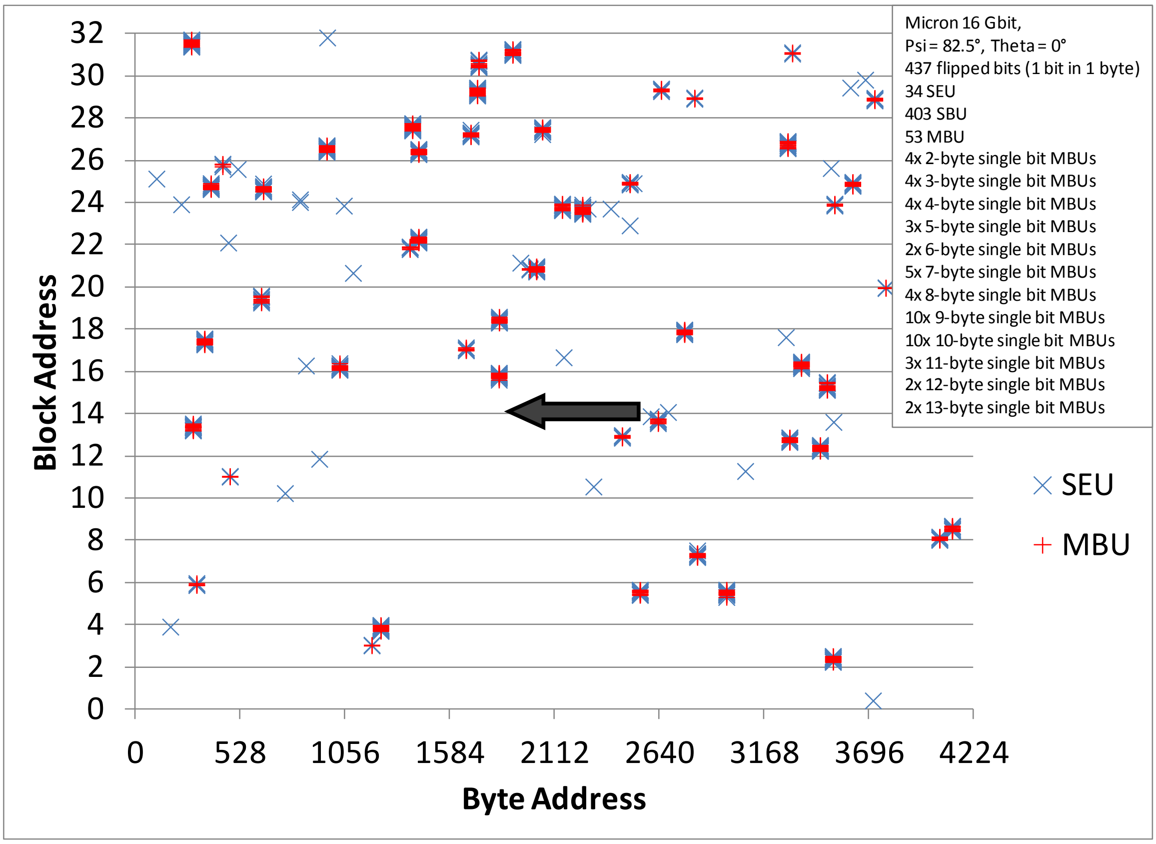

Fig. 14: Error map, ψ = 82.5°, Θ = 0°, Micron 16-Gbit NAND-Flash, fluence: 1× 10^5 cm^{-2}

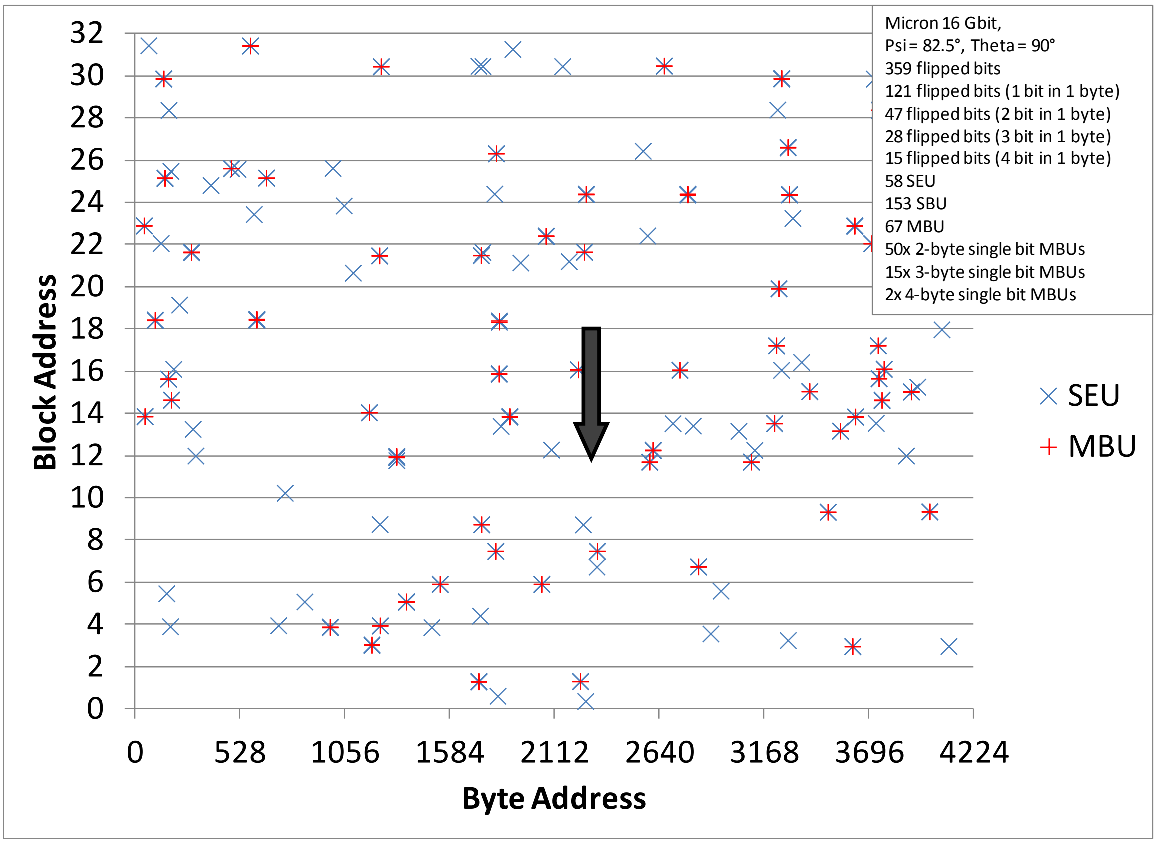

Fig. 15: Error map, ψ = 82.5°, Θ = 90°, Micron 16-Gbit NAND-Flash, fluence: 1×10^5 cm^{-2}

7 Run Table

Θ	ψ	stuck bits	Mode	Run IDA	Run TAMU	Time	Fluence	Flux	SEU	σ_SEU, bit	Remarks
0	0	0	M3a	1	132	49	5.01E+05	1.0E+04	40	2.31E-12	
0	0	0	M3a	2	133	19	9.94E+05	5.2E+04	96	2.79E-12	
15	60	0	M3a	3	134	18	9.92E+05	5.5E+04	55	1.60E-12	
30	60	0	M3a	4	135	13	1.03E+06	7.9E+04	76	2.13E-12	
45	60	0	M3a	5	136	16	9.83E+05	6.1E+04	42	1.23E-12	
60	60	0	M3a	6	137	17	9.96E+05	5.9E+04	20	5.80E-13	
75	60	0	M3a	8	-	-	-		20		
90	60	0	M3a	9	139	17	9.79E+05	5.8E+04	6	1.77E-13	
105	60	0	M3a	10	140	17	9.80E+05	5.8E+04	20	5.90E-13	
120	60	0	M3a	11	141	17	9.92E+05	5.8E+04	15	4.37E-13	
135	60	0	M3a	12	142	17	9.81E+05	5.8E+04	31	9.13E-13	
150	60	0	M3a	13	143	17	9.74E+05	5.7E+04	57	1.69E-12	
165	60	0	M3a	14	144	17	9.81E+05	5.8E+04	79	2.33E-12	
180	60	0	M3a	15	145	18	1.01E+06	5.6E+04	63	1.80E-12	
195	60	0	M3a	16	146	17	1.02E+06	6.0E+04	63	1.78E-12	
210	60	0	M3a	17	147	18	1.00E+06	5.6E+04	66	1.91E-12	
225	60	0	M3a	18	148	19	1.03E+06	5.4E+04	45	1.26E-12	
240	60	0	M3a	19	149	18	9.97E+05	5.5E+04	25	7.25E-13	
255	60	0	M3a	20	150	18	9.84E+05	5.5E+04	11	3.23E-13	
270	60	0	M3a	21	151	19	9.99E+05	5.3E+04	15	4.34E-13	
285	60	0	M3a	22	152	18	9.86E+05	5.5E+04	13	3.81E-13	
300	60	0	M3a	23	153	20	1.02E+06	5.1E+04	4	1.13E-13	
315	60	0	M3a	24	154	20	1.01E+06	5.1E+04	32	9.16E-13	
330	60	0	M3a	25	155	20	9.95E+05	5.0E+04	54	1.57E-12	
330	60	0	M3a	26	156	20	1.02E+06	5.1E+04	58	1.64E-12	

345	60	0	M3a	27	157	18	9.84E+05	5.5E+04	60	1.76E-12	
0	60	0	M3a	28	158	19	1.01E+06	5.3E+04		0.00E+00	
0	60	0	M3a	29				-	55	-	
30	60	0	M3a	30	159	24	9.98E+05	4.2E+04	62	1.80E-12	
165	60	0	M3a	31	160	20	1.01E+06	5.1E+04	60	1.72E-12	
210	60	0	M3a	32	161	21	1.00E+06	4.8E+04	53	1.53E-12	

Tab. 6: Run Table of Samsung DUT SI26

Θ	ψ	stuck bits	Mode	Run IDA	Run TAMU	Time	Fluence	Flux	SEU	σ_SEU, bit	Remarks
0	0	0	M3a	34	163	21	9.94E+05	4.7E+04	241	7.01E-12	
0	75	0	M3a	35	164	23	9.89E+05	4.3E+04	247	7.22E-12	
15	75	0	M3a	36	165	23	9.86E+05	4.3E+04	271	7.94E-12	
30	75	0	M3a	37	166	24	1.00E+06	4.2E+04	251	7.25E-12	
45	75	0	M3a	38	167	24	1.02E+06	4.3E+04	180	5.10E-12	
60	75	0	M3a	39	168	23	1.00E+06	4.3E+04	90	2.60E-12	
75	75	0	M3a	40	169	24	9.97E+05	4.2E+04	40	1.16E-12	
90	75	0	M3a	41	170	24	1.02E+06	4.3E+04	28	7.93E-13	
105	75	0	M3a	42	171	24	9.81E+05	4.1E+04	32	9.43E-13	
120	75	0	M3a	43	172	26	1.02E+06	3.9E+04		0.00E+00	
120	75	0	M3a	44	173	20	9.81E+05	4.9E+04	53	1.56E-12	
135	75	0	M3a	45	174	20	1.01E+06	5.1E+04	146	4.18E-12	
150	75	0	M3a	46	175	21	1.02E+06	4.9E+04	206	5.84E-12	
165	75	0	M3a	47	176	20	1.01E+06	5.1E+04	271	7.75E-12	
180	75	0	M3a	48	177	19	1.02E+06	5.4E+04	237	6.71E-12	
195	75	0	M3a	49	178	19	9.78E+05	5.1E+04	250	7.39E-12	
210	75	0	M3a	50	179	19	9.84E+05	5.2E+04	242	7.11E-12	
225	75	0	M3a	51	180	21	1.02E+06	4.9E+04	146	4.14E-12	
240	75	0	M3a	52	181	22	9.82E+05	4.5E+04	63	1.85E-12	

255	75	0	M3a	53	182	24	1.01E+06	4.2E+04	44	1.26E-12	
270	75	0	M3a	54	183	26	1.01E+06	3.9E+04	27	7.73E-13	
285	75	0	M3a	55	184	25	1.01E+06	4.0E+04	31	8.87E-13	
300	75	0	M3a	56	185	18	9.73E+05	5.4E+04	46	1.37E-12	
315	75	0	M3a	57	186	21	1.02E+06	4.9E+04	144	4.08E-12	
330	75	0	M3a	58	187	19	1.00E+06	5.3E+04	229	6.62E-12	
345	75	0	M3a	59	188	20	1.02E+06	5.1E+04		0.00E+00	SEFI
			PC,R	60				-		-	SEFI remains
			WR					-		-	program operation failed
			WR					-		-	inverted pattern, same
			WR					-		-	test at other address range, same

Tab. 7: Run Table of Samsung DUT SI21

Θ	ψ	stuck bits	Mode	Run IDA	Run TAMU	Time	Fluence	Flux	SEU	σ_SEU, bit	Remarks
345	75	0	M3a	61	189	20	1.00E+06	5.0E+04	123	3.55E-12	
0	75	0	M3a	62	190	20	1.02E+06	5.1E+04	135	3.82E-12	
0	0	0	M3a	63	191	22	1.03E+06	4.7E+04	111	3.11E-12	
330	75	0	M3a	64	192	22	1.01E+06	4.6E+04	109	3.12E-12	
0	85	0	M3a	65	193	21	1.01E+06	4.8E+04	394	1.13E-11	
180	85	0	M3a	66	194	20	1.00E+06	5.0E+04	471	1.36E-11	
15	85	0	M3a	67	195	21	1.01E+06	4.8E+04	390	1.12E-11	
30	85	0	M3a	68	196	22	9.94E+05	4.5E+04	401	1.17E-11	
45	85	0	M3a	69	197	22	1.00E+06	4.5E+04	297	8.58E-12	

60	85	0	M3a	70	198	23	1.00E+06	4.3E+04	143	4.13E-12	
75	85	0	M3a	71	199	24	9.82E+05	4.1E+04	74	2.18E-12	
90	85	0	M3a	72	200	24	9.93E+05	4.1E+04	55	1.60E-12	
105	85	0	M3a	73	201	23	1.02E+06	4.4E+04	53	1.50E-12	
120	85	0	M3a	74	202	29	1.00E+06	3.4E+04	123	3.55E-12	
135	85	0	M3a	75	203	23	1.00E+06	4.3E+04	220	6.36E-12	
150	85	0	M3a	76	204	22	9.91E+05	4.5E+04	367	1.07E-11	
165	85	0	M3a	77	205	22	1.02E+06	4.6E+04	407	1.15E-11	
180	85	0	M3a	78	206	22	1.00E+06	4.5E+04	503	1.45E-11	
195	85	0	M3a	79	207	23	9.91E+05	4.3E+04	464	1.35E-11	
210	85	0	M3a	80	208	25	9.97E+05	4.0E+04	404	1.17E-11	
225	85	0	M3a	81	209	25	9.93E+05	4.0E+04	255	7.42E-12	
240	85	0	M3a	82	210	26	9.94E+05	3.8E+04	509	1.48E-11	
255	85	0	M3a	83	211	28	1.01E+06	3.6E+04	57	1.63E-12	
240	85	0	M3a	84	212	28	9.83E+05	3.5E+04	473	1.39E-11	
255	85	0	M3a	85	213	30	1.01E+06	3.4E+04	30	8.58E-13	
270	85	0	M3a	86	214	33	1.02E+06	3.1E+04	2	5.67E-14	
285	85	0	M3a	87	215	19	1.03E+06	5.4E+04	25	7.01E-13	
300	85	0	M3a	88	216	20	9.82E+05	4.9E+04	207	6.09E-12	
315	85	0	M3a	89	217	19	9.92E+05	5.2E+04	257	7.49E-12	
330	85	0	M3a	90	218	19	9.92E+05	5.2E+04	362	1.05E-11	
345	85	0	M3a	91	219	21	1.02E+06	4.9E+04	395	1.12E-11	
0	85	0	M3a	92	220	21	9.90E+05	4.7E+04	358	1.05E-11	
0	0	0	M3a	93	221	21	1.01E+06	4.8E+04	104	2.98E-12	
270	85	0	M3a	94	222	21	9.89E+05	4.7E+04	23	6.72E-13	
270	80	0	M3a	95	223	20	9.88E+05	4.9E+04	11	3.22E-13	
270	75	0	M3a	96	224	21	9.89E+05	4.7E+04	5	1.46E-13	
270	60	0	M3a	97	225	22	1.02E+06	4.6E+04	12	3.40E-13	
270	45	0	M3a	98	226	21	9.79E+05	4.7E+04	15	4.43E-13	

270	30	0	M3a	99	227	21	9.85E+05	4.7E+04	53	1.55E-12	
0	0	0	M3a	100	228	24	9.80E+05	4.1E+04	98	2.89E-12	
270	75	0	M3a	101	229	19	9.87E+05	5.2E+04		0.00E+00	
			WR	102				-		-	
270	75	0	M3a	103	230	23	1.02E+06	4.4E+04	41	1.16E-12	
270	85	0	M3a	104	231	21	1.02E+06	4.9E+04	101	2.86E-12	
255	85	0	M3a	105	232	21	9.97E+05	4.7E+04	285	8.26E-12	
285	85	0	M3a	106	233	23	1.02E+06	4.4E+04	122	3.47E-12	
240	85	0	M3a	107	234	23	1.00E+06	4.3E+04	663	1.92E-11	
300	85	0	M3a	108	235	21	9.83E+05	4.7E+04	358	1.05E-11	
270	85	0	M3a	109	236	22	1.01E+06	4.6E+04	77	2.20E-12	
225	85	0	M3a	110	237	22	9.90E+05	4.5E+04	457	1.33E-11	
180	85	0	M3a	111	238	23	1.01E+06	4.4E+04	601	1.72E-11	
0	85	0	M3a	112	239	31	1.00E+06	3.2E+04	595	1.72E-11	

Tab. 8: Run Table of Samsung DUT SI22

Θ	ψ	stuck bits	Mode	Run IDA	Run TAMU	Time	Fluence	Flux	SEU	σ_SEU, bit	Remarks
0	0	0	M3a	113	240	17	9.81E+05	5.8E+04	125	3.68E-12	
0	82.5	0	M3a	114	241	18	1.03E+06	5.7E+04	348	9.76E-12	
15	82.5										
30	82.5	0	M3a	115	242	19	1.01E+06	5.3E+04	329	9.41E-12	
15	82.5	0	M3a	116	243	19	1.01E+06	5.3E+04	327	9.36E-12	
45	82.5	0	M3a	117	244	18	1.00E+06	5.6E+04	250	7.22E-12	
60	82.5	0	M3a	118	245	16	1.00E+06	6.3E+04	133	3.84E-12	
75	82.5	0	M3a	119	246	8	1.02E+06	1.3E+05	46	1.30E-12	
90	82.5	0	M3a	120	247	18	9.73E+05	5.4E+04	32	9.50E-13	
105	82.5	0	M3a	121	248	17	9.86E+05	5.8E+04	40	1.17E-12	
120	82.5	0	M3a	122	249	18	1.02E+06	5.7E+04	58	1.64E-12	

135	82.5	0	M3a	123	250	17	9.99E+05	5.9E+04	151	4.37E-12	
150	82.5	0	M3a	124	251	17	9.84E+05	5.8E+04	253	7.43E-12	
165	82.5	0	M3a	125	252	17	1.01E+06	5.9E+04	312	8.93E-12	
180	82.5	0	M3a	126	253	17	9.87E+05	5.8E+04	349	1.02E-11	
195	82.5	0	M3a	127	254	18	1.01E+06	5.6E+04	340	9.73E-12	
210	82.5	0	M3a	128	255	16	9.70E+05	6.1E+04	292	8.70E-12	
225	82.5	0	M3a	129	256	17	9.85E+05	5.8E+04	211	6.19E-12	
240	82.5	0	M3a	130	257	17	1.01E+06	5.9E+04	99	2.83E-12	
255	82.5	0	M3a	131	258	20	1.01E+06	5.1E+04	27	7.73E-13	
270	82.5	0	M3a	132	259	23	9.98E+05	4.3E+04	40	1.16E-12	
285	82.5	0	M3a	133	260	24	9.81E+05	4.1E+04	47	1.38E-12	
300	82.5	0	M3a	134	261	25	9.91E+05	4.0E+04	75	2.19E-12	
315	82.5	0	M3a	135	262	20	1.00E+06	5.0E+04	162	4.68E-12	
330	82.5	0	M3a	136	263	20	1.00E+06	5.0E+04	256	7.40E-12	
345	82.5	0	M3a	137	264	21	1.00E+06	4.8E+04	336	9.71E-12	
0	82.5	0	M3a	138	265	19	9.87E+05	5.2E+04	365	1.07E-11	

Tab. 9: Run Table of Samsung DUT SI23

Θ	**ψ**	**stuck bits**	**Mode**	**Run IDA**	**Run TAMU**	**Time**	**Fluence**	**Flux**	**SEU**	**σ_SEU, bit**	**Remarks**
0	0		M3a	139	266	19	1.02E+06	5.4E+04	3011	8.53E-11	reduce flux
0	0	38	M3a	140	267	14	1.01E+05	7.2E+03	318	9.10E-11	stuck bits!
0	82.5	30	M3a	141	268	14	1.01E+05	7.2E+03	437	1.25E-10	
15	82.5	42	M3a	142	269	13	9.98E+04	7.7E+03	393	1.14E-10	
30	82.5	49	M3a	143	270	21	9.83E+04	4.7E+03	455	1.34E-10	
45	82.5	57	M3a	144	271	25	1.02E+05	4.1E+03	368	1.04E-10	
60	82.5	47	M3a	145	272	25	1.02E+05	4.1E+03	328	9.29E-11	
75	82.5	44	M3a	146	273	25	1.01E+05	4.0E+03	322	9.21E-11	

90	82.5	45	M3a	147	274	25	1.01E+05	4.0E+03	359	1.03E-10	
105	82.5	42	M3a	148	275	26	9.99E+04	3.8E+03	365	1.06E-10	
120	82.5	39	M3a	149	276	26	1.02E+05	3.9E+03	417	1.18E-10	
135	82.5	35	M3a	150	277	27	1.00E+05	3.7E+03	365	1.05E-10	
150	82.5	39	M3a	151	278	28	9.87E+04	3.5E+03	441	1.29E-10	
165	82.5	47	M3a	152	279	28	1.00E+05	3.6E+03	340	9.83E-11	
180	82.5	43	M3a	153	280	27	9.96E+04	3.7E+03	442	1.28E-10	
195	82.5	68	M3a	154	281	27	9.86E+00	3.7E-01	334	9.79E-07	
210	82.5	63	M3a	155	282	30	9.92E+04	3.3E+03	430	1.25E-10	
225	82.5	58	M3a	156	283	15	9.84E+04	6.6E+03	385	1.13E-10	
240	82.5	54	M3a	157	284	15	9.82E+04	6.5E+03	345	1.02E-10	
255	82.5	51	M3a	158	285	16	1.03E+05	6.4E+03	319	8.95E-11	
270	82.5	45	M3a	159	286	29	9.94E+04	3.4E+03	305	8.87E-11	
285	82.5	45	M3a	160	267	27	9.89E+04	3.7E+03	341	9.96E-11	
300	82.5	43	M3a	161	268	26	9.99E+04	3.8E+03	268	7.75E-11	
315	82.5	39	M3a	162	269	27	1.00E+05	3.7E+03	325	9.39E-11	
330	82.5	42	M3a	163	270	28	1.00E+05	3.6E+03	408	1.18E-10	
345	82.5	44	M3a	164	271	26	1.00E+05	3.8E+03	387	1.12E-10	
0	82.5	47	M3a	165	272	25	9.98E+04	4.0E+03	1020	2.95E-10	
			PC,R	166				-		-	
			WR					-	569	-	

Tab. 10: Run Table of Micron DUT M356

Θ	ψ	stuck bits	Mode	Run IDA	Run TAMU	Time	Fluence	Flux	SEU	σ_SEU, bit	Remarks
0	0	0	M3a	167	293	27	1.01E+05	3.7E+03	281	8.04E-11	
0	60	8	M3a	168	294	26	9.91E+04	3.8E+03	325	9.48E-11	
15	60	18	M3a	169	295	27	1.01E+05	3.7E+03	345	9.87E-11	
30	60	17	M3a	170	296	27	1.02E+05	3.8E+03	350	9.92E-11	

45	60	19	M3a	171	297	27	9.85E+05	3.6E+04	306	8.98E-12	
60	60	11	M3a	172	298	28	1.01E+05	3.6E+03	303	8.67E-11	
75	60	12	M3a	173	299	28	1.00E+05	3.6E+03	283	8.18E-11	
90	60	10	M3a	174	300	28	1.01E+05	3.6E+03	340	9.73E-11	
120	60	13	M3a	175	301	28	9.82E+04	3.5E+03	292	8.59E-11	
150	60	6	M3a	176	302	30	1.01E+05	3.4E+03	333	9.53E-11	
180	60	9	M3a	177	303	18	1.00E+05	5.6E+03	261	7.54E-11	
210	60	16	M3a	178	304	17	9.98E+04	5.9E+03	367	1.06E-10	
240	60	18	M3a	179	305	16	1.03E+05	6.4E+03	305	8.56E-11	
270	60	14	M3a	180	306	16	9.96E+04	6.2E+03	329	9.55E-11	
300	60	13	M3a	181	307	16	1.00E+05	6.3E+03	299	8.64E-11	
330	60	10	M3a	182	308	16	1.01E+05	6.3E+03	281	8.04E-11	
0	60	12	M3a	183	309	16	9.80E+04	6.1E+03	323	9.52E-11	
0	0	20	M3a	184	310	16	9.96E+04	6.2E+03	331	9.60E-11	
270	82	27	M3a	185	311	16	9.99E+04	6.2E+03	401	1.16E-10	
			R	186					402		
			R	187					400		
			R	188					398		

Tab. 11: Run Table of Micron DUT M357

8 Package pictures

Fig. 16: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 17: Micron MT29F16G08ABACAWP-IT:C NAND-Flash

Fig. 18: Samsung K9F8G08U0M-PCB0 NAND-Flash

Fig. 19: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 20: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 21: Micron MT29F32G08ABAAAWP-IT:A NAND-Flash

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