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Functional TID Test of 16-Gbit/32-Gbit Micron SLC NAND-Flash Memory Devices

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Test Report

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1 Abstract

From January 17th to 24th 2014, we performed a functional TID test campaign [1] with NAND-Flash and DDR3 SDRAM devices [2] at ESA-ESTEC. This document reports on the findings for NAND-Flash devices.

The previous TID test of 4 x 8-Gbit Samsung NAND-Flash delivered [3]:

1. No breakdown of principal device functions did occur within the applied dose regime (up to 60 - 150 krad),
2. at ambient temperature the first errors occurred slightly above 40 krad,
3. always biased DUTs showed above 50 krad a progressive increase of the standby current,
4. mostly unbiased DUTs showed the same error share as always biased DUTs, but the increase of the standby current was significantly reduced,
5. erase after 5 krad each shifts the onset of errors to doses substantially above 50 krad, at some DUTs above 150 krad,
6. dose rate reduction from 135 rad / min to 37.1 rad / min did not change the radiation response (error share, standby current, operating current),
7. Baking does not change the radiation response,
8. Heating up to 85°C lowers the error onset dose from 40 krad to 30 krad and increases the standby current by roughly a factor of two.

2 Test setup

2.1 DUTs

The DUTs are described in Tab. 1.

Manufacturer	Capacity [Gbit]	Feature Size [nm]	Package	Part Number	Date Code	Lot Code	Samples	IDA ID
Samsung [4]	4x8	51	QDP	K9WBG08U1M-PIB0 (Fig. 1)	0837	FMH030X2	1	SA20
Micron [5]	16	25	SDP	MT29F16G08ABACAWP-IT:C (Fig. 2)	1218	-	6	M40 - M45
Micron [6]	32	25	SDP	MT29F32G08ABAAAWP-IT:A (Fig. 3)	1134	-	6	M50 - M55
Micron [6]	4x32	25	QDP	MT29F128G08AJAAAWP-ITZ:A (Fig. 4)	1314	-	2	M60 - M61

Tab. 1: NAND-Flash DUTs

Fig. 1: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 2: Micron MT29F16G08ABACAWP-IT:C NAND-Flash

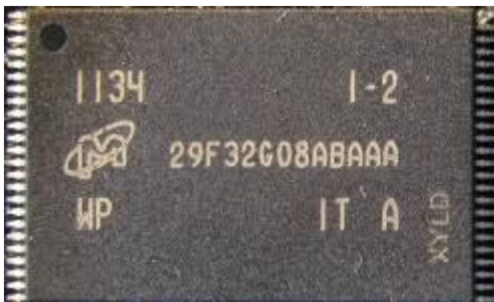

Fig. 3: Micron MT29F32G08ABAAAWP-IT:A NAND-Flash

Fig. 4: Micron MT29F128G08AJAAAWP-ITZ:A NAND-Flash

The DUTs are soldered on DUT carriers.

First all DUTs were marked by an individual ID and were checked for factory marked bad blocks. The ID and the bad block table were programmed into block 0 which is guaranteed to be valid by the manufacturer for every DUT. These bad blocks were not accessed by erase or program operations anymore.

2.2 Test facility

The tests were performed at the ESTEC Co-60 facility, Noordwijk described in [7]. The activity of the source and the positioning of the test bench relative to the source id described in [8].

2.3 Test bench

The test bench RTMC5 (Fig. 5, Fig. 6) is capable of operating 16 NAND-Flash DUTs in the configuration for TID tests.

In order to perform irradiation tests with a high total dose, all sensitive parts except the DUTs must be shielded from the radiation (Fig. 6 and Fig. 7). For this purpose, we developed a shielding box made of lead (where space is critical) and steel. The box weighs about 1300 kg and is assembled from individual parts of about 10 kg to 20 kg each. It has several curved channels for feeding electrical wires and water tubes for the cooling system into the box.

The NAND-Flash DUTs are shielded against electrons by a 6-mm acrylic glass between the Co-60 source and the DUTs (Fig. 7).

Fig. 5 shows the block diagram of the TID Test Set Up. Up to sixteen DUT Carriers are exposed simultaneously to a beam of 10 cm by 10 cm. Each DUT Carrier is served by its own Fast Test Unit (FTU). In contrast to the DUT Carriers the sixteen FTU boards are allocated outside of the beam, approximately 30 cm below the DUT Carriers inside the shielding box.

The FTUs are supplied by 5 and 12V and generate a DUT supply voltage between 2.7V and 3.6 V, settable by the Remote Control Unit (RCU).
The FTUs measure continuously the standby current and the operating current of the DUTs.
The FTUs are equipped with a Latch Up Switch. Its current threshold is RCU settable between 50 mA and 200 mA, and its delay time between 1 µs and 1 ms.
Measurement of Program Time and Erase Time is an additional feature of the FTUs.

Four of the ten DUT Carriers are equipped with a Peltier element for temperature control between –20°C and +85°C.

The FTUs communicate with the RCU via an Ethernet link.

The Remote Control Unit is based on a PC running our proprietary configurable GESOS V test S/W package.

The RCU provides (i) control of the test sequences (test modes), (ii) generates specific data pattern and address loops, (3) supports the setting of all test parameters, (iv) performs a real time pattern verification, (v) counts data errors in real time, (vi) records all error vectors, current and time measurements, Latch up trigger actions and all parameter settings for offline evaluation of the test data files, (vii) delivers a real time visualization of the error distribution, of several statistical distributions a.s.o.

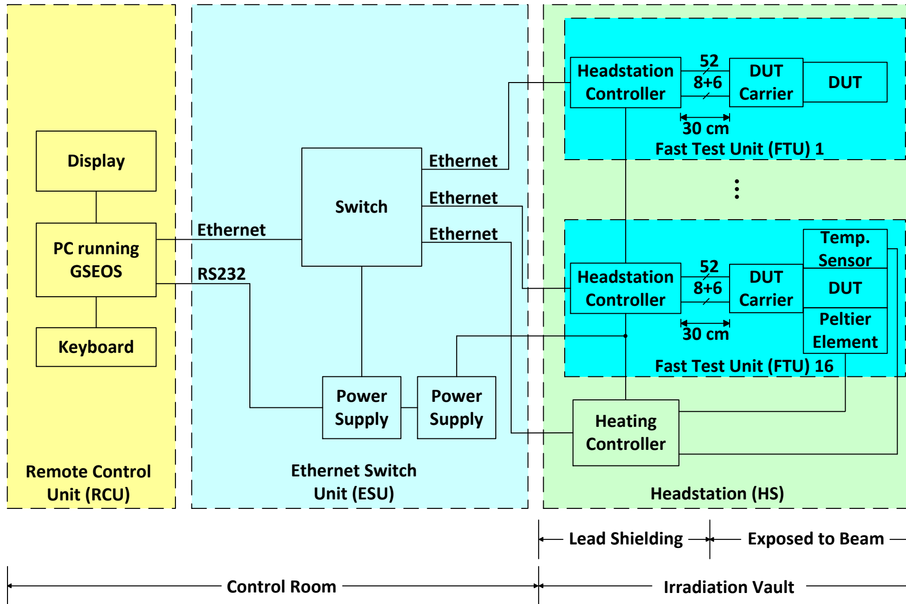

Fig. 5: Block Diagram of the NAND-Flash test setup with 16 DUTs configured for TID tests

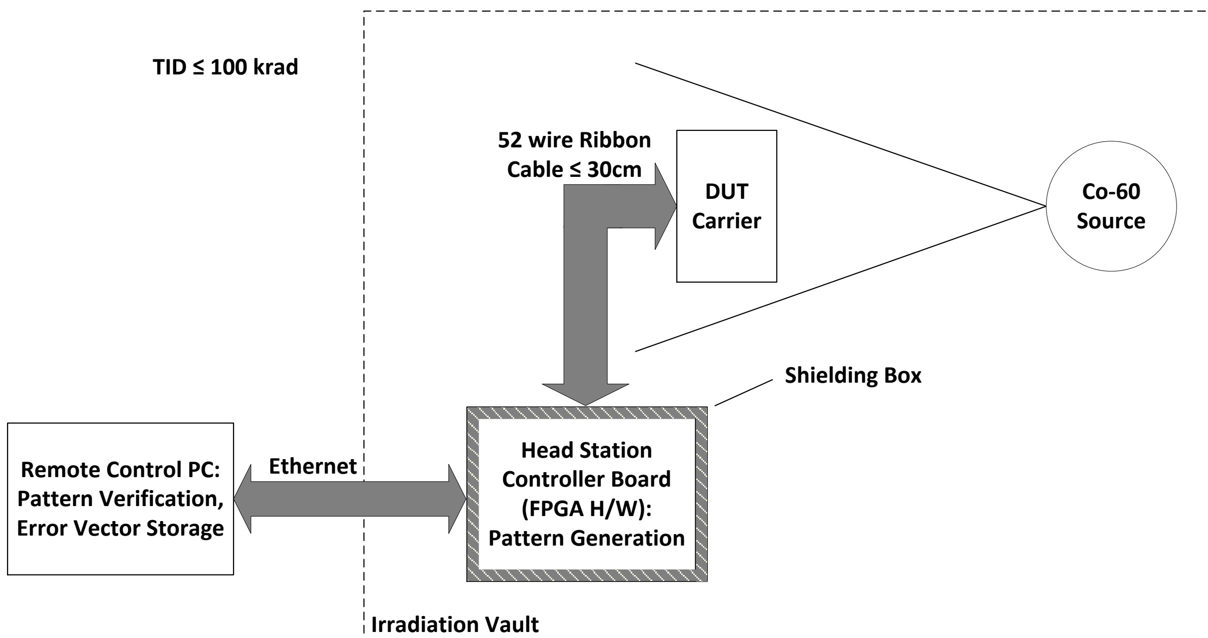

Fig. 6: NAND-Flash test setup at the ESTEC Co-60 irradiation facility

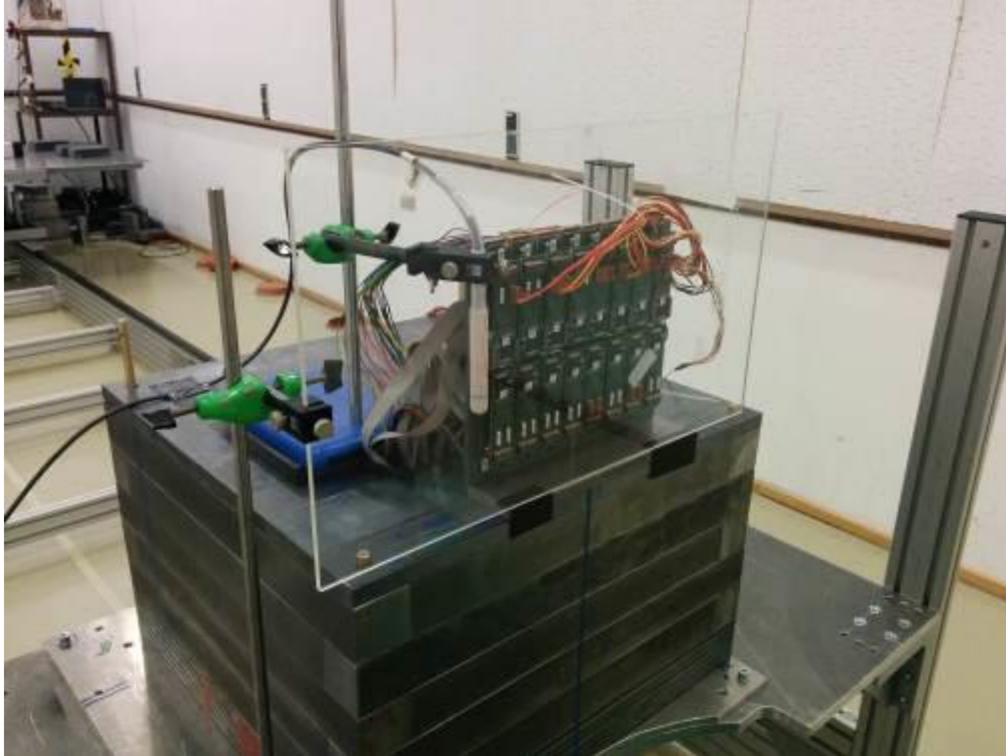

Fig. 7: Shielding box with 16 NAND-Flash DUTs above

2.4 Test sequence

The goal of this functional TID test was to test 16/32-Gbit NAND-Flash devices in-situ.

The DUTs were tested in six modes:

A. Storage Mode with read every 2.5 krad
   1. Mostly Unbiased 25°C, 3.3 Volt
   2. Biased 25°C, 3.3 Volt
   3. Biased, 85°C, 3.6 Volt
B. Refresh Mode by (i) read, (ii) erase/write inverted pattern and (iii) read every 2.5 krad
   1. Mostly Unbiased 25°C, 3.3 Volt
   2. Biased, 25°C, 3.3 Volt
   3. Biased, 85°C, 3.6 Volt

In all modes a checkerboard background pattern was programmed before irradiation.

With increasing dose the threshold distribution of the cell transistors is shifted towards the decision level with the consequence that data errors come up. Erase drives the threshold distribution back to its initial position. Using this “Periodic Refresh” the “Error Count versus Dose” curve is shifted repetitively to higher dose values.

In Mostly Unbiased Storage without Refresh the DUTs were powered every 2.5 krad during a short time span for verification read and the recording of the standby current.

In case of additional refresh the DUTs were powered for a longer time span, but in any case for less than 10 % of time.

During all test runs 12 DUTs were at ambient temperature (approximately 25°C). In addition four other DUTs were heated up to +85°C.

2.5 Error classification

Several error classes are distinguished, according to the overview shown in Fig. 8.

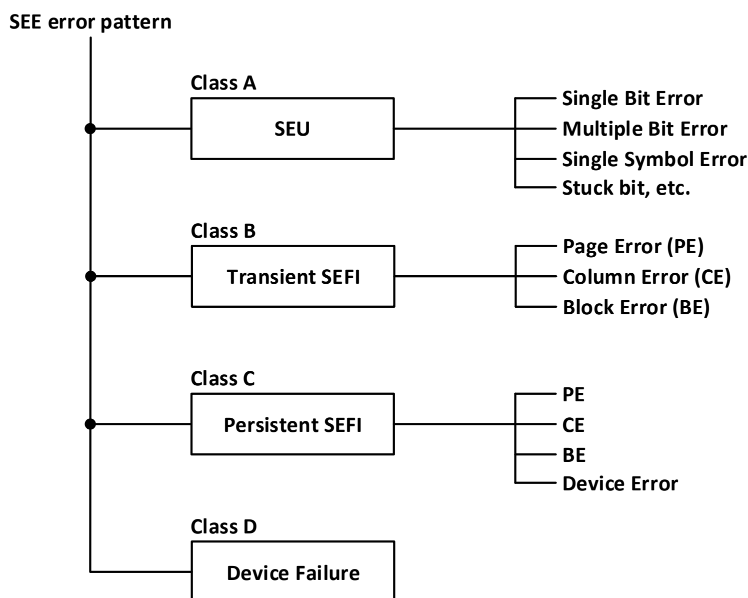

Fig. 8: Error classification scheme

2.6 Test restrictions

2.6.1 Overall test time

The major restriction is the time needed to reach relevant dose values.

With the new shielding box we reached a dose rate of about 110 rad/min (H_2O) for DDR3 SDRAM and of about 85 rad/min (H_2O) for NAND-Flash which allows two runs of DDR3 SDRAM up to a dose of 400 krad (H_2O) and one run of NAND-Flash to about 70 krad (H_2O)

in eight days (Tab. 2). Both test benches are capable of operating unattended during the night/weekend.

In order to perform two DDR3 SDRAM test runs up to 400 krad the NAND-Flash test run was started from the 23th January afternoon until the next morning. For this reason the TID exposure was not stopped immediately after device failure and all DUTs were irradiated up to 90.2 krad (Si).

	Fri, 17	Sat, 18	Sun, 19	Mon, 20	Tue, 21	Wed, 22	Thu, 23	Fri, 24
morning	installation of DDR3 test equipment	Micron 4 Gbit DDR3	Micron 4 Gbit DDR3	Hynix 4 Gbit DDR3	Hynix 4 Gbit DDR3	Hynix 4 Gbit DDR3	installa-tion of NAND-Flash test equip-ment	Micron 16/32 Gbit NAND-Flash
afternoon	Micron 4 Gbit DDR3	Micron 4 Gbit DDR3	Micron 4 Gbit DDR3	Hynix 4 Gbit DDR3	Hynix 4 Gbit DDR3	Hynix 4 Gbit DDR3	Micron 16/32 Gbit NAND-Flash	de-installa-tion

Tab. 2: Test schedule

2.6.2 Tested NAND-Flash subset

The verification read operation in Storage Mode and the refresh operation in Refresh Mode should be limited to 10% of the irradiation time. Therefore only a subset of 64 blocks of the DUTs were accessed.

The verification and refresh interval was shortened to 2.5 krad because of the expected faster error increase and the expected earlier device breakdown of the 25 nm Micron devices. In the TID Test of 4 x 8-Gbit Samsung NAND-Flash [3] this interval was 5 krad.

3 Test Results

In the error share and standby current diagrams the functional breakdown of each DUT is marked with dotted line. The chronology of DUT breakdowns is reflected in the order of the diagram legend.

3.1 Error share

3.1.1 Storage Mode, all DUTs

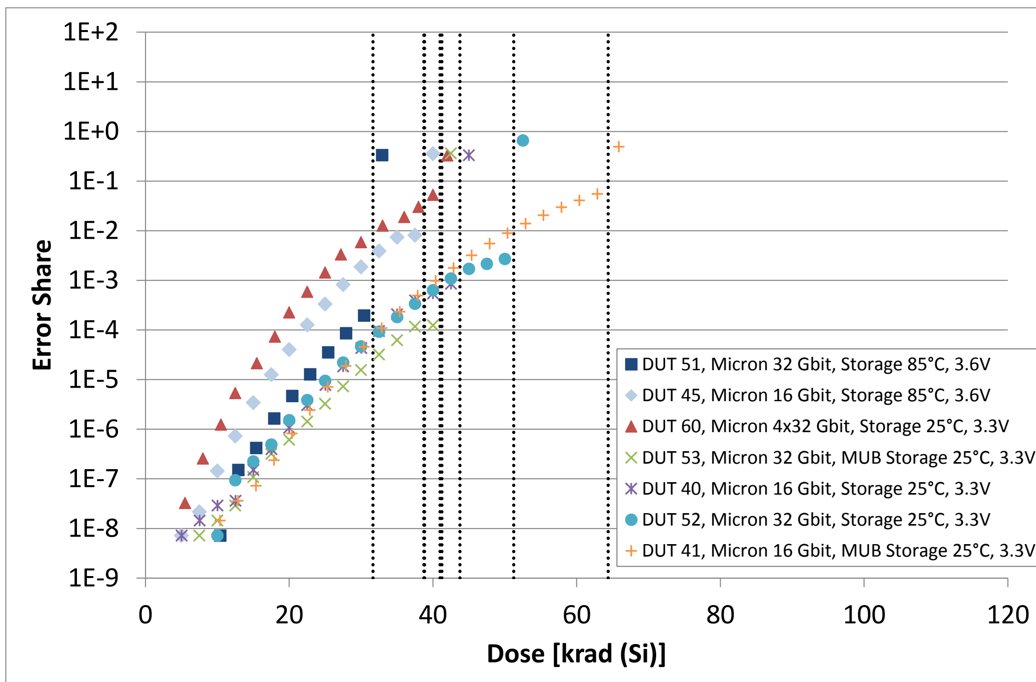

Fig. 9: Error share versus dose of DUTs in Storage Mode

3.1.2 Refresh Mode, all DUTs

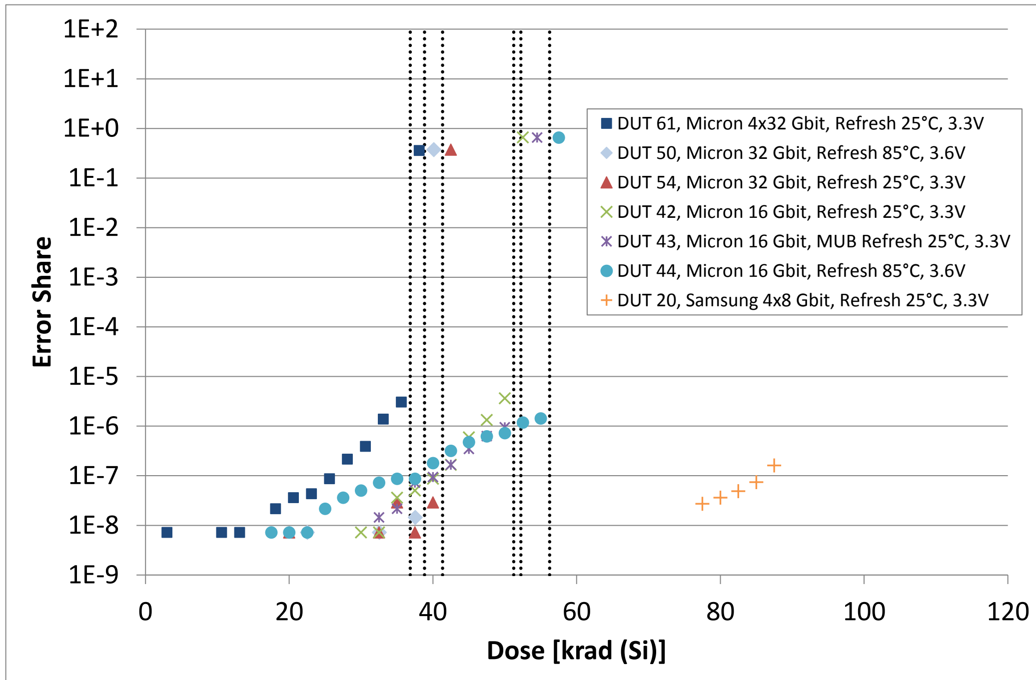

Fig. 10: Error share versus dose of DUTs in Refresh Mode

3.1.3 Micron 16 Gbit, all modes

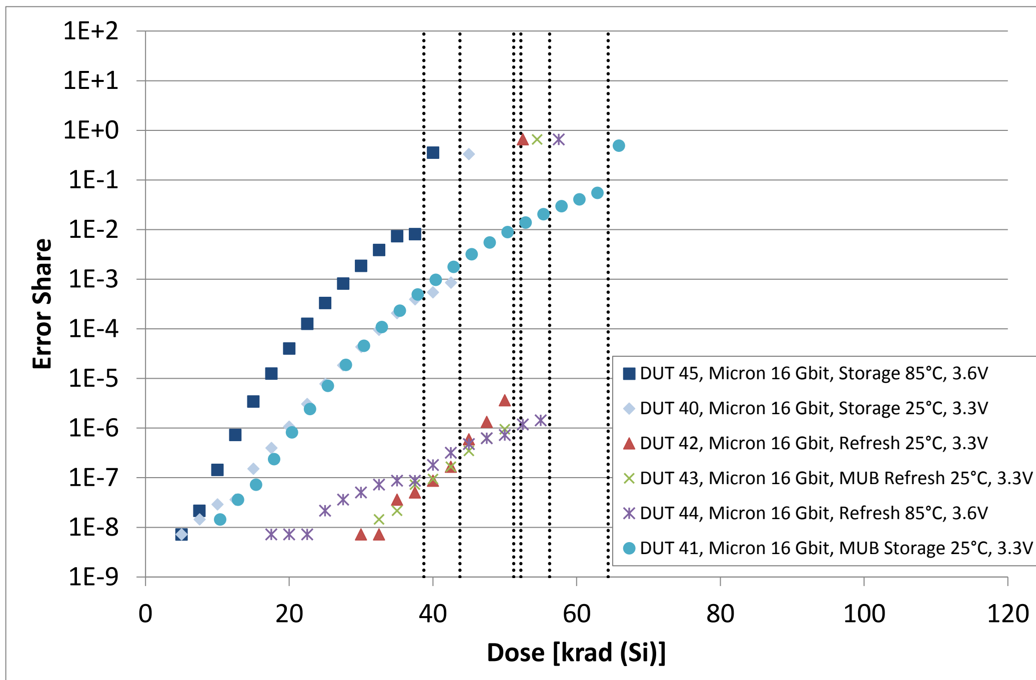

Fig. 11: Error share versus dose of all Micron 16 Gbit DUTs

3.1.4 Micron 32 Gbit, all modes

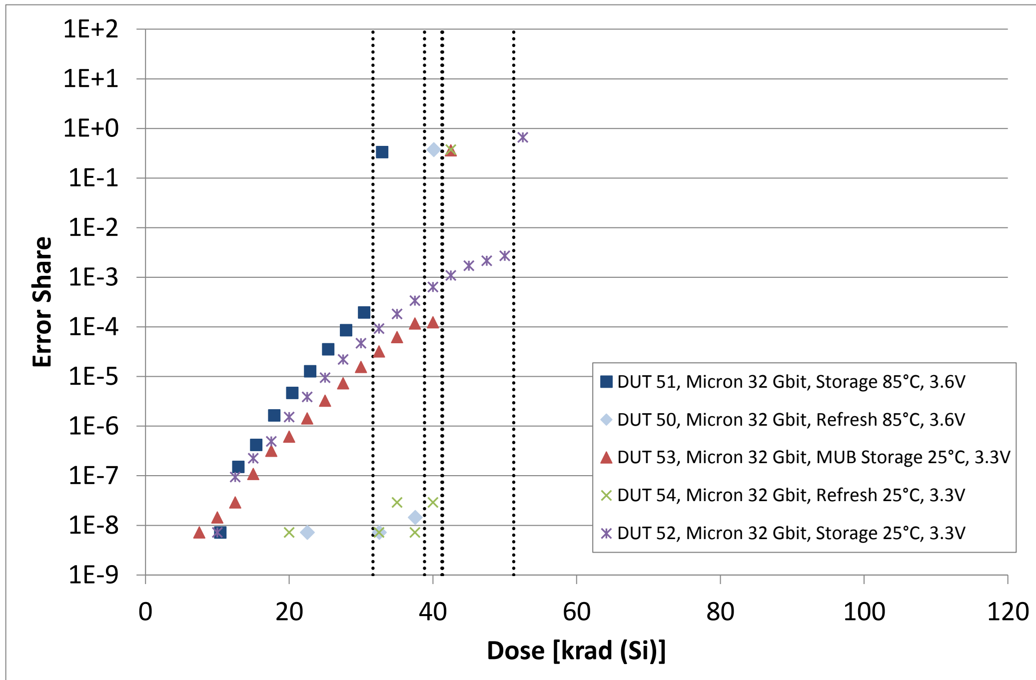

Fig. 12: Error share versus dose of all Micron 32 Gbit DUTs

3.1.5 Micron 128 Gbit, all modes

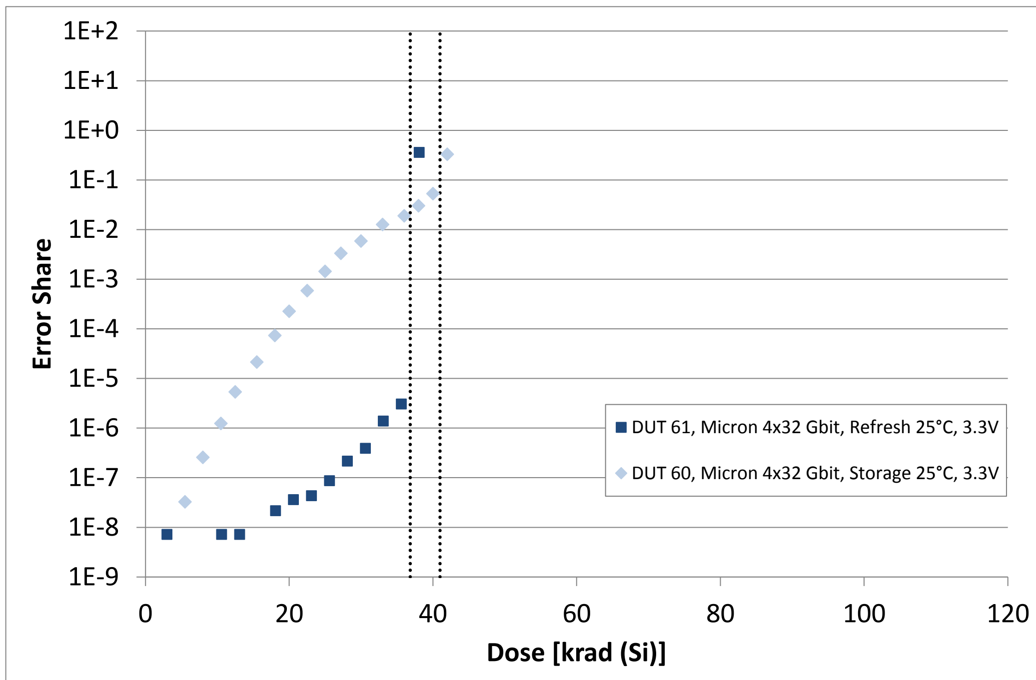

Fig. 13: Error share versus dose of all Micron 4x32 Gbit DUTs

3.2 Standby Current

The typical and maximum standby currents given in the datasheet are given in Tab. 3. If the values are given per die (LUN) the values are converted per package.

Manufacturer	Capacity [Gbit]	Symbol acc. to the datasheet	Typical standby current [µA]	Maximum standby current [µA]
Samsung	4x8	I_{SB2}	40	200
Micron	16	I_{SB}	10	50
Micron	32	I_{SB}	10	50
Micron	4x32	I_{SB}	40	200

Tab. 3: Typical and maximum standby currents per package

The measurements are done while all chip enables of the respective DUT are disabled.

3.2.1 Storage Mode, all DUTs

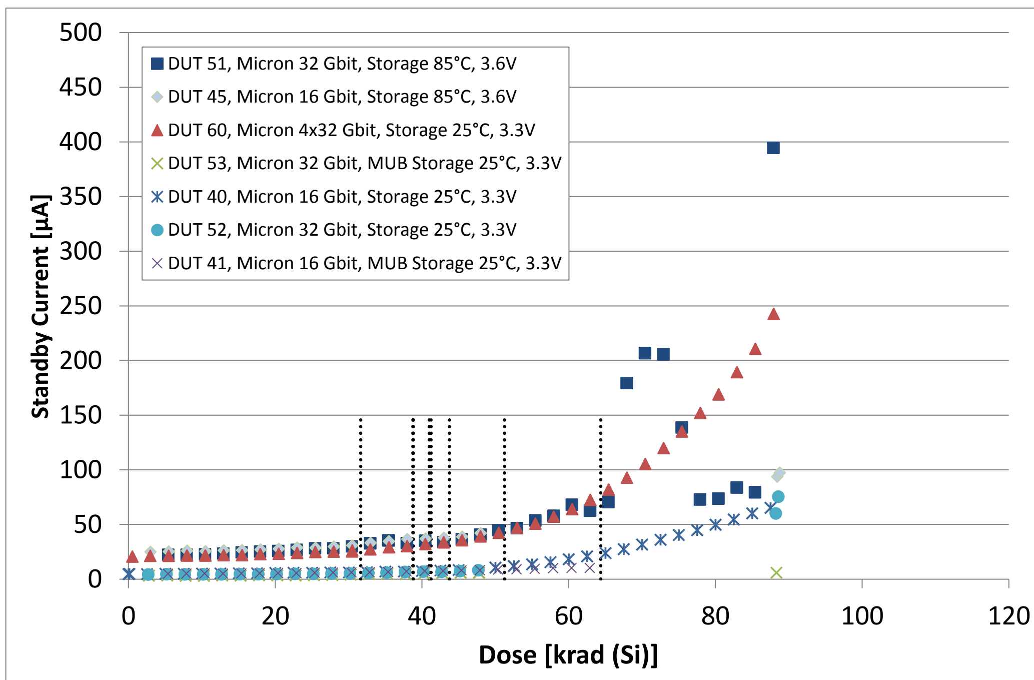

Fig. 14: Standby current versus dose of DUTs in Storage Mode

3.2.2 Refresh Mode, all DUTs

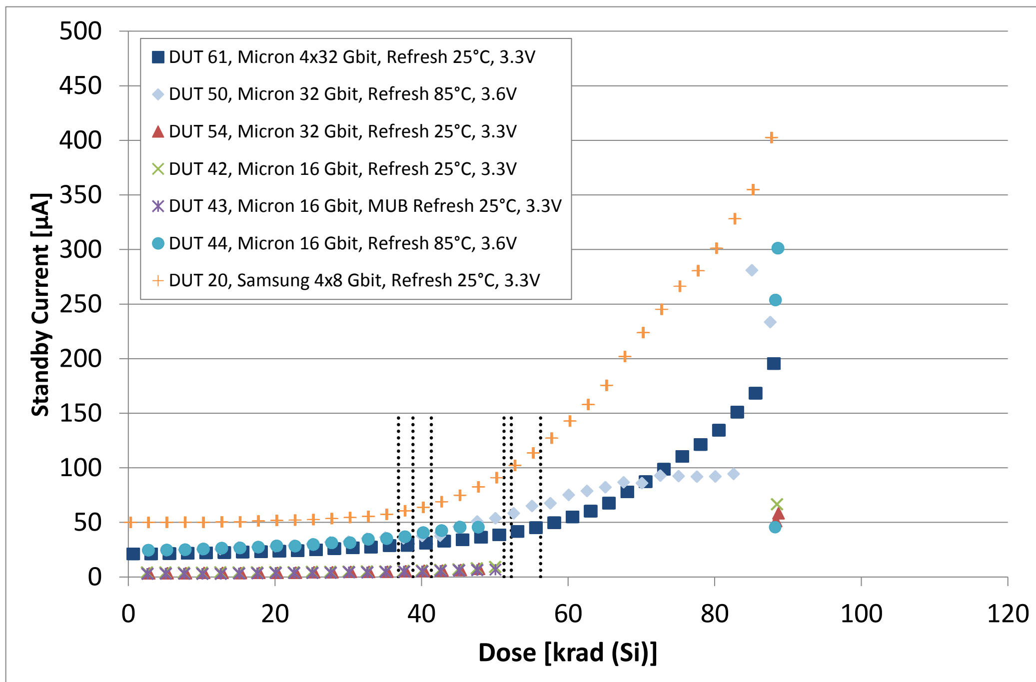

Fig. 15: Standby current versus dose of DUTs in Refresh Mode

3.2.3 Micron 16 Gbit, all modes

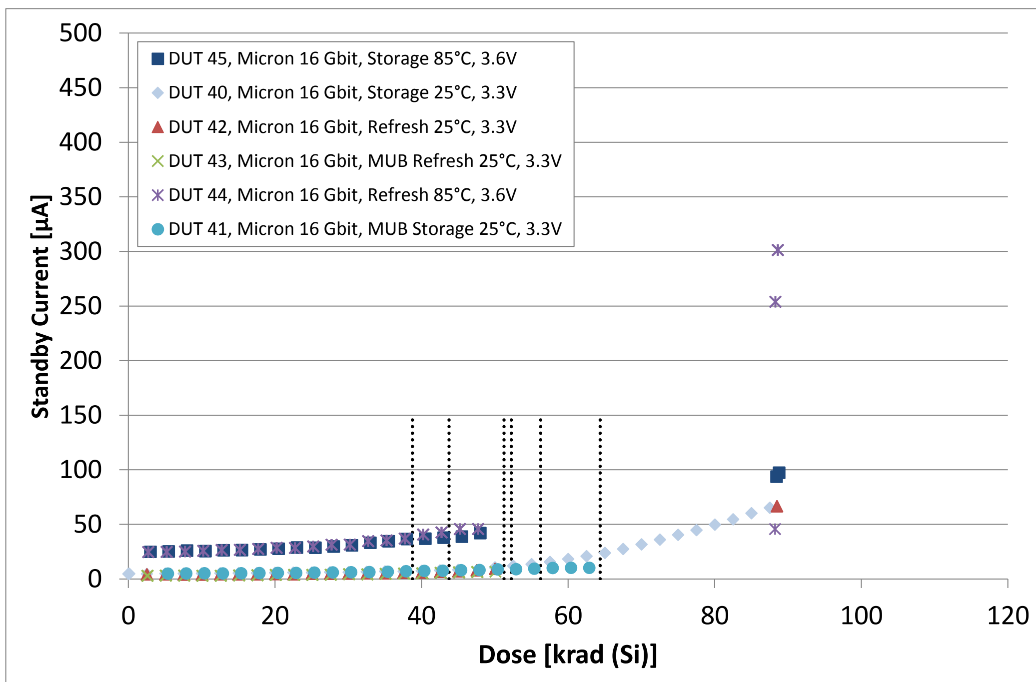

Fig. 16: Standby current versus dose of all Micron 16 Gbit DUTs

3.2.4 Micron 32 Gbit, all modes

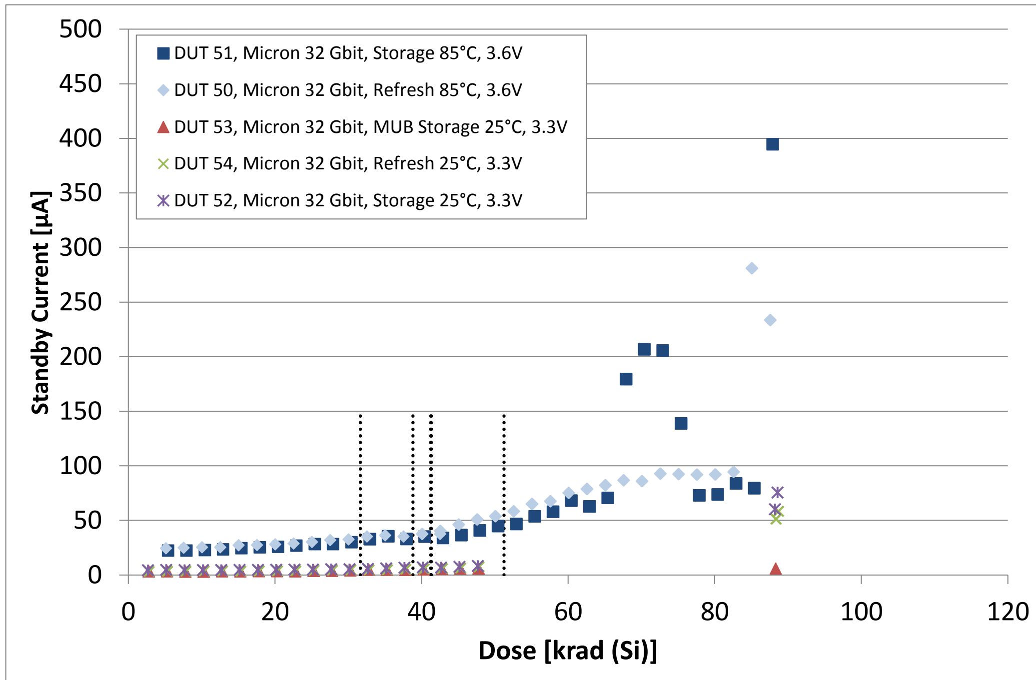

Fig. 17: Standby current versus dose of all Micron 32 Gbit DUTs

3.2.5 Micron 128 Gbit, all modes

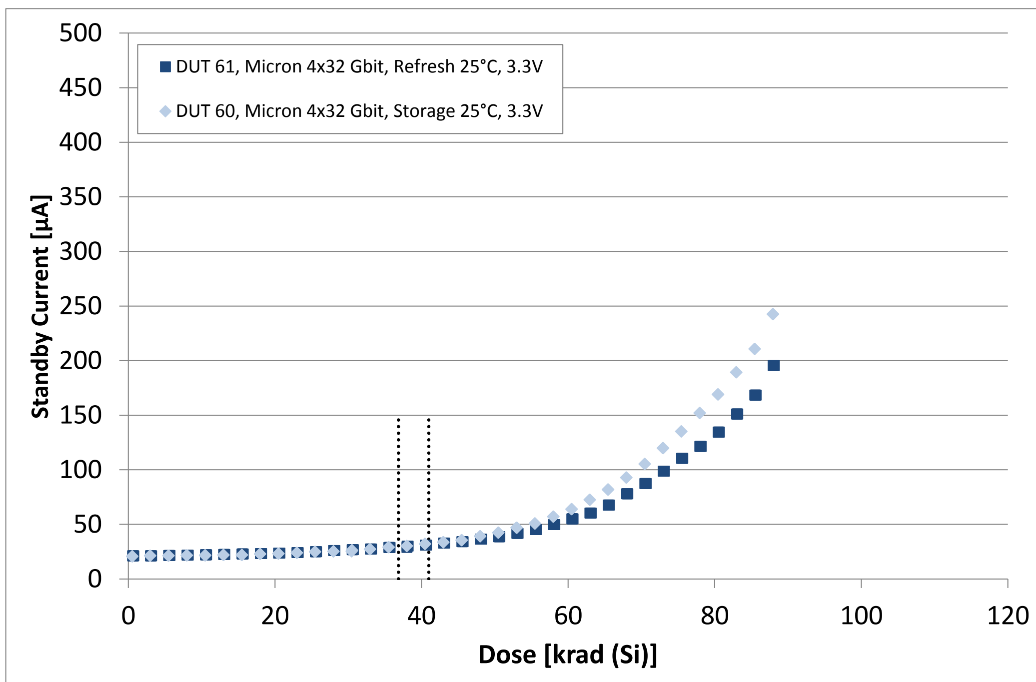

Fig. 18: Standby current versus dose of all Micron 4x32 Gbit DUTs

4 Discussion

During the test campaign Class A SEUs and Class D Device Failures were observed. Class B or C SEFIs did not occur.

4.1 Class A SEUs

The 25 nm Micron devices showed the first random data errors already between 5 and 10 krad (Si) in Storage Mode (Fig. 9) and between 3 and 30 krad (Si) in Refresh Mode (Fig. 10).

In contrast the 51 nm Samsung devices showed the first errors between 40 krad and 50 krad in earlier tests [3, Fig. 7.2] with a refresh period of 5 krad (Si). In this test the Samsung DUT20 in Refresh Mode showed the first errors after 70 krad (Si).

Compared to the previous 51nm Samsung NAND-Flash generation the TID tolerance of the more scaled 25 nm Micron NAND-Flash generation is reduced significantly with respect to the occurrence of random data errors (Fig. 7). Even the periodic refresh (Fig. 7) of the stored data after a few (in our test 2.5 krad (Si)) leads to no substantial shift of the error onset compared to Fig. 6.

Before ECC an error share of $1 \cdot 10^{-5}$ is tolerable, which is reached at 18 krad (Si) in Storage Mode, 85°C and at 25 krad (Si) in Storage Mode, 25°C. In contrast in Refresh Mode the error share threshold of $1 \cdot 10^{-5}$ is not reached until the occurrence of the Class D Device Failure. In conclusion the measure of periodic refresh of the stored data is effective.

In general the discrimination between the first TID induced Class A errors and errors originating from weak cells of the highly scaled NAND-Flash devices becomes more difficult with decreasing feature size because of the more frequent appearance of weak cell errors.

For example the early first error in Refresh Mode (Fig. 10, DUT61) could also be caused by a weak cell and therefore may have appeared also without irradiation.

As a countermeasure against the increased general error sensitivity the NAND-Flash manufacturers add a spare area to be used for ECC. At our tested so called “raw” NAND-Flash devices this error correction has to be built in by the user using this spare area.

The increasing sensitivity to not radiation induced FG errors is reflected by the increasing minimum number of additionally provided ECC bits with decreasing feature size (Fig. 19).

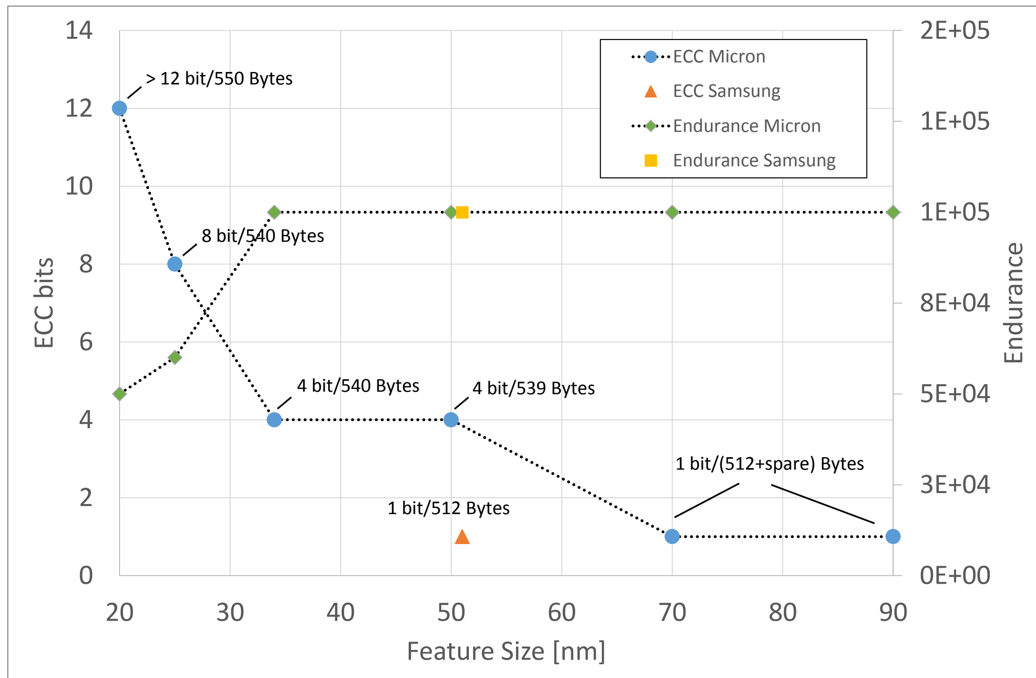

Fig. 19: Number of ECC bits and Endurance over feature size, data taken from various data sheets and roadmaps (the value 12 ECC bits per 550 bytes at 20 nm feature size is divided by two for comparability, according to the data sheet: 24 bit / 1110 Bytes, the exact value will be even higher than 12 bits)

As an additional measure the Micron 20 nm SLC devices have implemented a read retry feature in order to recover data that is beyond the ECC correction threshold but flagged by the error detection. The host controller can repeat the page read operation up to three times with different NAND-Flash internal read retry settings in order to attempt to retrieve a page with less errors that can be corrected by the ECC.

4.2 Class D Device Failure

In the dose range between 30 and 50 krad all Micron 25 nm DUTs showed a failure of the internal microcontroller which means that the stored data are not accessible anymore. The cause of defect is believed to be the internal microcontroller because not even a GetID-Command returned the correct 5 byte ID. Sometimes the first byte (0x2C) is retrieved correctly but already the bytes 2 to 5 are returned as 0x00. Also the ready-not-busy (R/B) signalling after an erase, program or read command is not working anymore. The dedicated R/B output of the NAND-Flash indicates activity of the internal circuitry.

Assuming that only this dedicated output is not working anymore a further functional test was done after irradiation. Instead of using the R/B output of the DUT to determine the ready state, always the maximum R/B time was inserted by the FTU. Also in this test no correct data could be read from the DUTs, neither before nor after the annealing test (chapter 4.3).

In contrast the 51 nm Samsung devices showed no complete loss of functionality within the applied dose regime (up to 60 - 150 krad) [3]. This is well in line with DUT 20 of this test which is completely functional after 90 krad (Fig. 10).

4.3 Annealing of Class D Device Failure

Three days after irradiation the DUTs were tested at room temperature. None of the DUTs was functional.

After that a high temperature annealing test was performed at 100° C for 168 h. Within this period the DUTs were checked twice, again none of the DUTs was functional.

Therefore the temperature was elevated to 150°C which is the maximum storage temperature of the Micron DUTs [5, 6] for another 168h. After that again none of the DUTs recovered.

4.4 Standby current

Tab. 4 shows the standby current at the beginning of the irradiation in the regime of 0 to 5 krad and at the point in time of the device failure (≈ 32 – 64 krad (Si)) for each DUT.

Those DUTs operated at the maximum supply voltage of 3.6 V show a standby current increased by a factor of 5 at the beginning of the irradiation compared to DUTs at the nominal supply voltage of 3.3 V.

Even in the dose regime of the Micron Device Failures the standby current is below the specified maximum datasheet value.

After the Micron Device Failures the standby current increases further. At the majority of the DUTs this increase is smooth but at some DUTs the standby current fluctuates. The standby current of all DUTs stays below 400 µA at 90.2 krad (Si).

The Samsung DUT shows an increase of factor 8 until the end of test at 90.2 krad (Si).

DUT	Mode	I_{SB} [µA] @ 0-5 krad	I_{SB} [µA] @ Device Failure
Micron 16 Gbit			
40	Storage, 25°C, 3.3V	4.6	8.4
41	MUB Storage, 25°C, 3.3V	5.0	10.3
42	Refresh, 25°C, 3.3V	4.1	9.1
43	MUB Refresh, 25°C, 3.3V	3.0	6.6
44	Refresh, 85°C, 3.6V	24.6	45.7
45	Storage, 85°C, 3.6 V	24.9	36.6
Micron 32 Gbit			
50	Refresh, 85°C, 3.6V	24.5	37.6

51	Storage, 85°C, 3.6V	22.4	32.9
52	Storage, 25°C, 3.3V	4.3	8.2
53	MUB Storage, 25°C, 3.3V	3.2	5.1
54	Refresh, 25°C, 3.3V	3.3	5.6
Micron 4x32 Gbit			
60	Storage, 25°C, 3.3V	20.7	32.0
61	Refresh, 25°C, 3.3V	21.1	28.8
Samsung 4x8 Gbit			
20	Refresh, 25°C, 3.3V	49.8	403 @ end of test

Tab. 4: Standby current at irradiation start and at device failure

4.5 Influence on temperature and supply voltage

All Micron 25nm DUTs operated at room temperature and 3.3 V supply voltage show a Class D Device Failure at an average dose of 47 krad (Si) compared to 41 krad (Si) for the four Micron 25nm DUTs operated at 85°C and 3.6 V supply voltage.

Taking (i) the sampling rate of 2.5 krad (Si) and (ii) the overall spread of 32 to 64 krad (Si) for the Micron Device Failures into account the influence of the temperature and supply voltage is only minor.

4.6 Comparison with the outcome of an unbiased pre-test

The different behaviour between Micron 25 nm and Samsung 51 nm devices is underlined by an unbiased TID test performed from March 11 - 18, 2013. During the unbiased irradiation of DDR3 SDRAM devices [9] also 6 NAND-Flash devices were irradiated unbiased up to 376 krad (Si) (Fig. 20, Tab. 5).

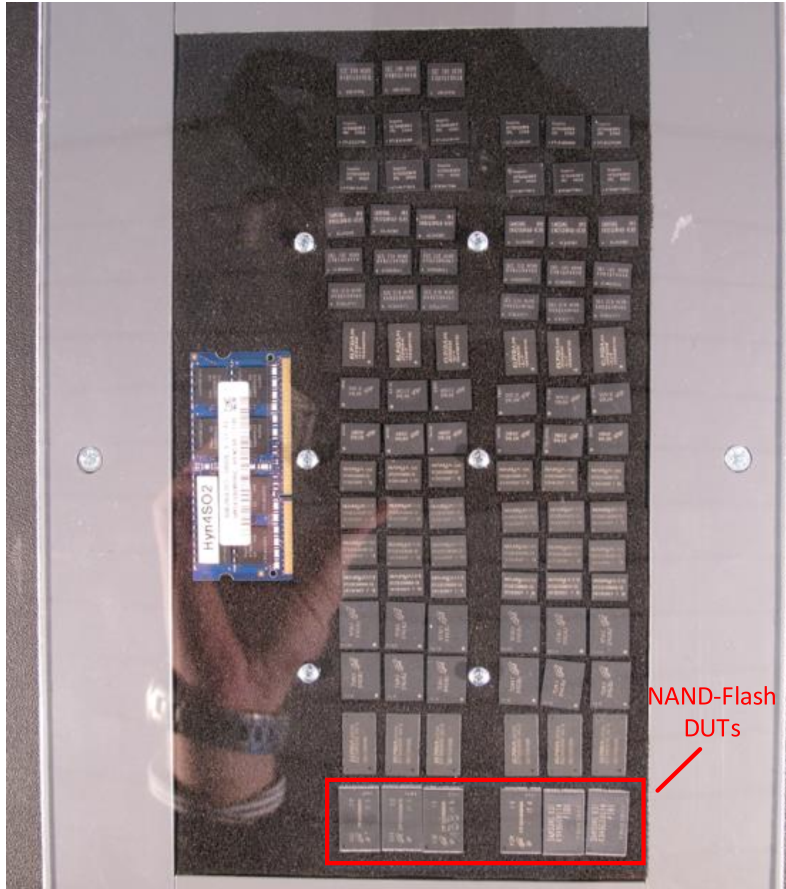

Fig. 20: Unbiased irradiation of 6 NAND-Flash DUTs mounted in a plastic frame with an acrylic glass cover

Manufacturer	Capacity [Gbit]	Feature Size [nm]	Package	Part Number	Date Code	Lot Code	Samples IDA ID
Samsung [4]	4x8	51	QDP	K9WBG08U1M-PIB0 (Fig. 21)	0837	FMH030X2	2 DUT5, DUT6
Micron [5]	16	25	SDP	MT29F16G08ABACAWP-IT:C (Fig. 22)	1212	-	1 DUT1
Micron [5]	16	25	SDP	MT29F16G08ABACAWP-IT:C (Fig. 23)	1218	-	1 DUT2
Micron [6]	32	25	SDP	MT29F32G08ABAAAWP-IT:A (Fig. 24)	1130	-	1 DUT3
Micron [6]	32	25	SDP	MT29F32G08ABAAAWP-IT:A (Fig. 25)	1134	-	1 DUT4

Tab. 5: NAND-Flash DUTs of unbiased TID test

Fig. 21: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 22: Micron MT29F16G08ABACAWP-IT:C NAND-Flash

Fig. 23: Micron MT29F16G08ABACAWP-IT:C NAND-Flash

Fig. 24: Micron MT29F32G08ABAAAWP-IT:A NAND-Flash

Fig. 25: Micron MT29F32G08ABAAAWP-IT:A NAND-Flash

All four Micron 25 nm devices are no more functional. Again even the basic internal controller functions like Get ID deliver only zeroes instead of 0x2C, 0x48, 0x00, 0x26, 0xA9 for the 16 Gbit Micron device and 0x2C, 0x68, 0x00, 0x27, 0xA9 for the 32 Gbit Micron device.

In contrast both 51 nm Samsung devices are functional. After irradiation a checkerboard pattern was written into 256 blocks. The read out afterwards delivered 2073 (Fig. 26) and 39990 (Fig. 27) SEUs.

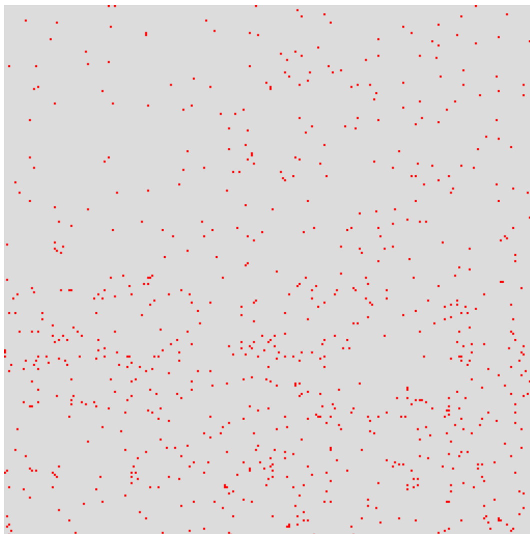

Fig. 26: Error map of Samsung 51 nm DUT5

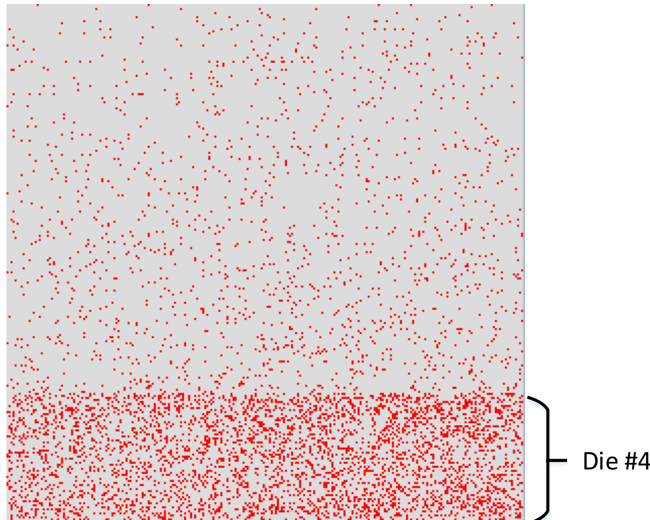

Fig. 27: Error map of Samsung 51 nm DUT6

The majority of SEUs in DUT6 appeared in the fourth die of the quad die package. The partially different error counts in dies assembled in one package were also observed in the in-situ test of Samsung 51 nm devices [3, Fig. 6.1 to 6.4b].

At Samsung DUT5 a wear out test was performed in order to check for an impaired endurance which is specified as 100K program/erase cycles [4].

In contrast to previous IDA wear out tests were Samsung 51nm devices reached about 1E6 program/erase cycles with [10] or without (Fig. 28) gamma irradiation the test sequence was modified in this test. Instead of programming only one page of the 64 pages of one block with zeroes, in this test all pages of the accessed blocks were programmed with zeroes, which induces the maximum stress to the FG cells and the high voltage generator during the program/erase operations. The reached wear-out cycles are compared in Fig. 28 for both wear out test routines.

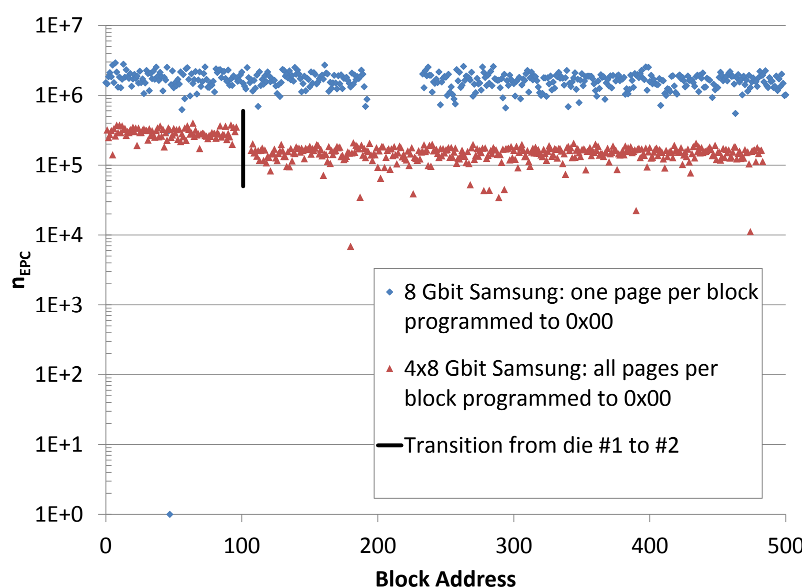

Fig. 28: Distribution of the wear-out limits in the first 500 blocks, Samsung 8 Gbit and Samsung 4x8 Gbit 51nm NAND-Flash

If all pages are programmed to zero the number of erase/program cycles (n_{EPC}) is reduced to 1.5E5 to 3E5. Again different dies of the quad die package behave slightly different (Fig. 28, black line) with respect to the mean erase program cycle count as shown also for SEUs (Fig. 27).

The tested five blocks of Samsung DUT5 showed comparable numbers of erase/program cycles (Tab. 6), all well above the specified limit of 100K cycles.

Block No	n_{EPC}	Status flag (E: erase, P: program operation failed)
1	342988	E
2	475266	E
3	396789	E
4	460299	E
5	352366	E

Tab. 6: Distribution of the wear-out limits in the first 5 blocks, Samsung 4x8 Gbit 51nm NAND-Flash DUT5

The stored content (all 0xFF after erase and all 0x00 after program) was checked every 20K erase/program cycles. No errors were detected.

In conclusion compared to the previous 51nm Samsung NAND-Flash generation the TID tolerance of the 25 nm Micron NAND-Flash generation is reduced significantly with respect to the complete loss of storage functionality as well as to the SEU sensitivity.

This is well in line with the results presented by F. Irom [11]. In this work five samples of 32 Gbit 25 nm Micron devices with the same part number (MT29F32G08ABAAA) but different date code were tested. They failed (i) post 40 krad (Si) and post 50 krad (Si) using a refresh mode and (ii) at 55, 75 and 70 krad using a storage mode with read after irradiation.

5 Conclusion

The general rule that decreasing feature size (from 50 nm to 25 nm) should result in a better TID tolerance does not hold. It is not the case for the Micron 25 nm generation. Neither the error onset nor the Device Failure can be influenced by the operating conditions like test mode, supply voltage or DUT temperature. Only the steep error increase (Fig. 9) can be suppressed by periodic refresh of the stored data at least every 2.5 krad (Fig. 10).

From the TID point of view the 25 nm Micron generation is suitable for applications up to a total dose of 25 krad using a suitable error correction scheme and using a periodic refresh. The periodic refresh keeps the error share below $1 \cdot 10^{-5}$ which is tolerable before ECC. Therefore with periodic refresh the Device Failure occurrence determines the total dose.

6 References

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