Technische Universität
Braunschweig

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UND KOMMUNIKATIONSNETZE

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K. Grürmann, M. Herrmann, F. Gliem

Proton Test
of
16-Gbit/32-Gbit Micron
SLC NAND-Flash Memory Devices

PSI PIF, April 4-6, 2014

Test Report

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Contents

1 Abstract

From April 4 to April 6, 2014, we performed a proton SEE test with NAND-Flash devices at Paul Scherrer Institut, Villigen, Switzerland. This document reports on the findings.

2 Test setup

2.1 DUTs

The DUTs are described in Tab. 1. Package figures are shown in chapter 8.

Manufacturer	Capacity [Gbit]	Feature Size [nm]	Package	Part Number, Chip picture	Date Code	Lot Code	Samples	IDA ID
Samsung [1]	4x8	51	QDP	K9WBG08U1M-PIB0	0837	FMH030X2	2x1	SA26 - SA27
Micron [2]	16	25	SDP	MT29F16G08ABACAWP-IT:C	1218	-	5x3	M46 - M60
Micron [3]	32	25	SDP	MT29F32G08ABAAAWP-IT:A	1134	-	5x3	M76 - M90
Micron [3]	4x32	25	QDP	MT29F128G08AJAAAWP-ITZ:A	1314	-	4x1	M95 - M98

Tab. 1: NAND-Flash DUTs

The DUTs are soldered on elongated DUT carriers.

First all DUTs were marked by an individual ID and were checked for factory marked bad blocks. The ID and the bad block table were programmed into block 0 which is guaranteed to be valid by the manufacturer for every DUT. These bad blocks were not accessed by erase or program operations anymore.

The die diagonal of the largest die is smaller than 21 mm.

2.2 Test facility

The tests were performed at the Proton Irradiation Facility (PIF) of Paul Scherrer Institut (PSI) at Villigen, Switzerland described in [4]. We used proton energies of 230 and 101.4 MeV as initial energies without degraders and 49.64, 32.88, 21.37, 13.28 MeV as degraded energies. The beam was collimated by a round collimator with a diameter of 30 mm.

2.3 Test bench

The test bench RTMC5 (Fig. 1, Fig. 2) is capable of operating up to 8 NAND-Flash DUTs in the configuration for proton tests.

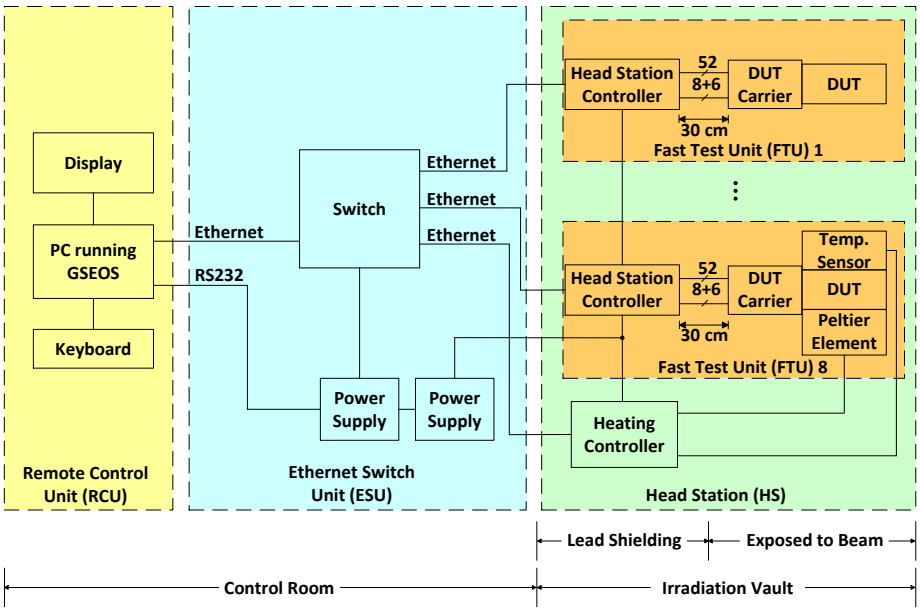

Fig. 1: Block Diagram of the NAND-Flash test setup with eight DUTs configured for proton SEE tests

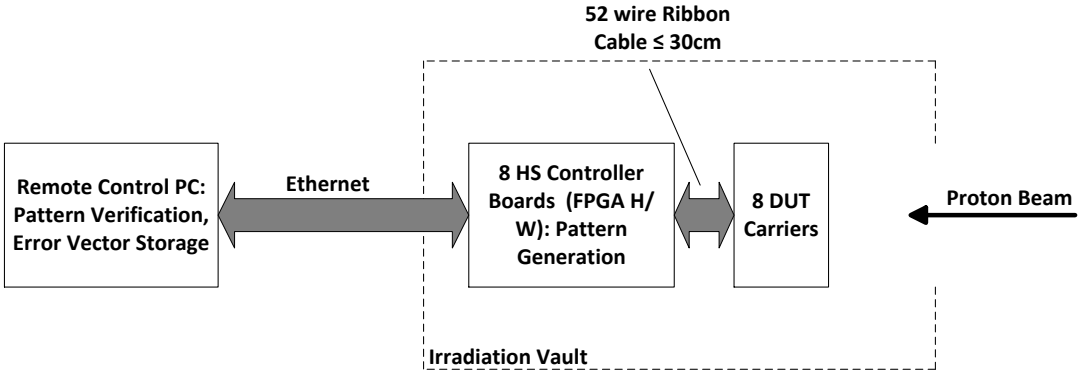

Fig. 2: NAND-Flash test setup at the proton irradiation facility

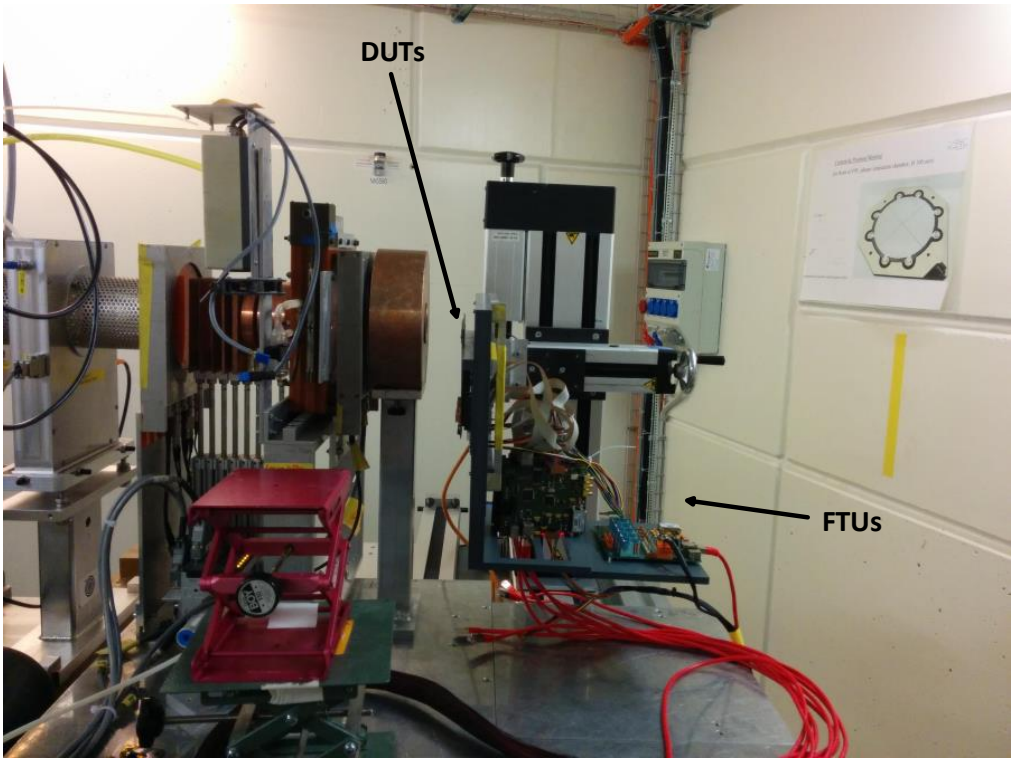

Fig. 3: Test bench mounted at the beam line

Eight elongated DUT carriers are exposed to the proton beam. Each DUT carrier is served by its own Fast Test Unit (FTU). The FTUs are supplied by 5 and 12V and generate a DUT supply voltage between 2.7V and 3.6 V, settable by the Remote Control Unit (RCU). The FTUs measure continuously the standby current and the operating current of the DUTs. The FTUs are equipped with a Latch Up Switch. Its current threshold is RCU settable between 50 mA and 200 mA, and its delay time between 1 µs and 1 ms. Measurement of program time and erase time is an additional feature of the FTUs. The Remote Control Unit is based on a PC running our proprietary configurable GSEOS V test S/W package. On the PC, an error map is displayed for preliminary visual analysis, along with a total error count and various statistics. The error vectors are stored on disk for offline analysis.

The RCU provides (i) control of the test sequences (test modes), (ii) generates specific data pattern and address loops, (3) supports the setting of all test parameters, (iv) performs a real time pattern verification, (v) counts data errors in real time, (vi) records all error vectors, current and time measurements, Latch up trigger actions and all parameter settings for off line evaluation of the test data files, (vii) delivers a real time visualization of the error distribution, of several statistical distributions, such as the direction of bit falsification or the number of falsified bits per byte.

2.4 Test sequence

The tests were performed with a checkerboard pattern.

To retrieve static and dynamic data errors as well as more sophisticated data error patterns such as error clusters, and also SEFIs, three main test modes with several options each have been developed and were used:

- Storage Mode (M3)

  Before irradiation a pattern (all ones, all zeros, checkerboard, random) is written into the DUT and verified. Default is the checkerboard pattern. Then the device is irradiated biased (M3a) or unbiased (M3b). After exposure the content of the device is read and verified. Only static data errors are delivered by this mode.

- Read Mode (M2R)

  Before irradiation a pattern is written into the DUT and verified. During the exposure the content of the device is continuously read and verified, each page either one time or two times. The dual read option provides differentiation between static and dynamic data errors. After the exposure the content of the device is read again. If SEFIs remain a power cycle and a reread is performed.

- Marching Mode (M1, M5)

  Before irradiation a pattern is written into the device and verified. During exposure the content of every single block of the device is read and verified; then erased and verified again; and then programmed and verified page by page with the inverted pattern, continuously block by block, again and again. This mode exercises a mixture of read, erase and program operations. In this mode the DUTs are susceptible to SEFIs of all kinds, in particular to Persistent SEFIs and also because of the numerous erase operations to Destructive SEFIs. For some NAND-Flash types the insertion of a power cycle (PC) after each erase operation reduces drastically the sensitivity to SEFIs, in particular to Destructive SEFIs [5]. The Marching Mode M1 runs without the insertion of PCs, the Marching Mode M5 with insertion of PCs. The power off duration is selectable (default: 1 ms).

2.5 Error classification

Several error classes are distinguished, according to the overview shown in Fig. 4.

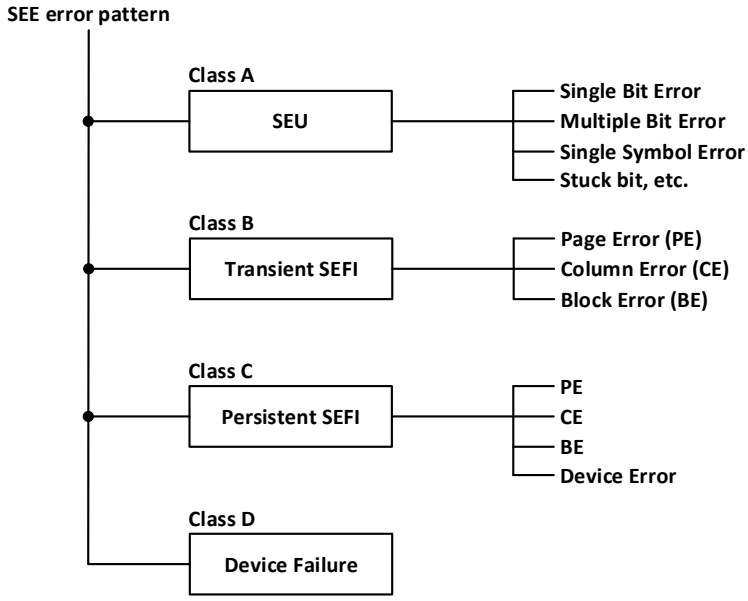

Fig. 4: Error classification scheme

An example error map, containing SEUs, page, row and block SEFIs is shown in Fig. 5.

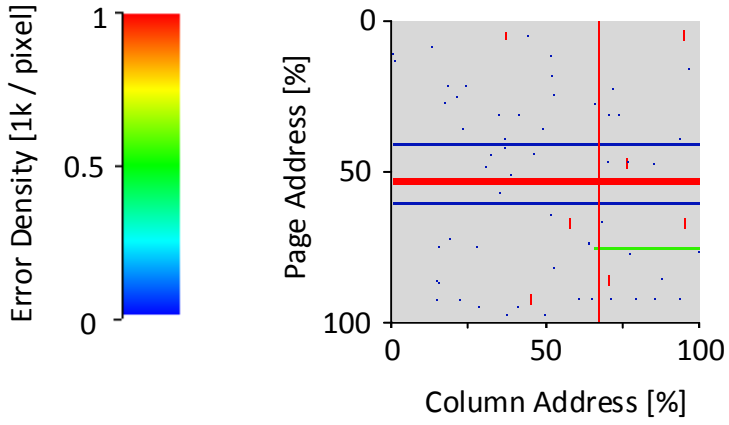

Fig. 5: Example quick look error image

2.6 Test restrictions

The main test restrictions are:

1) The Micron 25 nm 16 Gbit and 32 Gbit NAND-Flash DUTs should not be exposed to more than about 12.5 krad given by the TID response [6] in order to achieve a clear differentiation between SEE and TID induced errors and other impairments of the DUT functionality.

2) The test time was limited to 24h. Because of problems during customs clearance the start of the test was delayed by about 7 hours.

3) The PIF staff recommended us to start with the highest energy of 230 MeV. Furthermore we were recommended to do all test runs without any paraffin shielding of the test bench situated below the beam line (Fig. 3). This is a contrary approach compared to the last IDA NAND-Flash campaign at PIF in 2009.
At the high energy of 230 MeV the test bench switched into a current limiting mode several times. For safety reasons we reduced the number of FTUs from 8 to 4 operated simultaneously in order to have spare parts in case of a permanent damage which did not occurred. Below 100 MeV the test bench run without any further interference.
At a potential further test at PSI one should irradiate according to the test plan starting in the low energy regime.

3 Test results

The total dose received by any DUT was less than 14 krad. To avoid falsifications by dose effects at first only test runs with DUTs are shown which total dose received before is less than 3 krad. Test runs with previously irradiated DUTs are marked with the dose in the cross section diagram.

Error bars are calculated using the Poisson distribution with 95% confidence limits.

3.1 Class A SEUs

The following diagrams show the cross section versus energy for the Micron 16 Gbit and 32 Gbit device. In contrast to heavy ion irradiation with protons only one bit per byte is flipped.

For the 16 Gbit test runs a dependence on the used PIF x-y table position was found (blue and red diamonds of Fig. 6). With one exception the DUTs at position 3 showed a lower FG SEU count compared to x-y position 2.

At the energy of 32.88 MeV four fresh DUTs were irradiated. Two of them about 2 hours later than the first two (Fig. 6, question mark). The error count of both DUTs irradiated at a quarter past one is significantly reduced.

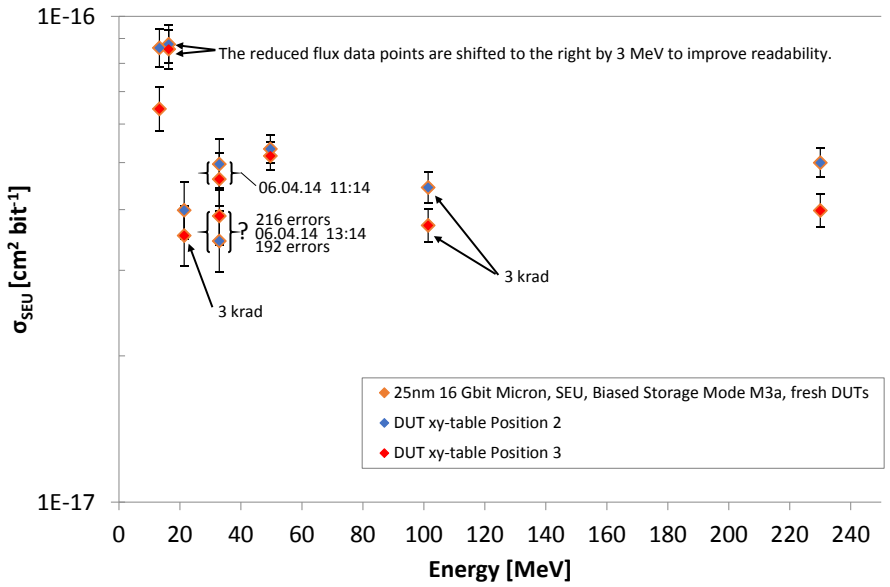

Fig. 6: SEU cross section versus proton energy in Biased Storage Mode M3a

For the 32 Gbit test runs (Fig. 7) the dependence on the used PIF x-y table position is more random.

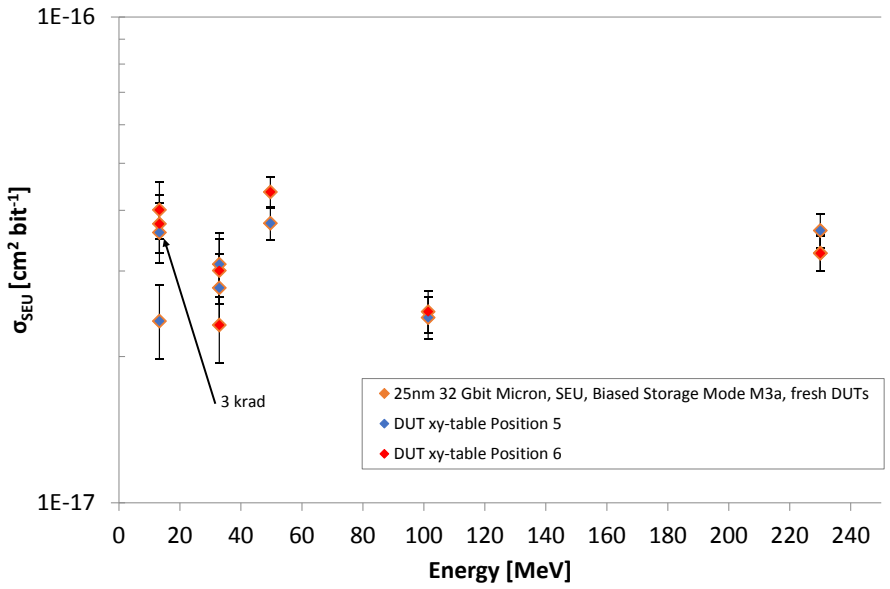

Fig. 7: SEU cross section versus proton energy in Biased Storage Mode M3a

3.2 Class B + C SEFIs

Because of (i) the reduced test time (section 2.6) and (ii) the time consuming investigation of the Class A SEUs at low energy (section 3.1), SEFI test runs with test modes M1 and M2 were conducted only at energies of 101.4 and 230 MeV.

No Class B SEFIs were observed. All 7 SEFIs were Class C SEFIs which means that they remained during the next read operation but disappeared after a power cycle.

3.2.1 Marching Mode M1

In Marching Mode M1 four SEFIs were found at the tested energies, fluence 3E10 cm^{-2}

- 1 Block Error (BE) @ 16 Gbit Micron, 101.4 MeV
- 1 Page Error (PE) @ 32 Gbit Micron, 230 MeV
- 2 Column Errors (CE) @ 32 Gbit Micron, 230 MeV

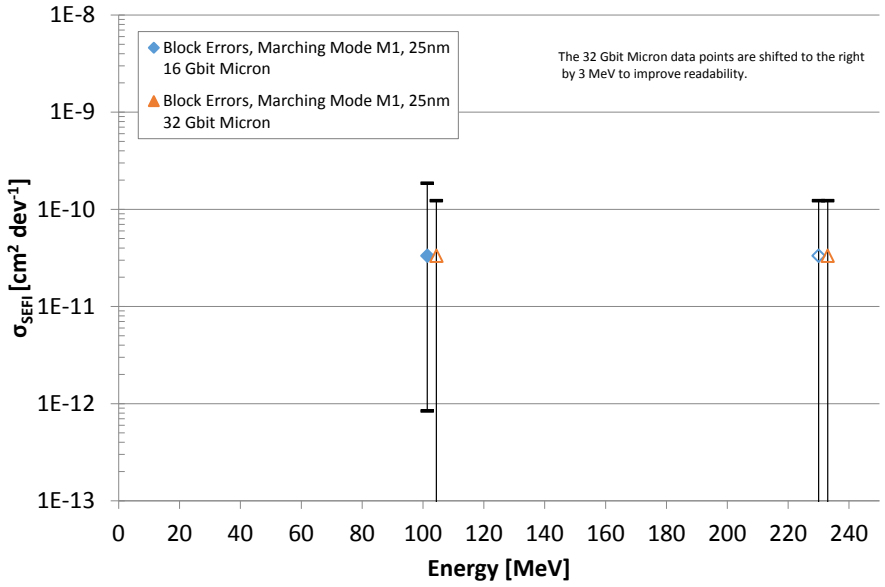

Fig. 8: Block Error cross section versus proton energy in Marching Mode M1

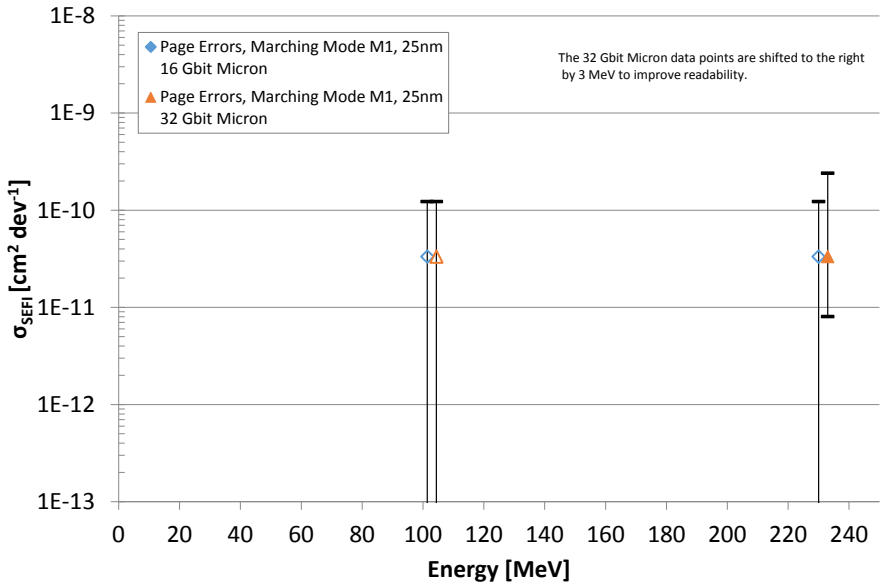

Fig. 9: Page Error cross section versus proton energy in Marching Mode M1

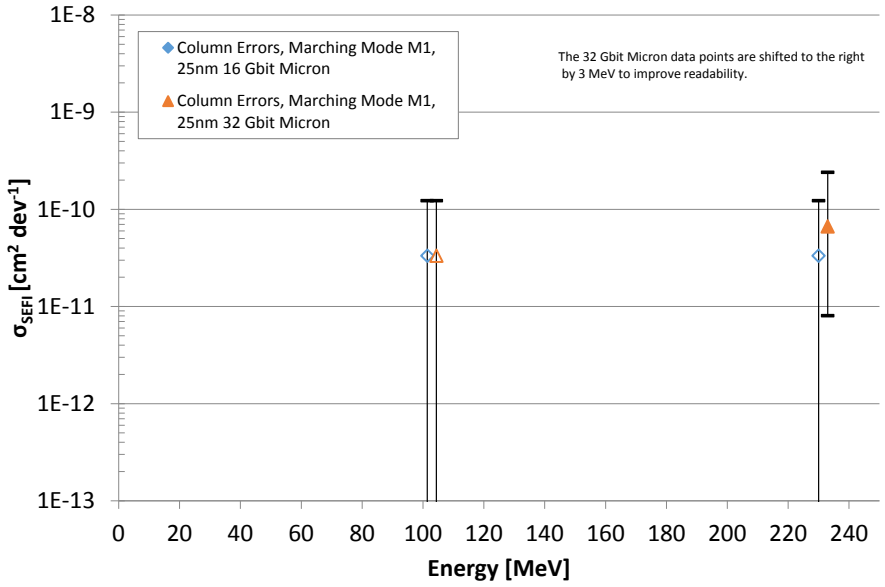

Fig. 10: Column Error cross section versus proton energy in Marching Mode M1

3.2.2 Read Mode M2R

In Read Mode M2R three SEFIs were found at the tested energies, fluence 3E10 cm^{-2}

- 2 CE @ 16 Gbit Micron, 230 MeV
- 1 PE @ 32 Gbit Micron, 230 MeV

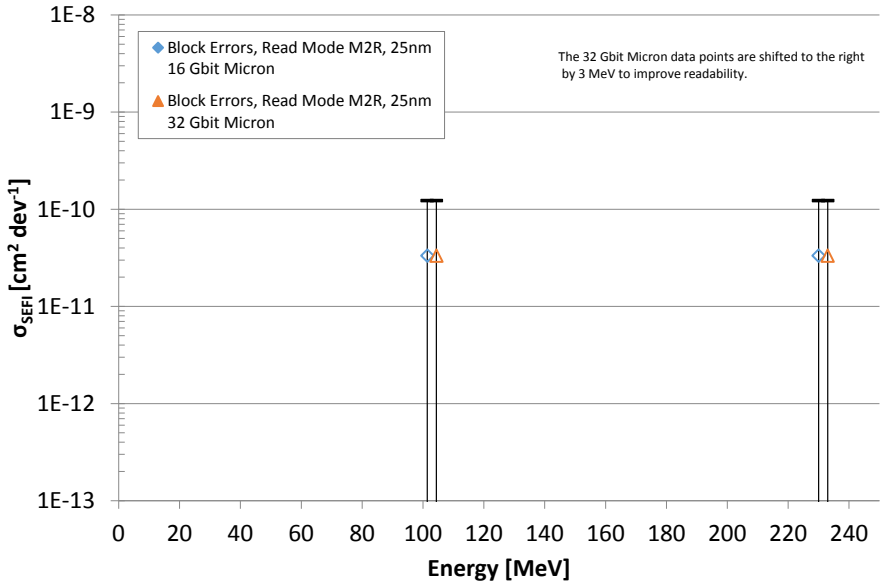

Fig. 11: Block Error cross section versus proton energy in Read Mode M2R

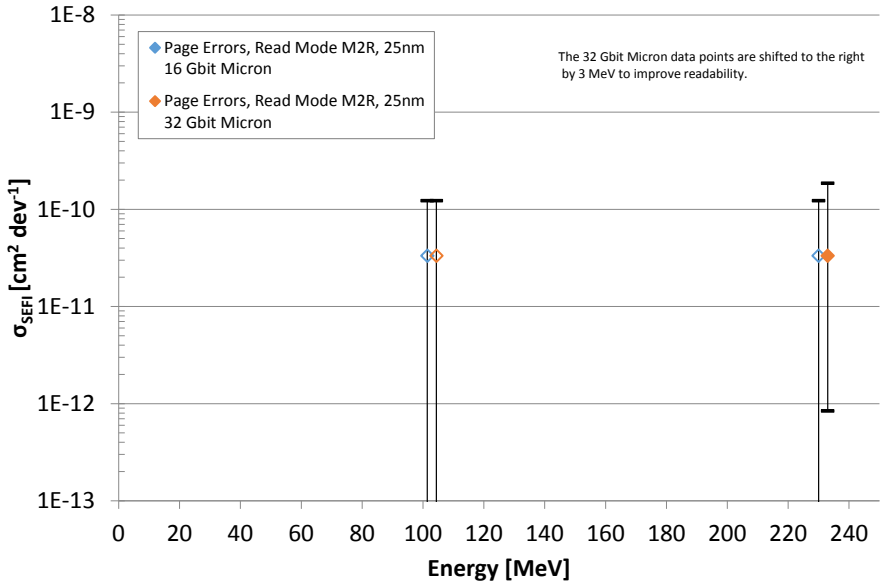

Fig. 12: Page Error cross section versus proton energy in Read Mode M2R

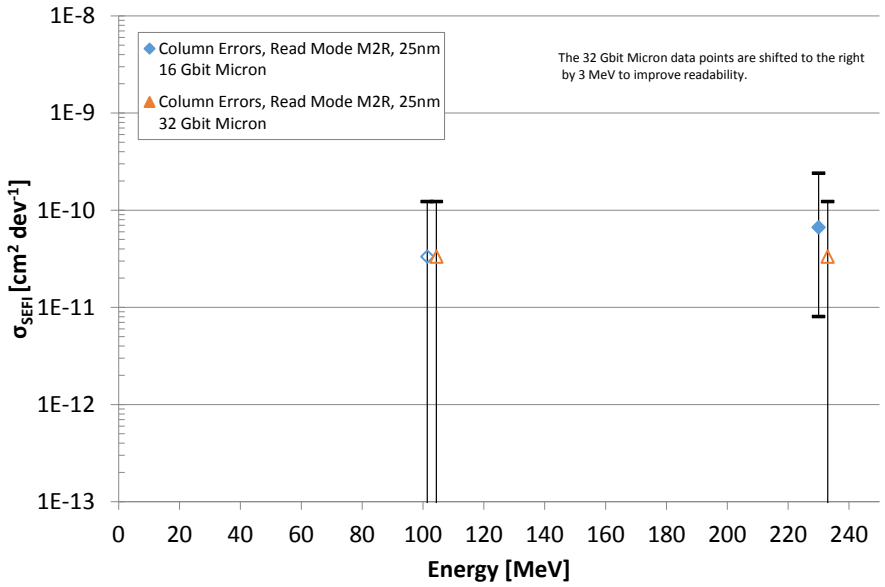

Fig. 13: Column Error cross section versus proton energy in Read Mode M2R

3.2.3 Storage Mode M3a

Also the biased storage mode (M3a) used for all Class A SEU investigations delivered 12 SEFIs.

Energy [MeV]	Fluence [cm^{-2}]	PE	CE	BE
13.28		-	-	-
21.37	1E10	-	1	-

32.88	3E10	1		
32.88	1E10		1	-
49.64	3E10	1	1	-
101.4	3E10	3		1
230	3E10	3	-	-

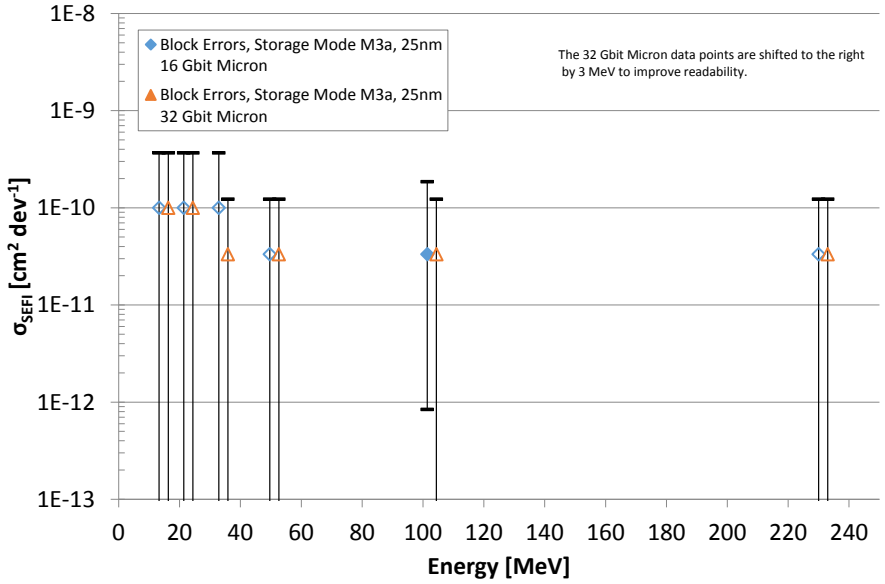

Fig. 14: Block Error cross section versus proton energy in Storage Mode M3a

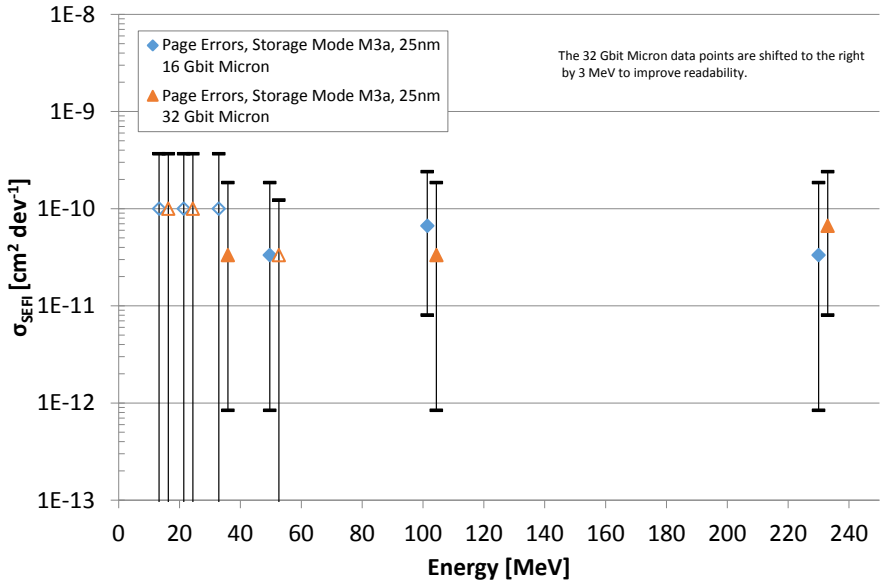

Fig. 15: Page Error cross section versus proton energy in Storage Mode M3a

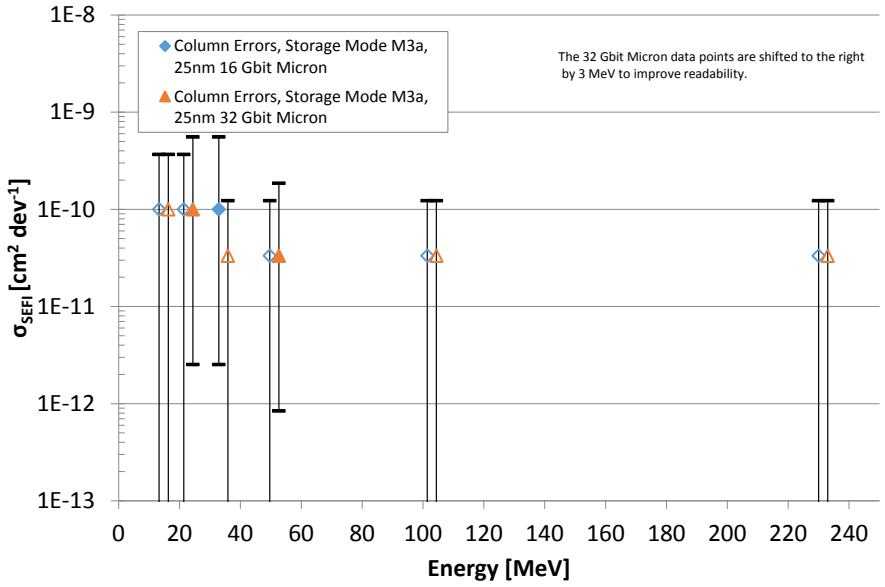

Fig. 16: Column Error cross section versus proton energy in Storage Mode M3a

3.3 Class D Device Failure

During the complete test no device failure such as Destructive Failure or SEL was observed.

3.4 Annealing

At two Micron 16 Gbit DUTs and two Micron 32 Gbit DUTs the annealing behaviour was studied. The four DUTs were irradiated with 1E10 cm^{-2} protons of 32.88 MeV energy. Directly after irradiation and after about 1.5, 4.5 and 13.5 hours the content of the tested subset was read (Fig. 17).

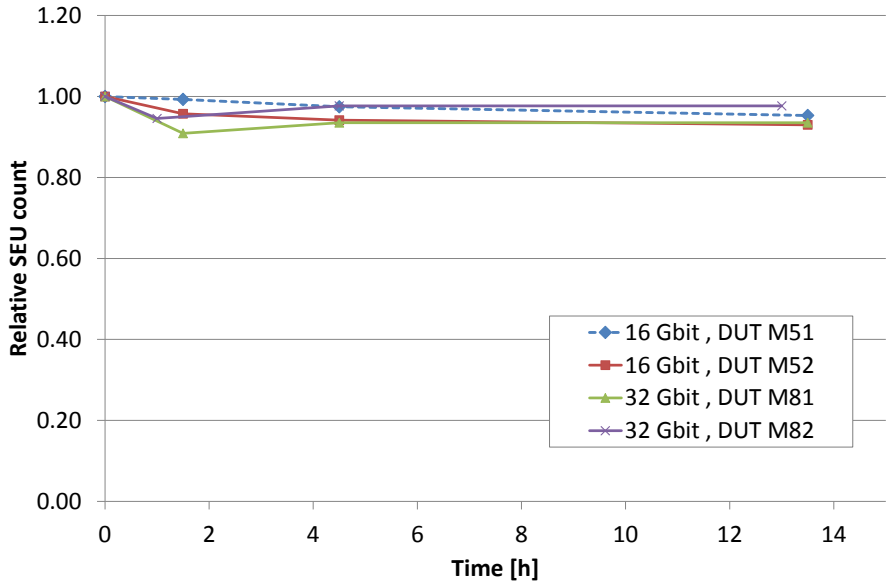

Fig. 17: Annealing of Micron FG SEUs, Fluence 1E10 cm-2, 32.88 MeV protons

4 Discussion

4.1 Class A SEUs

4.1.1 Comparison with previous NAND-Flash generations

Fig. 18 shows both, the Micron 25 nm and the Samsung 51 nm SEU cross sections derived by IDA. The Micron 25 nm cross section is about three orders of magnitude higher due to their more scaled cells.

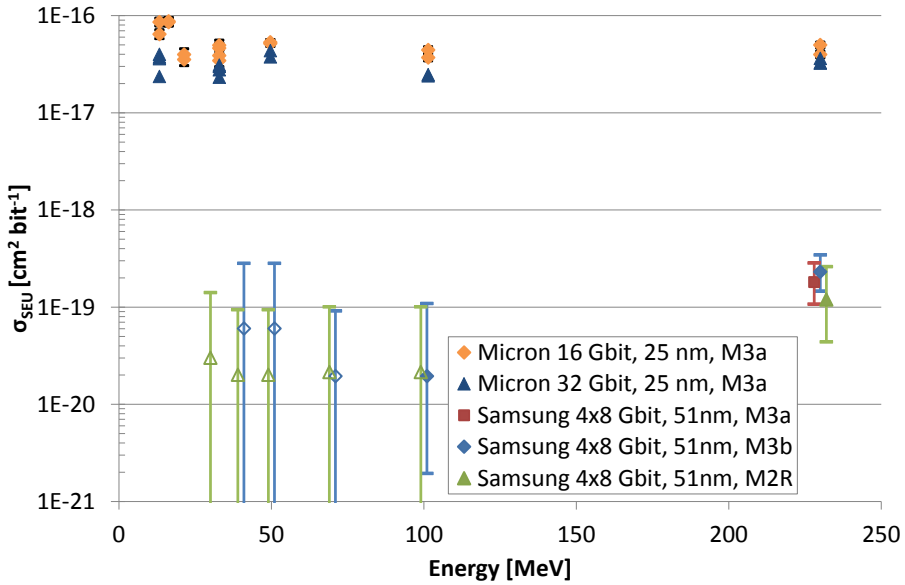

Fig. 18: Comparison between Micron 25 nm and Samsung 51 nm SEU cross sections

Fig. 19 shows the SEU cross sections reported for 34 nm Micron SLC NAND-Flash [7], which are situated between the 25 nm Micron and 51 nm Samsung cross section. As Tab. 2 shows the scaling from 51 nm to 25 nm leads to a substantially increased SEU sensitivity.

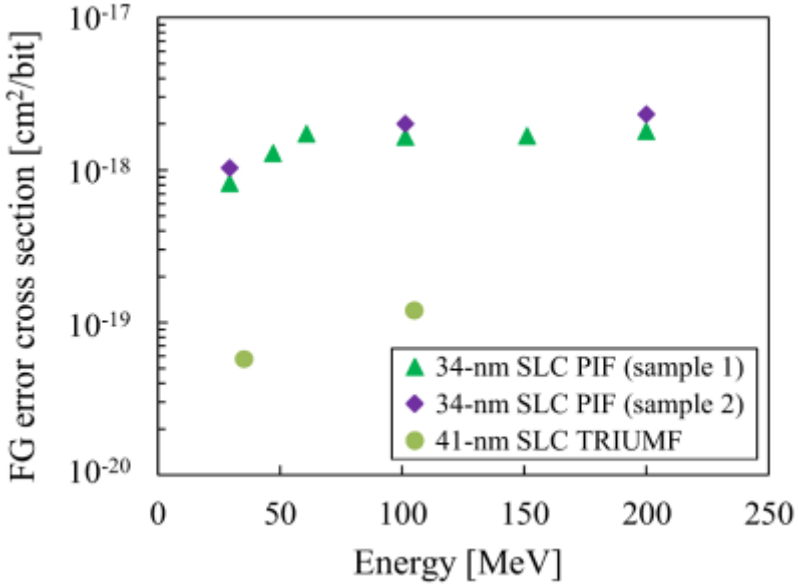

Fig. 19: Micron 34 nm and 41 nm SEU cross sections [7]

SLC Feature Size [nm]	Mean SEU cross section [cm2 /bit]	Trend to low energy
25 (16 Gbit)	≈ 5E-17	increasing
25 (32 Gbit)	≈ 3E-17	increasing ?
34	≈1.5E-18	decreasing
41	≈ 1E-19	decreasing
51	≈ 7E-20	no errors below 70 MeV

Tab. 2: Comparison of SEU cross section shapes from 25 nm to 51 nm SLC feature size

4.1.2 Low energy proton sensitivity

A potential larger error cross section due to direct ionisation in the low energy range is a point of concern for modern devices (≤ 25 nm).

The error counts at low energy unfortunately show a rather wide spread (Fig. 7 and Fig. 17). At least in Fig. 6 this spread seems to correlate with the position of the x-y table, and by that means with inhomogeneities of the degraded proton beam.

The data points in Fig. 6 and Fig. 7 give some indications of an increase of the error cross section towards lower energy, but no clear evidence.

At least for both tested DUTs no decrease of FG SEUs was measured as found at devices of larger feature size (Fig. 19).

Because of this ambiguous result this point was investigated further. Therefore two fresh 16 Gbit and two fresh 32 Gbit DUTs were irradiated first at 13.28 and thereafter at 21.37 MeV. The total dose of each DUT remained below 9 krad. The fluence was 1E10 cm^{-2} and the flux was reduced to about 7E6 cm^{-2} s^{-1} resulting in 24 minutes of beam time in order to exclude error variations coming from rapid annealing. The cross section of these low flux runs is shown in Fig. 20.

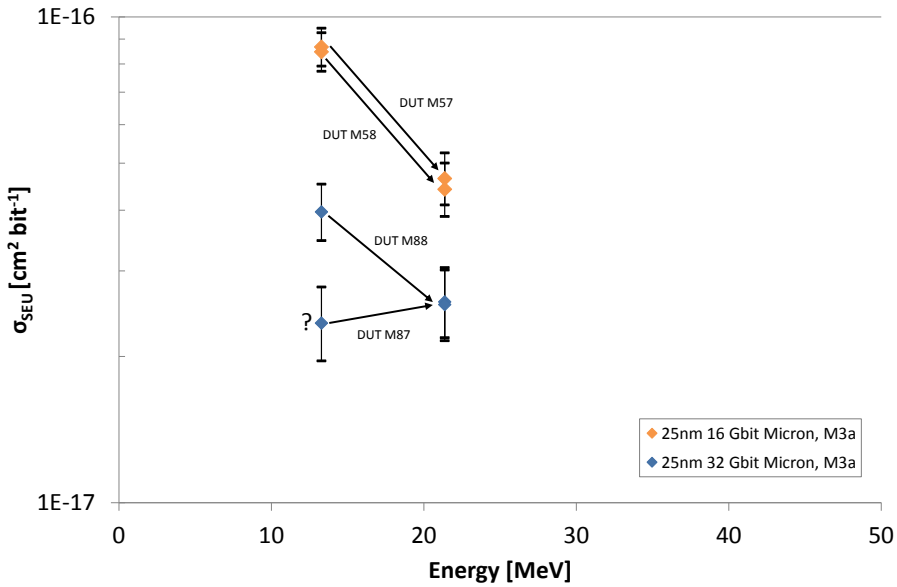

Fig. 20: Results of the low flux test runs, SEU cross section versus proton energy in Biased Storage Mode M3a.

Three out of four comparative low flux measurements between 13.28 and 21.37 MeV show a decrease of the error count in the same range. What happened at the test run marked with a question mark is unclear. At the subsequent 21.37 MeV test runs both measurements of 32 Gbit DUTs fit perfectly. No explanation could be found neither from the IDA test logs, nor from the PSI run files. The complete test configuration was unchanged, with the exception of the necessary x-y-table movements and the energy change by degraders. This is as dubious as the changed FG error count at 21.4 MeV at the test repetition two hours later (question mark in Fig. 6).

Nevertheless the test results show an increase of the error count with decreasing energy from 21.4 MeV down to 13.3 MeV by a factor of 2 for the 25 nm 16 Gbit SLC Micron devices and by a factor of 1.5 for the 25 nm 32 Gbit SLC Micron devices.

The increase of the error cross section towards low energy was reported by the Padua team [7, Fig. 2] on 25 nm Micron MLC devices. For SLC parts it should be investigated in more detail. One open question is at what proton energy the peak error count is reached. Therefore an additional test of SLC NAND-Flash should focus on low energy protons.

4.1.3 Annealing

In general the annealing of FG errors has a strong temperature dependence on the one hand concerning the temperature during the read out phase, on the other hand concerning the tem-

perature between the successive read outs. Here the DUT temperature is regarded as constant because the storage and read out of the DUTs was done in the PIF irradiation room.

Also during proton irradiation a small number of FG errors disappear with time (Fig. 17).

Already at the second read out about 1.5h after the irradiation the FG error count is reduced by 1 – 9 %. After about half a day the FG error count has reached a stationary value between 94% and 98% of the initial error count.

4.2 Class B + C SEFIs

The Marching Mode M1 without power cycling before the erase operation was used because it is a worst case test mode for SEFIs including erase, program and read operations.

During the whole test campaign no Class B SEFIs and 10 PE, 7 CE and 2 BE (all Class C) were observed at the Micron 16 and 32 Gbit DUTs. In comparison the whole Samsung 4x8 Gbit test campaign [8] delivered one Class B PE.

As shown at the heavy ion tests the 25 nm Micron NAND-Flash are more sensitive to SEFIs, in particular to CEs, which were not observed at Samsung devices.

In general an effective measure against all SEFIs is power cycling of the NAND-Flash. With a power cycle all proton induced SEFIs could be removed and the affected page, column or block was read out correctly apart from SEUs thanks to the non-volatility.

5 Conclusion

Scaling from about 50 nm down to 25 nm leads to (i) an increased SEU cross section by about three orders of magnitude and (ii) a constant or increasing SEU cross section down to the lowest energy of 13.3 MeV. This effect should be investigated in more detail with the focus on energies below 10 MeV. It might be even worse for 20 nm SLC NAND-Flash parts which are already in mass production.

All observed SEFIs belong to Class C which means that they can be removed only by power cycling of the DUT.

No Class D Device Failure was observed.

6 References

[1] Samsung NAND-Flash Data Sheet ”2G x 8 Bit / 4G x 8 Bit / 8G x 8 Bit NAND Flash Memory”, Rev. 1.3, Nov. 29th 2007

[2] Micron M72A_Production_Datasheet_RevG.pdf, Rev. G 5/12 EN

[3] Micron M73A_Production_Datasheet_RevF.pdf, Rev. F 5/12 EN

[4] PSI PIF High Energy Site, http://pif.web.psi.ch/

[5] M. Brüggemann, et al., “SEE Tests of NAND Flash Memory Devices for Use in a Safeguard Data Recorder”, RADECS 2006, A-3, 2006

[6] K. Grürmann et al., “Functional TID Test of 16-Gbit/32-Gbit Micron SLC NAND-Flash Memory Devices”, Test Report, TN-IDA-RAD-14/4, March 2014

[7] M. Bagatin et al., “Proton-Induced Upsets in SLC and MLC NAND Flash Memories”, IEEE Transactions on Nuclear Science, vol. 60, no. 6, pp. 4130-4135, December 2013.

[8] H. Schmidt et al., “Proton Test of 4 x 8-Gbit Samsung NAND-Flash Memory Devices K9WBG08U1M-PIB0”, Test Report, TN-IDA-RAD-09/7, Sept. 2009

7 Run tables

*) Without irradiation the following actions were performed and recorded: BG – Write Background, R – Reread, PC, R: Reread after power cycle

7.1 Micron 16 Gbit

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
05/04/2014 13:43:59	2			2	1	2	230	151	3.01E+10	1.61E+03	1.99E+08	2	832	
05/04/2014 14:34:43	7		M2_R	7	1	2	230	153	3.02E+10	3.22E+03	1.97E+08	32	918	1ce
05/04/2014 14:38:29	7a	R			1	2	230			3.22E+03			826	
05/04/2014 14:40:47	7b	PC, R			1	2	230			3.22E+03			826	
05/04/2014 14:45:30	8		M1	8	1	2	230	152	3.01E+10	4.82E+03	1.98E+08	0	342	
05/04/2014 18:01:15	20		M3a	20	1	2	101.4	339	3.01E+10	7.64E+03	8.87E+07	2	737	1pe
05/04/2014 18:03:47	20a	R			1	2	101.4			7.64E+03			737	1pe
05/04/2014 18:05:47	20b	PC, R			1	2	101.4			7.64E+03			728	
05/04/2014 18:10:47	21		M2_R	21	1	2	101.4	335	3.01E+10	1.05E+04	8.98E+07	30	1694	
05/04/2014 18:17:47	21a	R			1	2	101.4			1.05E+04			781	
05/04/2014 18:20:21	21b	PC, R			1	2	101.4			1.05E+04			776	
05/04/2014 18:24:31	22		M1	22	1	2	101.4	298	2.67E+10	1.30E+04	8.97E+07	0	400	
		BG			1	2	101.4			1.30E+04		0		

Tab. 3: Run table of DUT M46, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
05/04/2014 13:54:05	3			3	1	3	230	151	3.00E+10	1.60E+03	1.99E+08	1	662	1pe
05/04/2014 13:57:13	3a	R, PC			1	3	230			1.60E+03			649	
05/04/2014 14:54:26	9		M2_R	9	1	3	230	152	3.01E+10	3.21E+03	1.98E+08	1	612	
05/04/2014 14:58:06	9a	R			1	3	230			3.21E+03			672	
05/04/2014 15:00:08	9b	PC, R			1	3	230			3.21E+03			672	
05/04/2014 15:03:11	10		M1	10	1	3	230	152	3.01E+10	4.82E+03	1.98E+08	0	239	
05/04/2014 19:25:10	23		M3a	23	1	3	101.4	339	3.01E+10	7.63E+03	8.87E+07	0	618	1pe
05/04/2014 19:27:13	23a	R			1	3	101.4			7.63E+03			612	1pe
05/04/2014 19:28:59	23b	PC, R			1	3	101.4			7.63E+03			603	
05/04/2014 19:32:56	24		M2_R	24	1	3	101.4	329	3.01E+10	1.04E+04	9.14E+07	0	1406	
05/04/2014 19:40:01	24a	R			1	3	101.4			1.04E+04			774	
05/04/2014 19:41:49	24b	PC, R			1	3	101.4			1.04E+04				
05/04/2014 19:55:45	24c	R			1	3	101.4			1.04E+04			680	
05/04/2014 20:00:09	25		M1	25	1	3	101.4	340	3.00E+10	1.33E+04	8.83E+07	0	444	1be
05/04/2014 20:07:52	25a	R			1	3	101.4			1.33E+04				
		BG			1	3	101.4			1.33E+04		0		

Tab. 4: Run table of DUT M47, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
05/04/2014 14:11:41	4			4	1	4	230	152	3.01E+10	1.61E+03	1.98E+08	7	659	1pe
05/04/2014 14:14:02	4a	R, PC			1	4	230			1.61E+03			642	
05/04/2014 15:10:10	11		M2_R	11	1	4	230	152	3.01E+10	3.21E+03	1.98E+08	9	552	1ce

05/04/2014 15:14:15	11a	R			1	4	230			3.21E+03			611	1ce
05/04/2014 15:16:07	11b	PC, R			1	4	230			3.21E+03			606	
05/04/2014 15:20:52	12		M1	12	1	4	230	153	3.00E+10	4.81E+03	1.96E+08	7	191	

Tab. 5: Run table of DUT M48, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 08:02:40	30		M3a	30, 31	2	2	49.64	229	3.03E+10	4.81E+03	1.32E+08	0	894	
06/04/2014 08:06:54	30a	R			2	2	49.64			4.81E+03			871	
06/04/2014 09:00:59	34		M3a	35	2	2	32.88	334	3.01E+10	1.18E+04	9.01E+07	0	850	
06/04/2014 10:13:15	40		M3a	41	2	2	32.88	111	1.01E+10	1.40E+04	9.07E+07		289	

Tab. 6: Run table of DUT M49, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 08:15:52	31		M3a	32	2	3	49.64	237	3.01E+10	4.77E+03	1.27E+08	2	859	1pe
06/04/2014 08:17:50	31a	R			2	3	49.64			4.77E+03			859	1pe
06/04/2014 08:19:36	31b	PC, R			2	3	49.64			4.77E+03			859	
06/04/2014 09:11:53	35		M3a	36	2	3	32.88	332	3.00E+10	1.17E+04	9.04E+07	6	949	
06/04/2014 09:14:42	35a	PC, R			2	3	32.88			1.17E+04			921	
			M3a		2	3	32.88			1.17E+04		7		

06/04/2014 10:18:11	40a	R			2	3	32.88			1.17E+04		7		
06/04/2014 10:19:59	40b	R			2	3	32.88			1.17E+04		7		
06/04/2014 10:21:52	40c	PC, R			2	3	32.88			1.17E+04		7		
		BG			2	3	32.88			1.17E+04		4		
06/04/2014 10:27:37	40d	R			2	3	32.88			1.17E+04		4		
		PC, R			2	3	32.88			1.17E+04		4		
		BG			2	3	32.88			1.17E+04		4		
06/04/2014 10:29:39	40e	BG inv.			2	3	32.88			1.17E+04		5		
				42	2	3	32.88	5	0.00E+00	1.17E+04	0.00E+00			
06/04/2014 10:46:18	41		M3a mit inv	43	2	3	32.88	111	1.01E+10	1.39E+04	9.07E+07			
06/04/2014 10:48:43	42	Read mit No			2	3	32.88			1.39E+04			268	1ce
06/04/2014 10:51:12	42a	R inv.			2	3	32.88			1.39E+04			257	1ce
06/04/2014 10:52:54	42b	PC, R inv.			2	3	32.88			1.39E+04			257	

Tab. 7: Run table of DUT M50, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 11:14:45	43		M3a	44	3	2	32.88	111	1.01E+10	2.37E+03	9.09E+07	0	277	
06/04/2014 12:39:36	46a	R			3	2	32.88			2.37E+03			275	
06/04/2014 15:45:20	63a	R			3	2	32.88			2.37E+03			270	
07/04/2014 00:39:42	83e	R			3	2	32.88			2.37E+03			264	

Tab. 8: Run table of DUT M51, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 11:20:53	44		M3a	45	3	3	32.88	110	1.00E+10	2.36E+03	9.13E+07	0	257	
06/04/2014 12:41:20	46b	R			3	3	32.88			2.36E+03			246	
06/04/2014 15:47:56	63b	R			3	3	32.88			2.36E+03			242	
07/04/2014 00:41:30	83f	R			3	3	32.88			2.36E+03			239	

Tab. 9: Run table of DUT M52, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 13:07:07	47		M3a	48	4	2	21.37	15	9.68E+08	2.97E+02	6.46E+07	0	22	
06/04/2014 13:14:01	48		M3a	49	4	2	32.88	110	1.01E+10	2.70E+03	9.15E+07	0	192	
06/04/2014 13:44:11	52		M3a	53	4	2	21.37	155	1.00E+10	5.72E+03	6.46E+07	0	221	
06/04/2014 14:21:37	56		M3a	57	4	2	13.28	302	1.00E+10	1.02E+04	3.31E+07	0	359	
06/04/2014 14:53:41	59a	R			4	2	13.28			1.02E+04			335	
06/04/2014 15:05:39	60		M3a	61	4	2	32.88	110	1.00E+10	1.24E+04	9.09E+07	0	249	

Tab. 10: Run table of DUT M53, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 13:21:44	49		M3a	50	4	3	32.88	110	1.01E+10	2.40E+03	9.13E+07	0	216	
06/04/2014 13:51:02	53		M3a	54	4	3	21.37	155	1.00E+10	5.42E+03	6.46E+07	0	196	
06/04/2014 14:30:58	57		M3a	58	4	3	13.28	304	1.00E+10	9.87E+03	3.30E+07	0	480	

06/04/2014 14:55:30	59b	R			4	3	13.28			9.87E+03			460	
06/04/2014 15:12:32	61		M3a	62	4	3	32.88	110	1.01E+10	1.21E+04	9.16E+07	0	250	

Tab. 11: Run table of DUT M54, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 16:14:21	64		M3a	65	5	2	13.28	303	1.00E+10	5.53E+03	3.30E+07	0	477	
06/04/2014 16:55:15	67a	R			5	2	13.28			5.53E+03			440	
06/04/2014 17:08:17	68		M3a	70	5	2	21.37	155	1.01E+10	8.78E+03	6.49E+07	0	285	
06/04/2014 17:36:34	71a	R			5	2	21.37			8.78E+03			267	
06/04/2014 18:32:47	71e	R			5	2	21.37			8.78E+03			267	
06/04/2014 18:44:10	72		M3a	74	5	2	32.88	111	1.01E+10	1.11E+04	9.07E+07	0	303	
06/04/2014 19:46:43	75a	R			5	2	32.88						291	

Tab. 12: Run table of DUT M55, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 16:23:41	65		M3a	66	5	3	13.28	303	1.00E+10	5.54E+03	3.31E+07	0	358	
06/04/2014 16:57:29	67b	R			5	3	13.28			5.54E+03			329	
06/04/2014 17:15:09	69		M3a	71	5	3	21.37	155	1.01E+10	8.79E+03	6.48E+07	0	208	
06/04/2014 17:38:19	71b	R			5	3	21.37			8.79E+03			198	
06/04/2014 18:34:28	71f	R			5	3	21.37			8.79E+03			195	
06/04/2014 18:50:13	73		M3a	75	5	3	32.88	111	1.01E+10	1.12E+04	9.07E+07	0	237	
06/04/2014 19:48:41	75b	R			5	3	32.88			1.12E+04			219	

Tab. 13: Run table of DUT M56, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 20:30:37	76		M3a	82	6	2	13.28	1504	1.00E+10	5.53E+03	6.65E+06	0	485	
06/04/2014 22:05:42	79a	R			6	2	13.28			5.53E+03			455	
06/04/2014 22:50:13	80		M3a	89	6	2	21.37	1409	1.00E+10	8.76E+03	7.10E+06	0	260	
07/04/2014 00:18:34	83a	R			6	2	21.37			8.76E+03			248	

Tab. 14: Run table of DUT M57, Micron 16 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 21:00:58	77		M3a	83	6	3	13.28	1511	1.00E+10	5.53E+03	6.62E+06	0	474	
06/04/2014 22:07:49	79b	R			6	3	13.28			5.53E+03			436	
06/04/2014 23:18:37	81		M3a	90	6	3	21.37	1409	1.00E+10	8.76E+03	7.10E+06	0	247	
07/04/2014 00:20:20	83b	R			6	3	21.37			8.76E+03			236	

Tab. 15: Run table of DUT M58, Micron 16 Gbit NAND-Flash

7.2 Micron 32 Gbit

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
05/04/2014 15:31:14	13		M3a	13	1	5	230	152	3.01E+10	1.61E+03	1.98E+08	1	606	
			M2_R		1	5	230			1.61E+03				
		PC			1	5	230			1.61E+03				
05/04/2014 20:20:51	26		M3a	26	1	5	101.4	336	3.00E+10	4.42E+03	8.93E+07		400	1pe
05/04/2014 20:22:48	26a	R			1	5	101.4			4.42E+03			390	1pe
05/04/2014 20:24:28	26b	PC, R			1	5	101.4			4.42E+03			388	
05/04/2014 20:52:33	29		M1	29	1	5	101.4	334	3.00E+10	7.22E+03	8.99E+07	0		
		BG			1	5	101.4			7.22E+03				
		BG			1	5	101.4			7.22E+03		0		
					1	5	101.4			7.22E+03				
					1	5	101.4			7.22E+03				
					1	5	101.4			7.22E+03				

Tab. 16: Run table of DUT M76, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
05/04/2014 15:43:31	14		M3a	14	1	6	230	153	3.02E+10	1.61E+03	1.97E+08	0	545	1pe
	14a	PC, R			1	6	230			1.61E+03			546	
05/04/2014 15:51:24	15		M2_R	15	1	6	230	152	3.01E+10	3.22E+03	1.98E+08	0	481	
05/04/2014 15:55:43	15a	R			1	6	230			3.22E+03			578	
05/04/2014 16:00:32	16		M1	16	1	6	230	151	3.01E+10	4.82E+03	1.99E+08	6		1pe
					1	6	230			4.82E+03		0		
05/04/2014 20:36:18	27		M3a	27	1	6	101.4	334	3.00E+10	7.63E+03	8.98E+07	0	411	

05/04/2014 20:42:04	28		M1	28	1	6	101.4	334	3.00E+10	1.04E+04	8.99E+07	0	246	

Tab. 17: Run table of DUT M77, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
			M3a PC		1	7	230			0				
			M3a		1	7	230			0		106		
					1	7	230			0		3		
05/04/2014 16:46:57	17		M3a	17	1	7	230	153	3.01E+10	1.61E+03	1.97E+08	3	545	
05/04/2014 16:53:04	18		M2_R	18	1	7	230	156	3.02E+10	3.22E+03	1.94E+08	2	564	1pe
05/04/2014 16:57:31	18a	R			1	7	230			3.22E+03			586	1pe
05/04/2014 16:59:28	18b	PC, R			1	7	230			3.22E+03		33358	588	1ce
05/04/2014 17:01:31	18c	PC, R			1	7	230			3.22E+03		33353	583	1ce
05/04/2014 17:22:06	19		M1	19	1	7	230	155	3.00E+10	4.82E+03	1.94E+08	1	117	2ce
					1	7	230			4.82E+03				

Tab. 18: Run table of DUT M78, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 08:28:45	32		M3a	33	2	5	49.64	240	3.01E+10	4.78E+03	1.25E+08		627	
06/04/2014 08:30:57	32a	R			2	5	49.64			4.78E+03			624	
06/04/2014 09:25:36	36		M3a	37	2	5	32.88	334	3.01E+10	1.17E+04	9.00E+07	0	667	1pe
06/04/2014 09:27:32	36a	R			2	5	32.88			1.17E+04			657	1pe
06/04/2014 09:29:21	36b	PC, R			2	5	32.88			1.17E+04			650	

06/04/2014 10:00:03	38		M3a	39	2	5	32.88	111	1.00E+10	1.39E+04	9.03E+07	0	205	

Tab. 19: Run table of DUT M79, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 08:39:50	33		M3a	34	2	6	49.64	249	3.01E+10	4.78E+03	1.21E+08	0	727	1ce
06/04/2014 08:42:46	33a	R			2	6	49.64			4.78E+03			717	1ce
06/04/2014 08:45:04	33b	PC, R			2	6	49.64			4.78E+03			719	
06/04/2014 09:40:28	37		M3a	38	2	6	32.88	334	3.01E+10	1.17E+04	9.00E+07	0	684	
06/04/2014 10:07:01	39		M3a	40	2	6	32.88	111	1.00E+10	1.39E+04	9.04E+07		238	

Tab. 20: Run table of DUT M80, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 11:27:16	45		M3a	46	3	5	32.88	111	1.00E+10	2.36E+03	9.04E+07	0	154	
06/04/2014 12:43:08	46c	R			3	5	32.88			2.36E+03			140	
06/04/2014 15:49:41	63c	R			3	5	32.88			2.36E+03			144	
07/04/2014 00:43:40	83g	R			3	5	21.37			2.36E+03			144	

Tab. 21: Run table of DUT M81, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI

06/04/2014 11:35:13	46		M3a	47	3	6	32.88	111	1.00E+10	2.36E+03	9.04E+07	0	129	
06/04/2014 12:44:49	46d	R			3	6	32.88			2.36E+03			122	
06/04/2014 15:51:32	63d	R			3	6	32.88			2.36E+03			126	
07/04/2014 00:45:26	83h	R			3	6	21.37			2.36E+03			126	

Tab. 22: Run table of DUT M82, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 13:28:29	50		M3a	51	4	5	32.88	111	1.01E+10	2.41E+03	9.09E+07	0	173	
06/04/2014 13:58:55	54		M3a	55	4	5	21.37	156	1.00E+10	5.44E+03	6.44E+07	0	126	
06/04/2014 14:41:16	58		M3a	59	4	5	13.28	306	1.00E+10	9.89E+03	3.28E+07	0	200	
06/04/2014 14:57:13	59c	R			4	5	13.28			9.89E+03			179	
06/04/2014 15:19:24	62		M3a	63	4	5	32.88	111	1.01E+10	1.22E+04	9.07E+07	0	179	

Tab. 23: Run table of DUT M83, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 13:35:29	51		M3a	52	4	6	32.88	111	1.01E+10	2.41E+03	9.09E+07	0	168	
06/04/2014 14:06:22	55		M3a	56	4	6	21.37	156	1.01E+10	5.44E+03	6.45E+07	0	138	
06/04/2014 14:08:14	55a	R			4	6	21.37			5.44E+03			139	
06/04/2014 14:10:02	55b	PC, R			4	6	21.37			5.44E+03			139	
06/04/2014 14:51:05	59		M3a	60	4	6	13.28	303	1.00E+10	9.89E+03	3.31E+07	0	196	

06/04/2014 14:58:55	59d	R			4	6	13.28			9.89E+03			181	
06/04/2014 15:25:55	63		M3a	64	4	6	32.88	110	1.00E+10	1.22E+04	9.12E+07	0	189	

Tab. 24: Run table of DUT M84, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
			(M3a)	67	5	5	13.28	29	9.67E+08	5.34E+02	3.33E+07	8		
06/04/2014 16:36:37	66		M3a	68		5	13.28	302	1.00E+10	6.08E+03	3.32E+07	0	200	
06/04/2014 16:59:21	67c	R			5	5	13.28			6.08E+03			178	
06/04/2014 17:22:33	70		M3a	72	5	5	21.37	155	1.00E+10	9.31E+03	6.46E+07	0	150	
06/04/2014 17:40:00	71c	R			5	5	21.37			9.31E+03			143	
06/04/2014 18:36:17	71g	R			5	5	21.37			9.31E+03			139	
06/04/2014 18:56:46	74		M3a	76	5	5	32.88	110	1.00E+10	1.17E+04	9.11E+07	0	170	
06/04/2014 19:50:26	75c	R			5	5	32.88			1.17E+04			160	

Tab. 25: Run table of DUT M85, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 16:46:39	67		M3a	69	5	6	13.28	302	1.00E+10	5.53E+03	3.32E+07		208	
06/04/2014 17:01:04	67d	R			5	6	13.28			5.53E+03			187	
06/04/2014 17:29:41	71		M3a	73	5	6	21.37	155	1.00E+10	8.77E+03	6.46E+07	0	193	
06/04/2014 17:41:46	71d	R			5	6	21.37			8.77E+03			194	
06/04/2014 18:37:58	71h	R			5	6	21.37			8.77E+03			187	
06/04/2014 19:03:34	75		M3a	77	5	6	32.88	111	1.01E+10	1.11E+04	9.07E+07	0	189	

06/04/2014 19:52:50	75d	R			5	6	32.88			1.11E+04			187	

Tab. 26: Run table of DUT M86, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 21:32:11	78		M3a	84	6	5	13.28	1509	1.00E+10	5.53E+03	6.63E+06	0	131	
06/04/2014 22:09:38	79c	R			6	5	13.28			5.53E+03			130	
06/04/2014 23:47:15	82		M3a	91	6	5	21.37	1410	1.00E+10	8.76E+03	7.10E+06	0	145	
07/04/2014 00:22:04	83c	R			6	5	21.37			8.76E+03			138	

Tab. 27: Run table of DUT M87, Micron 32 Gbit NAND-Flash

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
06/04/2014 22:02:59	79		M3a	85	6	6	13.28	1514	1.00E+10	5.53E+03	6.61E+06	0	222	
06/04/2014 22:11:27	79d	R			6	6	13.28			5.53E+03			214	
07/04/2014 00:16:05	83		M3a	92	6	6	21.37	1412	1.00E+10	8.76E+03	7.08E+06	0	143	
07/04/2014 00:24:00	83d	R			6	6	21.37			8.76E+03			138	

Tab. 28: Run table of DUT M88, Micron 32 Gbit NAND-Flash

7.3 Samsung 4x8 Gbit

Time	IDA No	Runs without irradiation *)	Mode	PIF No	DUT Set	DUT	Size	Pos	Energy	Time[s]	Fluence [p/cm2]	accumulated Dose [rad]	Flux [p/cm2/sec]	BG Verify	SEU	SEFI
05/04/2014 13:31:07	1		M3a	1	1	SA26	4x8	1	230	152	3.01E+10	1.61E+03	1.98E+08	0	2	
05/04/2014 14:18:53	5		M2_R	5	1	SA26	4x8	1	230	153	3.02E+10	3.22E+03	1.97E+08	0	8	
05/04/2014 14:23:17	5a	R			1	SA26	4x8	1	230			3.22E+03			0	
05/04/2014 14:27:00	6		M1	6	1	SA26	4x8	1	230	152	3.01E+10	4.82E+03	1.98E+08		4	

Tab. 29: Run table of DUT SA26, Samsung 4x8 Gbit NAND-Flash

8 Package pictures

Fig. 21: Samsung K9WBG08U1M-PIB0 NAND-Flash

Fig. 22: Micron MT29F16G08ABACAWP-IT:C NAND-Flash

Fig. 23: Micron MT29F32G08ABAAAWP-IT:A NAND-Flash

Fig. 24: Micron MT29F128G08AJAAAWP-ITZ:A NAND-Flash