Technische Universität
Braunschweig

INSTITUT FÜR DATENTECHNIK
UND KOMMUNIKATIONSNETZE

TN-IDA-RAD-14/14

K. Grürmann, M. Herrmann, F. Gliem

Radiation Hard Memory (RHM)

Comparison between NAND-Flash and DDR3 SDRAM Test Results

Contract number: ESTEC Contract No. 4000101358/10/NL/AF
Contract title: Radiation hard memory, Radiation testing of candidate memory devices for Laplace mission
Technical officer: V. Ferlet-Cavrois
Date of first writing: September, 22, 2014
Date of final issue: September, 22, 2014

Contents

1 Scope

This document focusses on the comparison of NAND-Flash and DDR3 SDRAM test results derived from SEE Heavy Ion (chapter 3), SEE Proton (chapter 4) and TID (chapter 5) tests.

The results are extracted from the test reports compiled in the frame of ESA Radiation Hard Memory study (chapter 8).

The comparison comprises all types of data errors like SEUs and SEFIs and to device damaging effects like Destructive Failures and SELs as a starting point for the calculation of error rates. Therefore the heavy ion test results are given as Weibull fits.

Details of (i) the test equipment, (ii) the DUT preparation, (iii) the test modes and (iv) the error classification are given individually for the DUT types and for the test campaigns in the respective test reports.

Details of the test results like (i) stuck bits (hard SEU), (ii) annealing, (iii) error polarity (iv) uncertainty margins and (v) angular dependence are device individual and therefore they are not repeated in this comparison.
Stuck bits show a strong temperature dependence. Between 1% and 10% of the SEUs of DDR3 SDRAMs are stuck bits.
Only minor annealing effects were observed.
The angular dependence was studied only for NAND-Flash.

2 Introduction

2.1 General remarks

SDRAM are designed for use in ground mass memories and are used also in space mass memories, where they compete with Single Level Cell (SLC) NAND-Flash. The usual Reed Solomon error correction (RS-ECC) is very effective against sparsely distributed Single Event Upsets (SEU), which therefore are of minor concern.

Therefore, the data integrity of SDRAM- and NAND-Flash-based space mass memories is determined mainly by radiation induced break down of the device functionality, in case of SDRAM several types of SEFI, in particular Device SEFI, and in case of NAND-Flash several types of SEFI including Device SEFI and in particular Destructive Failures (DF).

Device SEFI cause a transient or persistent blocking of the device functionality, but no physical destruction. Device SEFI can be resolved by corrective actions, sometimes by reset measures and always by power cycling.

Power cycling destroys the data contents of SDRAM, in contrast to Flash.

NAND-Flash is prone to Destructive Failure, in contrast to SDRAM. The main reason for this is the on-chip High Voltage (≈ 20 V) generation and distribution.

Both, NAND-Flash and SDRAM combine the storage array with an on-chip processor, which controls various operation sequences. The existence of the on-chip processor grants the implementation of several modes of device operation and of device communication with the memory controller.

In consequence it is not possible to achieve full test coverage over all operational mode combinations of the respective device within the given beam time restrictions. Instead, only a subset of operational conditions can be tested, which is believed to be more or less representative for future device applications.

The synchronous high data rate communication with the memory controller implies a tight coupling between the SDRAM device and its external controller. Details of the interaction between device and controller can cause significant modifications of the error image.

If, such as in this campaign, a survey of the devices on the market is intended, the test coverage necessarily is even more restricted. What the survey can deliver is an assessment of the general usability of these devices in the space radiation environment, in particular in comparison to the competing NAND-Flash.

The gained test data show that state of the art commercial DDR3 SDRAM are strong candidates for the implementation of space mass memories. The parts of the different manufacturers are fabricated according to a common JEDEC specification of their functionality to be interchangeable for ground applications. Never the less we see differences in their SEE response, which reflect differences in the chip design.

In view of any real application we do strongly recommend to test the device chosen for that application again under the exact conditions of the respective application, in particular with respect to its specific operational mode and in combination with the intended memory controller.

2.2 Specific remarks

As already mentioned the SEE performance of the SDRAM devices is mainly determined by their sensitivity to SEFI, especially to Device SEFI. Proper device operation depends on the writable contents of several on-chip control registers. Corruption of the regular contents causes severe disruptions of the device functionality, which appear in the retrieved data as SEFI. A recommended countermeasure is Software Conditioning, namely a periodic rewrite of the control registers. By comparison with test runs without S/W conditioning we proved the effectiveness also in our case.

Accordingly, we tried to get test runs with S/W conditioning over the full LET scale, because we assume that the advantage by S/W conditioning will be exploited in space applications. As expected, S/W conditioning has an only minor influence on the SEU cross section. But it provides a significant improvement of the SEFI cross sections.

Main attention was given to the 4-Gbit devices of Elpida and Samsung, and also to the 2-Gbit devices of Samsung, rev. D and Micron. Unfortunately, Elpida went out of business. Samsung is the major player. Micron is another important supplier using another chip design. Additional tests were performed for the 2-Gbit Hynix and the 2-Gbit Nanya device.

Removal of Device SEFI by power cycling destroys the stored data. Therefore, it is of interest to circumvent this “ultima ratio” by more mitigant reset measures. Respective tests were performed and show substantial differences between the investigated DUT types.

3 SEE HI

The tested devices are ordered according to their heavy ion response in both, the legends of the cross section diagrams and the Weibull parameter tables. NAND-Flash cross sections are plotted with dashed lines.

3.1 SEU

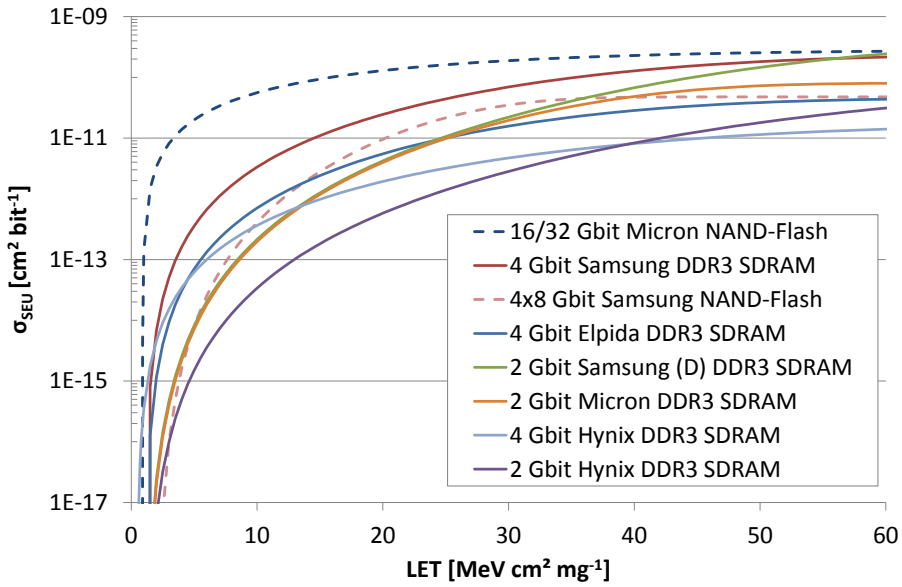

Fig. 1: SEU cross section

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 bit^{-1}]
16/32 Gbit Samsung NAND-Flash	0.891	25.31372	1.39516	2.75E-10
4 Gbit Samsung DDR3 SDRAM	1.08901	42.82953	2.71533	2.38E-10
4x8 Gbit Samsung NAND-Flash	1.98001	26.11168	4.0306	4.76E-11
4 Gbit Elpida DDR3 SDRAM	1.08901	39.29846	2.80791	4.57E-11
2 Gbit Samsung (D) DDR3 SDRAM	1.08901	59.09633	3.96459	3.88E-10
2 Gbit Micron DDR3 SDRAM	1.08901	39.73573	4.02061	8.06E-11
4 Gbit Hynix DDR3 SDRAM	0.47768	47.4727	2.38903	1.71E-11
2 Gbit Hynix DDR3 SDRAM	1.08901	65.69309	3.77954	6.43E-11

Tab. 1: SEU cross section, Weibull parameters

The 25 nm NAND-Flash cross section at low LET is about two orders of magnitude higher compared to the DDR3 SDRAM cross section and the 4x8 Gbit NAND-Flash cross section.

3.2 SEFI

3.2.1 Column SEFI

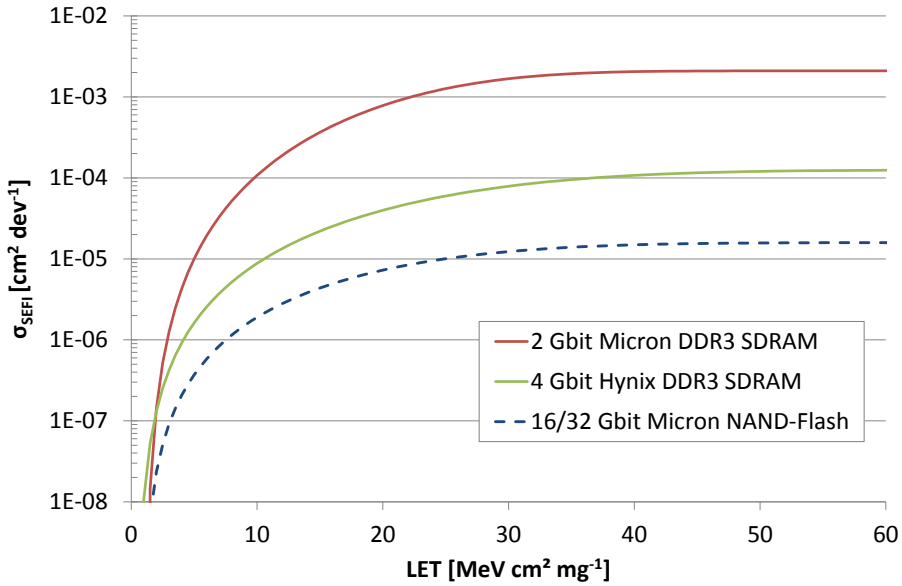

Fig. 2: Column SEFI cross section

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 dev^{-1}]
2 Gbit Micron DDR3 SDRAM	1.08901	24.57988	2.90497	2.10E-03
4 Gbit Hynix DDR3 SDRAM	0.47768	29.56913	2.31072	1.25E-04
16/32 Gbit Micron NAND-Flash	0.891	28.99148	2.82071	3.10E-04

Tab. 2: Column SEFI cross section, Weibull parameters

The column SEFI cross section of the 2 Gbit Micron DDR3 SDRAM is two orders of magnitude higher compared to the respective 16/32 Gbit NAND-Flash cross section.

3.2.2 Row SEFI

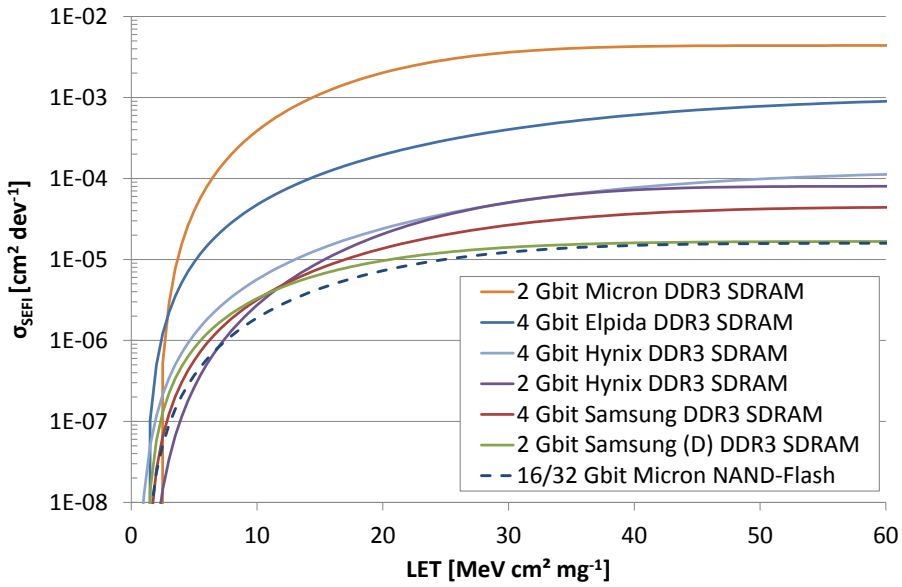

Fig. 3: Row SEFI cross section

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 dev^{-1}]
2 Gbit Micron DDR3 SDRAM	2.04188	22.07522	2.33245	4.39E-03
4 Gbit Elpida DDR3 SDRAM	1.08901	40.94838	2.00165	1.03E-03
4 Gbit Hynix DDR3 SDRAM	0.47768	40.3647	2.12692	1.25E-04
2 Gbit Hynix DDR3 SDRAM	1.08901	28.93276	2.85419	8.01E-05
4 Gbit Samsung DDR3 SDRAM	1.08901	30.37955	2.12843	4.48E-05
2 Gbit Samsung (D) DDR3 SDRAM	1.08901	20.4938	1.81476	1.67E-05
16/32 Gbit Micron NAND-Flash	0.891	24.14201	2.11722	1.59E-05

Tab. 3: Row SEFI cross section, Weibull parameters

There are big differences among the DDR3 SDRAM Row SEFI cross sections. The 2 Gbit Micron cross section is about two orders of magnitude above the favourable DDR3 parts. The 16/32 Gbit NAND-Flash cross section is similar to the favourable DDR3 SDRAM cross sections.

3.2.3 Block SEFI, Class B (NAND-Flash only)

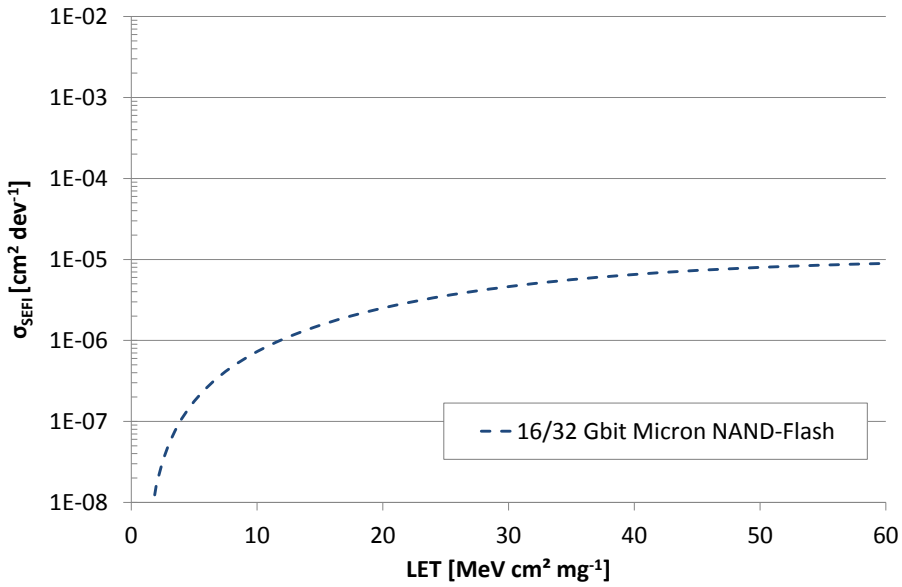

Fig. 4: Class B Block SEFI cross section

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 dev^{-1}]
16/32 Gbit Micron NAND-Flash	0.891	37.90396	1.81179	1.00E-05

Tab. 4: Class B Block SEFI cross section, Weibull parameters

3.2.4 Block SEFI, Class C (NAND-Flash only)

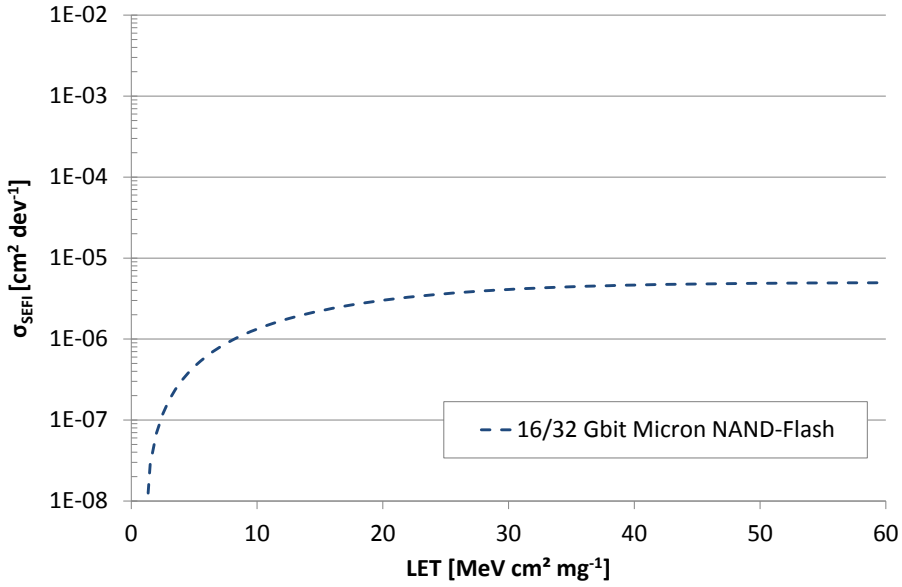

Fig. 5: Class C Block SEFI cross section

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 dev^{-1}]
16/32 Gbit Micron NAND-Flash	0.891	20.19565	1.4752	5.00E-06

Tab. 5: Class C Block SEFI cross section, Weibull parameters

3.2.5 All SEFI (NAND-Flash only)

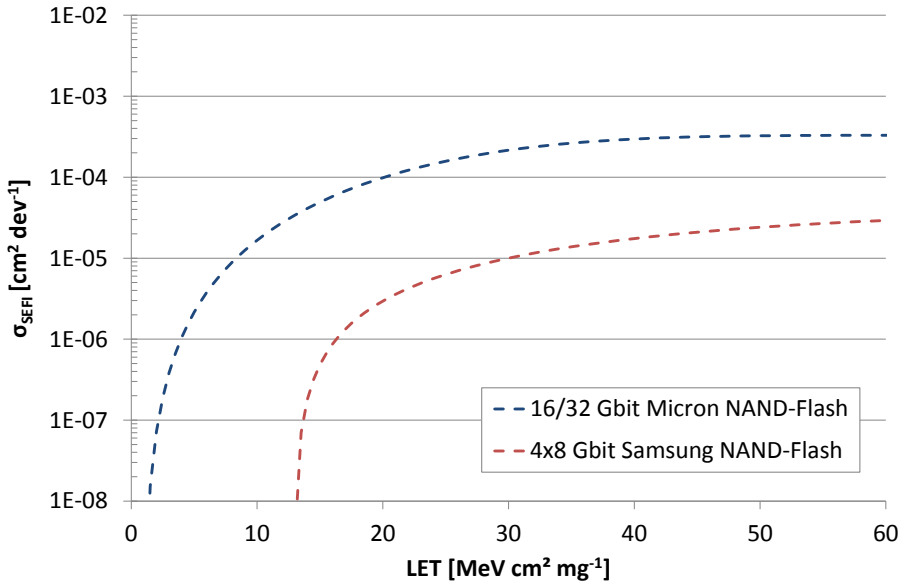

Fig. 6: All SEFI cross section

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 dev^{-1}]
16/32 Gbit Micron NAND-Flash	0.891	28.46587	2.59854	3.30E-04
4x8 Gbit Samsung NAND-Flash	12.93	39.17	1.5	4.0E-5

Tab. 6: All SEFI cross section, Weibull parameters

3.2.6 Device SEFI without software conditioning (DDR3 SDRAM only)

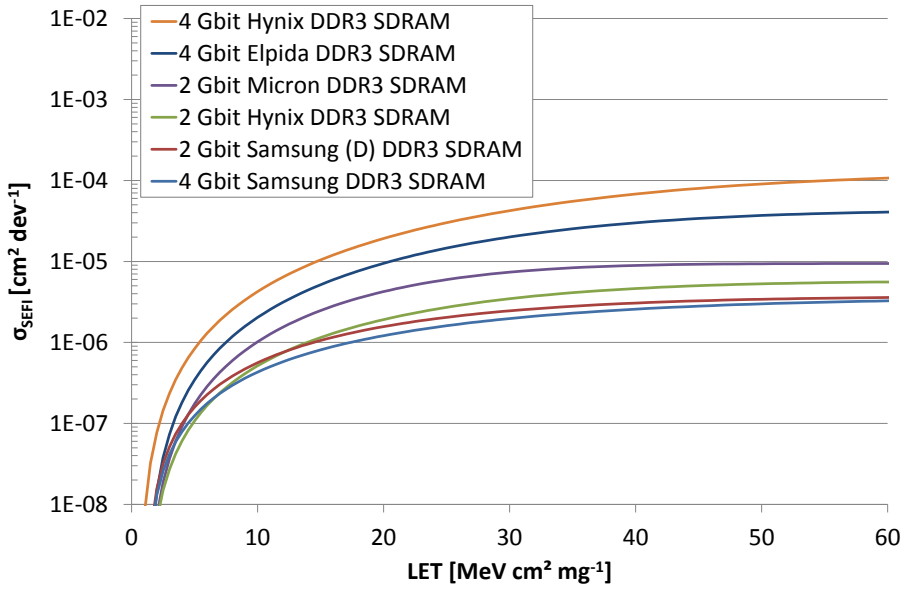

Fig. 7: Device SEFI without software conditioning (DDR3 SDRAM only)

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 dev^{-1}]
4 Gbit Hynix DDR3 SDRAM	0.47768	44.13651	2.19475	1.25E-04
4 Gbit Elpida DDR3 SDRAM	1.08901	35.75128	2.17616	4.29E-05
2 Gbit Micron DDR3 SDRAM	1.08901	23.91031	2.19817	9.44E-06
2 Gbit Hynix DDR3 SDRAM	1.08901	29.98794	1.94599	5.72E-06
2 Gbit Samsung (D) DDR3 SDRAM	1.08901	27.4693	1.6044	3.71E-06
4 Gbit Samsung DDR3 SDRAM	1.08901	33.24872	1.55915	3.57E-06

Tab. 7: Device SEFI without software conditioning, Weibull parameters

3.2.7 Device SEFI with software conditioning (DDR3 SDRAM only)

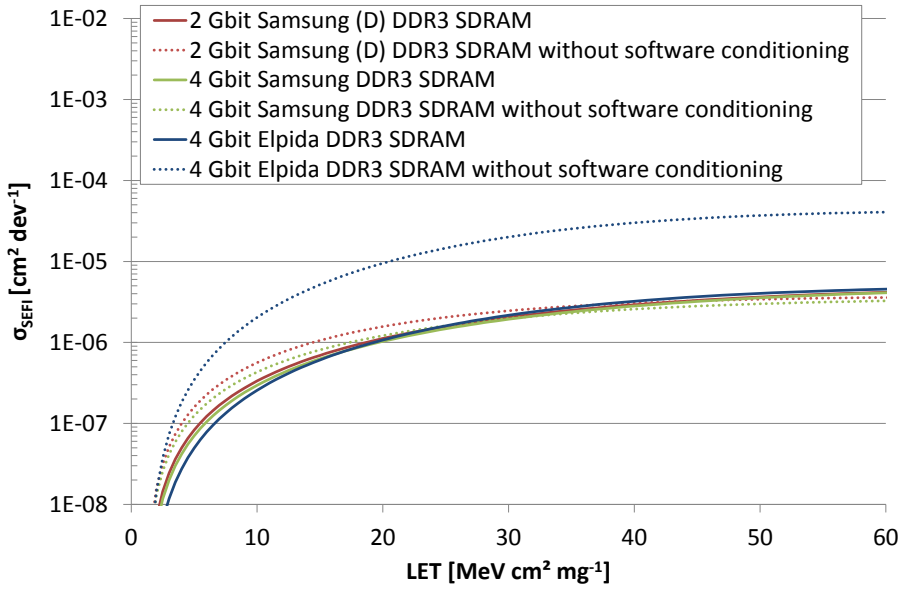

Fig. 8: Device SEFI with software conditioning (DDR3 SDRAM only)

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 dev^{-1}]
2 Gbit Samsung (D) DDR3 SDRAM	1.08901	41.93824	1.72404	4.99E-06
4 Gbit Samsung DDR3 SDRAM	1.08901	43.25729	1.77031	4.99E-06
4 Gbit Elpida DDR3 SDRAM	1.08901	38.28862	2.01972	5.00E-06

Tab. 8: Device SEFI with software conditioning, Weibull parameters

The effectiveness of software conditioning depends on the manufacturer.

3.3 Destructive Failure (NAND-Flash only)

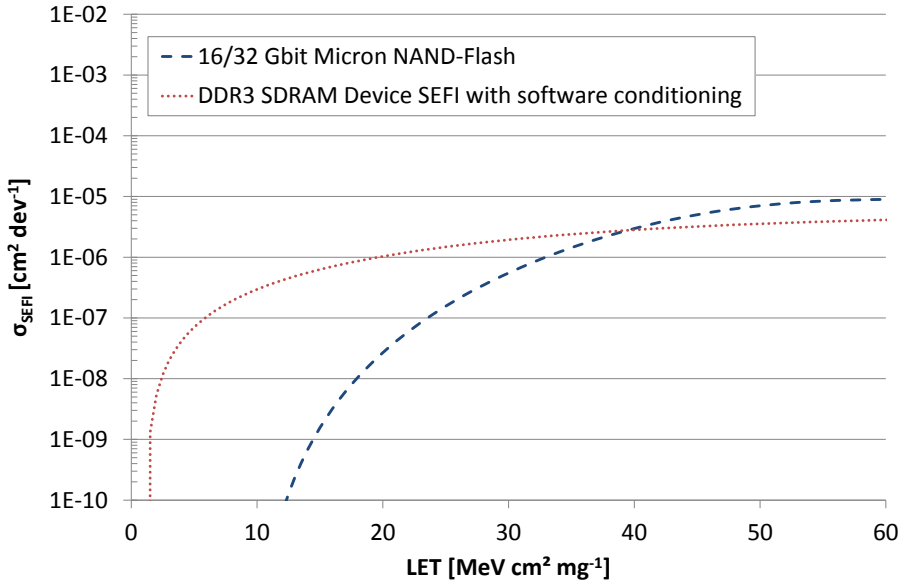

Fig. 9: Destructive Failure cross section

Device	LET_{th} [MeV cm^2 mg^{-1}]	W [MeV cm^2 mg^{-1}]	s	σ_{sat} [cm^2 dev^{-1}]
16/32 Gbit Micron NAND-Flash	8.91	37.82186	4.74968	9.11E-06

Tab. 9: Destructive Failure cross section, Weibull parameters

The NAND-Flash Destructive Failure is permanent damage with definite data loss.

3.4 SEL

Neither NAND-Flash nor DDR3 SDRAM suffered from SEL.

4 SEE Proton

4.1 SEU

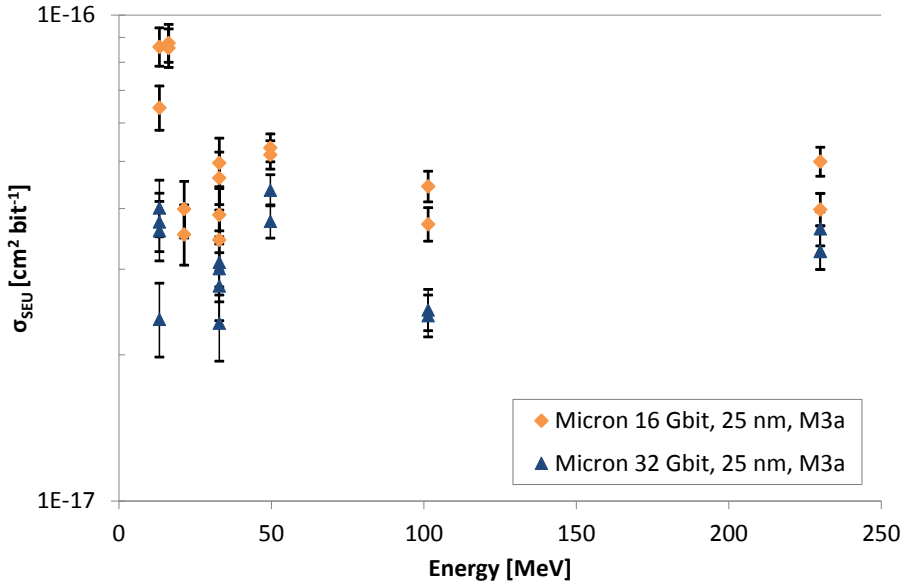

Fig. 10: Micron 25 nm NAND-Flash SEU cross section

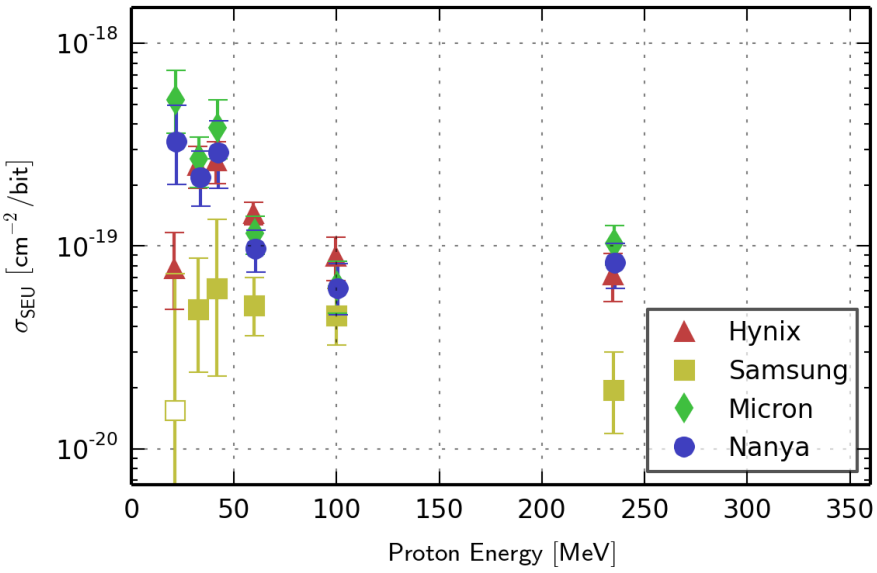

Fig. 11: DDR3 SDRAM SEU cross sections

25 nm NAND-Flash is by the factor of 400 more sensitive to proton SEUs than DDR3 SDRAM (feature size ≈ 35 nm). NAND-Flash and DDR3 SDRAM show an increase of SEUs towards low energies. This should be investigated further to exclude peculiarities of the source.

4.2 SEFI

In most cases the SEFI count is very low. To get more SEFI events the fluence a higher fluence is needed, which is hard to realize because of the limited beam time and in case of NAND-Flash because of the limited total dose.

4.2.1 Column SEFI

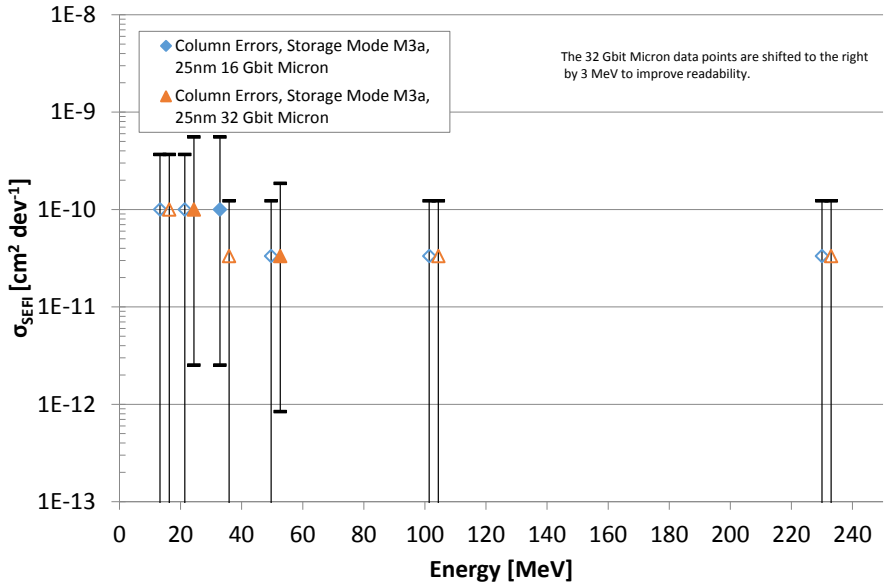

Fig. 12: Micron 25 nm NAND-Flash Column SEFI cross section

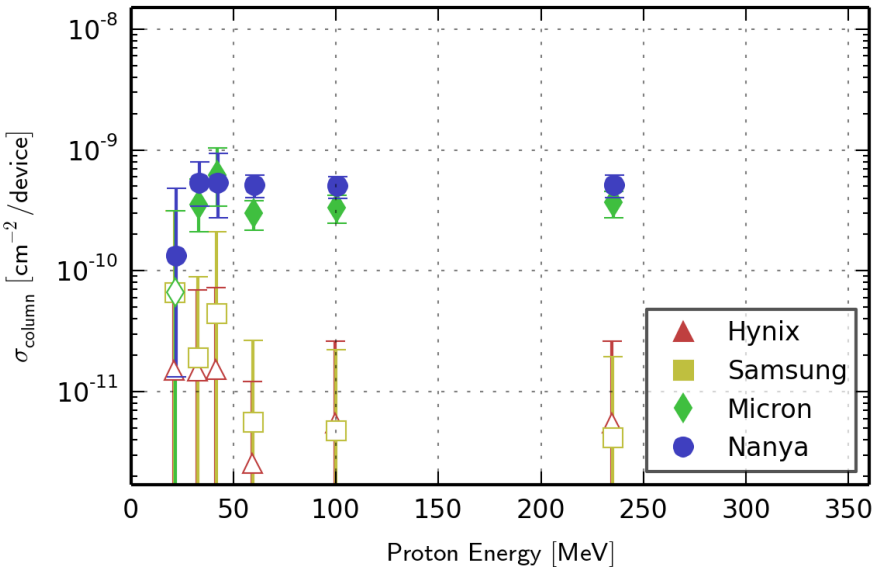

Fig. 13: DDR3 SDRAM Column SEFI cross sections

4.2.2 Row SEFI

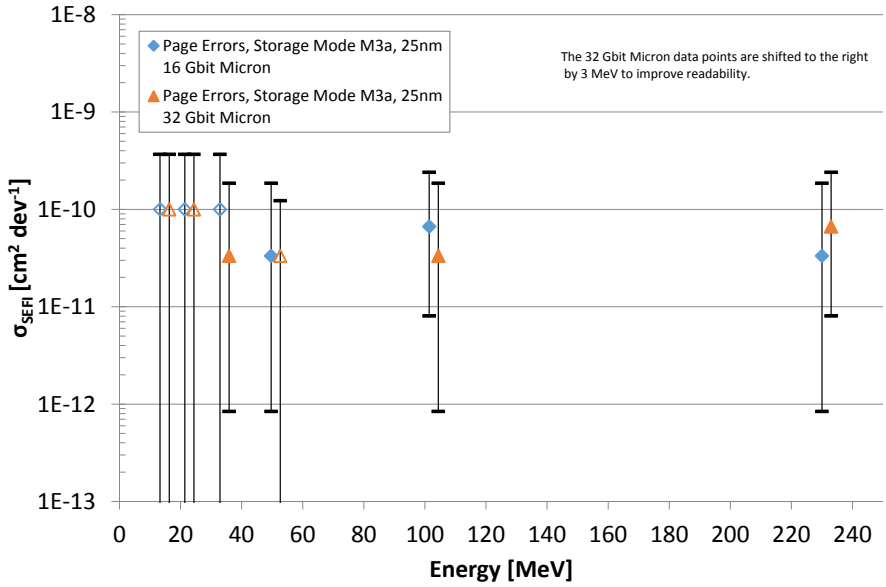

Fig. 14 Micron 25 nm NAND-Flash Row SEFI cross section

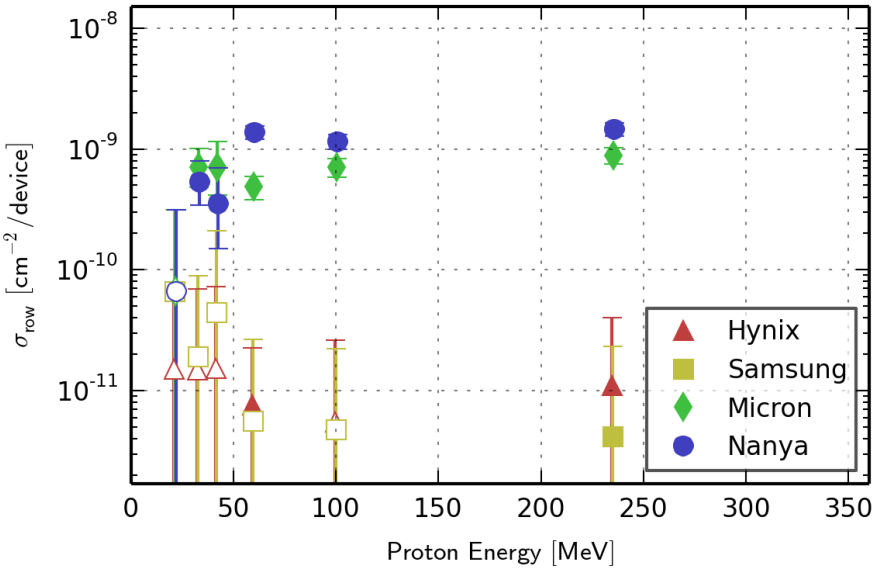

Fig. 15: DDR3 SDRAM Row SEFI cross sections

4.2.3 Block SEFI (NAND-Flash only)

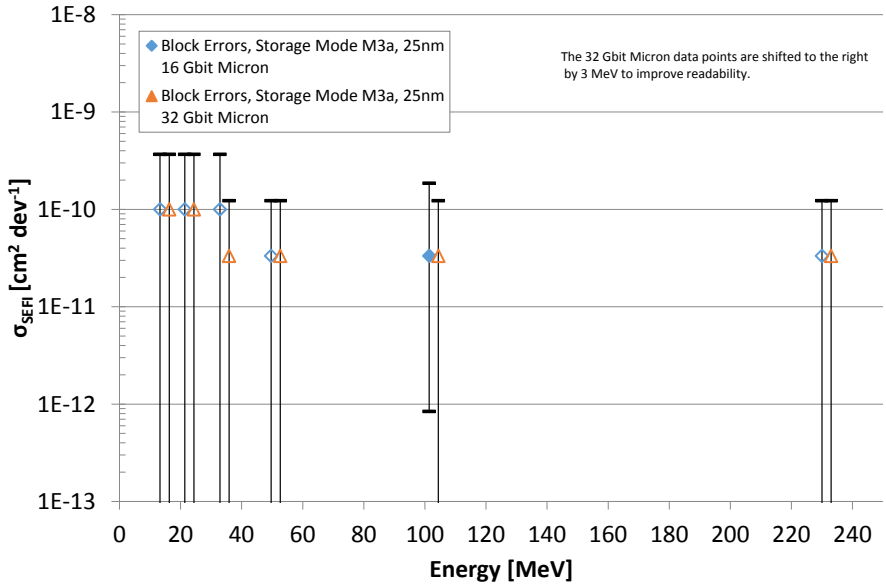

Fig. 16: Micron 25 nm NAND-Flash Block SEFI cross section

4.2.4 Device SEFI (DDR3 SDRAM only)

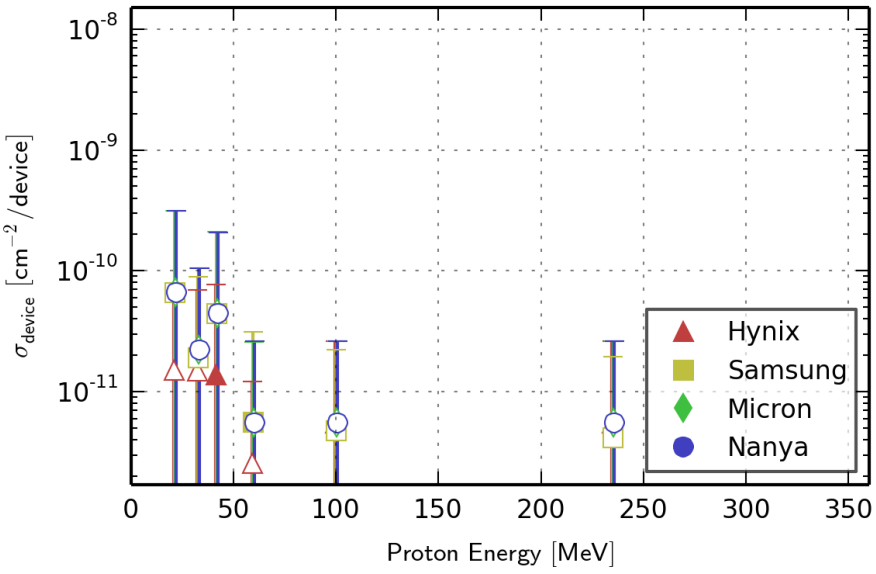

Fig. 17: DDR3 SDRAM Device SEFI cross sections

4.3 Destructive Failure, SEL

Neither NAND-Flash nor DDR3 SDRAM suffered from permanent damaging effects like Destructive Failure or SEL.

5 TID

5.1 16/32 Gbit NAND-Flash

In the error share diagrams the functional breakdown of each DUT is marked with dotted line. The chronology of DUT breakdowns is reflected in the order of the diagram legend.

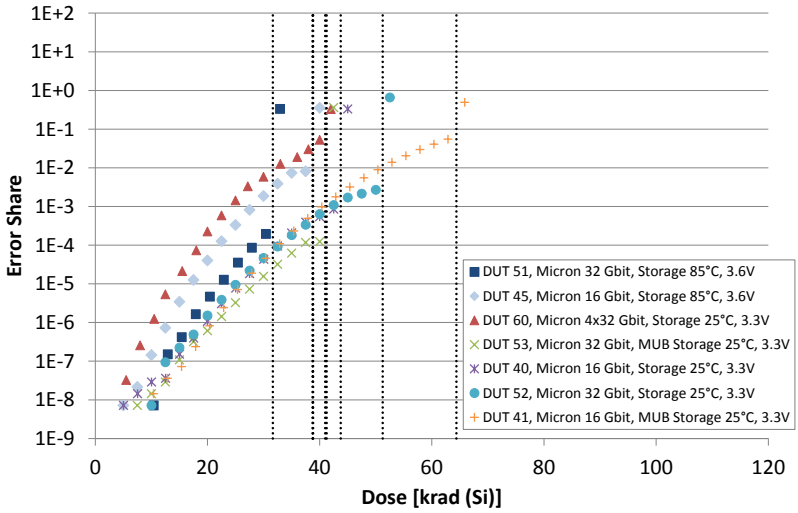

Fig. 18: Error share versus dose of DUTs in Storage Mode, 16/32 Gbit NAND-Flash

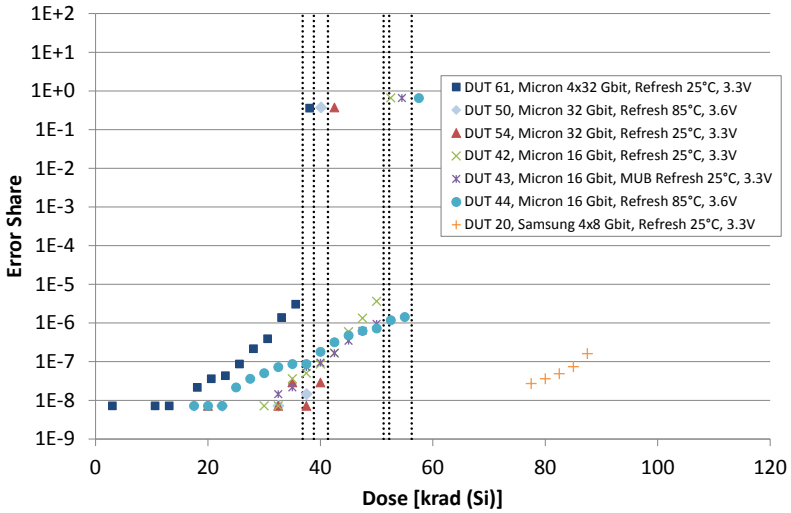

Fig. 19: Error share versus dose of DUTs in Refresh Mode, 16/32 Gbit NAND-Flash

The periodic refresh keeps the error share below $1 \cdot 10^{-5}$ which is tolerable before ECC. Therefore with periodic refresh the Device Failure occurrence determines the total dose.

5.2 4 Gbit Samsung DDR3 SDRAM

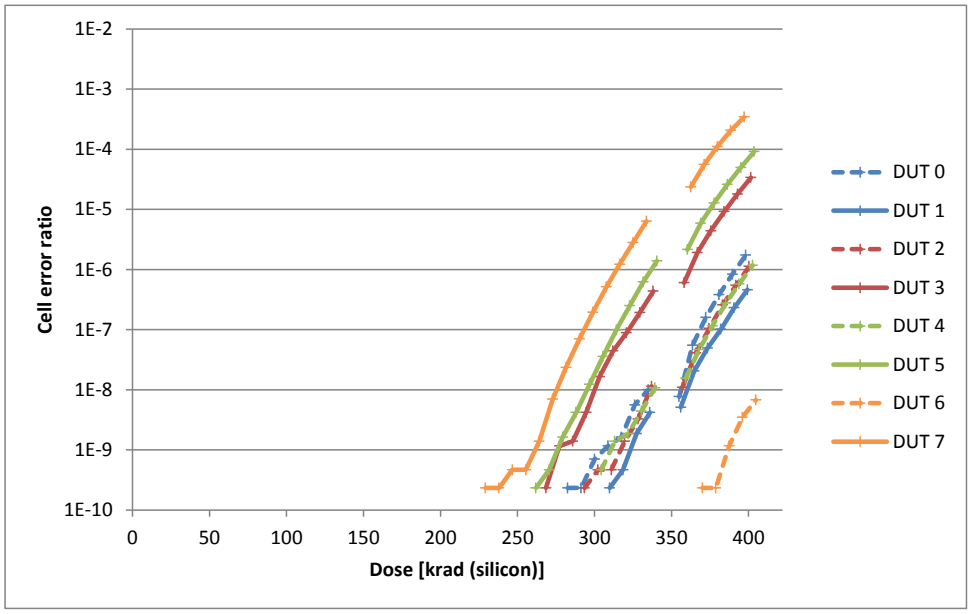

Fig. 20: Error share versus dose, 4 Gbit Samsung DDR3 SDRAM

Tolerating an error share of 1E-5 before ECC, the Samsung DDR3 SDRAM device can be used up to 350 krad(Si).

5.3 4 Gbit Micron DDR3 SDRAM

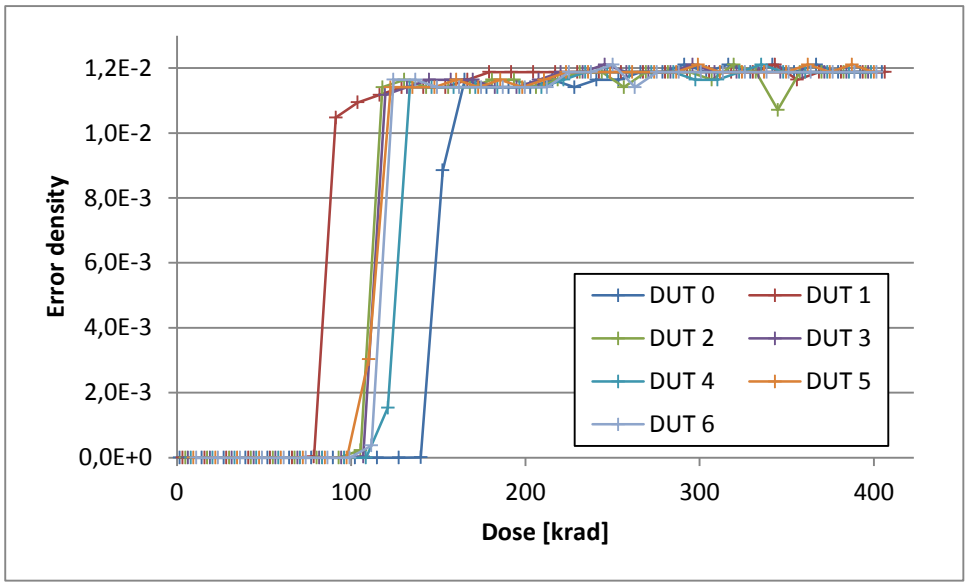

Fig. 21: Error share versus dose, 4 Gbit Micron DDR3 SDRAM

The steep error increase is presumably caused by the current increase (Fig. 22) resulting in a voltage drop by more than the specified 0.075 V.

5.4 4 Gbit Hynix DDR3 SDRAM

The 4 Gbit Hynix DUTs showed no errors up to 423 krad (Si).

5.5 DDR3 SDRAM current measurement

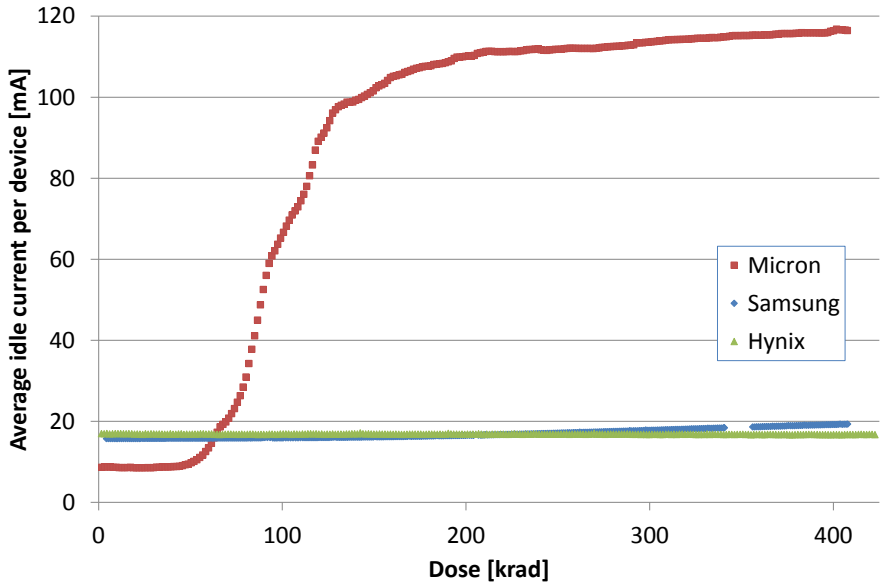

Fig. 22: DDR3 SDRAM average idle current per device

5.6 Conclusion

The TID response of all tested DDR3 SDRAMs is much better than the NAND-Flash TID response.

6 Conclusion

6.1 SEE HI

Regarding SEU DDR3 SDRAM are less sensitive than latest SLC NAND Flash devices. Nevertheless, DDR3 SDRAM devices are very sensitive to SEFI. Due to their volatility of stored data, special measures have to be taken for mitigation. In contrary, tested SLC NAND Flash devices showed a much better SEFI behaviour. Furthermore, SEFI can be easily mitigated by power cycling of the devices without data loss.

None of the tested devices exhibit Single Event Latch-up, even at elevated temperatures at LET $\geq$ 60 MeV cm^2 mg^{-1}. But, NAND Flash devices are sensitive to DF in the high voltage circuitry. Compared to heritage SLC NAND Flash devices i.e., Samsung 8 Gbit, the onset LET is reduced from about 30 MeV cm^2 mg^{-1} to about 10…15 MeV cm^2 mg^{-1}. However, the predicted rates are still low enough to use these devices in space. These errors can be mitigated by advanced EDAC designs, i.e. Reed Solomon codes such as for DDR3 SDRAM.

6.2 SEE Proton

Regarding NAND-Flash scaling from about 50 nm down to 25 nm leads to (i) an increased SEU cross section by about three orders of magnitude and (ii) a constant or increasing SEU cross section down to the lowest energy of 13.3 MeV (Fig. 10). To exclude to be an artefact of the source, this effect should be investigated in more detail with the focus on energies below 10 MeV. It might be even worse for 20 nm SLC NAND-Flash parts which are already in mass production.

The DDR3 SDRAM devices show an increasing SEU cross section at low energies, too (Fig. 11).

No destructive events occurred at protons irradiations.

6.3 TID

With respect to the envisaged JUICE (Laplace) mission, the TID sensitivity is the main driver for part selection. For mission to Jovian system TID levels of more than 300krad inside equipments are expected.

For NAND-Flash neither the error onset nor the Device Failure can be influenced by the operating conditions like test mode, supply voltage or DUT temperature. Only the steep error increase (Fig. 18) can be suppressed by periodic refresh of the stored data at least every 2.5 krad (Fig. 19).

From the TID point of view the 25 nm Micron NAND-Flash generation is suitable for applications up to a total dose of 25 krad using a suitable error correction scheme and using a peri-

odic refresh. The periodic refresh keeps the error share below $1 \cdot 10^{-5}$ which is tolerable before ECC. Therefore with periodic refresh the Device Failure occurrence determines the total dose.

The latest SLC NAND Flash devices show functional loss already at 32 krad(Si) in worst case in contrast to heritage parts with TID sensitivities > 90 krad(Si). They won't be feasible for the use in JUICE mission without exhaustive shielding. Nevertheless, they are still good candidates for applications in LEO missions.

3 state of the art DDR3 SDRAM devices have been tested regarding their TID sensitivities. Two very promising candidates could be found usable up to 350 - 400 krad(Si) accumulated dose.

7 Ranking

Tab. 10 shows a comparison of the tested devices ordered by their sensitivity to the respective effect.

	Part type	HI SEU	HI Row SEFI	HI Column SEFI	HI Device SEFI	Proton SEU	Proton Row SEFI	Proton Column SEFI	Proton Device SEFI	TID
NAND-Flash	16/32 Gbit Micron	7	2	3	N/A	3	Not enough data			5
	4x8 Gbit Samsung	6	1	1	N/A	Not tested	Not enough data			4
DDR3 SDRAM	4-Gbit Elpida	4	7	2	2	Not tested				Not tested
	4-Gbit Samsung	5	4	2	1	1	1	1	1	2
	4 Gbit Hynix	**2**	**6**	**4**	**3**	**2**	**2**	**1**	**2**	**1**
	4-Gbit Micron	Not tested				2	3	2	1	3
	4-Gbit Nanya	Not tested				2	3	2	1	Not tested
	2-Gbit Samsung (B)	Not enough data				Not tested				Not tested
	2-Gbit Samsung (D)	3	3	2	1	Not tested				Not tested
	2-Gbit Hynix	1	5	2	1	Not tested				Not tested
	2-Gbit Micron	2	7	4	2	Not tested				Not tested
	2-Gbit Nanya	Not enough data				Not tested				Not tested

Tab. 10: Ranking of DDR3 SDRAM devices

8 Appendix

			Test Plan		Test Report	
Type	**Facility**	**Date**	**NAND-Flash**	**DDR3 SDRAM**	**NAND-Flash**	**DDR3 SDRAM**
SEE HI	RADEF	May 23 – 27 2011	TN-IDA-RAD-11/3 May 16, 2011		TN-IDA-RAD-11/5B May, 24, 2013	
		January 9 – 13 2012	TN-IDA-RAD-11/8E Jan. 07, 2012		TN-IDA-RAD-12/12 May, 29, 2013	TN-IDA-RAD-12/13 August 14, 2014
		April 16 – 20 2012	TN-IDA-RAD-12/6 April 14, 2012			
	TAMU	December 4 – 7 2012	TN-IDA-RAD-12/14 Nov 30, 2012		TN-IDA-RAD-13/2B May, 24, 2013	TN-IDA-RAD-13/1A March 5, 2013
TID in-situ	ESTEC	October 22 – 26 2012	-	TN-IDA-RAD-12/15 June 20, 2012	-	TN-IDA-RAD-13/4 April 30, 2013
TID unbiased		March 11 – 18 2013	-	-	-	TN-IDA-RAD-13/9B June 7, 2013
TID unbiased		October 18 – 22 2013	-	-	-	TN-IDA-RAD-13/12 November 2, 2013
TID in-situ		January 17 – 23 2014	TN-IDA-RAD-14/2 January, 15, 2014		TN-IDA-RAD-14/4 September, 9, 2014	TN-IDA-RAD-14/3 September 2014
SEE Pro-ton	PSI, PIF	March 22 – 23 2014	-	TN-IDA-RAD-14/6 March, 14, 2014	-	TN-IDA-RAD-14/8 September 11, 2014
		April 4 – 6 2014	TN-IDA-RAD-14/5 March, 14, 2014	-	TN-IDA-RAD-14/7 August, 15, 2014	-

Tab. 11: Technical notes