EVIDENCE OF DESTRUCTIVE SINGLE EVENT LATCH-UP ON VARIOUS DEVICES USING TILU2 TEST SYSTEM

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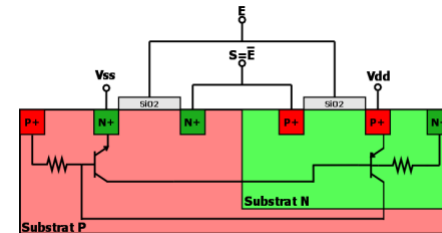Kevin SANCHEZ

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3/8/2015

In the frame of various activities (R&D, support to projects,…), we have collected SEE characterization data leading to the conclusion that samples were destroyed by SEL.

⇒ AD7688 (ADC SAR 16bits 500kSPS)

⇒ AD7982 (ADC SAR 18bits 1MSPS)

⇒ BSI BS62LV4006, (SRAM 4Mbits, 512Kx8)
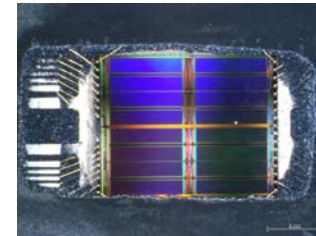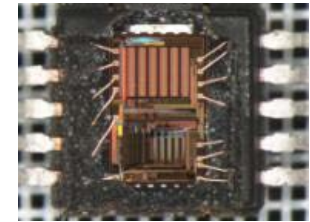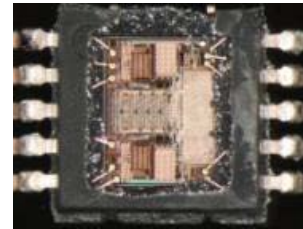
This work has been performed in the frame of internal R&D.
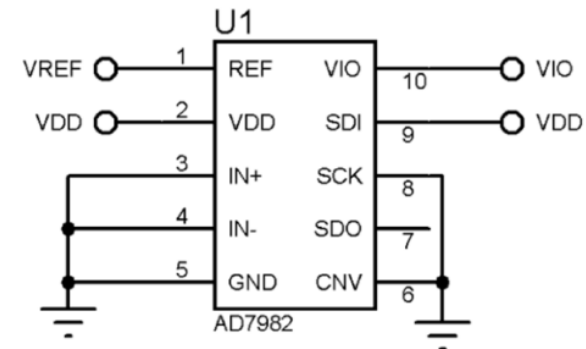
ANALOG DEVICES AD7688 (ADC SAR 16bits 500kSPS)

$\Rightarrow$ Tested by HIREX at TAMU: Destructive SEL on 4/4 DUTs

- Nominal Bias (3,3V-5V-5V)
- Ith=50mA (Inom~2mA)
- Tm = 2ms / Tc =1s
- Temp: 25°C

ANALOG DEVICES AD7982 (ADC SAR 18bits 1MSPS)

⇒ Tested by TRAD at UCL (static mode): Destructive SEL on 2/4* DUTs.

- VDD = +3V / **VREF = +6V / VIO = +6V**
- Ith: Idd = 10µA / Iref = 4mA / Iio = 4mA
- Tm = 1ms and 100µs / Tc = 7ms
- Temp: 25°C

2 DUT are not functional (no conversion), 2 other are functional with 300-400µA leakage currents. Physical Analysis shows metal migration on the 4 samples.

These Brilliance Semiconductors memories have been tested by CNES and have revealed a very high sensitivity to SEL even under Californium 252.
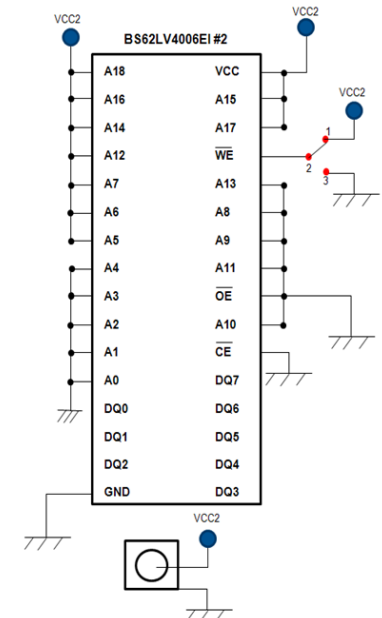
Candidates for in flight SEL mesurement.

BSI BS62LV4006, (SRAM 4Mbits, 512Kx8)

$\Rightarrow$ Tested by CNES (TILU2) under Cf252

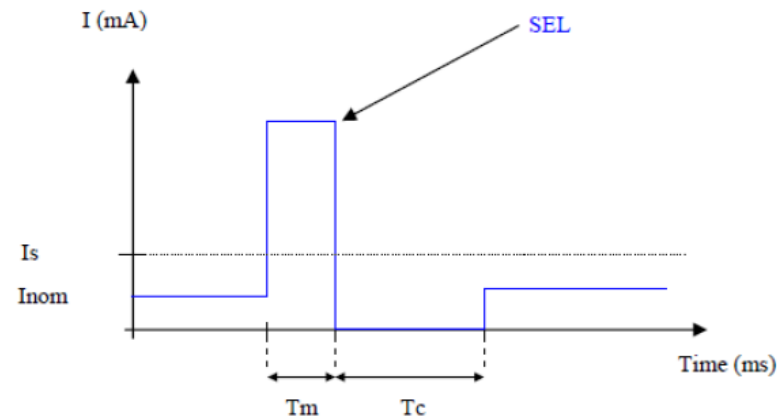$\Rightarrow$ Destruction of the DUT when accumulating SEL

$\Rightarrow$ Huge SEL current (I_{SEL}>1A when I_{nom}<1mA)

Each device has its own behavior.

Various parameters can influence the sensitivity of a DUT to SEL and destruction:

$\Rightarrow$ Bias

$\Rightarrow$ Current limitation

$\Rightarrow$ SEL detection threshold (current and timing)

$\Rightarrow$ Temperature

$\Rightarrow$ …

TEST PLAN

DUT	Bias	Lower I threshold	I max limitation	Temperature	Source
AD7688		x		25°C	UCL-HIF
AD7982	x			25°C	Laser
BS62LV4006			x	25°C	TRAD-Cf252
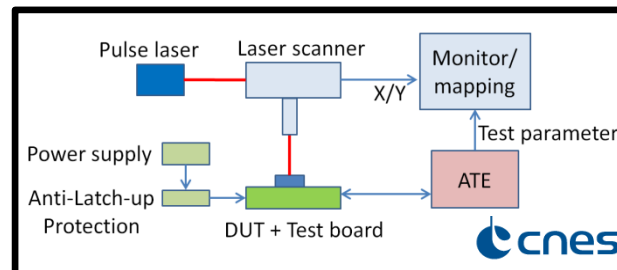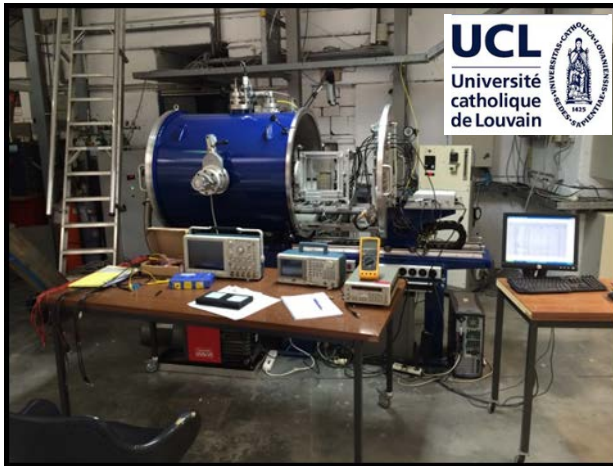
TILU2: Testeur Intégré de Latch Up 2eme génération
Integrated SEL Tester 2nd generation.

- 5 channels (see demo)
- Monitoring of I and V
- Temperature : 25 to 80°C
- Results: - I(t)
  - Isel distribution
 - Datalog of SEL
  - SEL Screenshots

RESULTS ON AD7688

- CH1: V_{io}/V_{ioAux}=3,3V; I_{nom}=1,7mA; $I_{threshold}$=15mA
- CH3: V_{dd}/V_{in-}=5V; I_{nom}<1mA; $I_{threshold}$=10mA
- CH4: V_{ddAux}=5V; I_{nom}<1mA; $I_{threshold}$=10mA
- Tc=Tm=10ms; Tinhib=0s

Irradiation:
Static mode
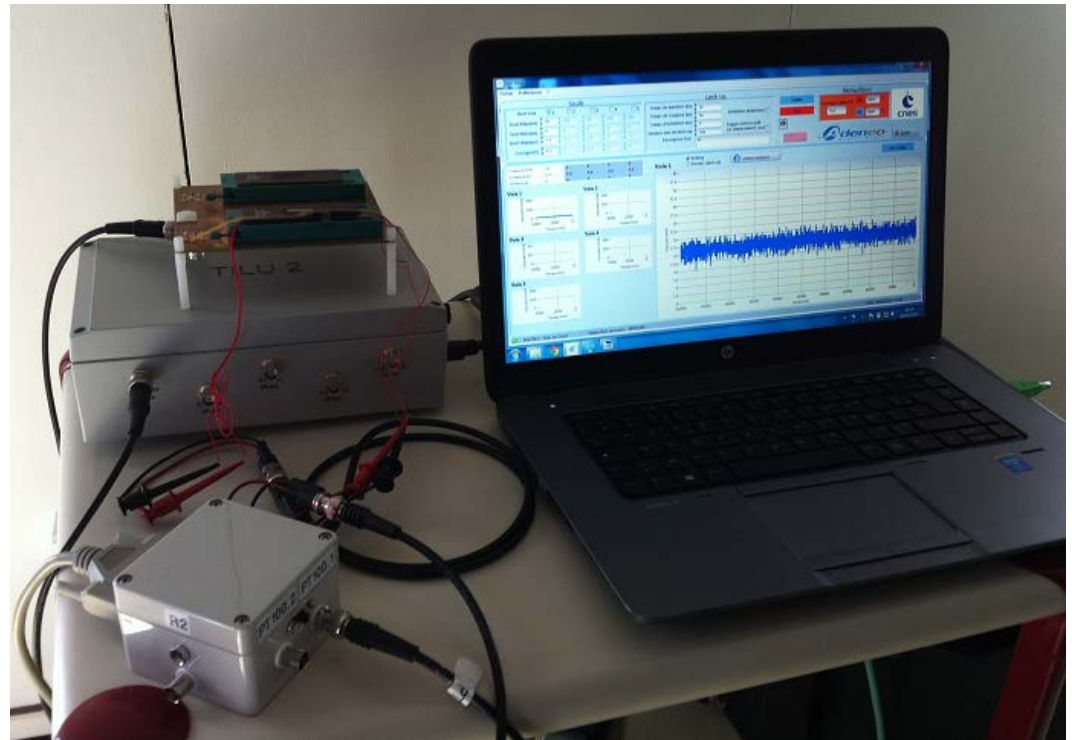
Post irradiation:
Dynamic functional test

RESULTS ON AD7688

- UCL-HIF, $_{83}$Kr *(E=756MeV, LET=32,6(MeV/mg)/cm²; r=92µm)*

⇒ SN6&8: Sensitive to SEL. Complete loss of functionality after ~15 SEL
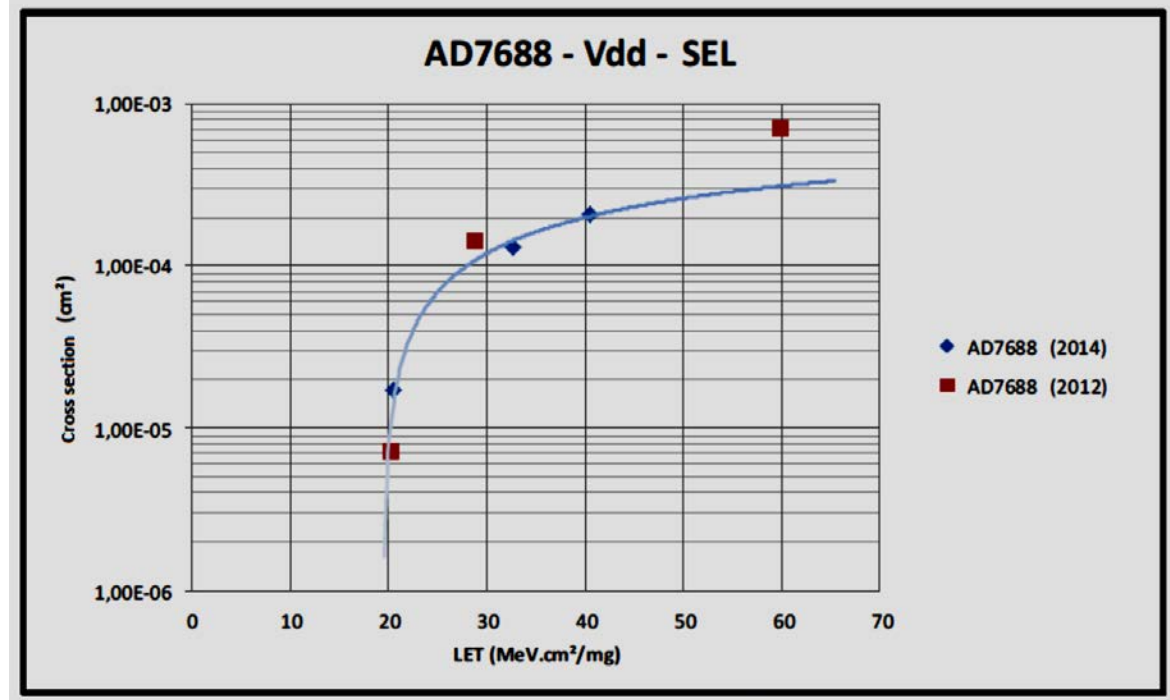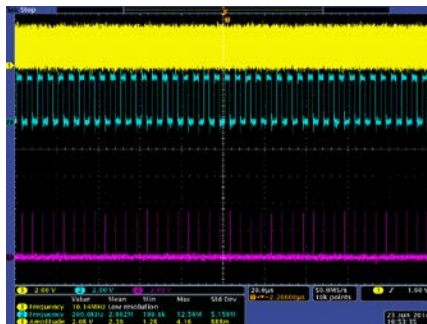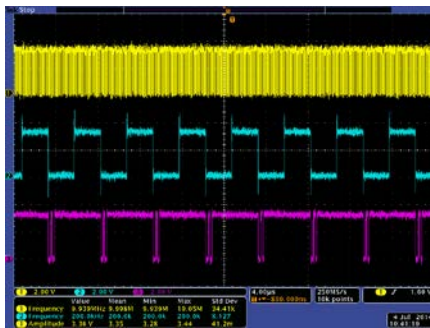
- UCL-HIF, $_{40}$Ar *(E=372MeV, LET=10,2(MeV/mg)/cm²; r=117µm)*

⇒ SN7 & SN9: No SEL, No loss of functionality.

- UCL-HIF, $_{83}$Kr *(E=756MeV, LET=32,6(MeV/mg)/cm²; r=92µm)*

$\Rightarrow$ SN6: Current vs time
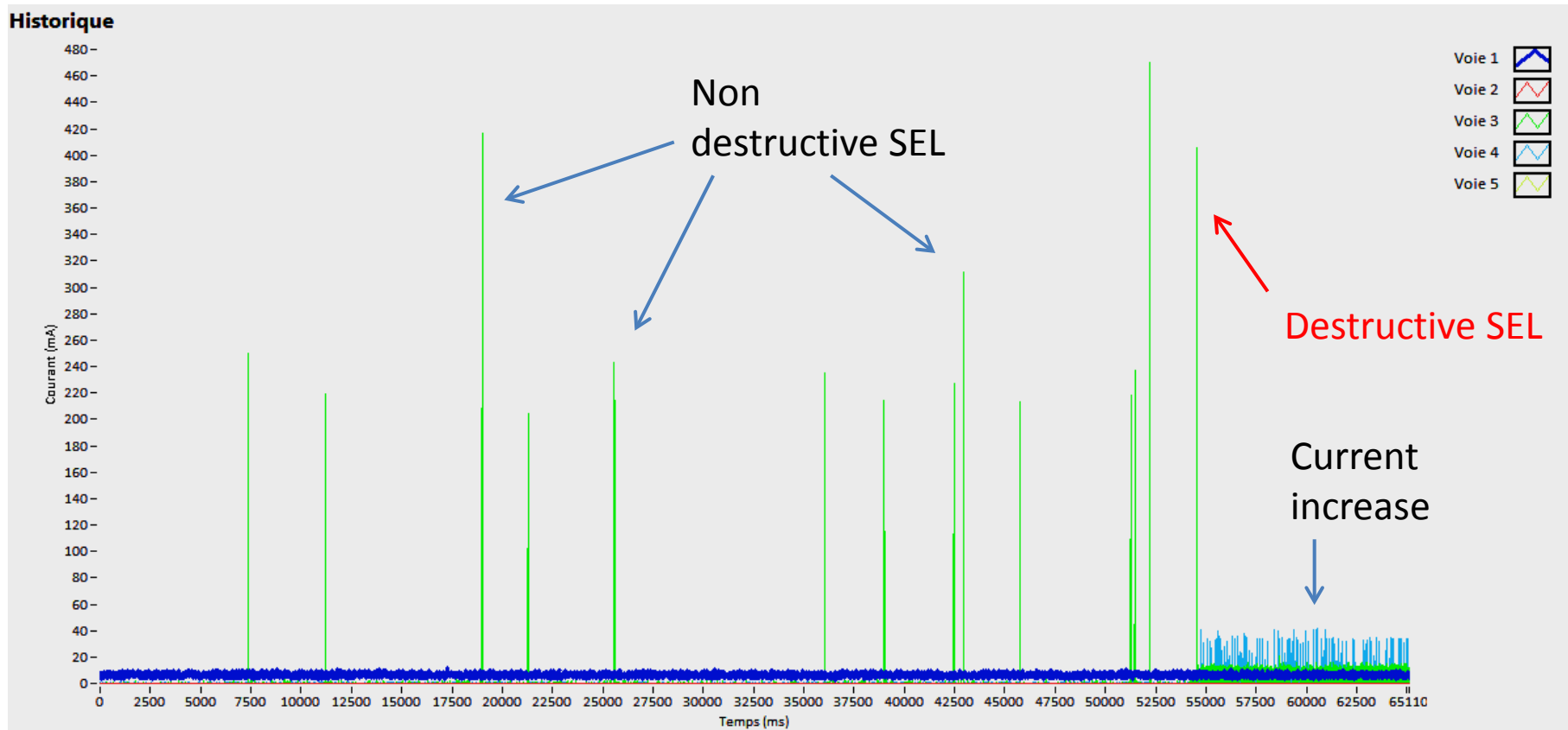
DUT are destroyed by SEL e event when $I_{threshold}$ is very low.

Tested under laser beam (CNES AQ/LE 2013):

$\Rightarrow$ No destructive SEL for standard bias, only non destructive SEL on Vdd.

$\Rightarrow$ Destructive SEL on Vio/Vref for Absolute Max Rating bias conditions only.
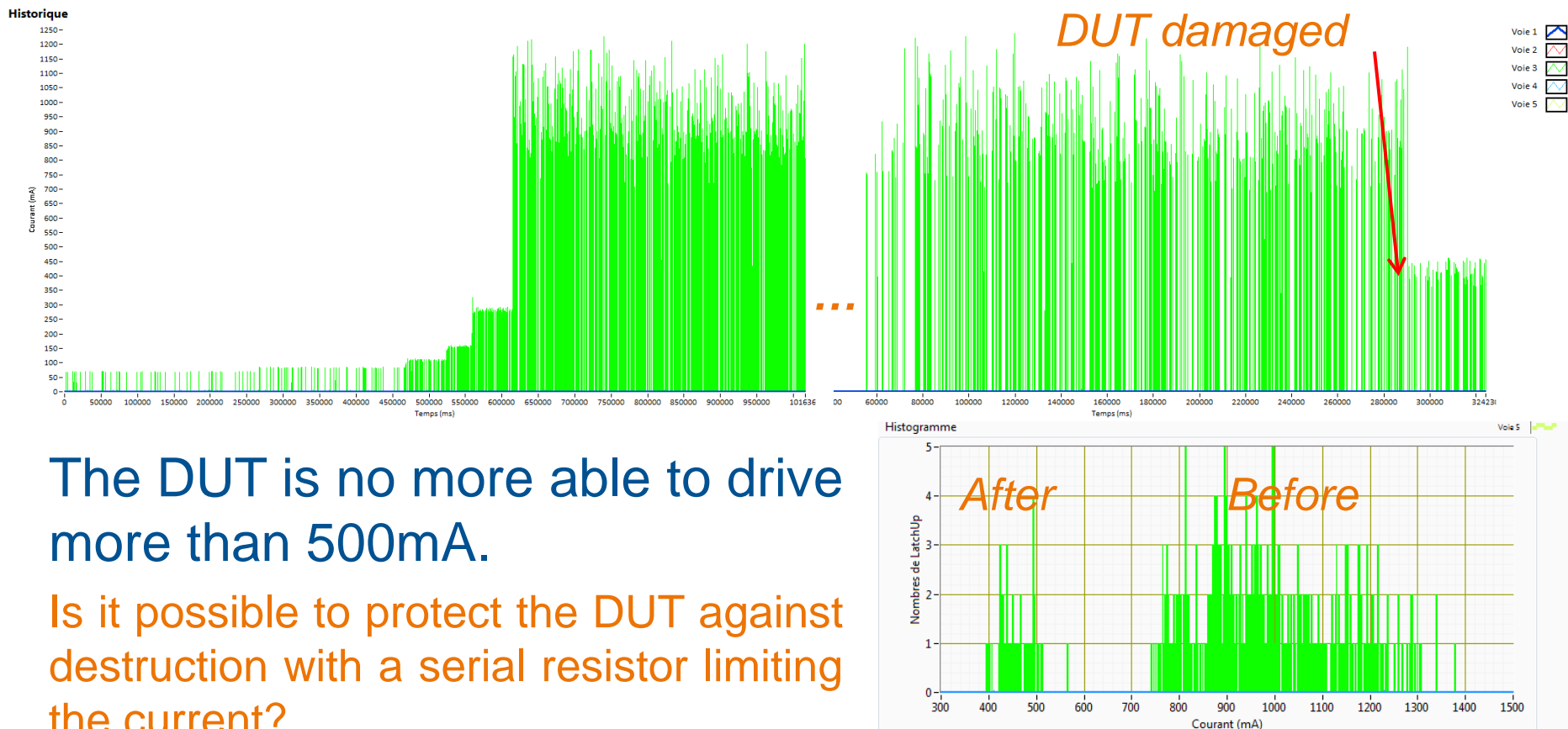
- CH3: V_{cc}=5V; I_{nom}<1mA; $I_{threshold}$=8mA
- Tc=Tm=50ms; Tinhib=0s

=> Isel distribution varies in time as well as SEL sensitivity. (thermal effect)
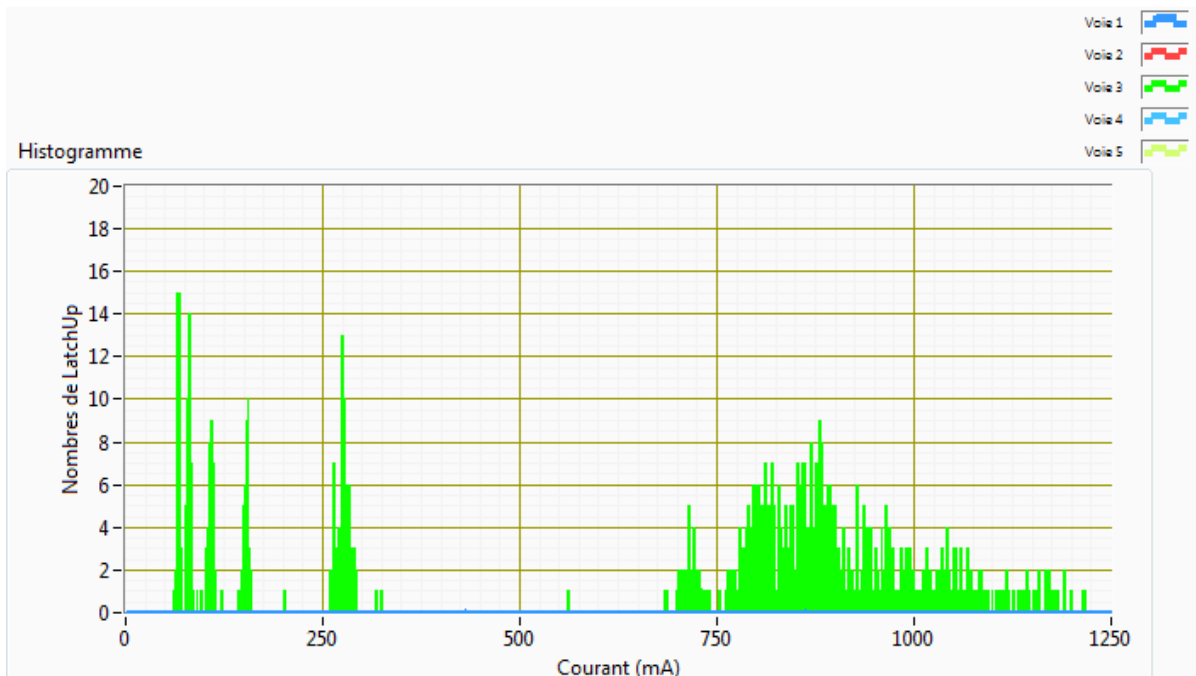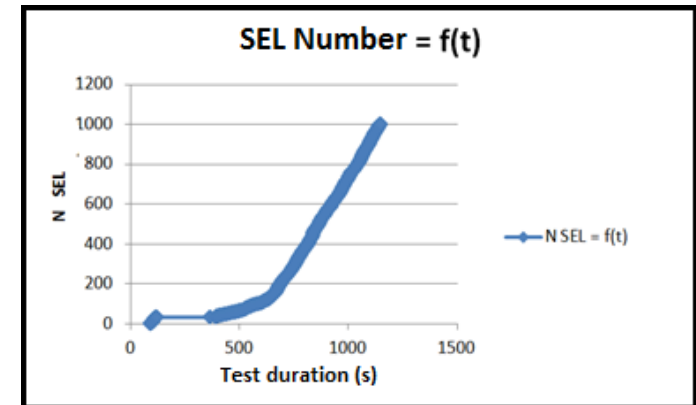
If the test is long without current limitation Isel increases with time and after a while, the DUT is damaged.

DUT damaged

The DUT is no more able to drive more than 500mA.

Is it possible to protect the DUT against destruction with a serial resistor limiting the current?

After ... *Before*

A variable serial resistor is used to limit I_{SelMax}:

- By limiting the current, the temperature increase is also reduced as well as the device sensitivity to SEL.

- With a serial resistor higher than 50 Ohms, no more destruction is observed.
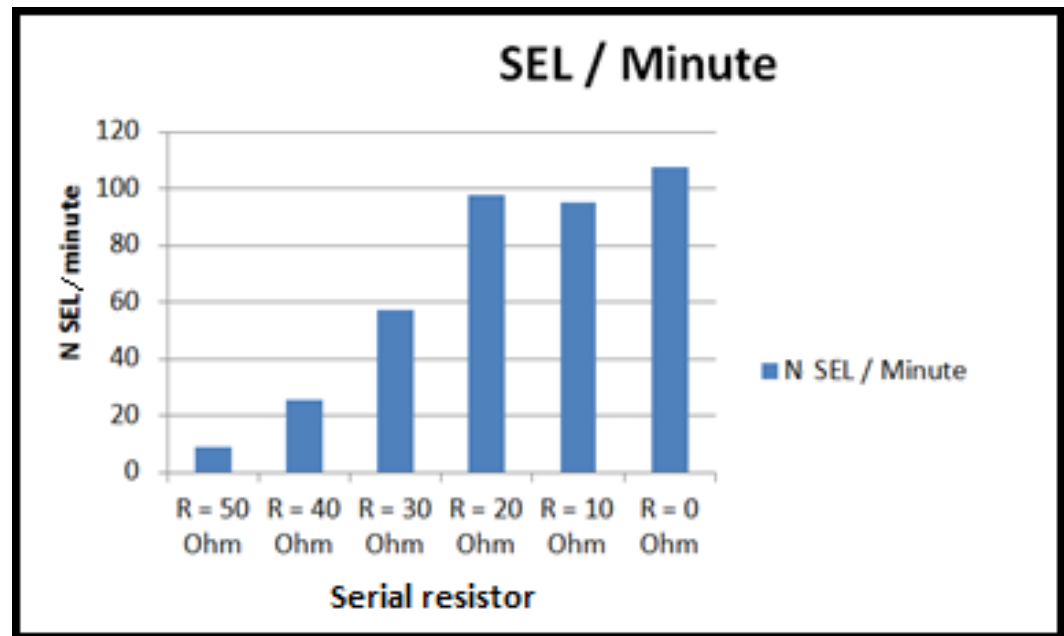
No solution was found to protect AD7688 against destruction.

The destructive SEL measured on the AD7982 were due to bias conditions more severe than specification (absolute max rating/Max rating).

By limiting the max Current, the BSI SRAM can be protected (thermal effect).

In some cases DUT cannot be protected from destruction due to SEL.

$\Rightarrow$ It is then very dangerous to build an « a priori » anti-latchup system without prior characterization of the behavior of the DUT.

$\Rightarrow$ The design of an anti latch-up system requires both the identification of SEL current signatures and SEL sensitivity.