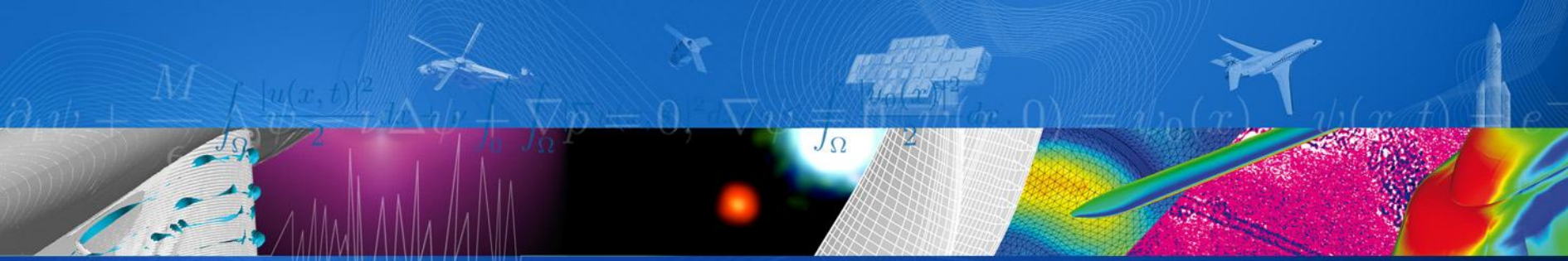

Single Event Upset Sensitivity on D-latches in Infrared Image Sensor for Low Temperature Applications

L. Artola[1], G. Hubert[1], O. Gilard[2], S. Ducret[3], F. Perrier[3], M. Boutillier[2], P. Garcia[4], G. Vignon[4], B. Baradat[2], and N. Ricard[3]

[1] ONERA DESP, Toulouse France
[2] CNES, Toulouse, France
[3] Sofradir, Veurey Voroize, France
[4] TRAD, Labége, France

Supported by R&T CNES contract no. 4500043111/DCT094

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retour sur innovation

Context of the CNES study (1/2)

- CMOS technology is relevant for integrate electronic functions in image sensors (raw decoders, registers, D-latches)
- The SEEs (SEU and SET) sensitivity of CMOS technology increases with technological roadmaps
- Sensitivity trends of SEU/SET are known for elevated temperatures
- High temperatures rise the soft error duration and the SEU occurrence
- For performance reasons, Infrared image sensors developed by Sofradir works at very low temperatures down to 77°K

→ What are the SEU sensitivity trends of D-latches for very low temperatures down to 77°K under heavy ions?

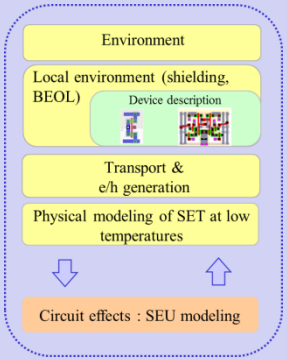
Context of the CNES study (2/2)

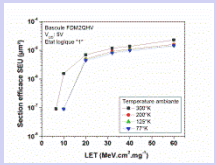
→ Two CNES R&T studies have been launched to investigate the SEU sensitivity of D-latches in image sensors for cryogenic temperatures under heavy ions

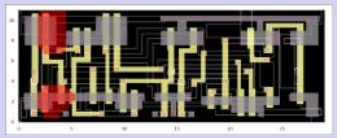
ONERA

R&T R-S13/MT-0003-122

- Modeling of SET/SEU in 0,25µm D-latches for low temperatures:



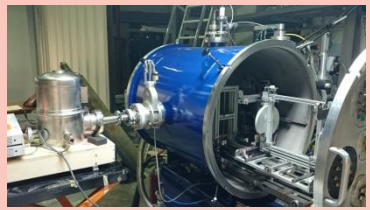


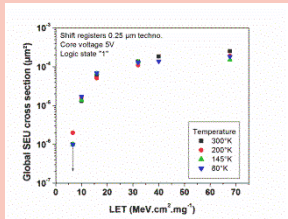


TRAD

R&T R-S13/MT4-151

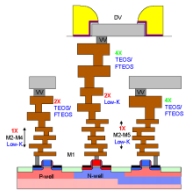
- SEU measurements in read circuit at cryogenic temperatures:





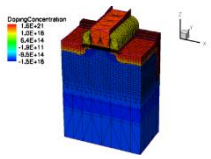
Goals and tasks of the R&T study

- Technical tasks and MUSCA SEP3 (ONERA prediction tool)



Task 1
Layout: GDS , circuit and model cards

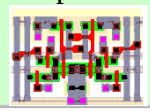
Task 2
Calibration of analytical models by TCAD simulations



Environment

Local environment (shielding, BEOL)

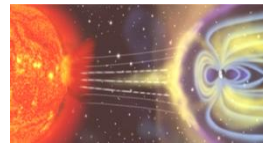
Device description



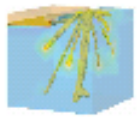
Transport & e/h generation

Physical modeling of SET at low temperatures

Circuit effects : SEU modeling

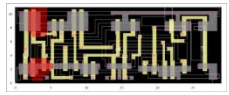


Interactions

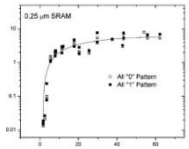


R&T CNES

Task 3
MUSCA SEP3 calculations & analyses



Task 4
Experimental comparisons



Outline of the presentation

- Modeling of the circuit at layout and schematics level
  - Design extraction from GDS and circuit modeling
- Calibration of analytical SET models at low temperatures
  - Study and modeling of low temperature effects on the transport and collection mechanics by TCAD simulation
- Estimation of SEU sensitivity of D-latches in 0.25µm technology
  - SEU cross section estimations and analyses
  - Failure analyses of D-latch by sensitivity maps modeling
- Comparisons of SEU estimations versus experimental measurements
  - Comparisons of the SEU occurrences prediction with the heavy ion experimental data

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D-latches cells modeling

- Test chip developed by Sofradir called SEU2_01A
  - 6 references of D-latches cells designs

Reference	Cell area (normalized)	Width (normalized)	High (normalized)	Techno. Node (µm)
SEU_01A				
Design 1	1,03	1,03	1	0,25
Design 2	1	1	1	0,25
Design 3	1,1	1,1	1	0,25
Design 4	1,07	1,07	1	0,25
Design 5	1,2	1,2	1	0,25
Design 6	1,17	1,17	1	0,25

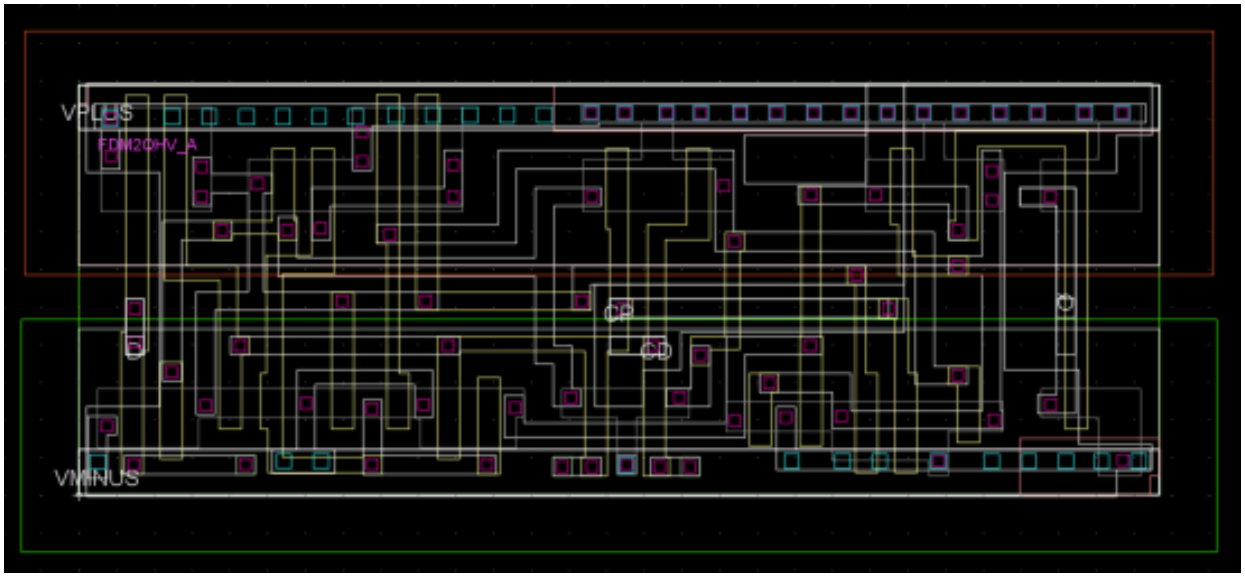
Analyzed designs

2 Designs are investigated for their criticality in Sofradir Infrared image sensors

Task1: Circuit modeling

- Modeling of the D-latch circuit at layout level
  - Design extraction from GDS and circuitry development

- Extraction of collection areas from Sofradir's GDS file
- Circuit development with Cadence software suite based on the netlist

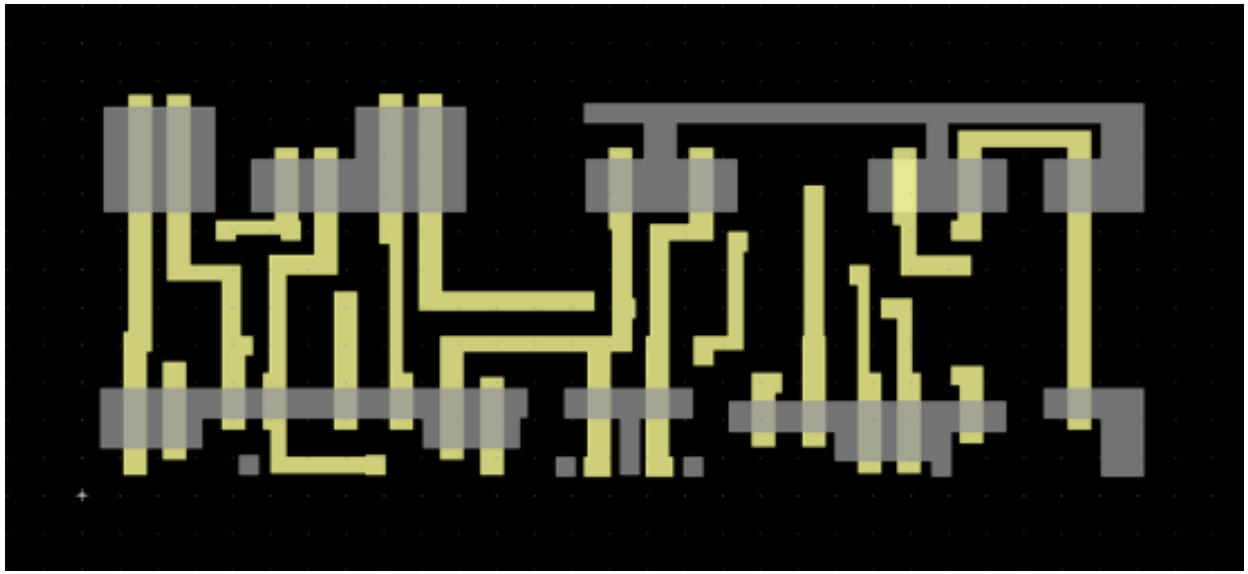


GDS file from Sofradir

Task1: Circuit modeling

- Modeling of the D-latch circuit at layout level
  - Design extraction from GDS and circuitry development

- Extraction of collection areas from Sofradir's GDS file
- Selection of relevant BEOL layers (polysilicon and active implants)

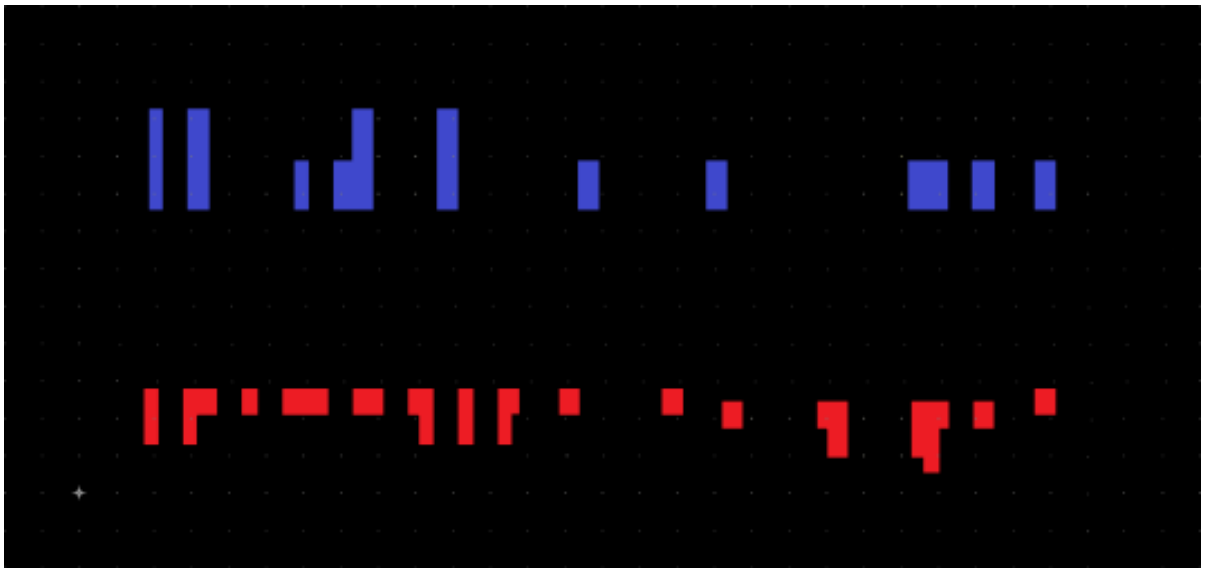


GDS file reworked

Task1: Circuit modeling

- Modeling of the D-latch circuit at layout level
  - Design extraction from GDS and circuitry development

- Extraction of collection areas from Sofradir's GDS file
- Determination of collection area: drains of p-MOS and n-MOS transistors of floating nodes



Extracted Design file

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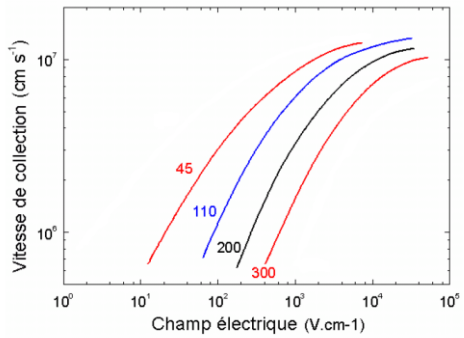
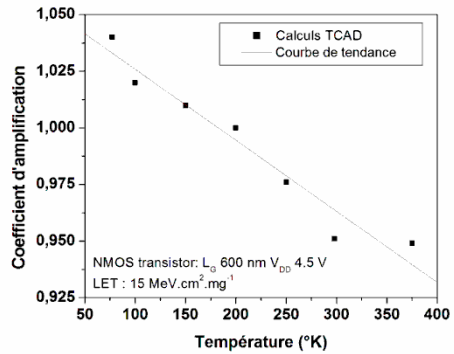
Task2: Calibration of SET models at low temperatures

- Study of low temperatures effects on SETs by TCAD simulations
  - Calibration of transport models in MUSCA SEP3 at low temperatures down to 77°K
    - Calibration of mobility models
    - Adjustment of ambipolar diffusion modeling
    - Adjustment of carrier-carrier scattering modeling
  - Calibration of collection models in MUSCA SEP3 at low temperatures down to 77°K
    - Expansion of electrical abacus of *Jacoboni et al* for the collection velocity modeling
    - Evaluation and calibration of bipolar amplification modeling

Collection velocity



Bipolar amplification



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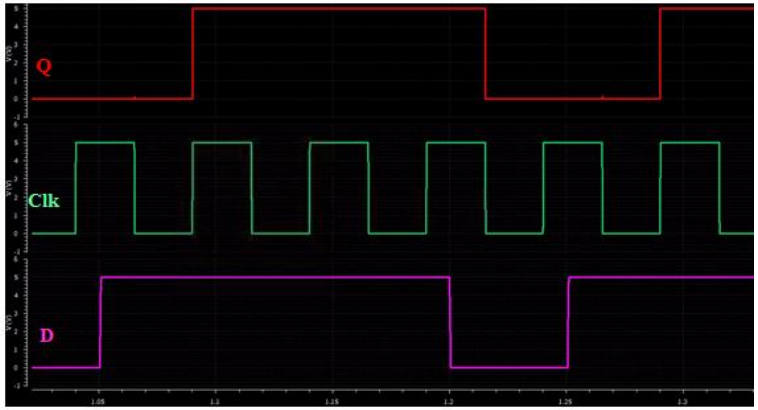
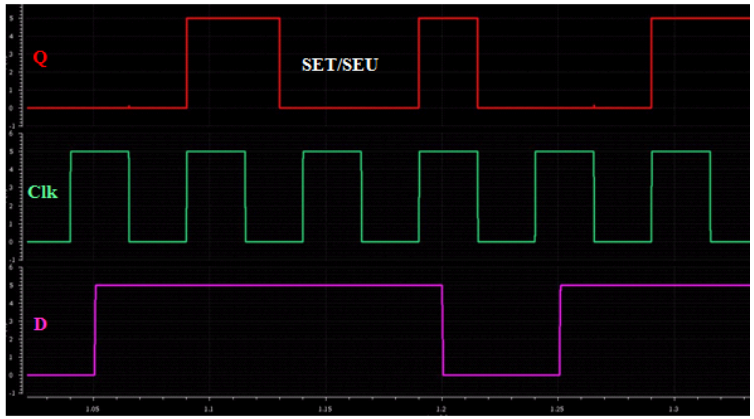
Task3: Estimation of SEU sensitivity (1/5)

- Detection of SETs in the D-latches (design 1 and 2)
  - Nominal working of the D-latch



No SEU

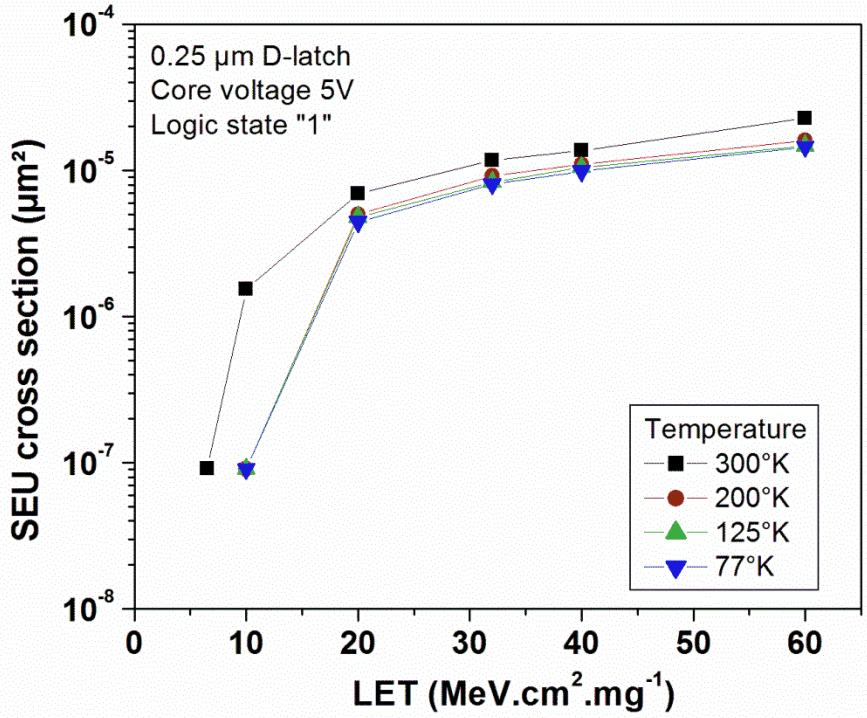
  - SET/SEU occurrence on the D-latch ouput



SEU

Task3: Estimation of SEU sensitivity (2/5)

- Effects of low temperatures on the SEU cross section of the D-latch FDM2QHV (design 2)

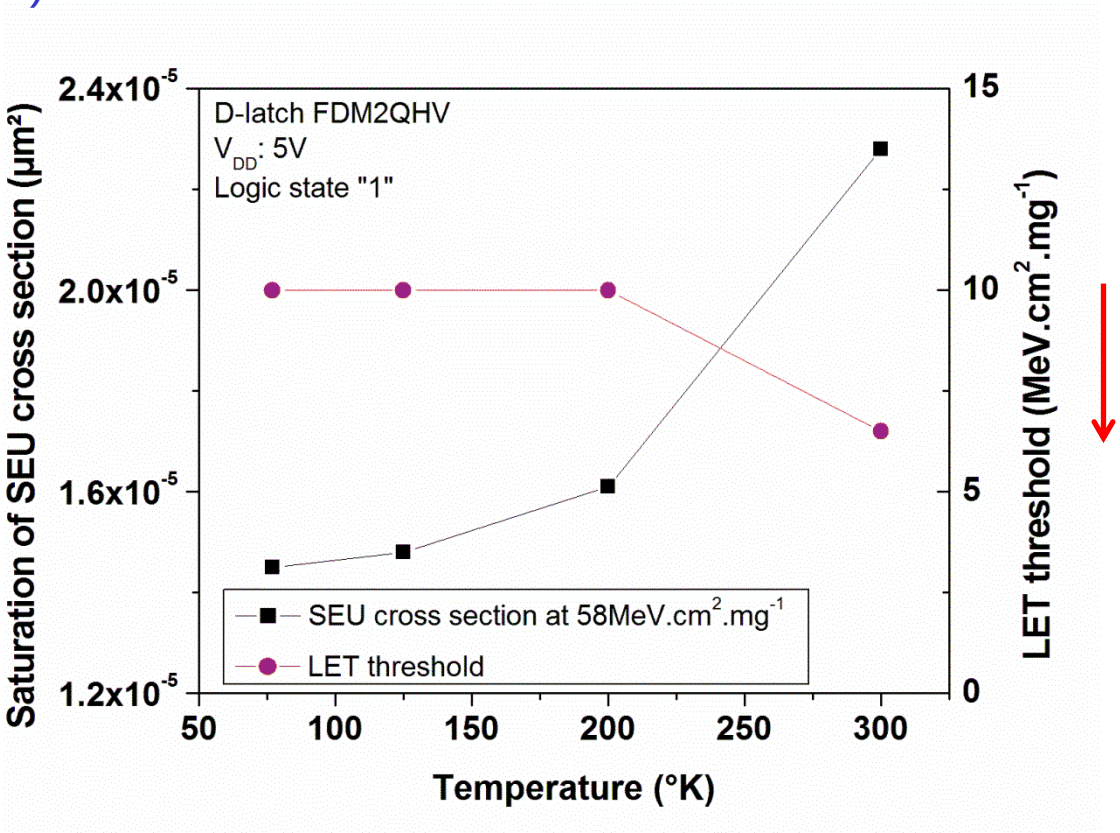


Lower temperatures → Lower SEU sensitivity

Saturation of the temperature effects on the SEU sensitivity

Task3: Estimation of SEU sensitivity (3/5)

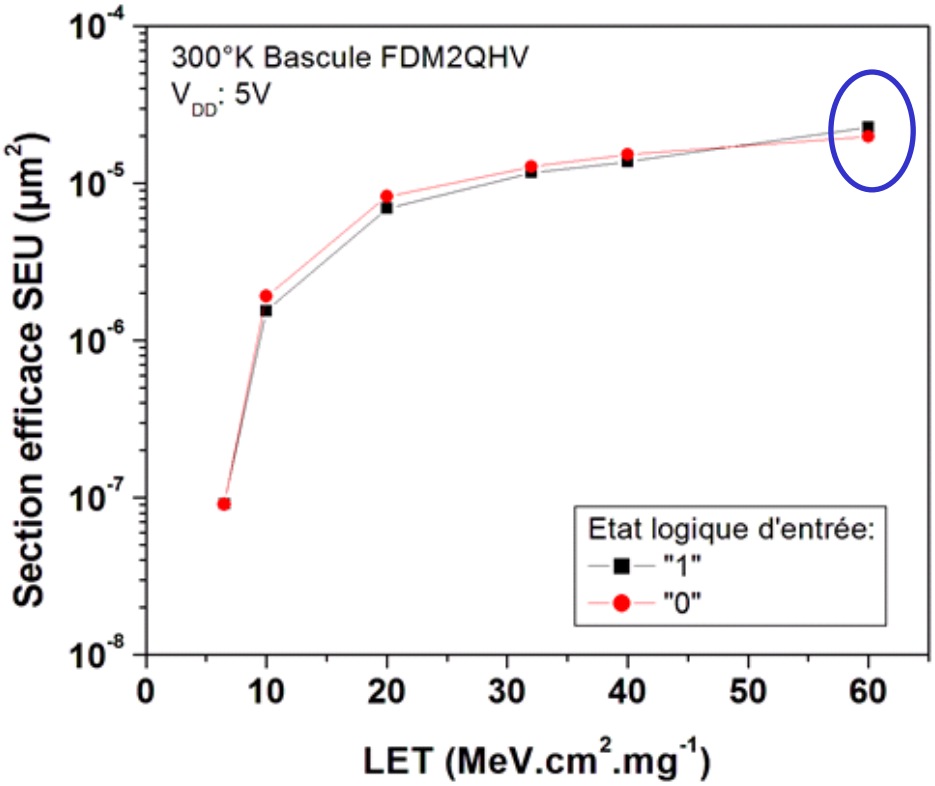
- Temperature effects on the SEU sensitivity metrics for the D-latch FDM2QHV (design 2)



Limitation of the impact of low temperatures on **LET threshold** and **cross section saturation**

Task3: Estimation of SEU sensitivity (4/5)

- Effects of logic state on the SEU cross section of the D-latch FDM2QHV (design 2)

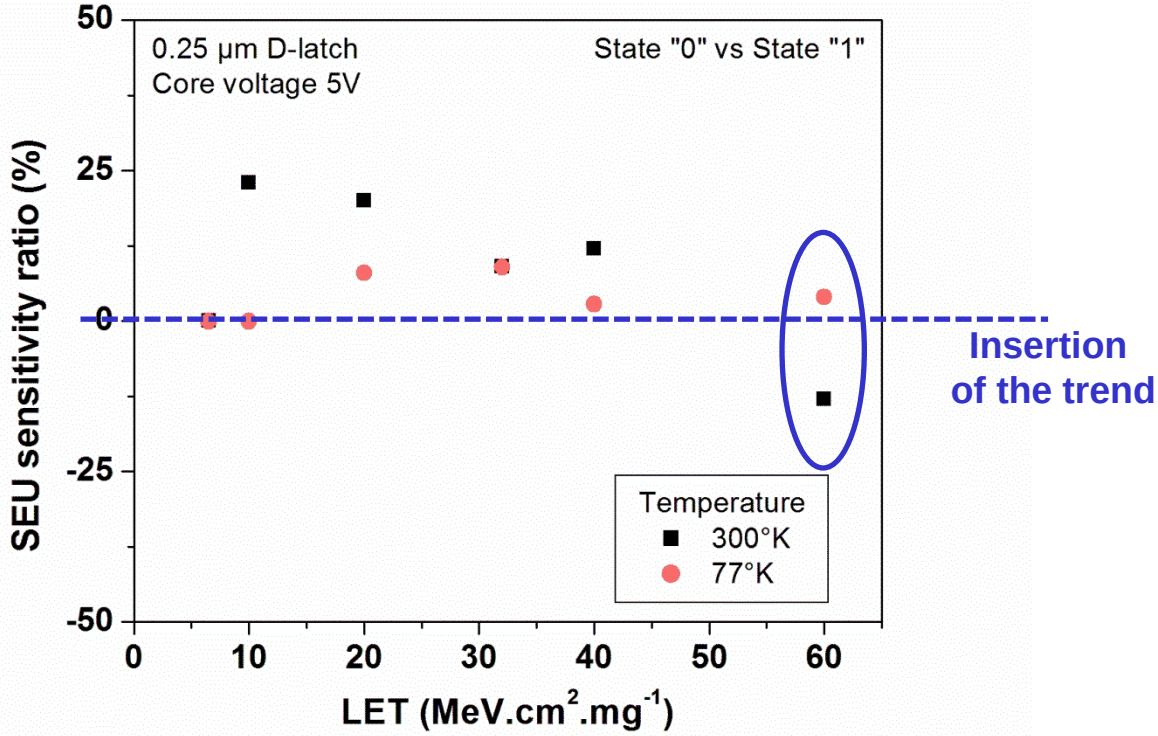


Insertion of the trend

Weak variations of the SEU sensitivity on the global SEU cross section

Task3: Estimation of SEU sensitivity (5/5)

- Effects of logic state on the SEU cross section of the D-latch FDM2QHV (design 2)



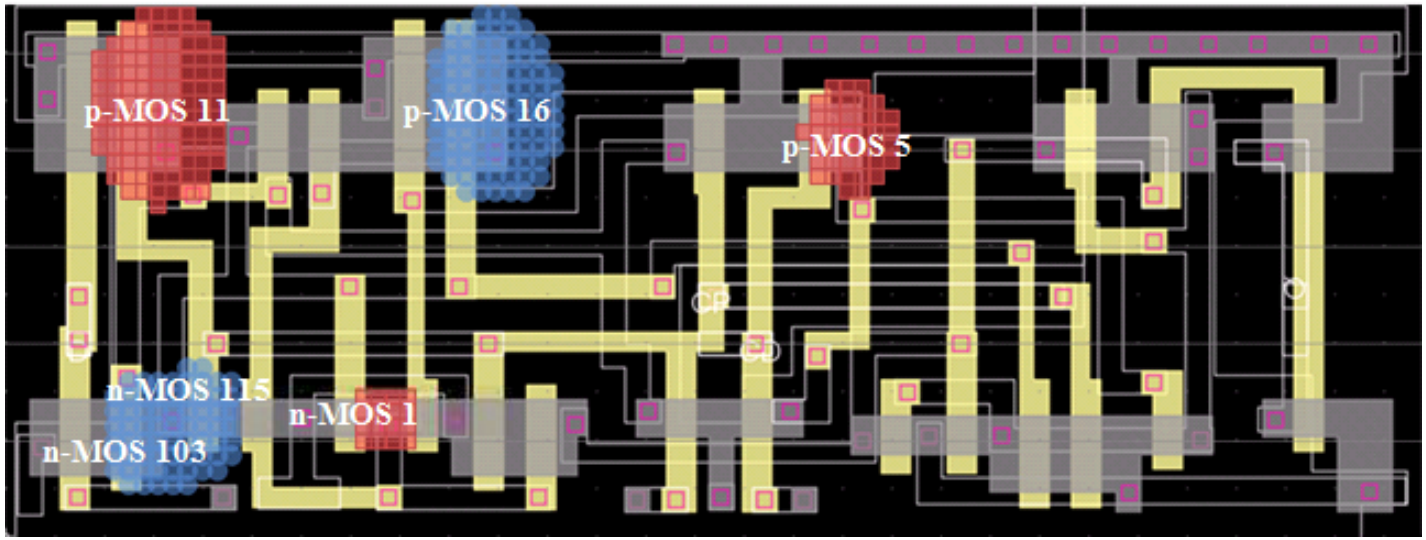
Lower SEU sensitivity at state “1” excepted at high LET and 300°K

Reduction of the logic state impact at low temperature 77°K

Task3: Failure analysis of the D-latch cell (design 2) (1/2)

- SEU sensitivity maps for a LET 58,8 MeV.cm^2.mg^{-1} at **77°K**

State « 1 » **State « 0 »**

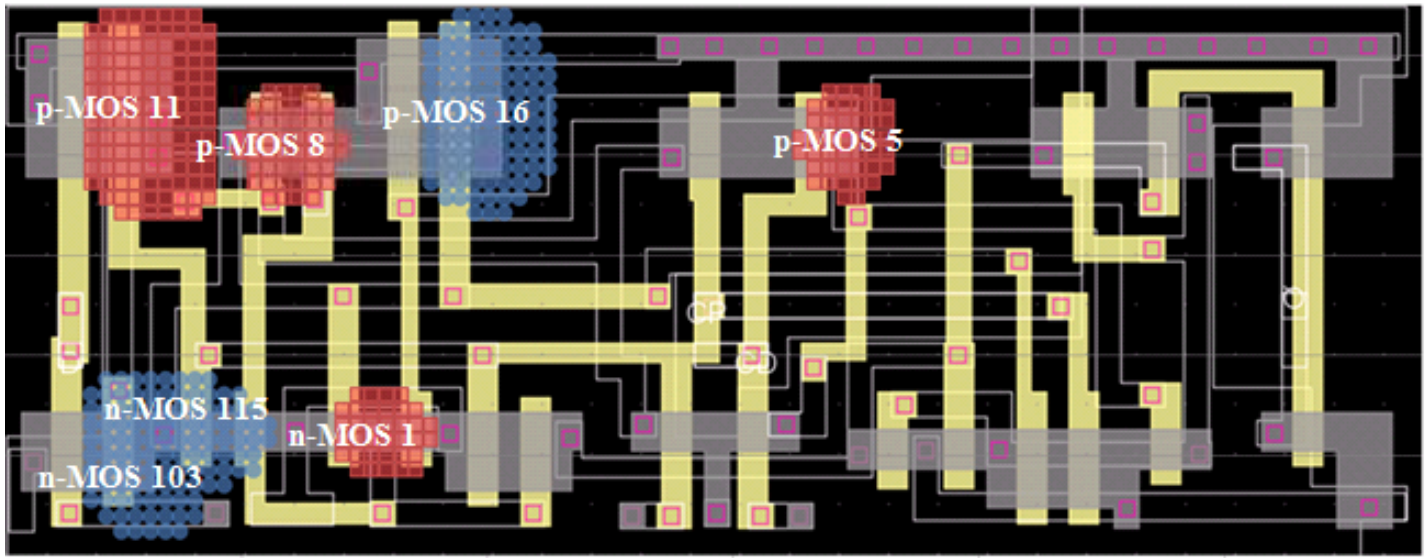


The logic state changes the SEU critical areas of D-latch cell

Task3: Failure analysis of the D-latch cell (design 2) (2/2)

- SEU sensitivity maps for a LET 58,8 MeV.cm^2.mg^{-1} at **300°K**

State « 1 » **State « 0 »**



At 300°K → New sensitive transistor (p-MOS 8) → State 1 more sensitive than State 0

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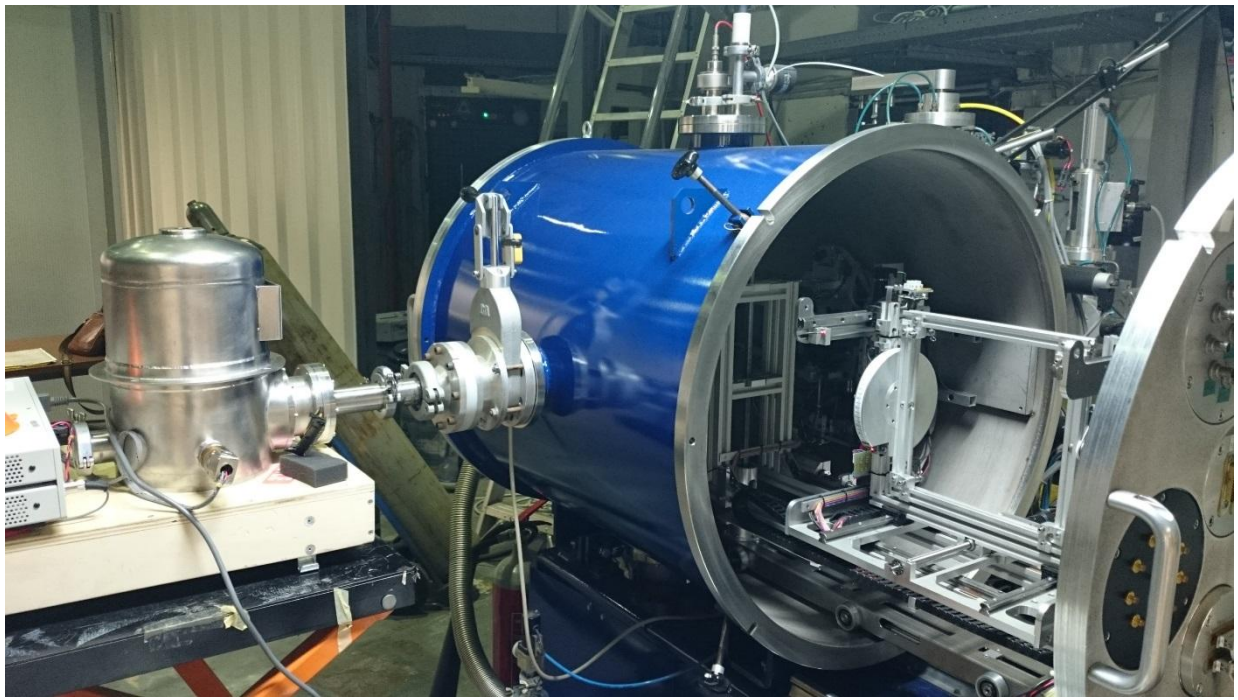
Task4: Comparison SEU estimation vs. Exp. Data (1/3)

- Experimental heavy ion irradiation for SEU measurements performed at UCL with CNES cryostat



Temperature monitoring and regulation from 300°K to 80°K

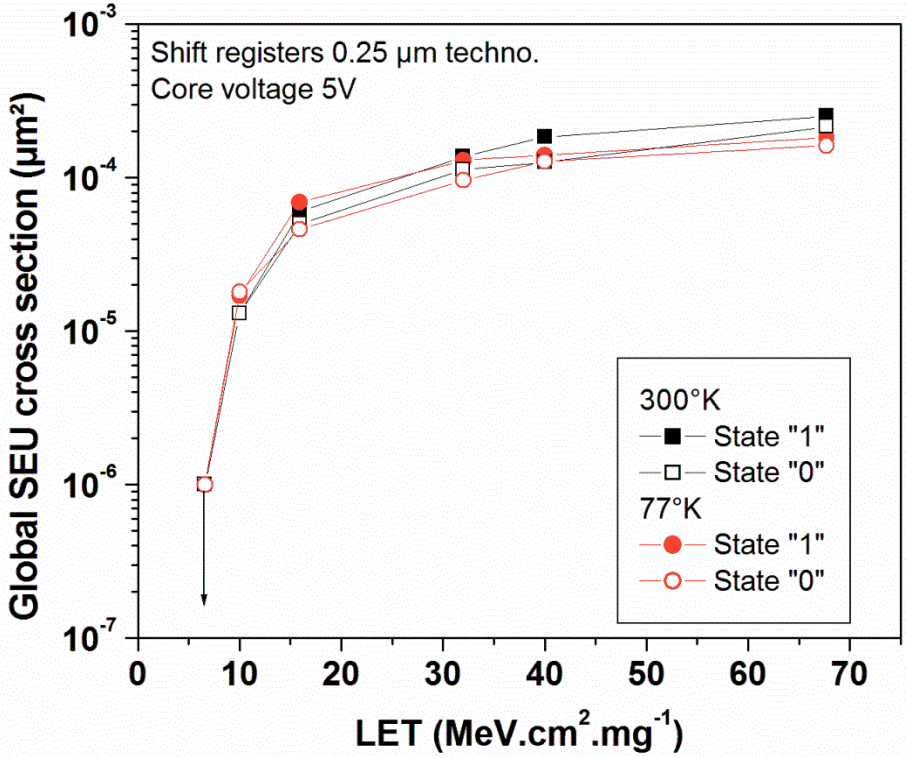
Heavy ion irradiation from 6.6MeV.cm^2.mg^{-1} to 67.7MeV.cm^2.mg^{-1}

Dynamic SEU testing with TRAD test board using CNES cryostat under heavy ions beam at UCL, Belgium

Logic state, temperature are considered depending on LET of heavy ions

Task4: Comparison SEU estimation vs. Exp. Data (2/3)

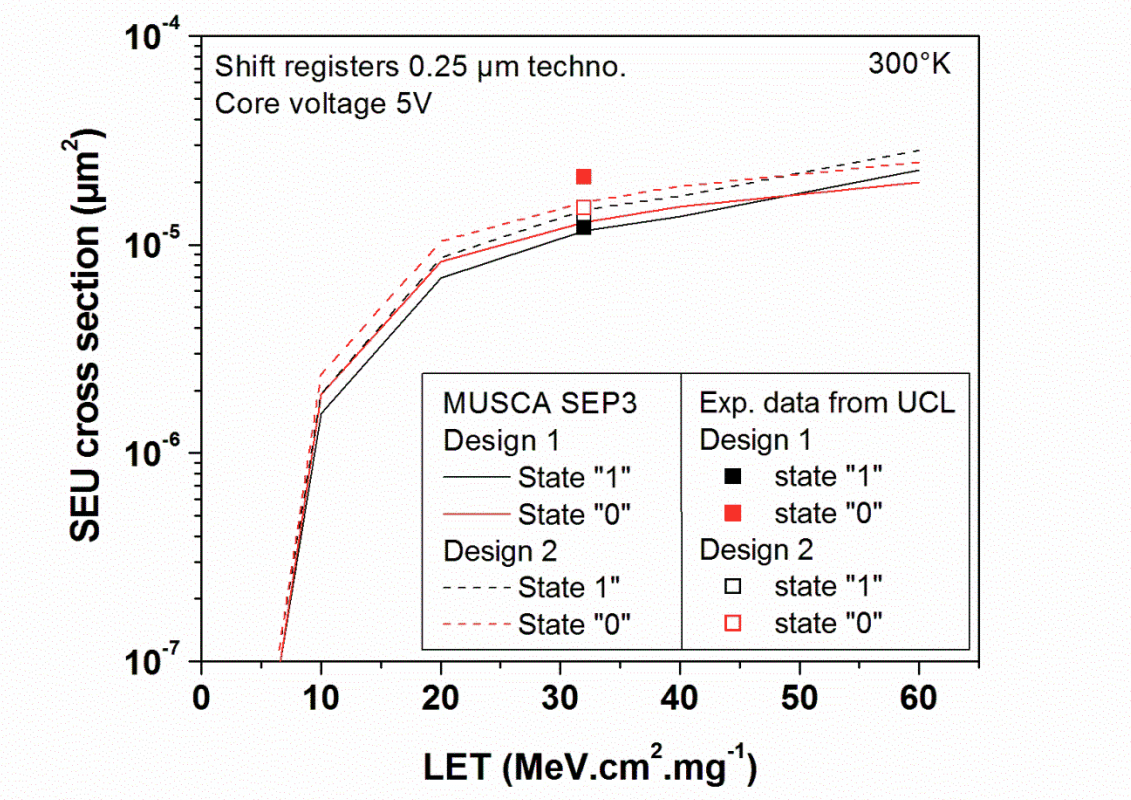
- Preliminary global SEU cross section of all D-latches of designed chip at 300°K and 77°K



The global SEU sensitivity of the DUT can not lead to extract a specific trend as a function of temperature → deeper analysis required

Task4: Comparison SEU estimation vs. Exp. Data (3/3)

- SEU cross section of D-latches **FDM2QHV** (design1) and **FDM2HV** (design2)



Really good correlation between calculations and experimental data for design2 on state0 and state1

Unexpectable variability of SEU sensitivity between design1 and design2 → statistical disparity ?

Conclusions and 2015 perspective

- Multi-scales modeling (with MUSCA SEP3 tool) leads to estimate the SEU sensitivity of digital cell such as D-latches for cryogenic temperatures.
- Modeling leads to propose failure analysis at circuit and layout level
- Good correlations of SEU calculations and experimental SEU measurements under heavy ion irradiations at UCL facility (Belgium)
- Comparisons between MUSCA SEP3 tool and experimental measurements emphasize the interest of modeling with the aim to define a new test plan for a better experimental statistics taking into account design parameters of the DUT

→ **New SEU test campaign is planned for 2015**