DEPARTMENT OF
INFORMATION
ENGINEERING
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Studies of radiation effects in new generations of non-volatile memories: Destructive SEEs in Single-Level Cell NAND Flash Memory

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Introduction and purpose

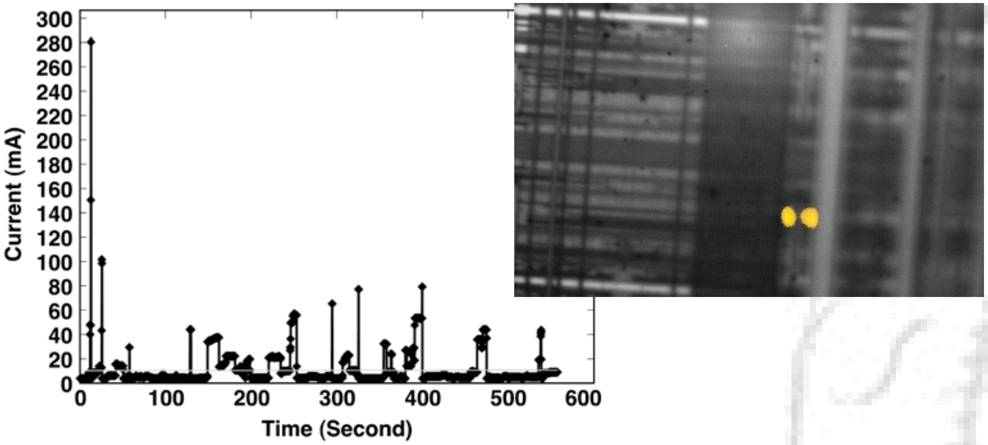
- **NAND Flash memories** are attractive for space designers due to their non-volatility, large size, small-power consumption, and low cost, not matched by rad-hard memories
- Radiation effects have been widely studied, but some of the mechanisms are still not completely understood
- In addition to SEUs/MBUs/SEFIs, several groups reported the occurrence of destructive events, i.e. the irradiated samples lose their functionality (fail to program and/or erase)

The purpose of this work is to **investigate the occurrence of destructive events in NAND Flash memories through ad hoc micro-beam and broad-beam experiments**

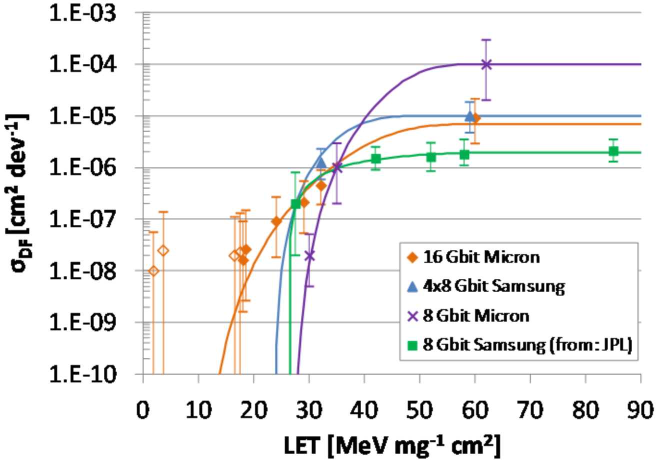
Outline

- NAND Flash memories (Single-Level Cell)
    - Context and previous work on destructive SEEs
    - Basic concepts on NAND Flash memories
    - Experimental set-up and tested devices
    - Results on destructive Single Event Effects
    - Annealing after irradiation

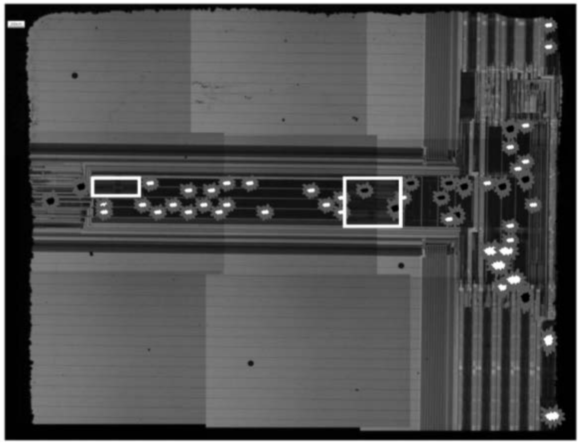
Context and previous work



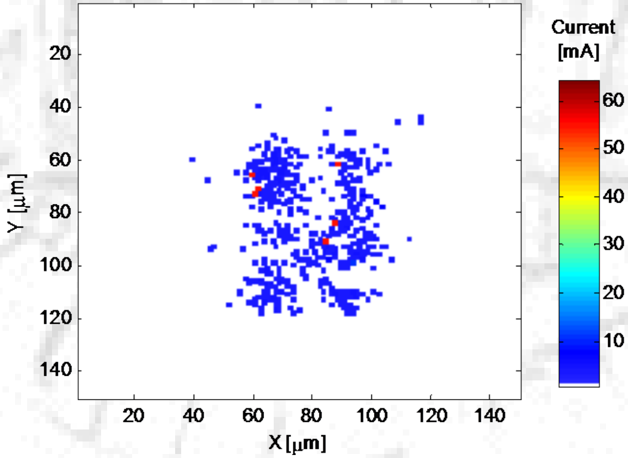
First observations of current spikes and SEGR by *F. Irom et al.*



Extensive test campaigns with broad beam by *K. Grürmann et al.*



Laser and milli-beam investigations by *T. Oldham et al.*



Micro-beam (180μm) and broad beam experiments by *S. Gerardin et al.*

Open questions

- Some observations from previous work
  - There is no direct correlation between current spikes and destructive events
  - Destructive events in some cases were observed only with broad beam and not with collimated beam
  - Experimental assessment is complicated by the small cross section and the large amount of samples and beam time needed for just a few observations, especially with collimated beams

Destructive events caused by two temporally close strikes in different parts of the memory, whose effects overlap in time?

Destructive events NOT a concern in space?

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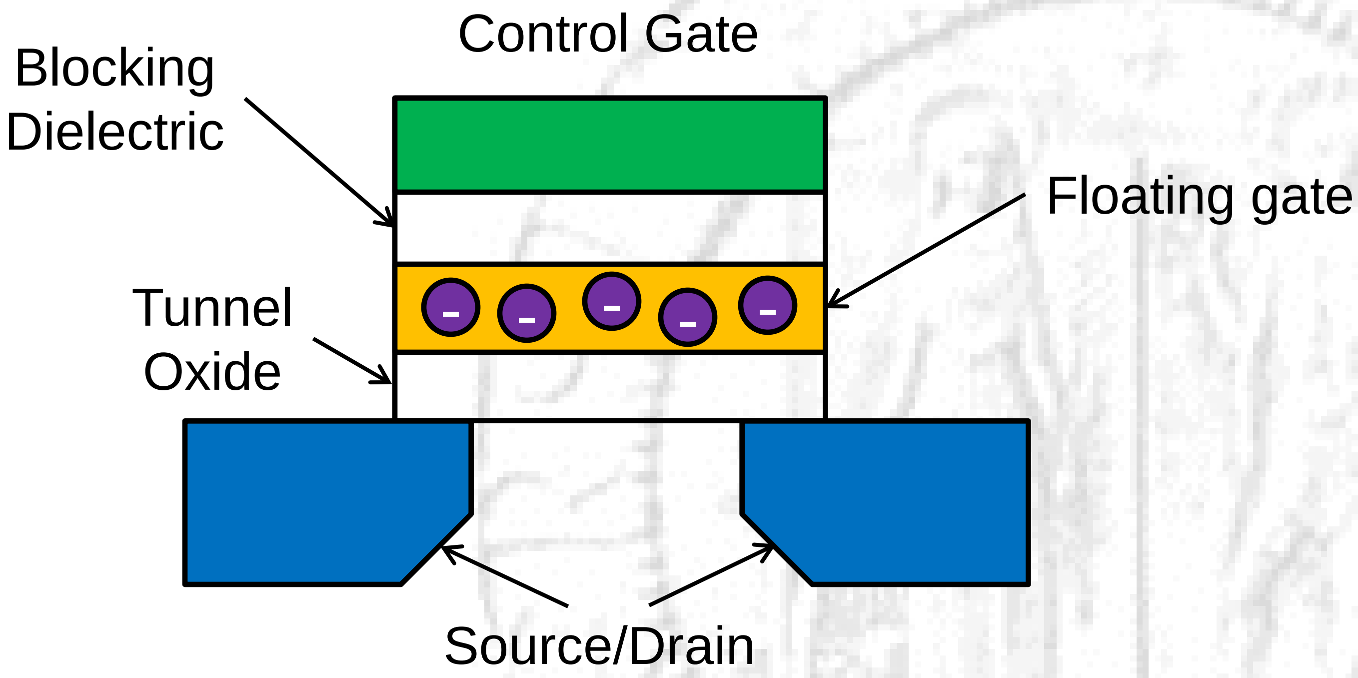
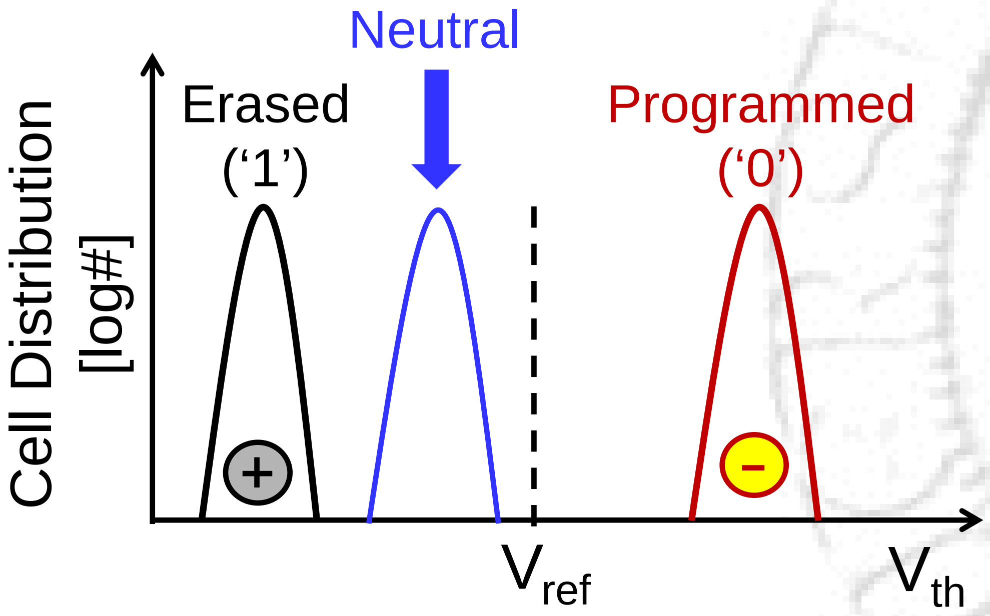
Floating Gate Cells



- <u>Storage concept</u>: Inject or remove **charge** in a **Floating Gate (FG)** between the control gate and the channel
- The threshold voltage (V_{th}) determines the status of the cell
- The cell is biased with a given reference voltage and the program status is determined based on the drawn current

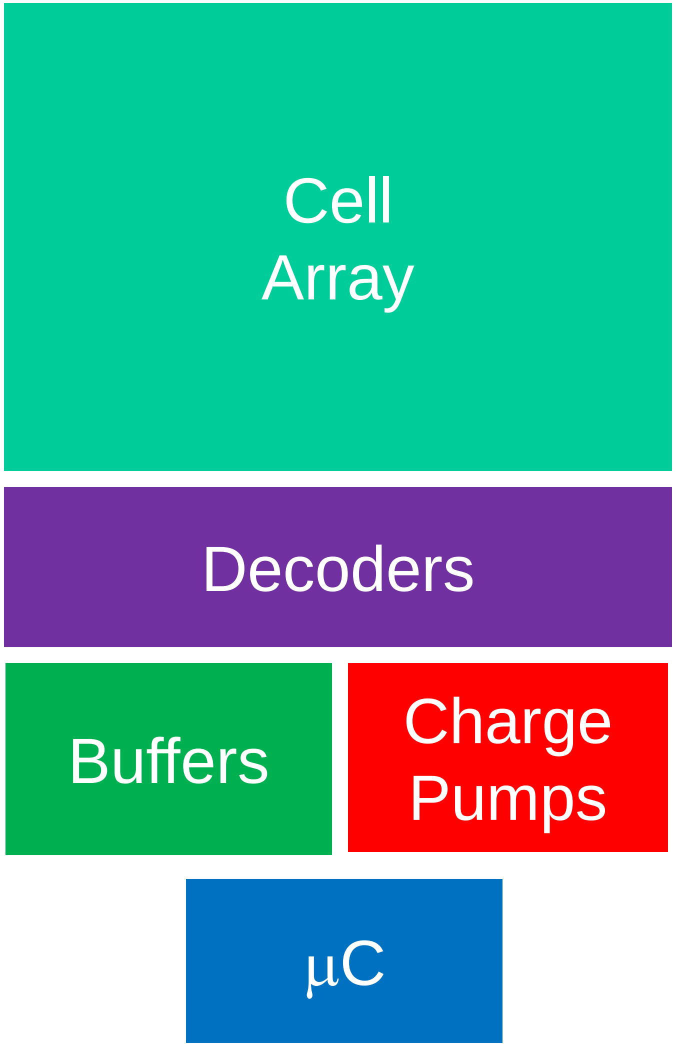
Threshold Voltage Distributions



Typical V_{th} distributions of single-level cell Flash

- V_{th} distributions are typically gaussian
- Programmed and erased peaks are separated by the reference voltage
- Distributions are **not visible to the end-user**, only digital values

Peripheral Circuitry



- Row and Column **Decoders**: block/page/cell selection
- **Charge pumps**: provide high voltages that are needed to program and erase FG cells (e.g., Fowler Nordheim injection)
- **Buffers**: temporarily store the content of the memory before/after program/read
- **Microcontroller**: executes complex program and erase algorithms

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Irradiation Details

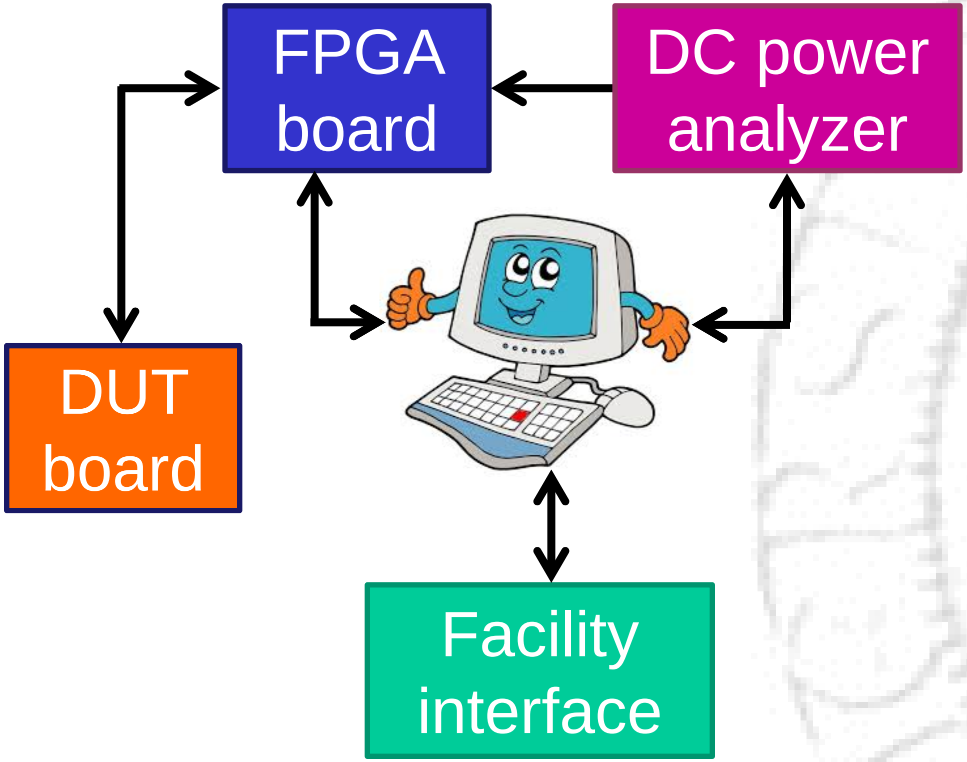
- Microbeam heavy-ion tests
  - GSI Microprobe, Darmstadt (Germany)

Ion Species	Energy [MeV]	Surface LET [MeV cm^2/mg]	Beam type
Au	379.2 MeV	94	Microbeam (max 432 x 342 μm^2)
Ti	133.1 MeV	17.4	Microbeam (max 675 x 559 μm^2)

- Broadbeam and collimated beam heavy-ion tests
  - Laboratori Nazionali di Legnaro (LNL), Padova (Italy)

Ion Species	Energy [MeV]	Surface LET [MeV cm^2/mg]	Beam type
I	266.7 MeV	59.2	Broad (3 x 3 cm^2) and collimated (Ø 1 mm)
Cl	171 MeV	12.5	Broad (3 x 3 cm^2)

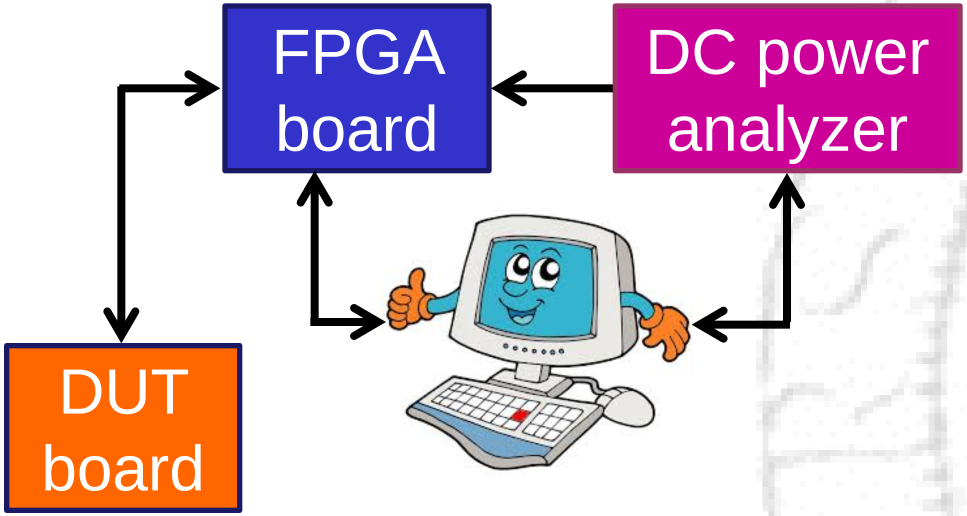
Experimental set-up at GSI microprobe



- FPGA motherboard controlled by PC and daughterboard with an open-top socket, where the DUT is placed for irradiation
- Connection between the two boards through a high-speed connectors and a ribbon cable
- Supply current drawn by the DUT monitored through a DC power analyzer

- Additional FPGA board to interface with the facility and synchronize the ion strikes with the memory operations
  - ☐ The board issued hit requests, sent a run number, and it recorded hit acknowledgments supplied by the facility acquisition hardware

Experimental set-up at LNL



FPGA board

DC power analyzer

DUT board

- FPGA motherboard controlled by PC and daughterboard with an open-top socket, where the DUT is placed for irradiation
- Supply current drawn by the DUT monitored through a fast DC power analyzer

DUT conditions during irradiation

- During irradiation at GSI and LNL a part of the memory was exercised with Erase/Read/Program/Read loops or Erase/Program loops at maximum speed
- At LNL the DUT was also irradiated in unbiased conditions
- After each Erase, Program, and Read operation, different parameters/signals were monitored:
  - Status Register (SR) signals if Erase and Program operations are successfully performed
  - Ready Busy (RB) is a device output indicating if the memory is busy (active) or is ready to accept new commands (inactive)
- After each irradiation run the memory was checked with Erase/Read/Program/Read loops

Irradiation procedure at GSI microprobe

- Two different modes were used for the microprobe tests
  - First we performed a **coarse scan** on the peripheral circuitry: beam with maximum size and the motorized sample holder was used to move the DUT and irradiate the whole area
    - **Goal**: identify possible areas sensitive to destructive events
    - At each position, a given ion fluence was delivered and then the memory functionality was tested. If a functional interrupt was detected, the beam was stopped, the DUT was powered-off and then checked
  - Afterwards, ions were delivered one by one, i.e. **fine scan** on the sensitive spots identified during the previous phase
    - **Goal**: check if destructive events are due to a single ion or if they result from an accumulation of consecutive events
    - After each strike the memory was tested and power-cycled

Irradiation procedure at LNL

Irradiate up to a given fluence (~10^6) and measure the current

Stop the beam

Functionality test

- Two different modes were used for the microprobe tests
  - Irradiations with heavy-ion broad-beam 3x3 cm
  - Irradiations using a collimated beam with a 1-mm diameter
  - In addition to E/R/P/R loops, irradiation were performed also on unbiased memory
    - **Goal**: check if destructive events may originate from FG cells (reference cells used to compare V_{th} during read operation)

Device Details

- NAND Flash memories with SLC architecture
  - Vendor: Micron Technology
  - Part number: MT29F32G08ABAAA
  - Technology node: 25 nm
  - Density: 32 Gbit
  - Package: 48-pin TSOP
  - Supply voltage 2.7 - 3.6 V
  - Operating temperature: 0°C to +70°C
- In total
  - 8 samples were irradiated at GSI microprobe
  - 5 samples were irradiated at LNL with collimated beam
  - 4 samples were irradiated at LNL with broad beam

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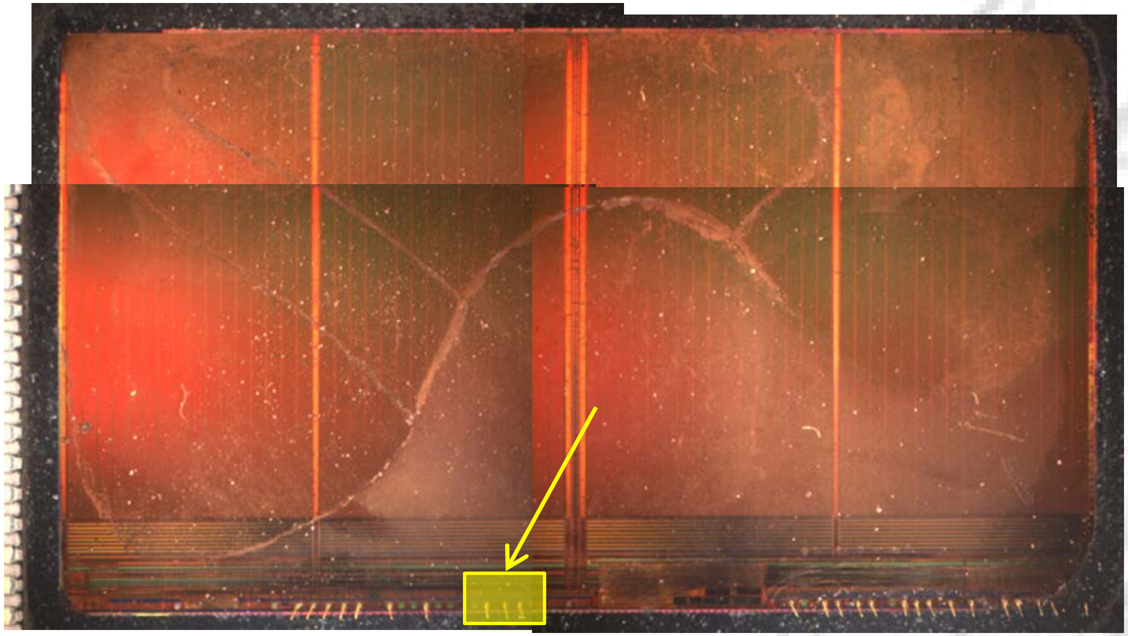
Types of SEEs

- Three different types of **single event effects** were observed during the test runs with the GSI microprobe
  1) Failure to erase one or more blocks
  2) Complete failure to operate the memory
  3) Failure to program one or more pages

1) Failure to Erase one or more blocks

- The memory was unable to erase 10 blocks, belonging to four different groups of adjacent addresses
- This effect was observed **on only one sample** during a **coarse scan** with **Au ions** (LET = 94 MeV·mg^{-1}·cm^2), and could not be reproduced on other samples and with the other ions at lower LET
- The sample was continuously operated with E/R/P/R loops and several 432 x 342 μm areas of the peripheral circuitry were irradiated with 1000 ions each (equivalent fluence 7·10^5 cm^{-2}), before the 'failure to Erase' was observed
- During the scan, numerous SEFIs, recoverable with power cycles, were observed

Strike location for Erase failure



- Erase failure occurred after striking the area close to the power supply pad of the memory

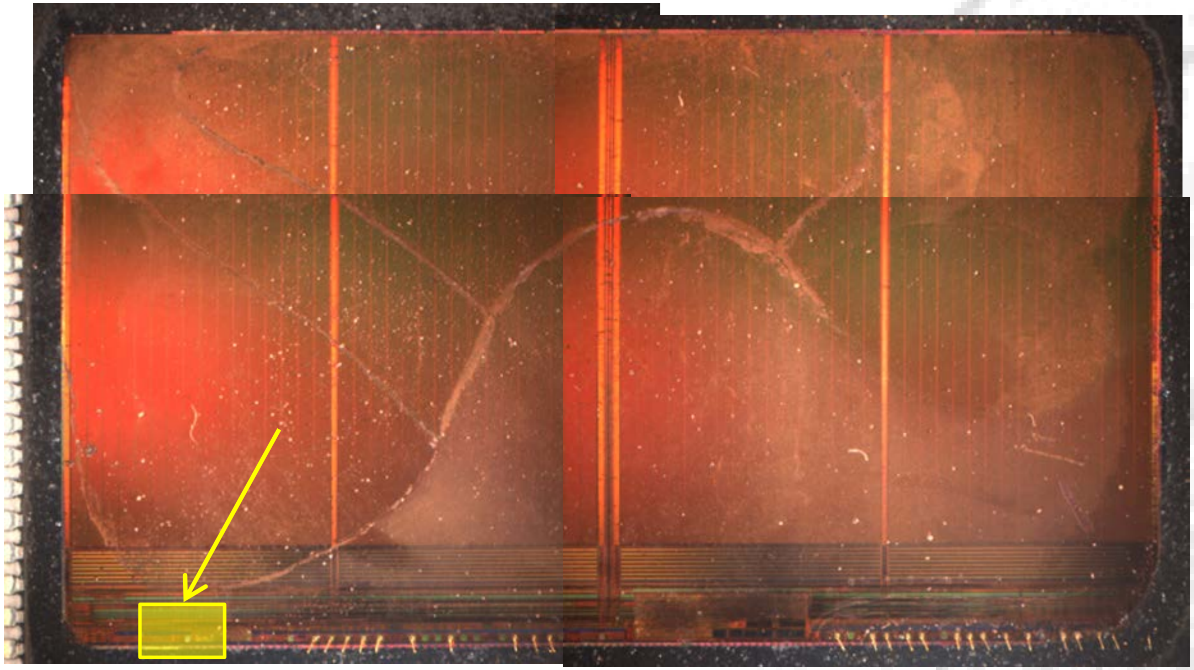
- The event occurred after about 42 ion strikes on the shot area ($3 \cdot 10^4$ ions/cm^2)
- Possible explanation: ‘unlucky’ accumulation of events and/or multiple strikes
  - The sample was irradiated multiple times before observing the failure
  - The effect could not be reproduced in other samples irradiated on the same area and its vicinity

2) Complete failure to operate the memory

- After this kind of failure (complete failure) no operation could be carried out (not even readout of the ID code and the SR)
- This effect was observed on 3 different memories only with Au (LET = 94 MeV·mg^{-1}·cm^{2}), but not with Ti (LET = 17.4 MeV·mg^{-1}·cm^{2}) both in large-scan (after 1.6·10^{5} ions/cm^{2}) and fine-scan mode (after 37 ions and after 298 ions, respectively)
- The device cross section results:

$$\sigma_{DEVICE} = \frac{\#events}{fluence} = 7.8 \cdot 10^{-6} cm^{-2}$$

Strike location for complete failure



- In all 3 samples, the 'complete failure' occurred after striking the area of the microcontroller

- The likely reason for this full loss of functionality is the corruption of the embedded microcontroller firmware
- This effect is clearly due to a single ion hit

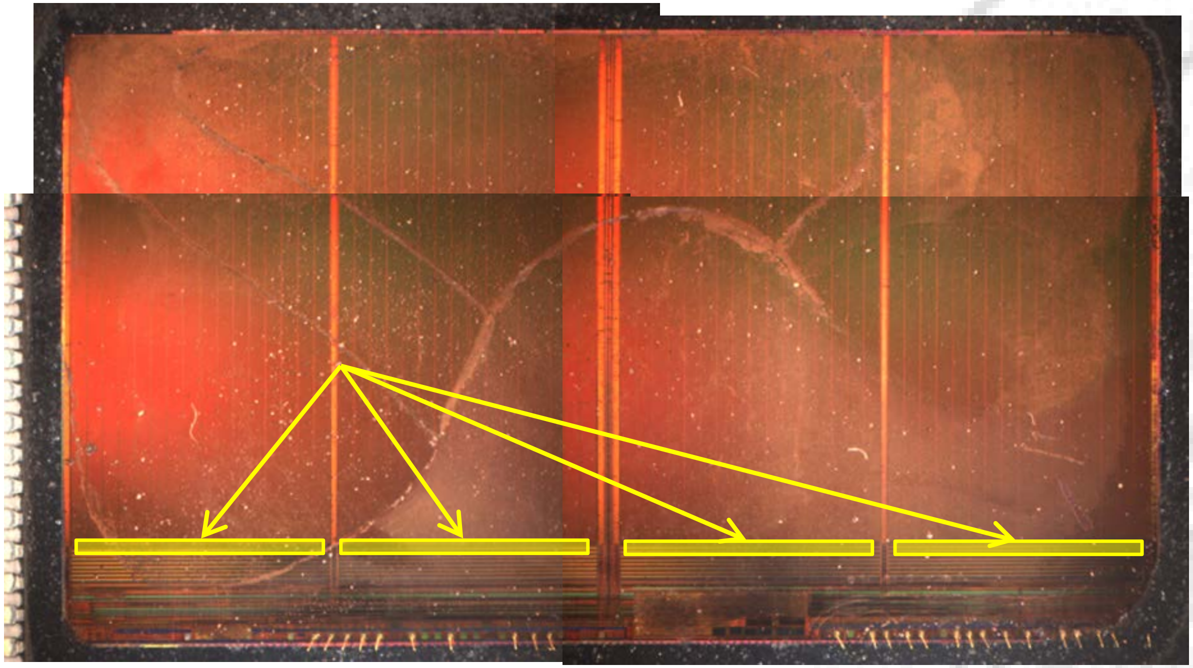
3) Failure to program one or more pages

- The status register after Program operation in failed page was wrong (0xE1), even though a Read on the affected pages showed that the correct values were stored
- This effect was observed with both Au (LET = 94 MeV·mg^{-1}·cm^{2}), and with Ti (LET = 17.4 MeV·mg^{-1}·cm^{2}) and it was experienced by 4 different memories in large-scan mode (after 1.6·10^{5} ions/cm^{2})
- The threshold LET is lower than 17.4 MeV mg^{-1} cm^{2}
- The page cross section (number of failed pages divided by the number of programmed pages) is

$$\sigma_{PAGE} = \frac{\#\, page\ program\ fails}{fluence \cdot \#\, exercised\ \ pages} = 8.4 \cdot 10^{-10}\, cm^{-2}$$

- The device cross section can be obtained multiplying σ_{PAGE} times the number of pages (524288) → σ_{DEVICE} = 4.4 ·10^{-4} cm^{-2}

Strike location for program failure



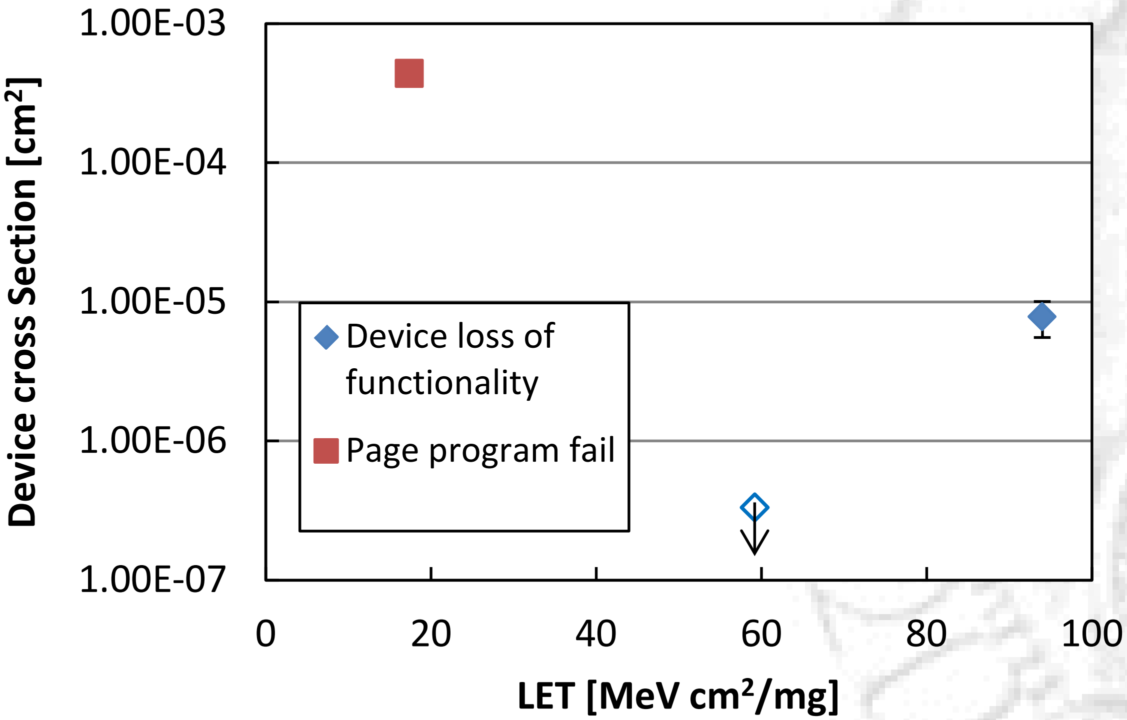
- In all 4 samples, the program failure occurred after striking one of the four areas highlighted in yellow (page buffer/sense amplifier)

- Possible explanation: leakage current in sense amplifier transistors?
- The exact origin of this kind of effect if not fully clear yet and it needs further investigations

Results of broad-beam irradiations at LNL

- Out of the 3 types of effects observed during the GSI microprobe sessions, only the program page fails were recorded at LNL
  - Both using a broad beam (3 x 3 cm^2) and a round collimated beam with a diameter of 1 mm
  - These effects were observed even in unbiased memories
- No ‘complete failures’ were observed at LNL, meaning that the threshold LET is higher than 59.2 $MeV·mg^{-1}· cm^2$ (maximum available at LNL)

Permanent SEEs cross sections



- The cross section for page program fails is higher than for device complete failure
- For erase failures (events #1) it is not meaningful to plot σ (only 1 event due to ion accumulation during multiple runs)

- *Open symbol shows the observability limit*
- *When not present, error bars are smaller than symbols*

Post-irradiation annealing

- All irradiated samples were annealed after exposure for one week at room temperature and for one additional week at 100°C with unbiased samples (shorted pins)
- None of the tested samples fully recovered functionality
- Only small changes in the memory behavior were observed after the annealing process:
  - Sample showing effect 1 (failure to Erase): the number of blocks failing to Erase increased after annealing
  - Samples showing effect 2 (complete failure): no change at all was observed after annealing (device still unable to read ID, etc.)
  - Samples showing effect 3 (failure to Program): the number of pages that could not be programmed decreased after annealing and some new pages failing to program showed up (intermittent behavior)

Conclusions

- Three kinds of destructive effects were observed
  1) Failure to erase one or more blocks
     - Observed only on one sample and at the highest LET
     - Originated close to the power supply pad of the memory
     - Likely due to unlucky accumulation of events from multiple runs
  2) Complete failure to operate the memory
     - Threshold LET located between 59 and 94 MeV·mg^{-1}·cm^{2}
     - Due to the corruption of the embedded microcontroller firmware
     - Destructive event with possible severe implications for use in space
  3) Failure to program one or more pages
     - Threshold LET lower than 17 MeV·mg^{-1}·cm^{2}
     - May occur even with unpowered devices
     - Origin needs further investigation
- None of the effects was seen to recover after annealing

Acknowledgments

- We wolud like to gratefully thank Kai Grürmann, for his precious help and useful discussions before, during, and after the test campaigns
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