Advanced Techniques for Radiation Characterization of ProASIC3 FPGAs

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CNES/ESA Radiation Effects Final Presentation Days 2015
CLS – Toulouse - 10-MAR-2015

Funded under ESA Contract : 4000107761/13/NL/CL / CCN2

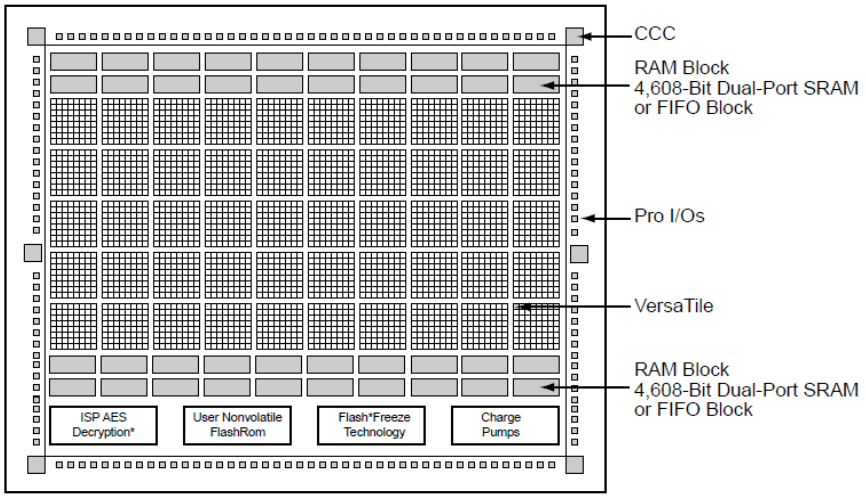
Outline

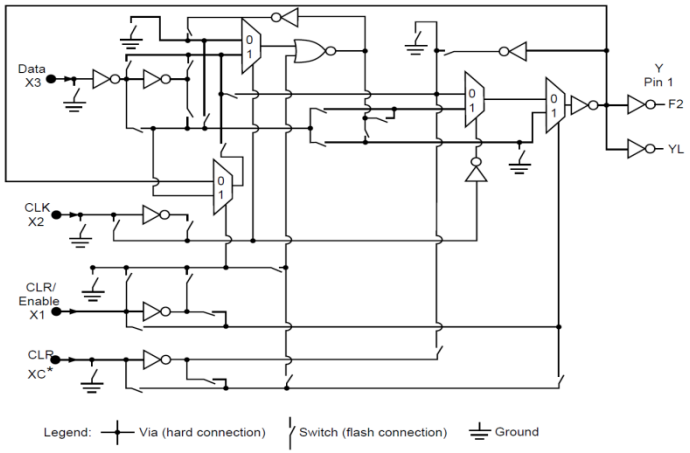
- Background on ProASIC3 FPGAs
- GSI Heavy-Ion Micro Beam Facility
- RAMs and Flip-Flops
- PLLs
- Conclusion

Background on ProASIC3 FPGAs

MicroSemi ProASIC 3L

	A3PE3000L
Core Voltage (V)	1.2 .. 1.5
Technology	130nm, 7ML
VeraTiles	75 264
4608 bit BRAMS	112
CCC (including PLL)	6
VersaNet Globals	18





One VersaTile can implement:

- Any 3 input combinatorial function
- A DFF or latch with options for preset, clear, enable
- Configuration is controlled by floating gate switch

SEE and Dose Extensively Studied

- C. Poivey, M. Grandjean, and F. X. Guerre, “Radiation characterization of microsemi proasic3 flash fpga family,” in Radiation Effects Data Workshop (REDW), 2011 IEEE, 2011.
- M. Berg, K. LaBel, H. Kim, M. Friendlich, A. Phan, and C. Perez, “A comprehensive methodology for complex field programmable gate array single event effects test and evaluation,” TNS, vol. 56, no. 2, 2009.

SEUs

- L. Sterpone, N. Battezzati, and V. Ferlet-Cavrois, “Analysis of set propagation in flash-based fpgas by means of electrical pulse injection,” Nuclear Science, IEEE Transactions on, vol. 57, no. 4, Aug 2010.
- A. Evans, D. Alexandrescu, V. Ferlet-Cavrois, M. Nicolaidis, "New Techniques for SET Sensitivity and Propagation Measurement in Flash-Based FPGAs," TNS, vol.61, no.6, Dec. 2014.

SETs

- L. Sterpone, N. Battezzati, and V. Ferlet-Cavrois, “Analysis of set propagation in flash-based fpgas by means of electrical pulse injection,” TNS, vol. 57, no 4, Aug 2010.
- L. Sterpone, N. Battezzati, F. Kastensmidt, and R. Chipana, “An analytical model of the propagation induced pulse broadening effects on SETs in flash-based fpgas,” TNS, vol. 58, no. 5, Oct 2011.

Pulse Broadening

- Micro Semi. Total Ionizing Dose Test Report. No. 11T-RT3PE3000L-CG484-QJA2G. February 2011.

Dose

- Radiation effects in ProASIC3 devices have been extensively studied !!
- New contributions :
  1. Micro beam study showing sensitive regions
  2. Image enhancement techniques for regular structures
  3. In-depth study of effects on PLLs

Device Under Study : A3P3000L

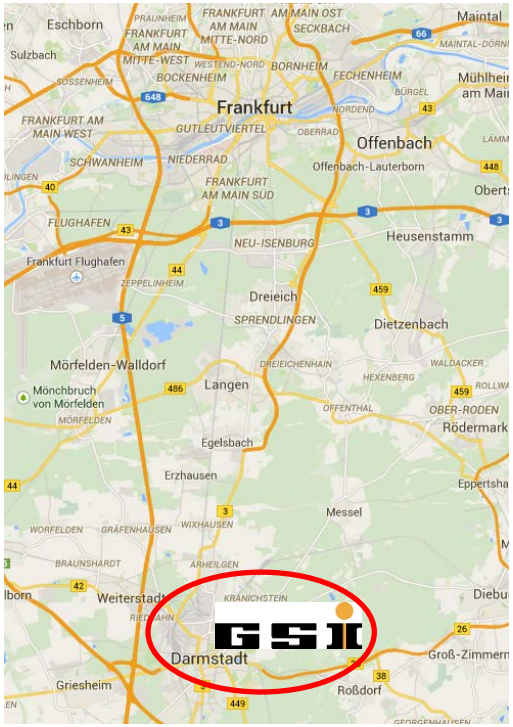
Opened A3P3000L

A3P3000L	
Number VersaTiles	75 264
Number RAMs (4608 bits)	504
Package	PQ208
PLL / CCC	2 / 6

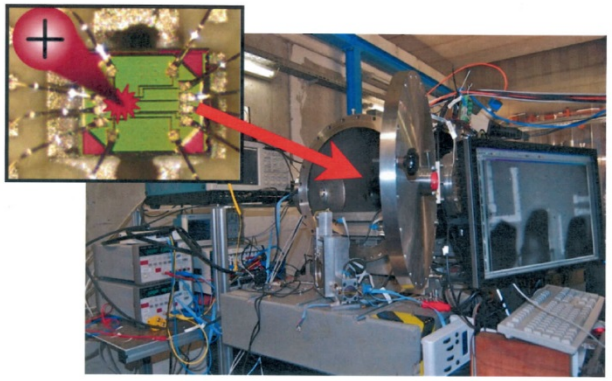
- Top-side opened by laser decapsulation, mechanical wet chemical finishing, coating removal, non-abrasive cleaner

GSI Heavy Ion Micro Beam Facility

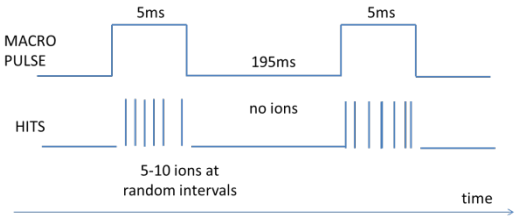
GSI Micro Beam Facility



- Helmholtzzentrum für Schwerionenforschung
- Located in Darmstadt (south of Frankfurt)



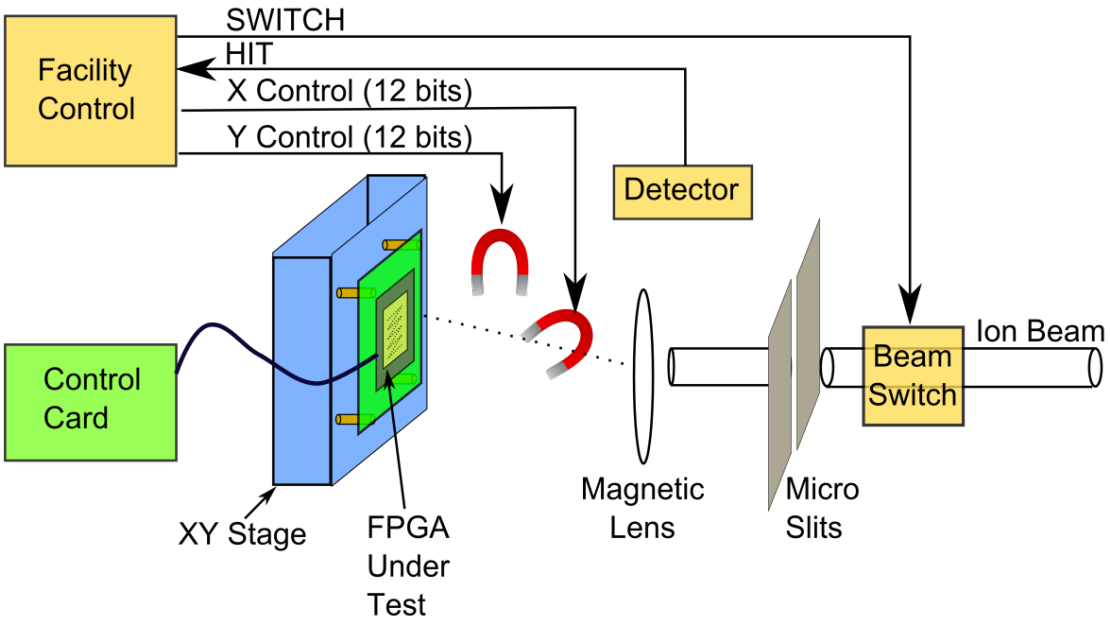
Vacuum Chamber



Temporal Beam Structure

- Ions are accelerated in linear accelerator (UNILAC) – up to 11.4 MeV/µm
- Burst of ≈10 ions arrive every 200 msecs
- Tests performed with 2 ions : Au (94 MeV∘cm^2/mg), Ti (19 MeV∘cm^2/mg)
- Beam resolution is ≈500 nm (≈90% probability radius)

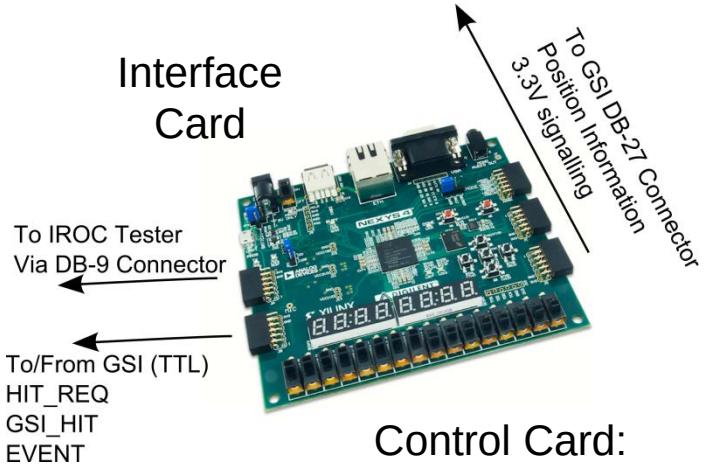
Experimental Setup



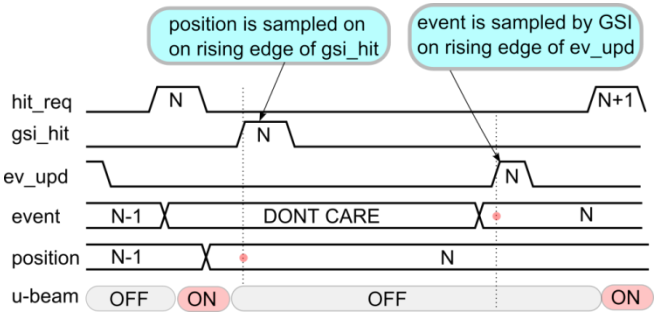
Test Iteration
1. Reset DUT
2. Open beam switch
3. Detect one ion
4. Close beam switch
5. Query DUT

- Individual ions targeted at specific locations on the die by X,Y magnets (12-bit resolution)
- After each ion is fired, the response on the DUT must be queried
- Control card performs hand-shaking between facility and DUT

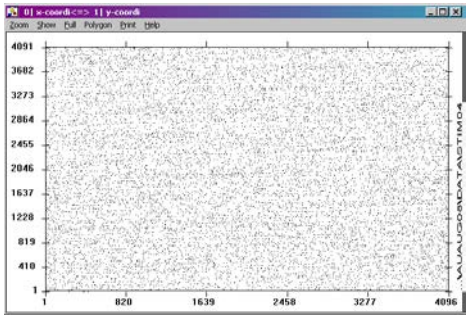
Synchronization Scan Pattern



Control Card:
Digilent Nexys 4
Xilinx Artix-7



Hand Shaking
with GSI Facility



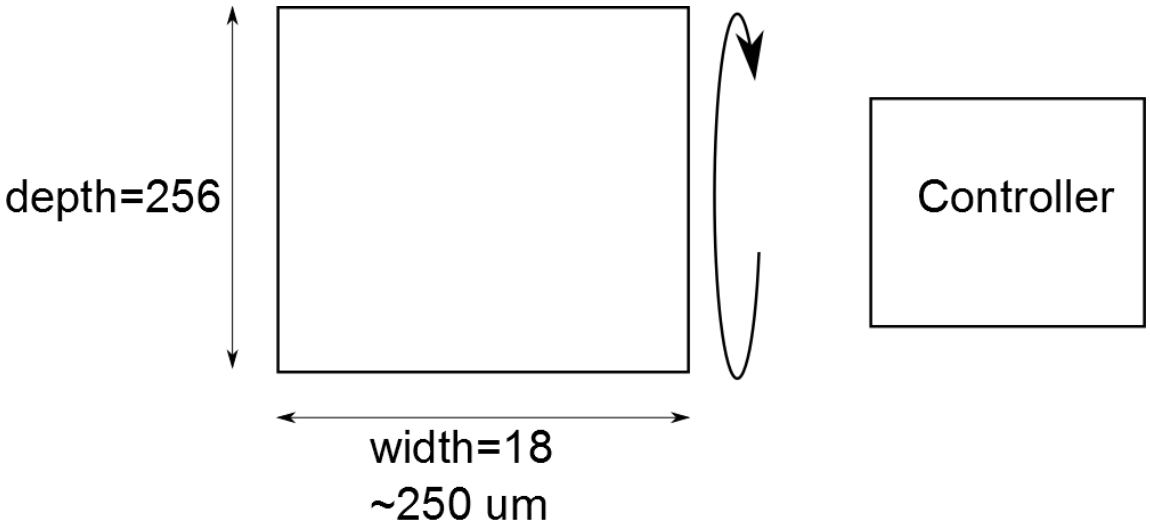
Free Running
Scan Mode

- Custom control card used to:
  - Reset DUT
  - Request an ion
  - Wait for ion to be detected
  - Record X,Y co-ordinates from facility
  - Query whether error detected in DUT

- Scan region
  - 16 µm x 16 µm
  - 48 µm x 48 µm
  - 144 µm x 144 µm
  - 432 µm x 432 µm
- Free running mode
  - Co-ordinates are “random”
  - Image progressively filled in

RAMs and Flip-Flops

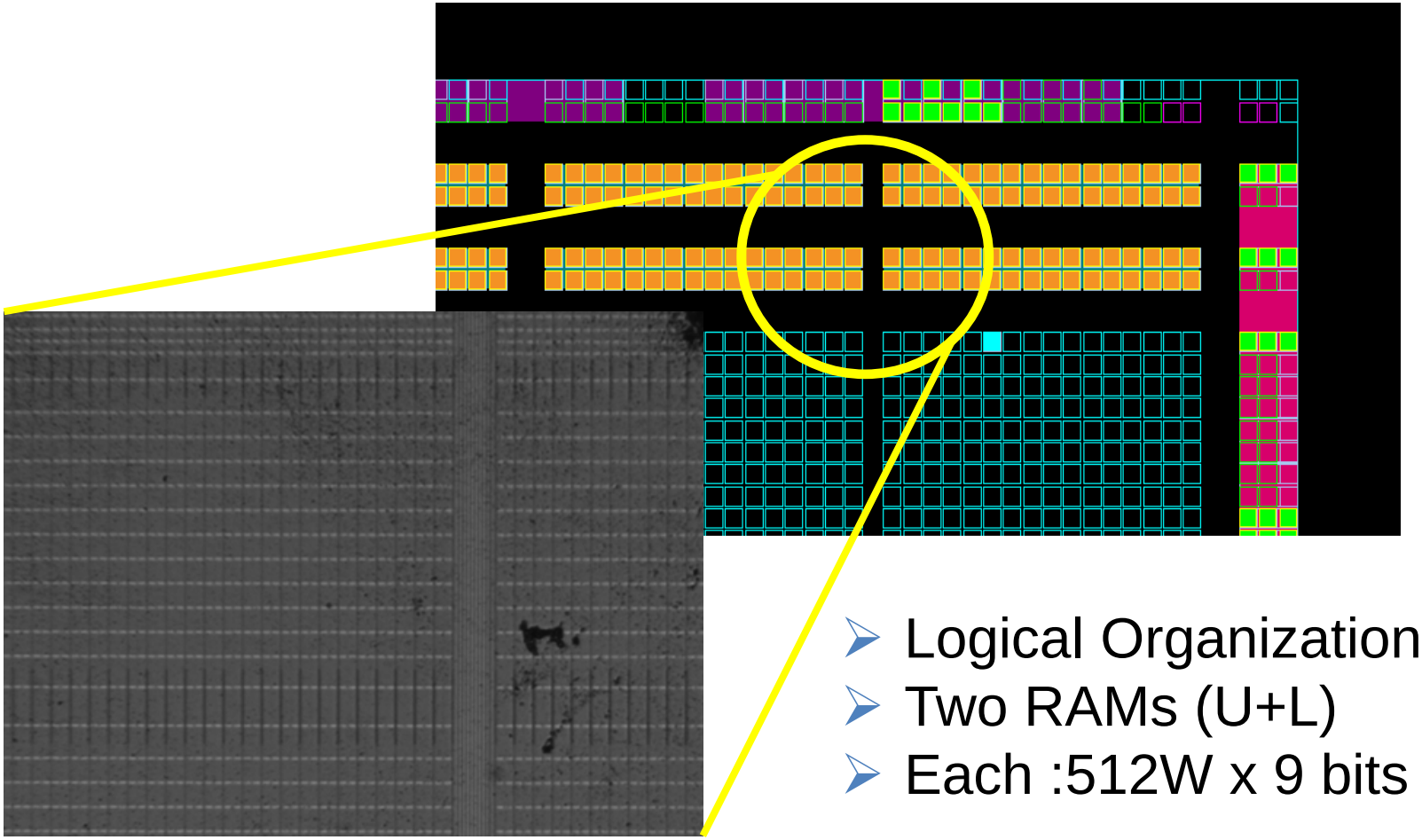
RAM / Flip-Flop Test Flow



Test Sequence

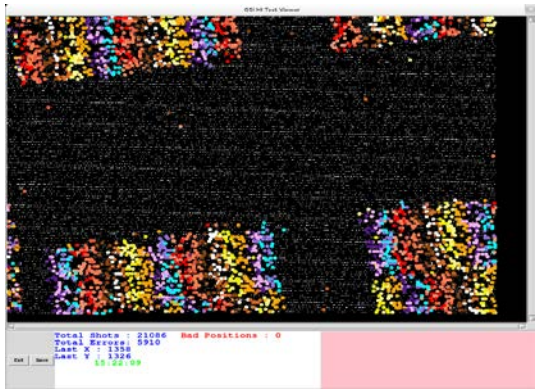
1. Write pattern into memory. (~1.3 usec).
2. Read back pattern from memory + check. (~1.3 usec).
3. Wait for ions. (Handshaking).
4. Read back pattern from memory. (~1.3 usec). -> Report errors (macro, addr, bit)
5. Read back pattern from memory. (~1.3 usec). -> Report errors (macro, addr, bit)

Imaging of BRAM (1)

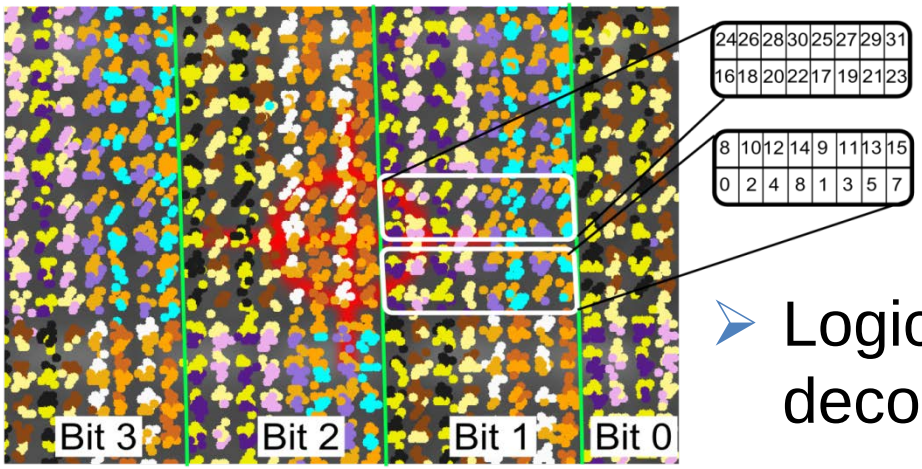


- Logical Organization:
- Two RAMs (U+L)
- Each :512W x 9 bits

Imaging of BRAM (2)



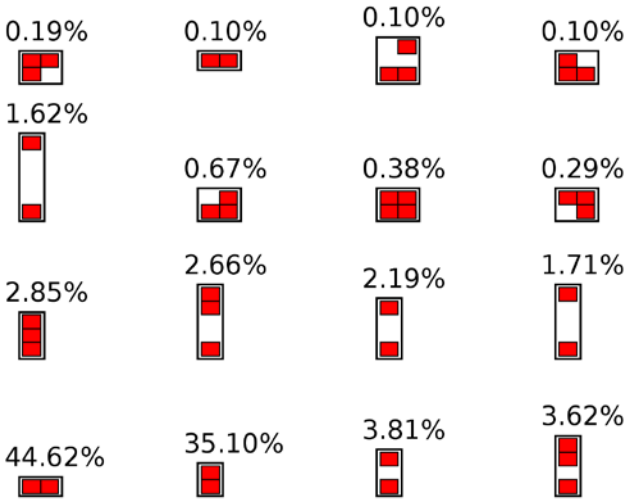
- Each colour dot represents an ion that produced a bit upset
- Colours assigned so each logical bit has unique colour
- Image is rotated versus optical image



BRAM (Ti ions – 17 MeVcm^2/mg)
48 µm x 38 µm

- Logical ⇔ Physical mapping can be decoded

MCU Patterns



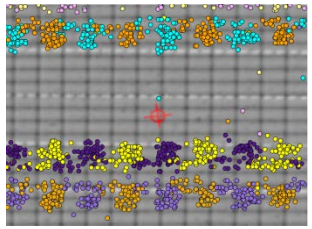
MCU Patterns
(Ti ions – 17 MeVcm^2/mg)

- Many ions produced MCUs
- Exact patterns extracted
- No MBUs observed
  (>=2 bits in same word)

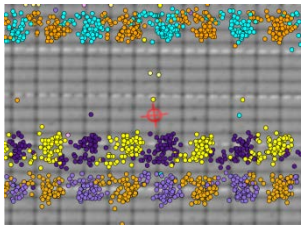
LET MeV◦cm2 /mg	Error %	SBU %	MCU2 %	MCU3 %	MCU4 %	MCU5 %	MCU6+ %
94 (Au)	79	52.6	16.8	5.13	3.58	0.6	0.23
17 (Ti)	35	29.2	5.1	0.66	0.02	0.02	0

Extent of MCUs (ratio versus number of ions fired)

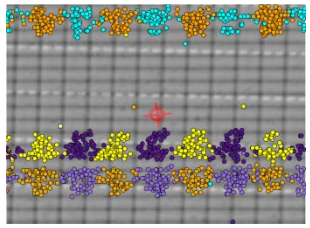
Imaging of Flip-Flops / Latches



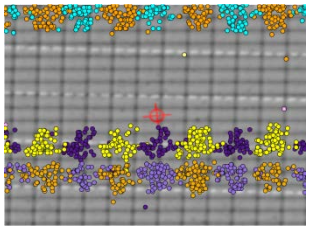
FF @ 0



FF @ 1



Latch @ 0



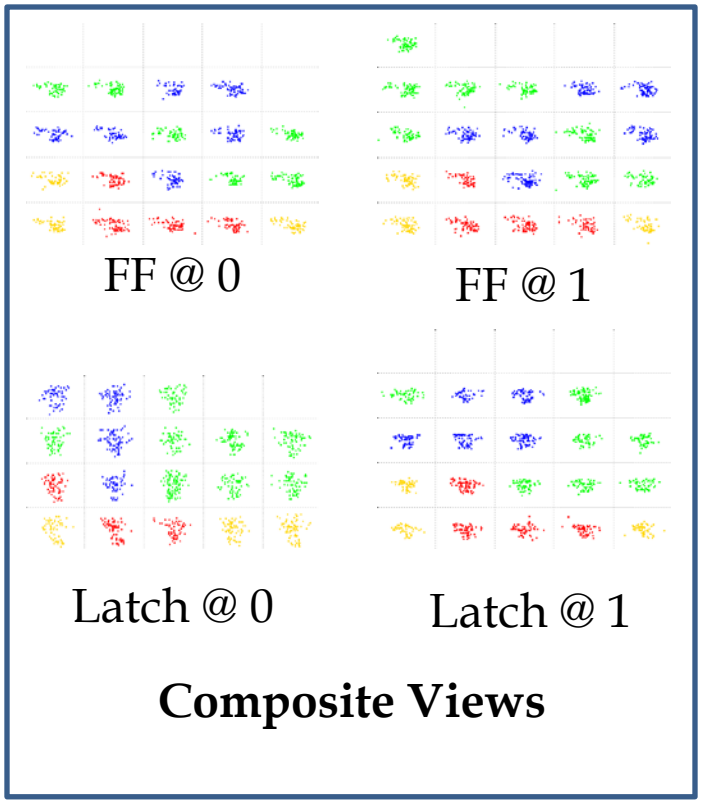
Latch @ 1

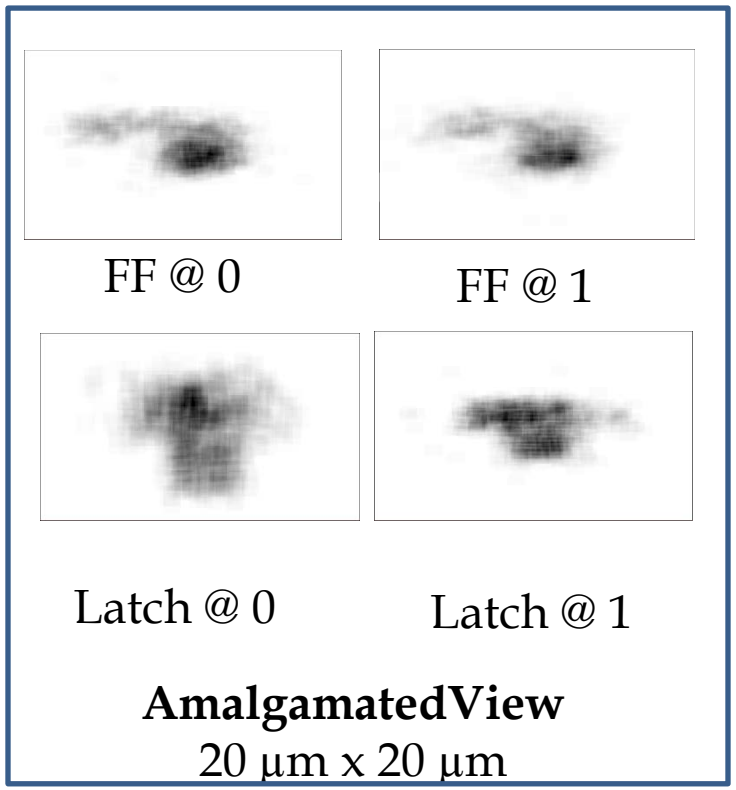
144 µm x 114 µm
FF and Latch
Au Ions (94 MeV◦cm2 /mg)

	Local CS (cm^2) Au ions 94 MeV◦cm2 /mg	Local CS (cm^2) Ti ions 19 MeV◦cm2 /mg
FF @ 0	9.03 e-6	2.58 e-6
FF @ 1	9.52 e-6	2.59 e-6
Latch @ 0	9.35 e-6	2.23 e-6
Latch @ 1	8.86 e-6	1.95 e-6

- Flip-flops, latches in arrays
- Sensitivity mapped storing 0,1
- Sensitive region is localized
- Local CS calculated as ratio of upsets to scanned area

Image Enhancement



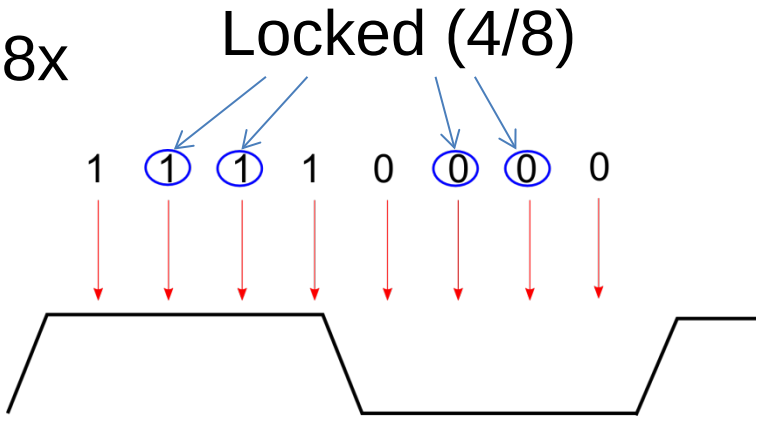


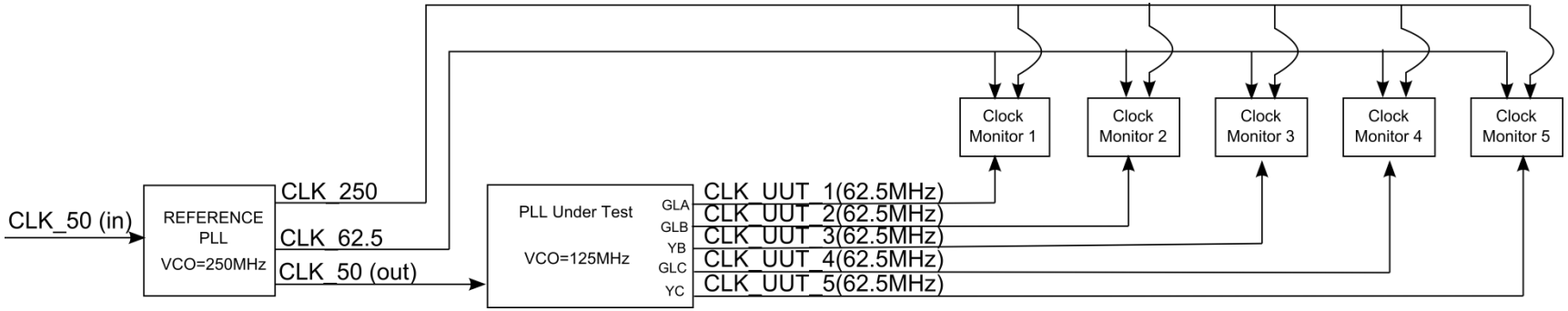
- Co-ordinates of each ion extracted to make a *composite* view for each logical bit position
- *Composite* images superimposed to build *amalgamated* view
- Increased spatial resolution of a single cell

PLLs

PLL Test Flow (On Chip Monitoring)

- Basic idea : sample CLK_UUT at 8x
- At power-up, each sample point “locks” into position
- 4 / 8 sample points “lock”
- Error if locked position moves (e.g. edge moves ≥ 25% cycle)



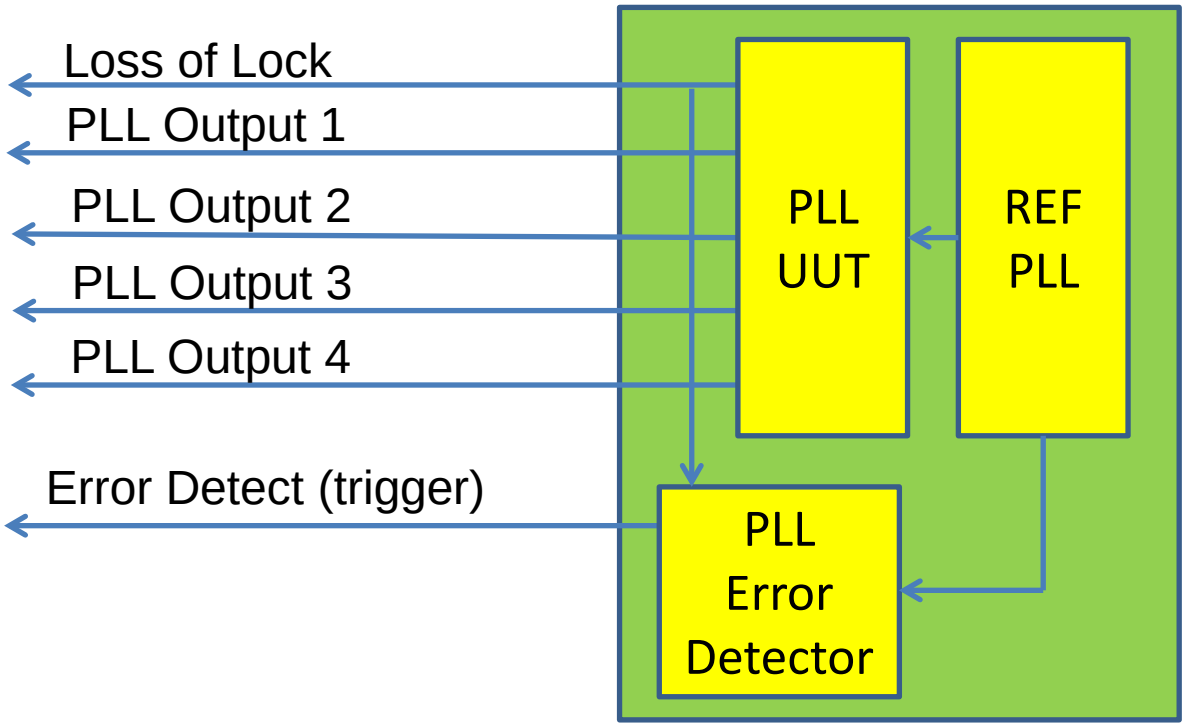


Reference PLL
In : 50 MHz
Out : 50,62.5,250 MHz

PLL Under Test
In : 50 MHz
Output : 5 x (62.5 MHz)

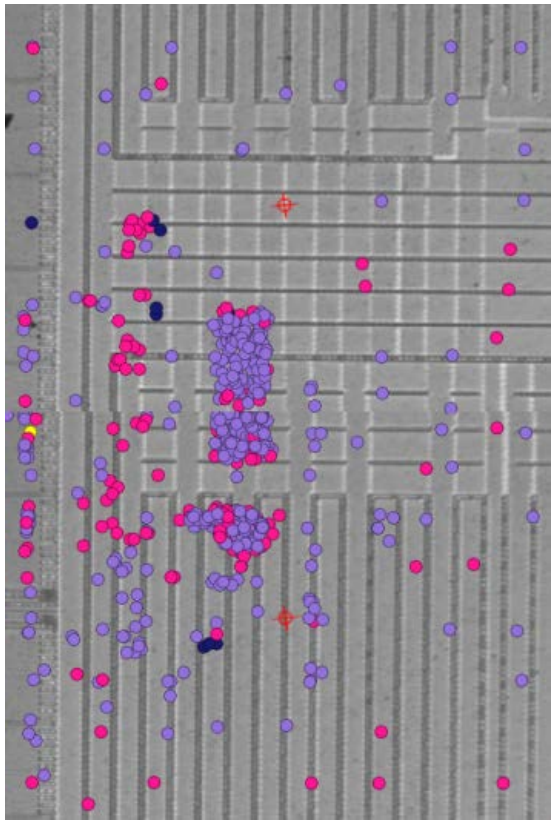
PLL Test Flow (Off Chip Monitoring)

LeCroy
WaveMaster
DSO



- To gain better insight into what is occurring when the PLL “error detector” triggers
- External DSO samples 4 of 5 of the PLL outputs
- Record signal trace if on-chip circuit triggers a PLL error

PLL Sensitivity Map

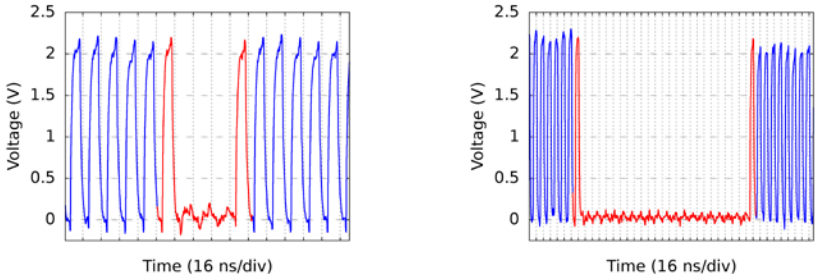


- Events classified based on
  - Did 1-4 or all 5 detectors fire?
  - Did loss of lock fire?

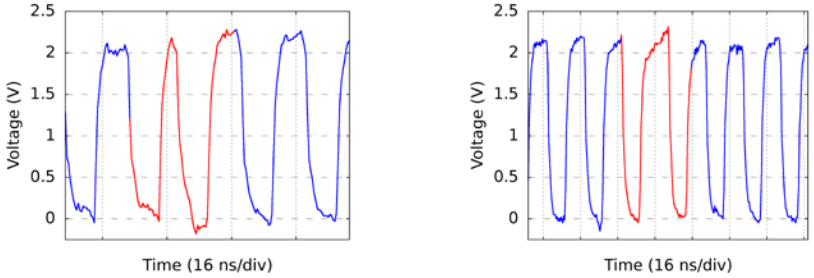
Very few of the real upsets triggered loss of lock (LoL). Can not use LoL for error detection….

PLL Sensitivity Map - 144 µm x 228 µm
(Au Ions 94 MeV∘cm²/mg)
light purple = 5 phase detectors triggered
pink = 1-4 phase detectors triggered
dark blue = loss of lock only
yellow = phase detector and loss of lock

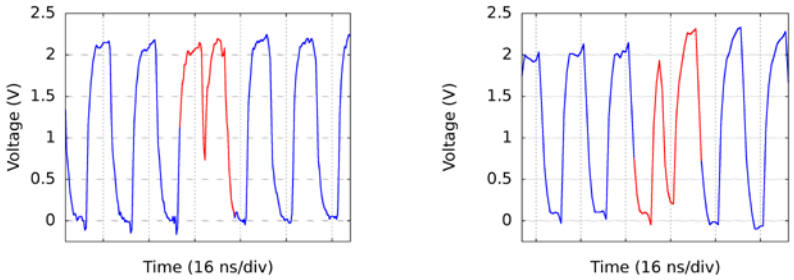
Detailed PLL Effects



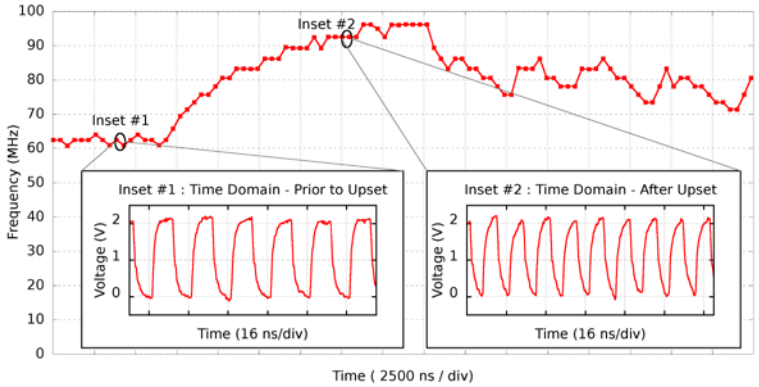
Missing Pulses



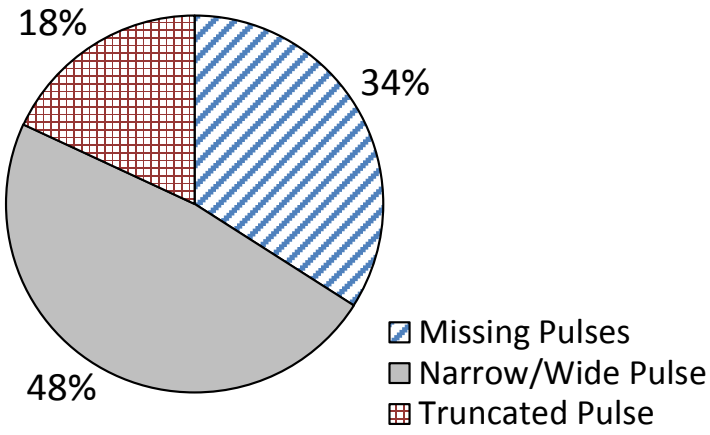
Narrow/Wide Pulses



Truncated Pulses



Temporary Frequency Shift



Conclusions

Conclusions

- HI micro-beam useful for identifying sensitive regions
  - Increased experimental complexity
  - Makes sense early in process/circuit development
- Potential to provide detailed insight
  - For circuit designers – SEE weak spots
  - For soft-error simulation – detailed mapping
- Combining on-chip (detection) and off-chip (capture) techniques for detailed PLL effects analyis
- PLL loss of lock can’t be used for error detection in ProASIC3

Thank You!

Contacts

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