SET Test Vehicle in STMicroelectronics 65nm Technology

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Outline

- Test Chip Goals
- SET Detectors
  - PWMT
  - CREST
  - DSET
- Conclusions
Test Chip Goals
ST’s 65nm Space Technology

- ST’s 65nm technology has been tuned for space applications
- Hardened for dose, SEL and SEE
- Extensively characterized for SEEs under HI, p+ and neutrons [1]
- Multiple test vehicles between 2009-2014
- Rich library offering (RAM, PLL, IO, …)
- Planned for use in NG FPGA and NG MP

However – characterization of SETs has been limited. This is the additional contribution of the SET test vehicle.

Test Chip Goals

- Detailed SET characterization of ST65nm technology
- Cell level study (rate and pulse width)
  - Core65 and SKYROB65
  - Drive strength
  - Cell function
  - Input pattern
  - Supply voltage
  - SEMT – Single Event Multiple Transient
- Study of SETs in “real digital circuits”
- Study pulse broadening effects
- Compare different SET measurement techniques
- Provide a re-usable SET analysis platform

Design Constraints

- Area: $\approx 4\text{mm}^2$
- On-chip high-speed clock generation
- Suitable for HI broad beam testing
  - Adequate cross-section for reasonable event counts
  - Control / multiplexing circuitry must be hardened
- Suitable for pulsed laser testing
  - Sensitive gates must be separated by $\sim 1-2\ \mu\text{m}$ to be individually targeted
  - Physical “markers” to facilitate laser alignment
SET Detectors
- Blocked transistor directly connected to IO pad
- Current monitored with a high speed oscilloscope (through a bias T)
- Several identical transistors connected to each pad to increase the number of events
- Multiple types of transistors (N/P, Width)

On-Chip SET Measurement

Sensor Chain of 256 Gates

Pulse Width Measurement Circuits

- PWMT = Pulse Width Measurement Topology
- Experiments with sensors: chains of gates
- Detector: asynchronous digital circuit to measure pulse width
Incoming pulse propagates down delay line
Pulse also sets off a trigger circuit
Capture latches close and store “snapshot” of SET along delay line

Temporal precision limited to 1 gate delay
Trigger delay is programmable – account for variation and de-risk
Delay line is calibrated using a configurable ring-oscillator (RO)
Pulse is subject to distortion (PIPB) along the delay line
Pulse Filter Detector

- Series of increasing pulse filters: PF1, PF2, …, PF\(n\)
- SETs will trigger the first ‘N’ filters then be blocked
- Linear topology avoids duplicating delay chains
- RO calibration possible with linear topology
- Temporal precision limited to 1 gate delay
Vernier SET Detector

- Based on design from previous work [1,2,3]
- Two latches used to detect SET (rising and falling edge)
  - Leading edge of SET propagates along slow delay line (t1)
  - Trailing edge of SET propagates along fast delay line (t2)
  - Edges across after $N(t_2-t_1)$ stages, corresponding to pulse width

Rise/Fall Time Calibration

- PWMT experiments need on-chip calibration
- Process, Voltage and Temperature (PVT) impact rise/fall times
- N/P MOS variability can involve pulse broadening/narrowing on buffer chains:

In case of fast PMOS and slow NMOS:

- Gate chain are used as Ring Oscillator (RO) to provide on chip calibration

\[
T_{RO} = T_{rise_{Chain}} + T_{fall_{Chain}}
\]

- RO frequency give the sum of rise and fall time of the gate chain
- RO sampled at low frequency to extract duty cycle and dissociate rise and fall time

Measure RO frequency
Measure RO duty cycle

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65nm SET Test Vehicle
Pulse Width Measurement Topology

- One incoming pulse
- Four parallel detectors
  - Small (yes/no)
  - Vernier (≈15 ps resolution)
  - Pulse capture (≈20 ps resolution)
  - Pulse filter (≈40 ps resolution)
- Simultaneous measurement of same event will provide insight into accuracy of detectors
- Advanced delay rise/fall time calibration

Circuit Simulation Result

Layout

- RO divider and sampling
- Output mux
- Pulse filter
- Vernier
- Pulse capture
- Small SET
Much discussion about SEMTs [1,2,3]

Proposed measurement approach

- Multiple logical chains of gates – but physically interleaved
- Each logical chain has its own detector
- A SEMT will be identified by multiple simultaneous logical events
- Multiple experiments to determine horizontal and vertical extent

C-Crest Topology

- Logic is placed between flip-flops and clocked at high speed
- Errors checked at output of shift register
- SEU cross-section measured at low frequency
- SET cross-section increases with frequency due to reduced latch window masking
- Pulse width measurement not possible
- Average pulse width can be inferred from cross-section versus frequency

Dynamic SET Detector

- Mimic the operation of “real” digital circuits
- Pseudo-random input vectors generated by an LFSR
- Triplicated combinatorial circuit
- 3-way output comparison (0 ↔ 1, 1 ↔ 2, 0 ↔ 2)
- SETs cause a two-way mis-match: (011, 110, 101)
- SEUs cause a one-way mis-match: 001, 010, 100

- Three circuits under study: 8-bit adder, 8-bit mag. compare, 16-bit ECC
### On-Chip SET Measurement Techniques

<table>
<thead>
<tr>
<th>Criterion</th>
<th>Elementary Transistors</th>
<th>Pulse Width Measure Topology (PWMT)</th>
<th>Single Event Multiple Transient (SEMT)</th>
<th>Combinational Circuit for Radiation Effect Self Test (C-CREST)</th>
<th>Dynamic complex circuits (DSET)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Objective</strong></td>
<td>Measure SET current</td>
<td>Measure SET pulse width distribution</td>
<td>Characterize SEMT (range, pulse width)</td>
<td>Measure average pulse width</td>
<td>Mimic combinational logic usage</td>
</tr>
<tr>
<td><strong>Measurement</strong></td>
<td>Analog Asynchronous</td>
<td>Digital Asynchronous</td>
<td>Digital Asynchronous</td>
<td>Digital Synchronous</td>
<td>Digital Synchronous</td>
</tr>
<tr>
<td><strong>Measured Masking Effect</strong></td>
<td>None</td>
<td>Electrical</td>
<td>Electrical</td>
<td>Electrical, Temporal</td>
<td>Logical, Electrical, Temporal</td>
</tr>
<tr>
<td><strong>Cost (area/power)</strong></td>
<td>--</td>
<td>-</td>
<td>-</td>
<td>+</td>
<td>++</td>
</tr>
</tbody>
</table>

- **Transistor Level**
- **Gate Level**
- **Gate to Gate Level**
- **Logical Chain Level**
- **Combinational Circuit Level**
Test Chip Top Level

- Tape-out (MPW) : JUN-2015
- Samples : SEP-2015
- HI and Laser testing : SEP..DEC-2015
Conclusions
Conclusions

- Accurate SET characterization is critical for
  - Risk assessment
  - Evaluating mitigation schemes (e.g. double sampling)
- Characterization is complex
  - Cell sensitivity depends on function, input state
  - Masking factors (logical, latch-window, electrical)
  - Pulse broadening effects (PIPB)
- Proposed circuits span the range from transistor level to “real” synchronous digital designs
  - New techniques for accurate on-chip calibration
  - In-depth measurement of SEMT effects
  - Actual SET measurement in active digital circuits
- Test results will provide new insights into best practices for SET test and measurement
Thank You!
Contacts

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          adrian@iroctech.com
Backup Slides
### PWMT experiments

<table>
<thead>
<tr>
<th>ID</th>
<th>Cell</th>
<th>Chain length</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Empty</td>
<td>0</td>
<td>Empty</td>
</tr>
<tr>
<td>1</td>
<td>CORE65LPSVT/HS65_LS_IVX9</td>
<td>512</td>
<td>reference inverter</td>
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<tr>
<td>2</td>
<td>CORE65LPSVT/HS65_LS_IVX4</td>
<td>512</td>
<td>small drive</td>
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<tr>
<td>3</td>
<td>CORE65LPSVT/HS65_LS_IVX18</td>
<td>512</td>
<td>large drive</td>
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<tr>
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<td>CORE65LPSVT/HS65_LS_IVX49</td>
<td>512</td>
<td>very large drive</td>
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<tr>
<td>5</td>
<td>CORE65LPSVT/HS65_LS_BFX9</td>
<td>512</td>
<td>buffer</td>
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<tr>
<td>6</td>
<td>CORE65LPSVT/HS65_LS_BFX49</td>
<td>512</td>
<td>large drive buffer</td>
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<tr>
<td>7</td>
<td>CORE65LPLVT/HS65_LL_IVX9</td>
<td>512</td>
<td>LVT effect</td>
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<td>8</td>
<td>CORE65LPSVT/HS65_LS_NAND2X</td>
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<td>NAND gate</td>
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<td>9</td>
<td>CORE65LPSVT/HS65_LS_NOR2X9</td>
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<td>NOR gate</td>
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<td>AND gate</td>
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<td>MUX gate</td>
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<td>Parity gate</td>
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<td>CORE65LPSVT/HS65_LS_AO22X9</td>
<td>512</td>
<td>AO gate</td>
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<td>16</td>
<td>CORE65LPSVT/HS65_LS_FA1X9</td>
<td>512</td>
<td>Full adder</td>
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<td>17</td>
<td>CORE65LPSVT/HS65_LS_IVX9</td>
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<td>18</td>
<td>SKYROB65LPSVT/SKY65BFX9</td>
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<td>19</td>
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<td>512</td>
<td>SKYROB large buffer</td>
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<tr>
<td>20</td>
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<td>SKYROB LVT buffer</td>
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<td>SKYROB NAND</td>
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<td>SKYROB NOR</td>
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<td>512</td>
<td>SKYROB AND</td>
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<td>SKYROB OR</td>
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<td>25</td>
<td>SKYROB65LPSVT/AO22X9</td>
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<td>SKYROB AO</td>
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<td>SKYROB Parity checker</td>
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<td>27</td>
<td>SKYROB65LPSVT/SKY65BFX9</td>
<td>512</td>
<td>low voltage (with a level shifter)</td>
</tr>
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<tr>
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<td>64</td>
<td>16 bit adder</td>
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<tr>
<td>1</td>
<td>64</td>
<td>16 bit ECC encoder</td>
</tr>
<tr>
<td>2</td>
<td>64</td>
<td>16 bit comparator</td>
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### C-CREST experiments

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<td>64</td>
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</tr>
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<td>1</td>
<td>64</td>
<td>16 bit ECC encoder</td>
</tr>
<tr>
<td>2</td>
<td>64</td>
<td>16 bit comparator</td>
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### C-CREST experiments

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</tr>
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<td>1</td>
<td>64</td>
<td>16 bit ECC encoder</td>
</tr>
<tr>
<td>2</td>
<td>64</td>
<td>16 bit comparator</td>
</tr>
</tbody>
</table>
Estimation of Required HI Fluence

- Heavy-ion beam time estimations based on:
  - 100 events for cross-section measurements
  - 500 events for pulse width distributions (PWMT experiments)
  - Heavy ion test planned at RADEF, with a flux of 1e6 HI/cm²/s
  - 2 dies simultaneously tested

<table>
<thead>
<tr>
<th>Experiment</th>
<th># LET</th>
<th># Pattern</th>
<th># Frequency</th>
<th>Beam time RADEF (h)</th>
<th>Total dose / DUT (rad)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWMT</td>
<td>4</td>
<td>3</td>
<td>-</td>
<td>6.1</td>
<td>2.29E+06</td>
</tr>
<tr>
<td>C-CREST</td>
<td>4</td>
<td>3</td>
<td>4</td>
<td>2.8</td>
<td>1.12E+06</td>
</tr>
<tr>
<td>Dynamic SET (Adder)</td>
<td>4</td>
<td>3</td>
<td>4</td>
<td>1.9</td>
<td>4.92E+05</td>
</tr>
<tr>
<td>Dynamic SET (ECC)</td>
<td>4</td>
<td>3</td>
<td>4</td>
<td>2.3</td>
<td>6.12E+05</td>
</tr>
<tr>
<td>Dynamic SET (magnitude comparator)</td>
<td>4</td>
<td>3</td>
<td>4</td>
<td>13.2</td>
<td>5.93E+06</td>
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</tbody>
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