SET Test Vehicle in STMicroelectronics 65nm Technology

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Outline

- Test Chip Goals
- SET Detectors
  - PWMT
  - CREST
  - DSET
- Conclusions

Test Chip Goals

ST's 65nm Space Technology

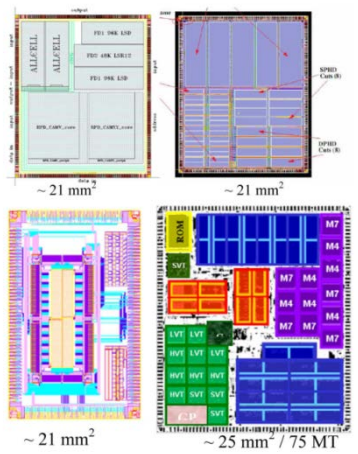


Fig. 2. Floor plans of the four test vehicles designed and manufactured in a 65 nm CMOS technology and then tested at ground level with space radiations.

65nm test chips [1]

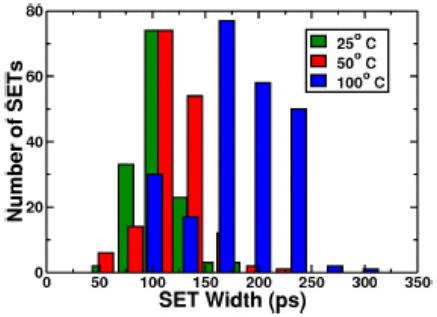
- ST's 65nm technology has been tuned for space applications
- Hardened for dose, SEL and SEE
- Extensively characterized for SEEs under HI, p+ and neutrons [1]
- Multiple test vehicles between 2009-2014
- Rich library offering (RAM, PLL, IO, …)
- Planned for use in NG FPGA and NG MP

However – characterization of SETs has been limited.
This is the additional contribution of the SET test vehicle.

[1] P. Roche, G. Gasiot, S. Uznansk, JM Daveau, et al. *A Commercial 65nm CMOS Technology for Space Applications: Heavy Ion, Proton and Gamma Results and modeling. TNS 2010.*

Test Chip Goals

- Detailed SET characterization of ST65nm technology
- Cell level study (rate and pulse width)
  - Core65 and SKYROB65
  - Drive strength
  - Cell function
  - Input pattern
  - Supply voltage
  - SEMT – Single Event Multiple Transient
- Study of SETs in “real digital circuits”
- Study pulse broadening effects
- Compare different SET measurement techniques
- Provide a re-usable SET analysis platform



SETs in 65nm [1]

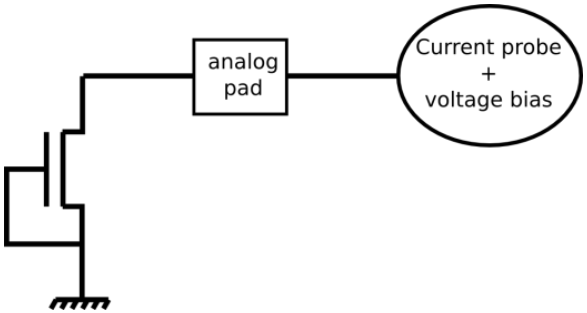
[1] M. J. Gadlage; Single Event Transient Pulse Width Measurements in a 65-nm Bulk CMOS Technology at Elevated Temperatures; IRPS 2010.

Design Constraints

- Area: ≈ 4mm^2
- On-chip high-speed clock generation
- Suitable for HI broad beam testing
  - Adequate cross-section for reasonable event counts
  - Control / multiplexing circuitry must be hardened
- Suitable for pulsed laser testing
  - Sensitive gates must be separated by ~1-2 µm to be individually targeted
  - Physical “markers” to facilitate laser alignment

SET Detectors

Elementary Transistors



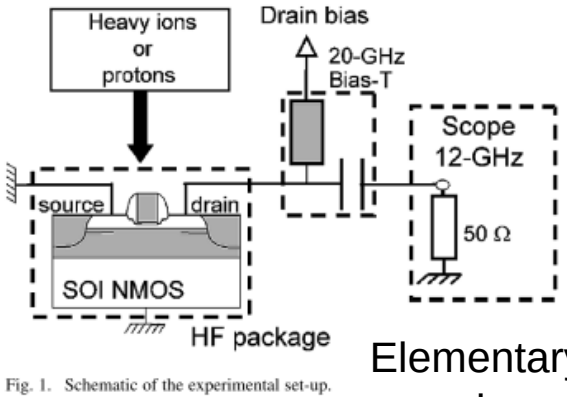


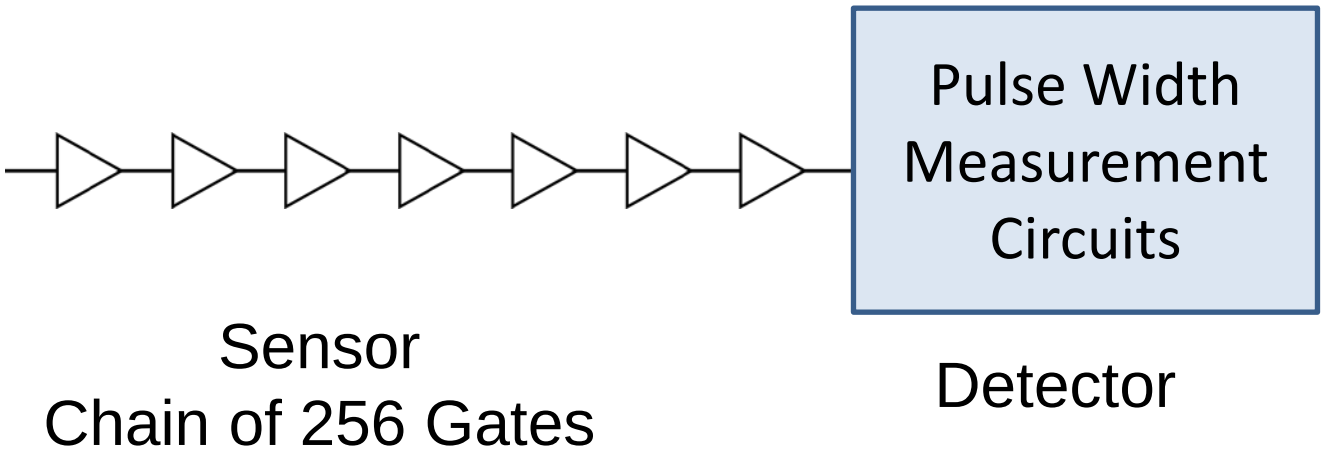
Fig. 1. Schematic of the experimental set-up.

Elementary transistor experimental setup[1]

- Blocked transistor directly connected to IO pad
- Current monitored with a high speed oscilloscope (trough a bias T)
- Several identical transistors connected to each pad to increase the number of events
- Multiple types of transistors (N/P, Width)

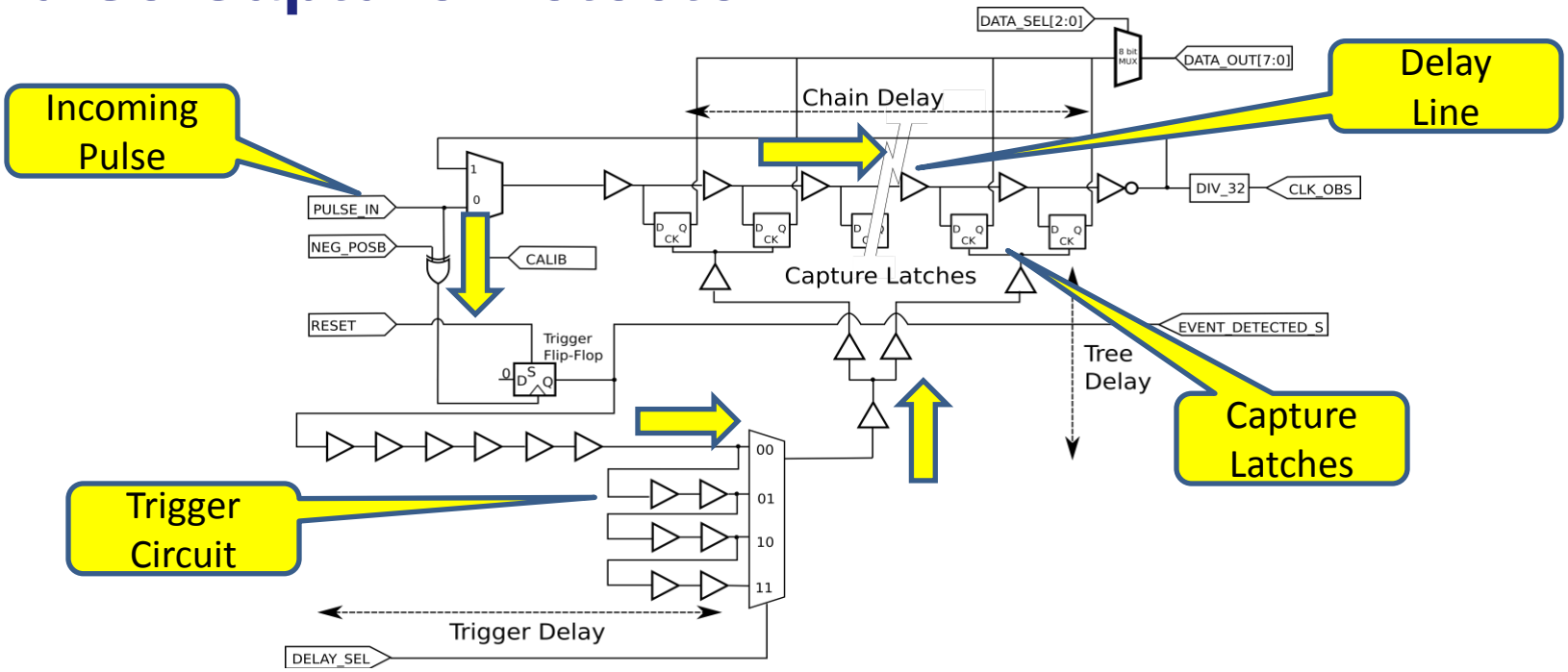
[1] V. Ferlet-Cavrois, *et al*; Statistical Analysis of the Charge Collected in SOI and Bulk Devices Under Heavy Ion and Proton Irradiation – Implications for Digital SETs, TNS 2006.

On-Chip SET Measurement



- PWMT = **P**ulse **W**idth **M**easurement **T**opology
- Experiments with sensors : chains of gates
- Detector : asynchronous digital circuit to measure pulse width

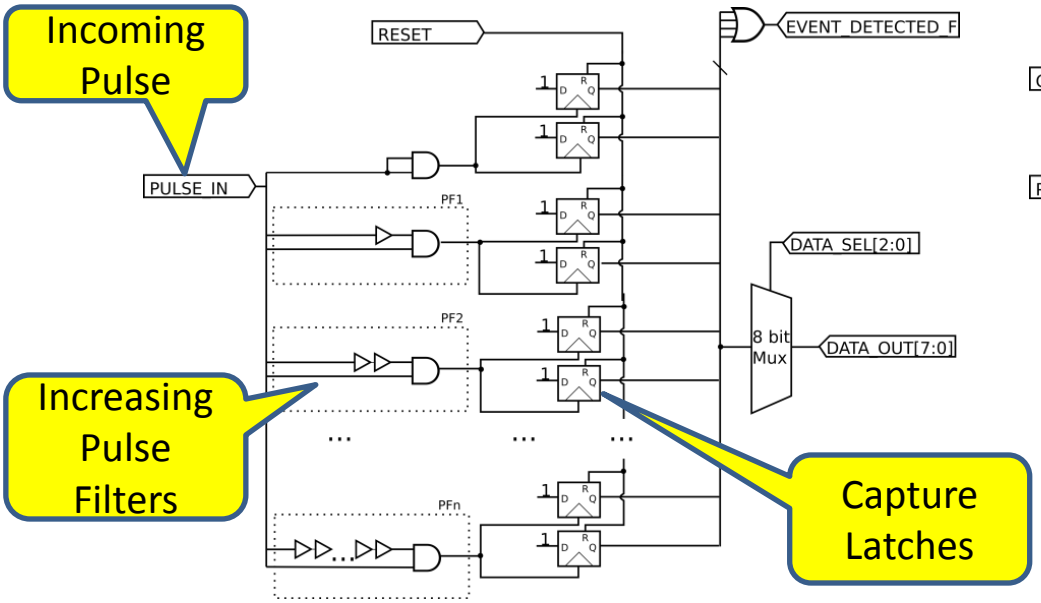
Pulse Capture Detector



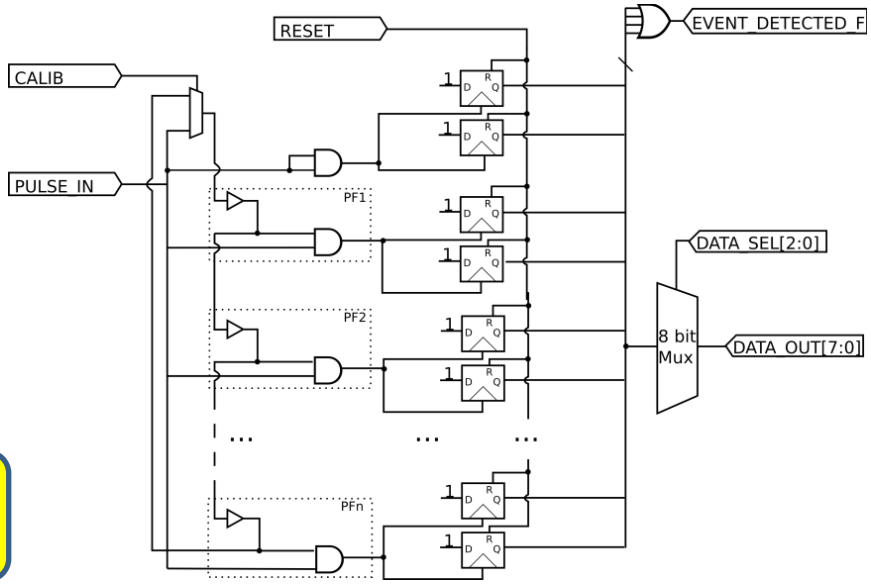
- Incoming pulse propagates down delay line
- Pulse also sets off a trigger circuit
- Capture latches close and store “snapshot” of SET along delay line

- Temporal precision limited to 1 gate delay
- Trigger delay is programmable – account for variation and de-risk
- Delay line is calibrated using a configurable ring-oscillator (RO)
- Pulse is subject to distortion (PIPB) along the delay line

Pulse Filter Detector



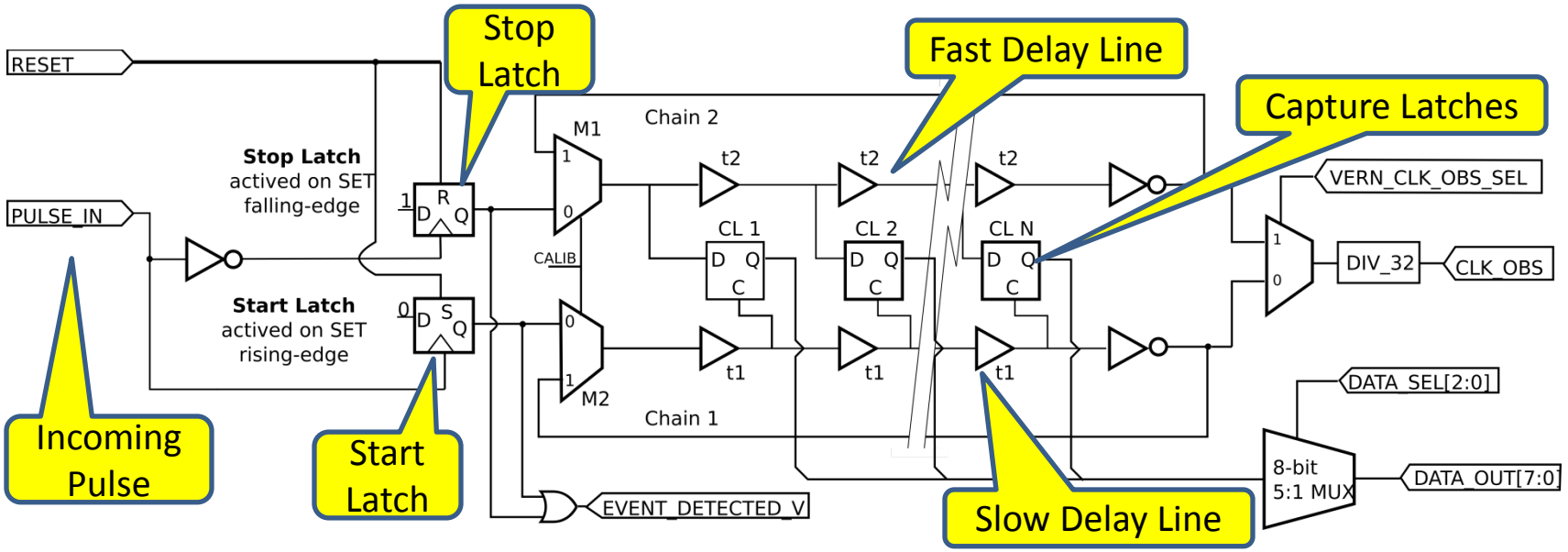
Parallel Pulse Filter circuit



Linear Pulse Filter

- Series of increasing pulse filters : PF1, PF2, …, PFn
- SETs will trigger the first 'N' filters then be blocked
- Linear topology avoids duplicating delay chains
- RO calibration possible with linear topology
- Temporal precision limited to 1 gate delay

Vernier SET Detector



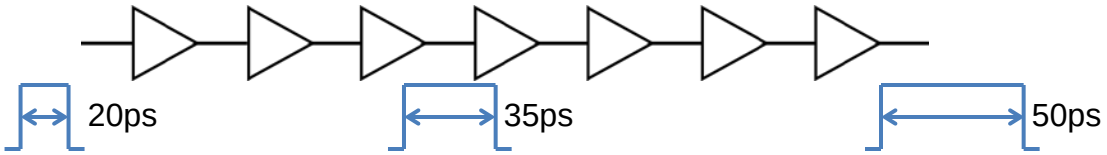
- Based on design from previous work [1,2,3]
- Two latches used to detect SET (rising and falling edge)
  - Leading edge of SET propagates along slow delay line (t1)
  - Trailing edge of SET propagates along fast delay line (t2)
  - Edges across after $N*(t_2-t_1)$ stages, corresponding to pulse width

[1] R. Harada, Y. Mitsuyama, M. Hashimoto, T. Onoye, *Measurement circuits for acquiring set pulsewidth distribution with sub-fo1-inverter-delay resolution*, ISQED 2010.
[2] A. Evans, D. Alexandrescu, V. Ferlet-Cavrois, M. Nicolaidis, *New Techniques for SET Sensitivity Measurement in Flash-Based FPGAs*, TNS 2014.
[3] R. Liu, A. Evans, Q. Wu, Y. Li, L. Chen, SJ Wen, R. Wong, R. Fung, *Analysis of Advanced Circuits for SET Measurement.* IRPS 2015.

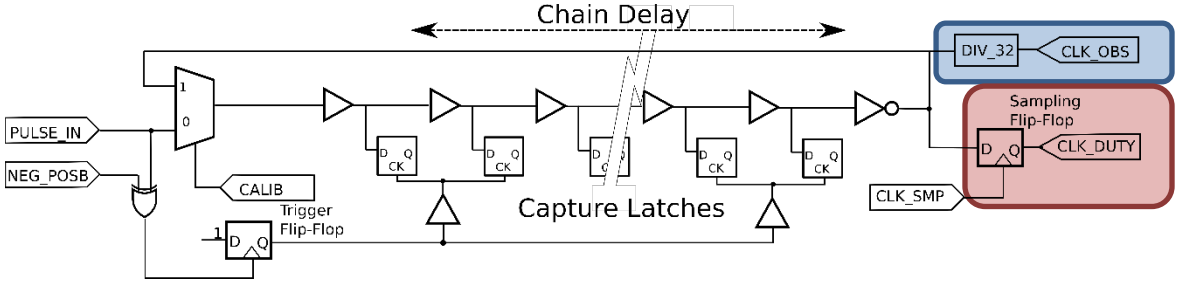
Rise/Fall Time Calibration

- PWMT experiments need on-chip calibration
  - Process, Voltage and Temperature (PVT) impact rise/fall times
  - N/P MOS variability can involve pulse broadening/narrowing on buffer chains:

In case of fast PMOS and slow NMOS



- Gate chain are used as Ring Oscillator (RO) to provide on chip calibration



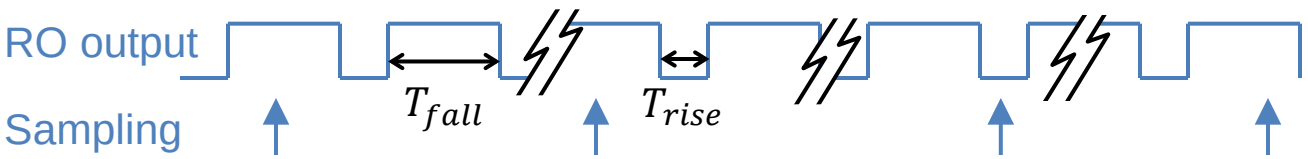
Measure RO frequency

Measure RO duty cycle

  - RO frequency give the sum of rise and fall time of the gate chain

$$T_{RO} = Trise_{Chain} + Tfall_{Chain}$$

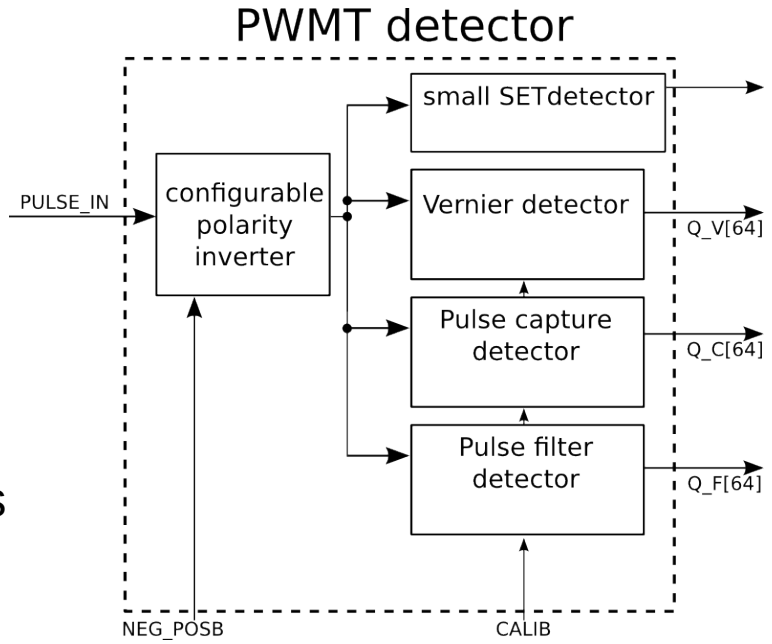
  - RO sampled at low frequency to extract duty cycle and dissociate rise and fall time

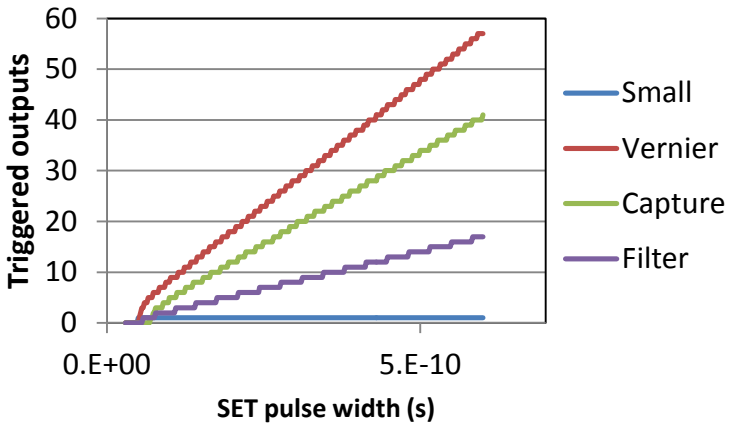


1 samples	75%
0 samples	25%

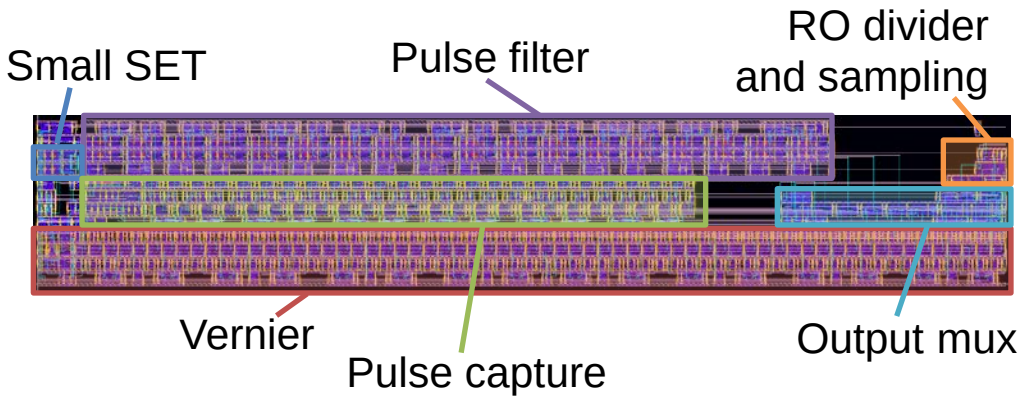
Pulse Width Measurement Topology

- One incoming pulse
- Four parallel detectors
  - Small (yes/no)
  - Vernier (≈15 ps resolution)
  - Pulse capture (≈20 ps resolution)
  - Pulse filter (≈40 ps resolution)
- Simultaneous measurement of same event will provide insight into accuracy of detectors
- Advanced delay rise/fall time calibration



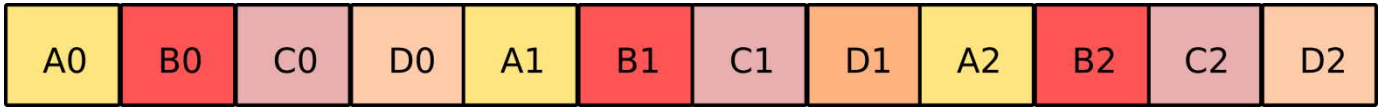


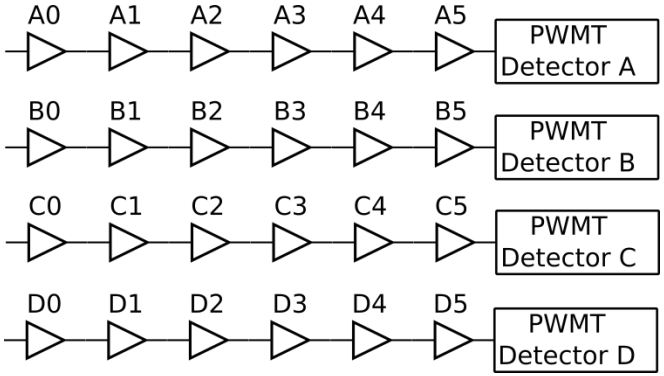
Circuit Simulation Result



Layout

Single Event Multiple Transient

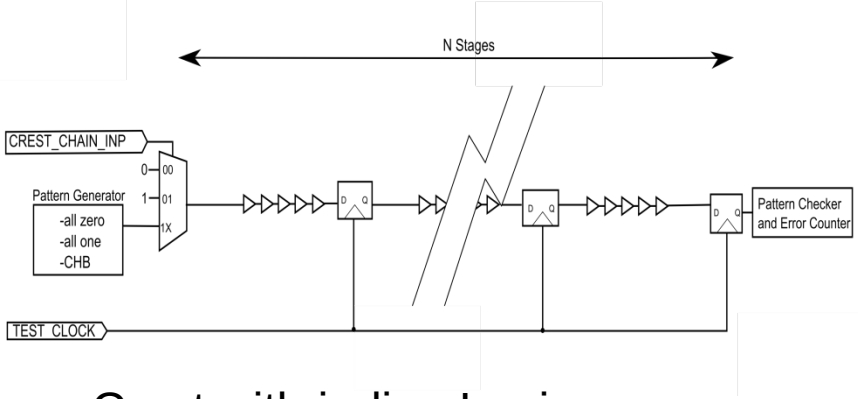




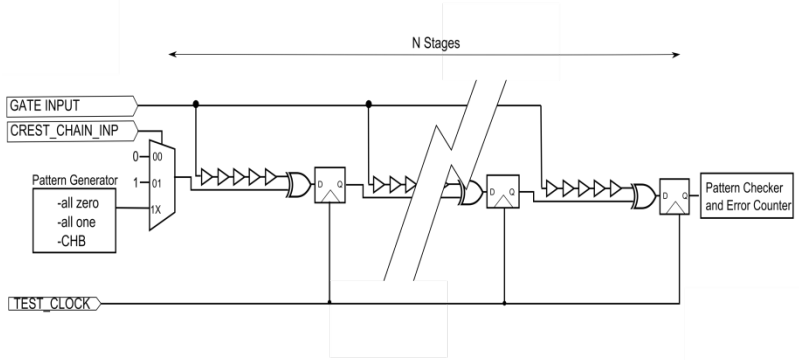
- Much discussion about SEMTs [1,2,3]
- Proposed measurement approach
  - Multiple logical chains of gates – but physically interleaved
  - Each logical chain has its own detector
  - A SEMT will be identified by multiple simultaneous logical events
- Multiple experiments to determine horizontal and vertical extent

[1] J. R. Ahlbin, T. D. Loveless, D. R. Ball, B. L. Bhuva, A. F. Witulski, et al., *Double-pulse-single-event transients in combinational logic*, IRPS 2011.
[2] Casey, M.C.; Duncan, A.R.; Bhuva, B.L.; Robinson, et al, *Simulation Study on the Effect of Multiple Node Charge Collection on Error Cross-Section in CMOS Sequential Logic*, TNS 2008.
[3] Ebrahimi, M.; Asadi, H.; Tahoori, M.B., A layout-based approach for Multiple Event Transient analysis", DAC 2013.

C-Crest Topology



Crest with in-line Logic

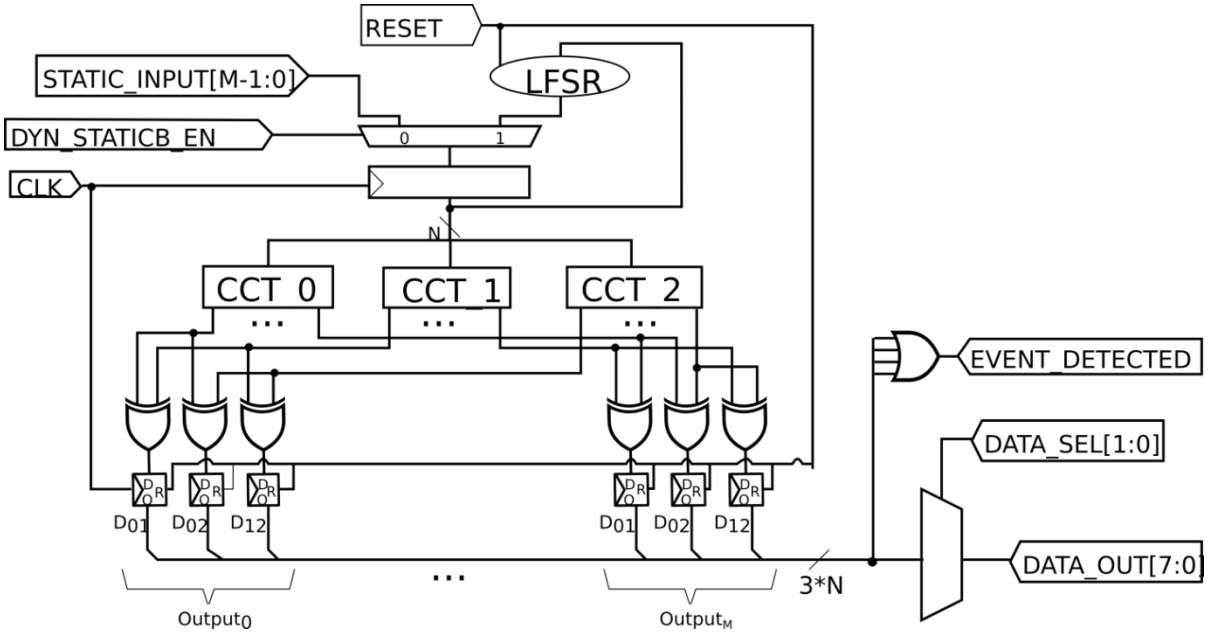


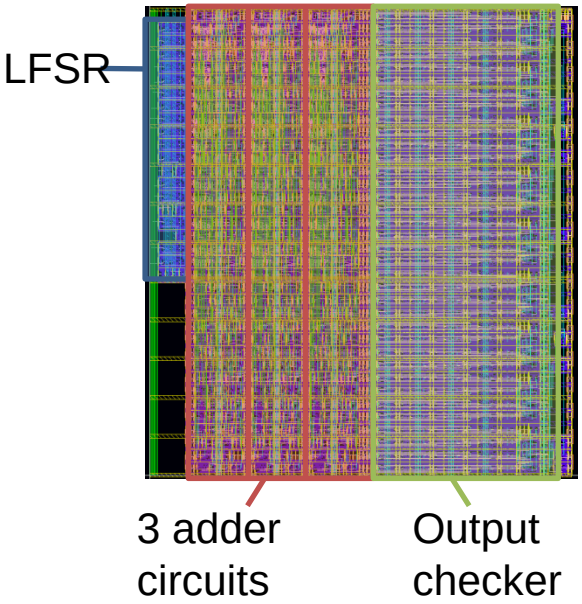
Crest with parallel Logic

- Logic is placed between flip-flops and clocked at high speed
- Errors checked at output of shift register
- SEU cross-section measured at low frequency
- SET cross-section increases with frequency due to reduced latch window masking
- Pulse width measurement not possible
- Average pulse width can be inferred from cross-section versus frequency

[1] M. J. Gadlage, R. D. Schrimpf, J. M. Benedetto, P. H. Eaton, et al., *Single event transient pulsewidths in digital microcircuits*, TNS 2004..
[2] J. Benedetto, P. Eaton, K. Avery, D. Mavis, M. Gadlage, et al., *Heavy ion-induced digital single-event transients in deep submicron processes*, TNS 2004.
[3] P. Marshall, M. Carts, S. Currie, R. Reed, B. Randall, et al., *Autonomous bit error rate testing at multi-gbit/s rates implemented in a 5 AM SiGe circuit for radiation effects self-test (CREST)*", TNS 2005

Dynamic SET Detector





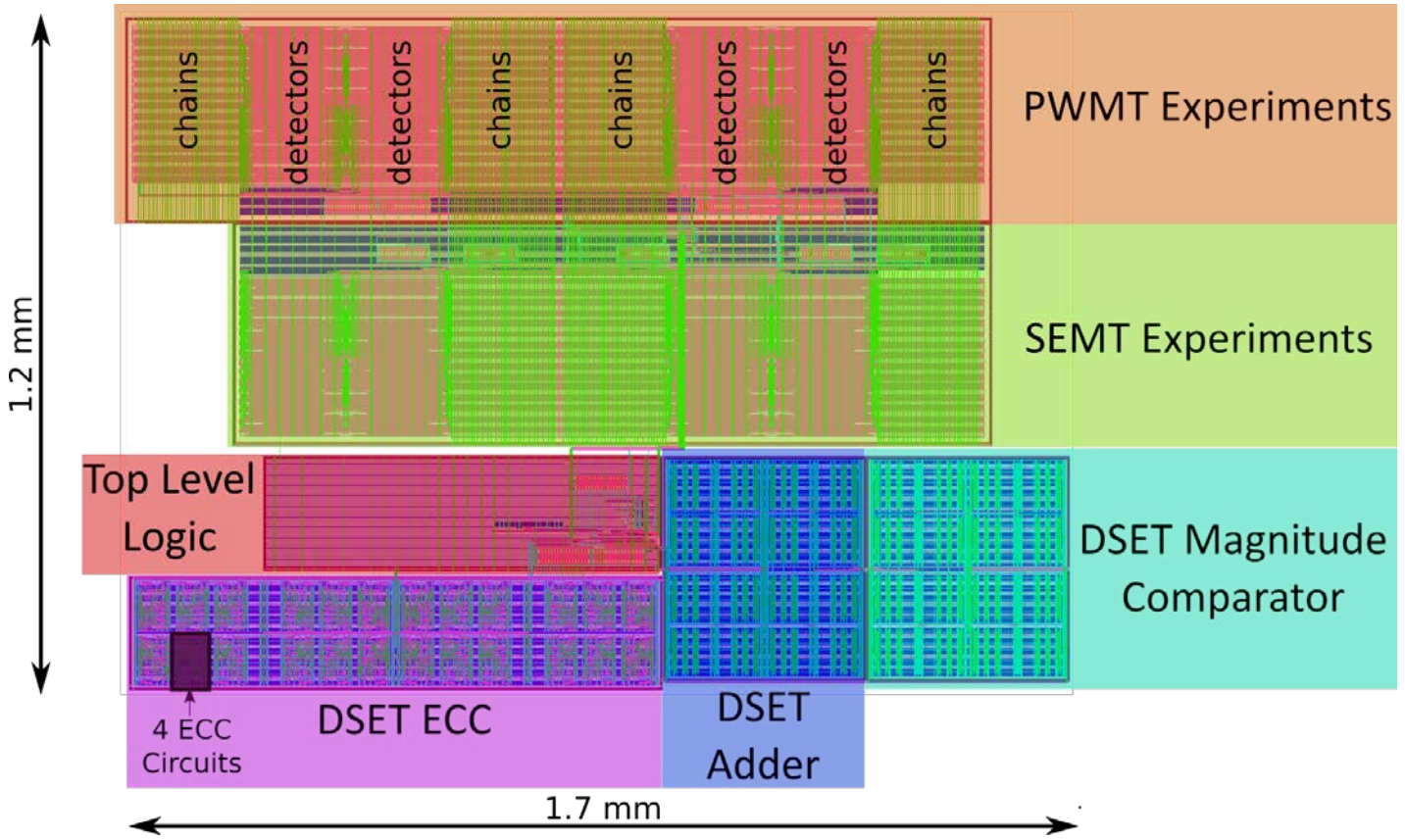
- Mimic the operation of “real” digital circuits
- Pseudo-random input vectors generated by an LFSR
- Triplicated combinatorial circuit
- 3-way output comparison (0⇔1, 1⇔2, 0⇔2)
- SETs cause a two-way mis-match : (011, 110, 101)
- SEUs cause a one-way mis-match : 001, 010, 100

- Three circuits under study : 8-bit adder, 8-bit mag. compare, 16-bit ECC

On-Chip SET Measurement Techniques

Criterion	Elementary Transistors	Pulse Width Measure Topology (PWMT)	Single Event Multiple Transient (SEMT)	Combinational Circuit for Radiation Effect Self Test (C-CREST)	Dynamic complex circuits (DSET)
Objective	Measure SET current	Measure SET pulse width distribution	Characterize SEMT (range, pulse width)	Measure average pulse width	Mimic combinational logic usage
Measurement	Analog Asynchronous	Digital Asynchronous	Digital Asynchronous	Digital Synchronous	Digital Synchronous
Measured Masking Effect	None	Electrical	Electrical	Electrical, Temporal	Logical, Electrical, Temporal
Cost (area/power)	--	-	-	+	++

Test Chip Top Level



- Tape-out (MPW) : JUN-2015
- Samples : SEP-2015
- HI and Laser testing : SEP..DEC-2015

Conclusions

Conclusions

- Accurate SET characterization is critical for
  - Risk assessment
  - Evaluating mitigation schemes (e.g. double sampling)
- Characterization is complex
  - Cell sensitivity depends on function, input state
  - Masking factors (logical, latch-window, electrical)
  - Pulse broadening effects (PIPB)

- Proposed circuits span the range from transistor level to "real" synchronous digital designs
  - New techniques for accurate on-chip calibration
  - In-depth measurement of SEMT effects
  - Actual SET measurement in active digital circuits

- Test results will provide new insights into best practices for SET test and measurement

Thank You!

Contacts

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Backup Slides

Annex: Preliminary list of experiments

PWMT experiments

ID	Cell	Chain length	Comment
0	Empty	0	
1	CORE65LPSVT/HS65_LS_IVX9	512	reference inverter
2	CORE65LPSVT/HS65_LS_IVX4	512	small drive
3	CORE65LPSVT/HS65_LS_IVX18	512	large drive
4	CORE65LPSVT/HS65_LS_IVX49	512	very large drive
5	CORE65LPSVT/HS65_LS_BFX9	512	buffer
6	CORE65LPSVT/HS65_LS_BFX49	512	large drive buffer
7	CORE65LPLVT/HS65_LL_IVX9	512	LVT effect
8	CORE65LPSVT/HS65_LS_NAND2X11	512	NAND gate
9	CORE65LPSVT/HS65_LS_NOR2X9	512	NOR gate
10	CORE65LPSVT/HS65_LS_AND2X9	512	AND gate
11	CORE65LPSVT/HS65_LS_OR2X9	512	OR gate
12	CORE65LPSVT/HS65_LS_XOR2X9	512	XOR gate
13	CORE65LPSVT/HS65_LS_MUX21X9	512	MUX gate
14	CORE65LPSVT/HS65_LS_PAO3X9	512	Parity gate
15	CORE65LPSVT/HS65_LS_AO22X9	512	AO gate
16	CORE65LPSVT/HS65_LS_FA1X9	512	Full adder
17	CORE65LPSVT/HS65_LS_IVX9	512	low voltage (with a level shifter)
18	SKYROB65LPSVT/SKY65BFX9	512	SKYROB buffer
19	SKYROB65LPSVT/SKY65BFX49	512	SKYROB large buffer
20	SKYROB65LPLVT/SKY65BFX9	512	SKYROB LVT buffer
21	SKYROB65LPSVT/NAND2X9	512	SKYROB NAND
22	SKYROB65LPSVT/NOR2X9	512	SKYROB NOR
23	SKYROB65LPSVT/AND2X9	512	SKYROB AND
24	SKYROB65LPSVT/OR2X9	512	SKYROB OR
25	SKYROB65LPSVT/AO22X9	512	SKYROB AO
26	SKYROB65LPSVT/PAO3X9	512	SKYROB Parity checker
27	SKYROB65LPSVT/SKY65BFX9	512	low voltage (with a level shifter)

SEMT experiments

ID	semt size	Cell	Chain length	Comment
0	6	CORE65LPSVT/HS65_LS_IVX9	64	basic inverter horizontal
1	4	CORE65LPSVT/HS65_LS_IVX9	64	basic inverter vertical
2	4	SKYROB65LPSVT/SKY65BFX9	64	Skyrob buffer horizontal
3	4	SKYROB65LPSVT/SKY65BFX9	64	Skyrob buffer vertical
4	3	CORE65LPSVT/HS65_LS_XOR2X9	64	XOR gate horizontal

C-CREST experiments

id	combinational logic	Number of stages	Comment
0	empty	0	Empty C-CREST to check intrinsic SER
1	8 CORE65LPSVT/HS65_LS_IVX9	1024	Reference
2	8 CORE65LPLVT/HS65_LL_IVX9	1024	LVT
3	8 CORE65LPSVT/HS65_LS_IVX18	1024	large drive
4	8 CORE65LPSVT/HS65_LS_BFX9	1024	Buffer
5	8 SKYROB65LPSVT/SKY65BFX9	1024	Skyrob buffer
6	8 SKYROB65LPLVT/SKY65BFX9	1024	Skyrob buffer lvt
7	8 SKYROB65LPLVT/SKY65BFX49	1024	Skyrob buffer large drive

SEMT experiments

ID	Bank size	Cell
0	64	16 bit adder
1	64	16 bit ECC encoder
2	64	16 bit comparator

Estimation of Required HI Fluence

- Heavy-ion beam time estimations based on:
  - 100 events for cross-section measurements
  - 500 events for pulse width distributions (PWMT experiments)
  - Heavy ion test planned at RADEF, with a flux of 1e6 HI/cm²/s
  - 2 dies simultaneously tested

Experiment	# LET	# Pattern	# Frequency	Beam time RADEF (h)	Total dose / DUT (rad)
PWMT	4	3	-	6,1	2,29E+06
C-CREST	4	3	4	2,8	1,12E+06
Dynamic SET (Adder)	4	3	4	1,9	4,92E+05
Dynamic SET (ECC)	4	3	4	2,3	6,12E+05
Dynamic SET (magnitude comparator)	4	3	4	13,2	5,93E+06