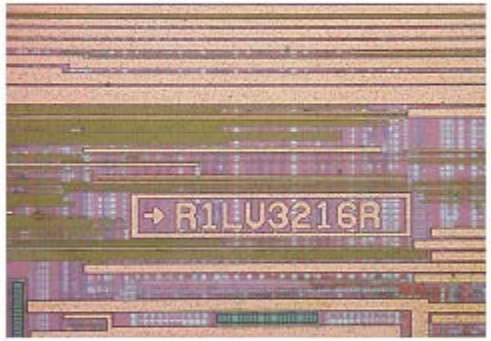
Radiation Final Presentation Days

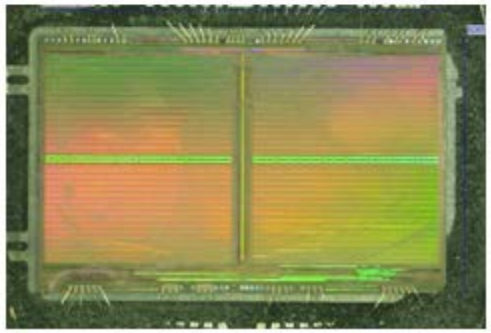
Tested parts

Part Type	Manufacturer	Package	Function	Testing
R1WV6416RSA	Renesas	TSOP 48	SRAM 64M – 4M x 16	SEE + TID
MR4A16BCYS35	Everspin	TSOP 54	MRAM 16M – 1M x 16	SEE
MT29F128G08JAAAWP	Micron	TSOP 48	NAND FLASH 128G	SEE + TID
IS46TR16256AL-125K	ISSI	FBGA 96	DDR3 4G – 256M x 16	SEE, TID on going
MT41K256M16HA-125AIT	Micron	FBGA 96	DDR3 4G – 256M x 16	SEE, TID on going

SRAM memory Renesas 4 Mi x 16 (1/2)

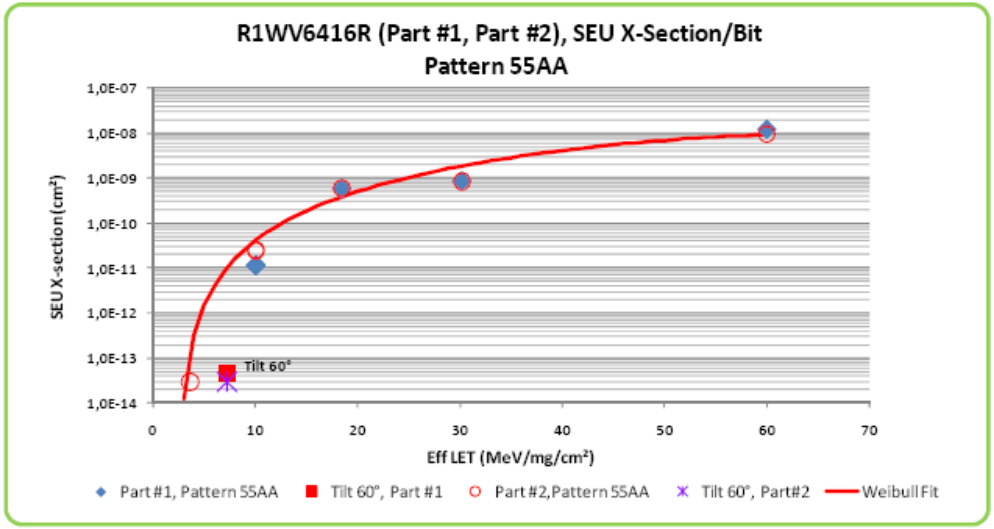
- Part type: R1WV6416RSA-5SI
- Part description: 64 Mb static RAM organized as 4,194,304 word x 16 bit - 2 die of 32 Mb
- Manufacturer: Renesas
- Package: 48 pin TSOP I
- Date code: 0930
- Die dimensions: 9750 x 6080 µm
- SEE Testing: RADEF (Jyvaskyla / Finland), April 2010, 2 parts





SRAM memory Renesas 4 Mi x 16 (1/2)

- No SEL at Xe and 60° angle (LET of 120 MeV.cm2.mg-1) up to a fluence of 1E7 part.cm2.
- Some MBU observed (most MBU are 2 bits MBU).
- Thanks to descrambling analysis, MCU have been observed (worst case is 9 cells).



- SEU saturation cross-section
  - 1.2E-8 cm2.bit-1
- LET threshold
  - 2.5 MeV.cm2.mg-1

TID - SRAM: R1WV6416RSA (1/8)

- TID source: UCL, May and June 2013
- 11 samples tested (5xON, 5xOFF, 1xREF)
- Low End digital tester used (400 Mbps pattern rate)
- Static biasing for ON parts
- Irradiation steps and dose rate :

Irradiation Steps	Dose rate	Annealing steps	Temperature
krad (Si)	rad(Si)/h	Hours	°C
0		-	Room
5	230	-	Room
10	230	-	Room
15	230	-	Room
30	230	-	Room
-	-	24h	Room
-	-	168h	100°C

Serial Number	Allocation
1	Control
2	Biased ON
3	Biased ON
4	Biased ON
5	Biased ON
6	Biased ON
7	Biased OFF
8	Biased OFF
9	Biased OFF
10	Biased OFF
11	Biased OFF

- Results :
  - Biased ON samples:
    - ✓ One failed (SN 3)part on tRC parameter (Read Cycle Time) at 15krad and 30 krad.
    - ✓ All parts failed functional test starting at 15 krad.
    - ✓ All parts recover after 168h @ 100°C annealing.
    - ✓ No samples recovery observed after 24h and 168h annealing steps.
  - Biased OFF samples:
    - ✓ No fail parts at both irradiation steps and after 24 h @ room and 168 h annealing @ 100°C.

TID - SRAM: R1WV6416RSA (2/8)

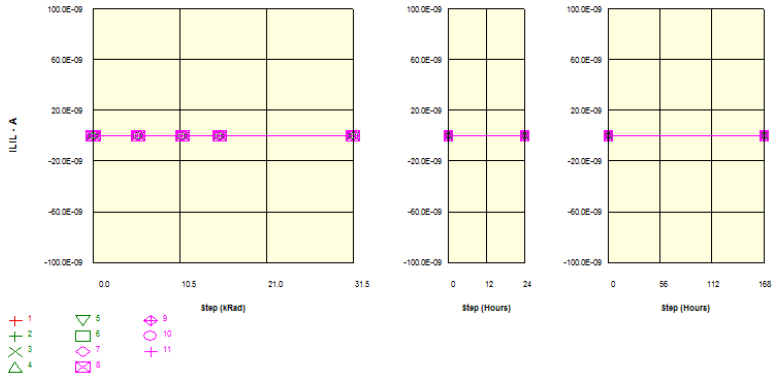
Symbol	Test Parameter	Test Conditions	Specification limits		Unit
			Min limit	Max limit	
ILIL	Input Leakage current	VCC = 3.6V, Vin= VSS	-1	1	µA
ILIH	Input Leakage current	VCC = 3.6V, Vin= VCC	-1	1	µA
ILOL	Output Leakage current	VCC=3.6V, BYTE# ≥ Vcc -0.2V CS1# =VIH, CS2 =VIL, OE# =VIH, WE# =VIL, LB# = UB# =VIH, VI/O =Vss	-1	1	µA
ILOH	Output Leakage current	VCC=3.6V, BYTE# ≥ Vcc -0.2V CS1# =VIH, CS2 =VIL, OE# =VIH, WE# =VIL, LB# = UB# =VIH, VI/O =VCC	-1	1	µA
VOL	Output Low Voltage	VDD = 3V IOL=2mA, BYTE# ≥ Vcc -0.2V	-	0.4	V
VOH	Output High Voltage	VDD = 3V IOH=-0.5mA, BYTE# ≥ Vcc -0.2V	2.4	-	V
ICC1	Average operating current	VCC= 3.6V, Min. cycle, II/O = 0mA BYTE# ≥ Vcc -0.2V, CS1# =VIL, CS2 =VIH, Others = VIH/VIL	-	60	mA
ICC2	Average operating current	VCC= 3.6V,Cycle =1µs, II/O = 0mA BYTE# ≥ Vcc -0.2V, CS1# ≤ 0.2V, CS2 ≥ VCC-0.2V, VIH ≥ VCC-0.2V, VIL ≤ 0.2V	-	10	mA
ISB	Standby current	VCC= 3.6V BYTE# ≥ Vcc -0.2V, CS2 =VIL, other pin at level VCC or VSS	-	300	µA

TID - SRAM: R1WV6416RSA (3/8)

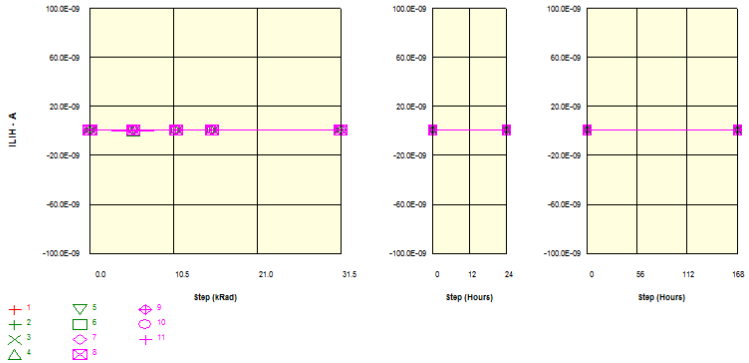
Symbol	Test Parameter	Test Conditions	Specification limits		Unit
			Min limit	Max limit	
tRC	Read cycle time	GO NOGO test , VCC=3V, Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		55	ns
tAA	Address access time	VCC=3V, Isink=2mA (for Vol=0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		55	ns
tACS1	Chip select access time	VCC=3V, Isink=2mA (for Vol =0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		55	ns
tACS2	Chip select access time	VCC=3V, Isink=2mA (for Vol =0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		55	ns
tOE	Output enable to output valid	VCC=3V, Isink=2mA (for Vol =0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		25	ns
tBA	LB#, UB# access time	VCC=3V, Isink=2mA (for Vol =0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		55	ns
tAW	Address valid to end of write	VCC=3V, Isink=2mA (for Vol =0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		50	ns
tWP	Write pulse width	VCC=3V, Isink=2mA (for Vol =0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		40	ns
tAS	Address setup time	VCC=3V, Isink=2mA (for Vol =0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		0	s
tDH	Data hold from write time	VCC=3V, Isink=2mA (for Vol =0.4V) Isource=2mA (for Voh=2.4V), VIL=0.4V VIH=2.4V		0	s
FCT_CHK	Checkerboard	VCC= 3.3V, f=10MHz, VIL=0V, VIH=3V, No Load	Go/Nogo	Go/Nogo	P/F
FCT_INVCHK	Checkerboard inverse	VCC = 3.3V, f=10MHz, VIL=0V, VIH=3V, No Load	Go/Nogo	Go/Nogo	P/F

TID - SRAM: R1WV6416RSA (4/8)

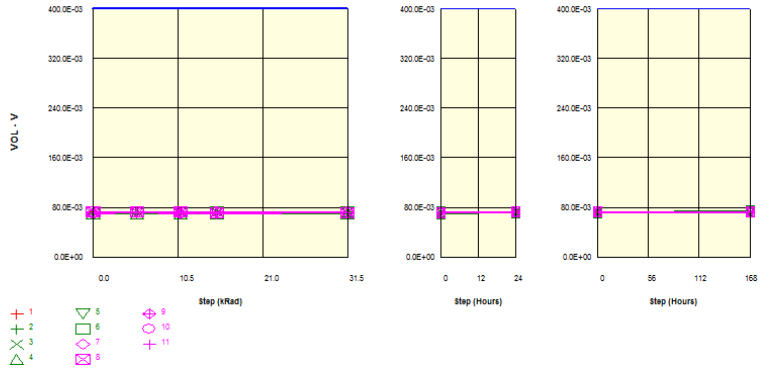
Parameter : Input Leakage current : [ILIL/CS1]
Test conditions : VCC = 3.6V. Vin= VSS
Unit : A
Spec Limit Min : -1.0E-06
Spec Limit Max : 1.0E-06
Spec limits are represented in bold lines on the graphic.



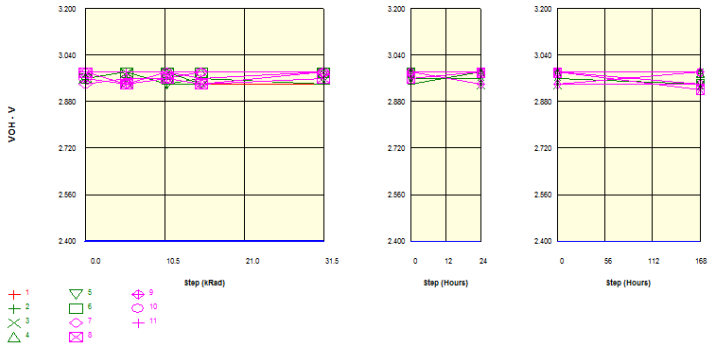
Parameter : Input Leakage current : [ILIH/CS1]
Test conditions : VCC = 3.6V. Vin= VCC
Unit : A
Spec Limit Min : -1.0E-06
Spec Limit Max : 1.0E-06
Spec limits are represented in bold lines on the graphic.



Parameter : Output Low Voltage : [VOLDQ15]
Test conditions : VDD = 3V IOL=2mA. BYTE# = Vcc -0.2V
Unit : V
Spec Limit Max : 400.0E-03
Spec limits are represented in bold lines on the graphic.

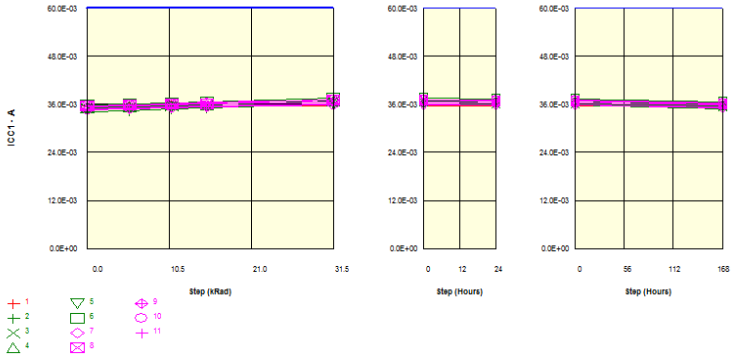


Parameter : Output High Voltage : [VOHDQ15]
Test conditions : VDD = 3V IOH=-0.5mA. BYTE# = Vcc -0.2V
Unit : V
Spec Limit Min : 2.400
Spec limits are represented in bold lines on the graphic.

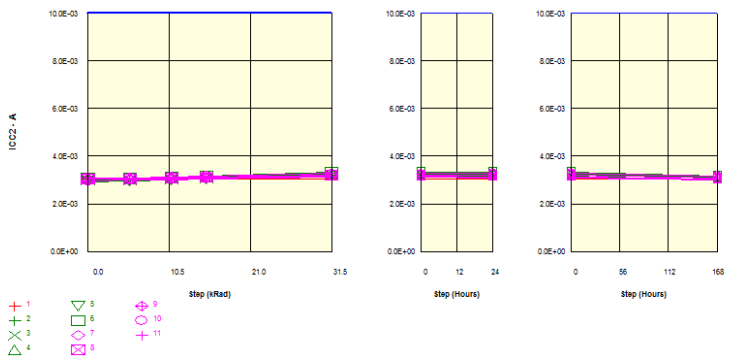


TID - SRAM: R1WV6416RSA (5/8)

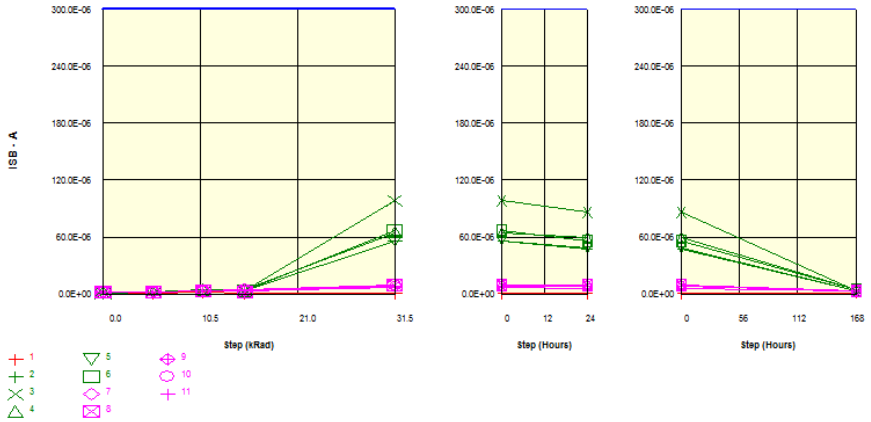
Parameter : Average operating current : ICC1
Test conditions : VCC= 3.6V. Min. cycle. II/O = 0mA. BYTE# = Vcc -0.2V. CS1# =VIL. CS2 =VIH. Others = VIH/VIL
Unit : A
Spec Limit Max : 60.0E-03
Spec limits are represented in bold lines on the graphic.



Parameter : Average operating current : ICC2
Test conditions : VCC= 3.6V.Cycle =1µs. II/O = 0mA. BYTE# = Vcc -0.2V. CS1# = 0.2V. CS2 = VCC-0.2V. VIH = VCC-0.2V. VIL = 0.2V
Unit : A
Spec Limit Max : 10.0E-03
Spec limits are represented in bold lines on the graphic.

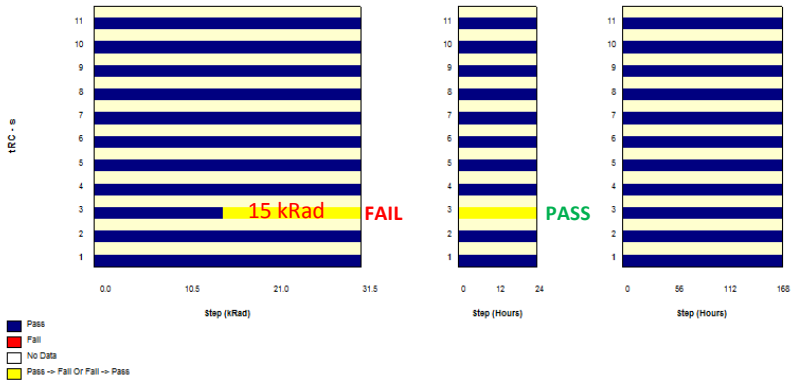


Parameter : Standby current : ISB
Test conditions : VCC= 3.6V BYTE# = Vcc -0.2V. CS2 =VIL. other pin at level VCC or VSS
Unit : A
Spec Limit Max : 300.0E-06
Spec limits are represented in bold lines on the graphic.

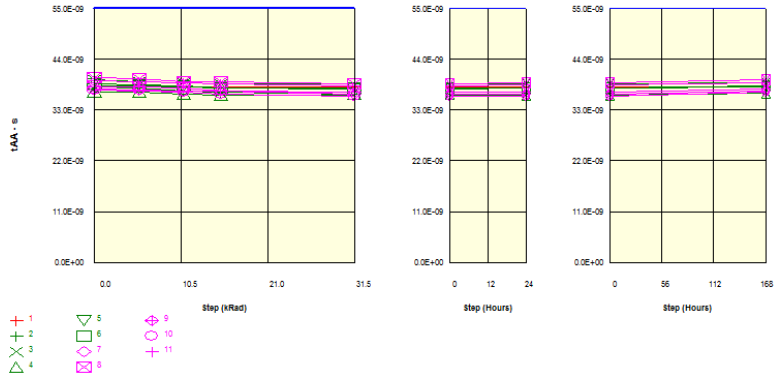


TID - SRAM: R1WV6416RSA (6/8)

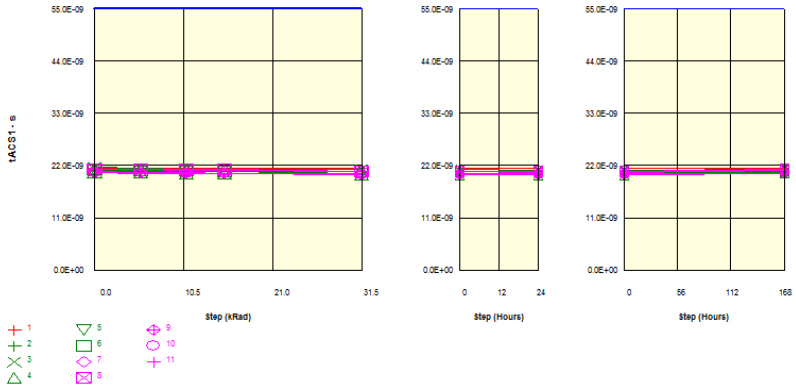
Parameter : Read cycle time : [tRC]
Test conditions : GO NOGO test . VCC=3V. Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V). VIL=0.4V VIH=2.4V
Unit : s
Spec Limit Max : 55.0E-09
Spec limits are represented in bold lines on the graphic.



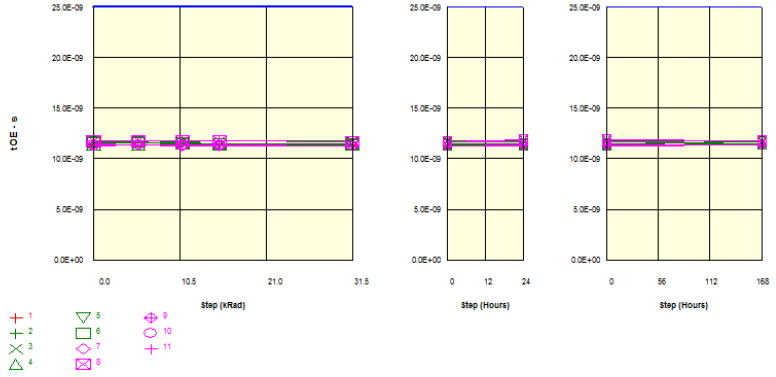
Parameter : Address access time : [tAA]
Test conditions : VCC=3V. Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V). VIL=0.4V VIH=2.4V
Unit : s
Spec Limit Max : 55.0E-09
Spec limits are represented in bold lines on the graphic.



Parameter : Chip select access time : [tACS]
Test conditions : VCC=3V. Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V). VIL=0.4V VIH=2.4V
Unit : s
Spec Limit Max : 55.0E-09
Spec limits are represented in bold lines on the graphic.

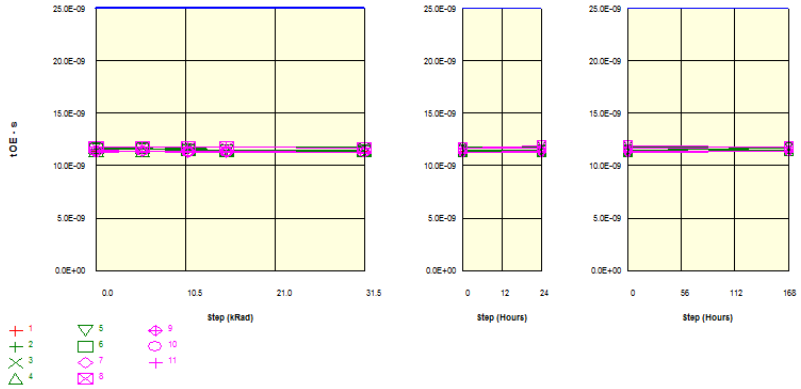


Parameter : Output enable to output valid : [tOE]
Test conditions : VCC=3V. Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V). VIL=0.4V VIH=2.4V
Unit : s
Spec Limit Max : 25.0E-09
Spec limits are represented in bold lines on the graphic.

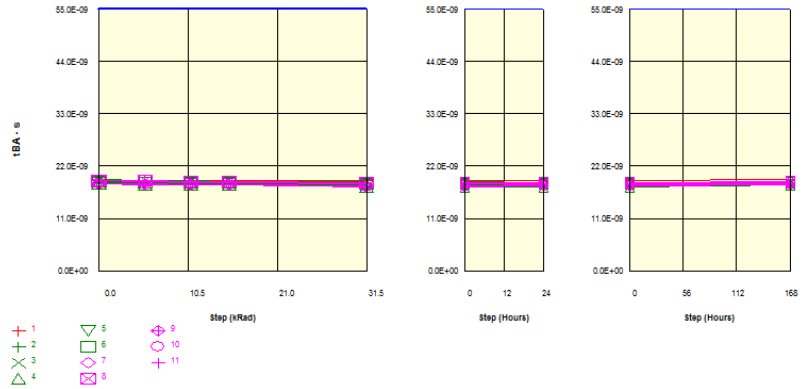


TID - SRAM: R1WV6416RSA (7/8)

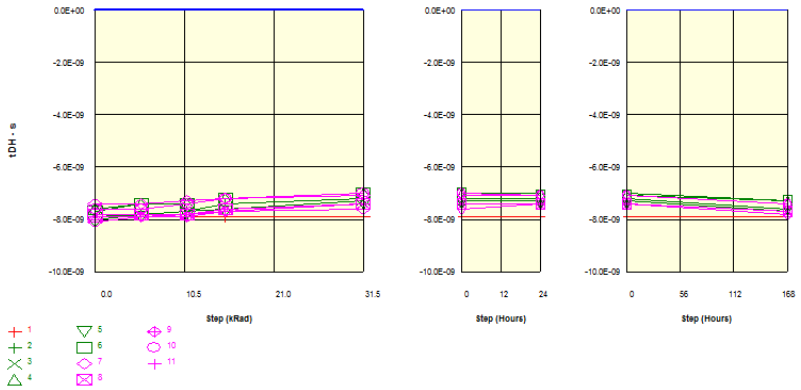
Parameter : Output enable to output valid :[tOE]
Test conditions : VCC=3V. Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V). VIL=0.4V VIH=2.4V
Unit : s
Spec Limit Max : 25.0E-09
Spec limits are represented in bold lines on the graphic.



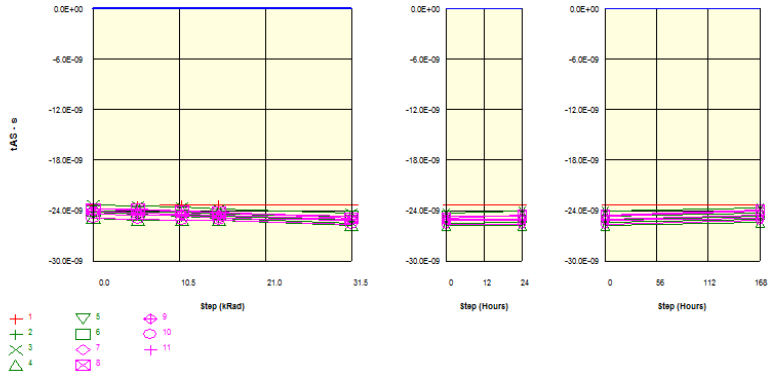
Parameter : LB#. UB# access time :[tBA]
Test conditions : VCC=3V. Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V). VIL=0.4V VIH=2.4V
Unit : s
Spec Limit Max : 55.0E-09
Spec limits are represented in bold lines on the graphic.



Parameter : Data hold from write time :[tDH]
Test conditions : VCC=3V. Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V). VIL=0.4V VIH=2.4V
Unit : s
Spec Limit Max : 0.0E+00
Spec limits are represented in bold lines on the graphic.

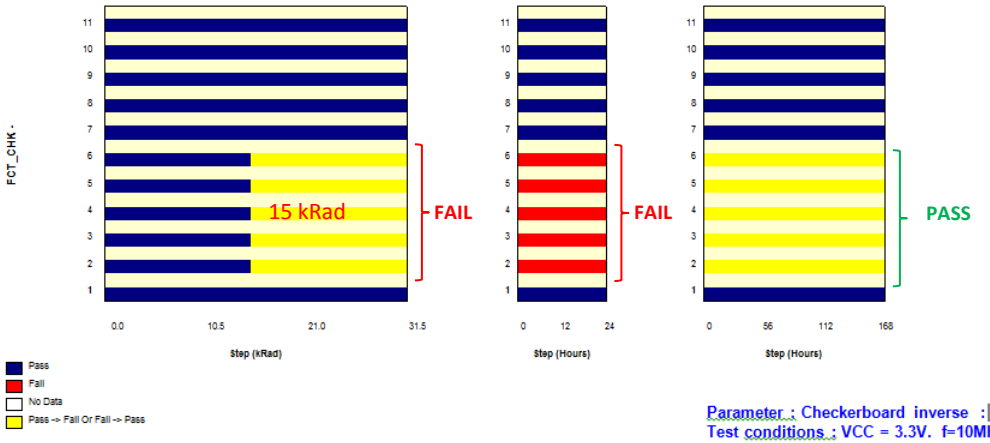


Parameter : Address setup time :[tAS]
Test conditions : VCC=3V. Isink=2mA (for vol=0.4V) Isource=2mA (for Voh=2.4V). VIL=0.4V VIH=2.4V
Unit : s
Spec Limit Max : 0.0E+00
Spec limits are represented in bold lines on the graphic.



TID - SRAM: R1WV6416RSA (8/8)

Parameter : Checkerboard :FCT_CHK
Test conditions : VCC= 3.3V. f=10MHz. VIL=0V. VIH=3V. No Load
Unit :
No spec limit specified.

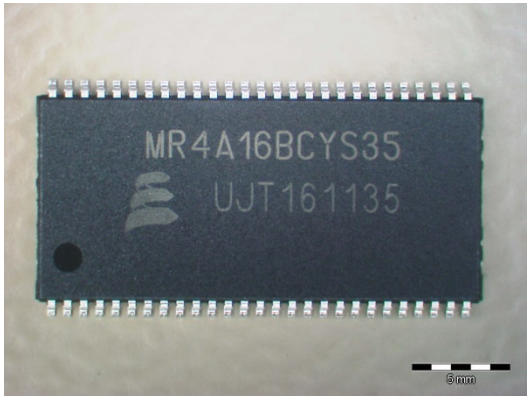


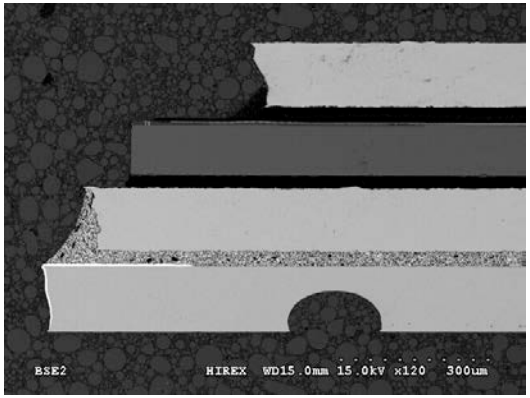
PASS

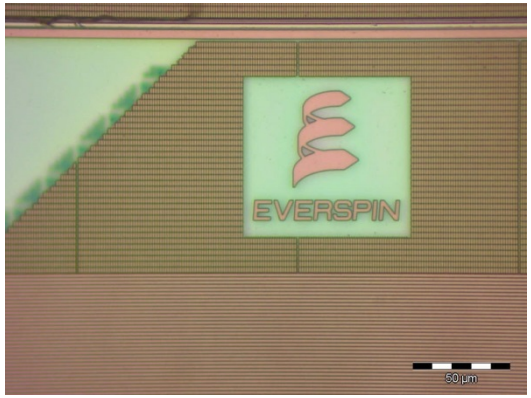
Parameter : Checkerboard inverse :FCT_INVCHK
Test conditions : VCC = 3.3V. f=10MHz. VIL=0V. VIH=3V. No Load
Unit :
No spec limit specified.

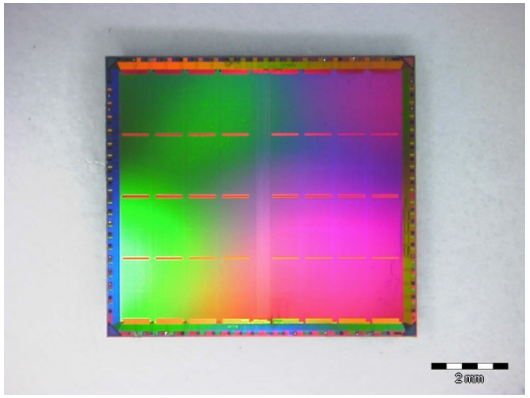
SEE - MRAM: MR4A14B (1/2)

- Part type: MR4A16BCYS35
- Part description: 16Mbit MRAM
- Manufacturer: Everspin
- Package: 54-pin TSOP2
- Die dimensions: 8084 x 7300 µm
- SEE testing: TAMU, March 2013
- Irradiation exposure : Air







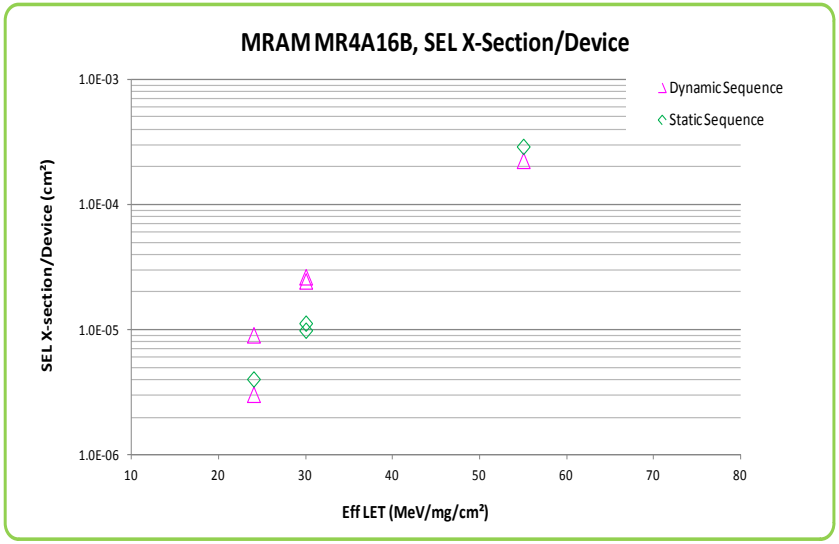


SEE - MRAM: MR4A14B (2/2)

- 2 test modes
  - Static (no access while beam is on)
  - Dynamic (read/write while beam is on)

- SEL at 24 MeV.mg^{-1}.cm^{-2} and higher at room temperature
  Maximum observed cross-section of 2.9E^{-4} cm^2/device
- Current steps at 30 MeV.mg^{-1}.cm^{-2} and higher

- No SEU up to 10 MeV.mg^{-1}.cm^{-2}
- Soft SEFI (power cycle not needed) starting at 10 MeV.mg^{-1}.cm^{-2}
- Hard SEFI (power cycle needed) starting at 24 MeV.mg^{-1}.cm^{-2}

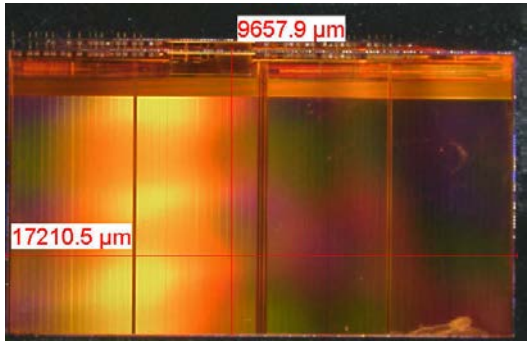


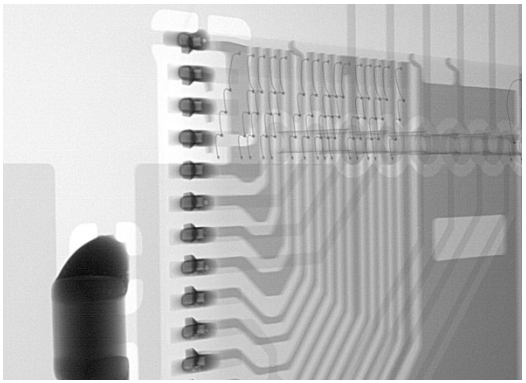
SEE - Flash: MT29F128G08A (1/2)

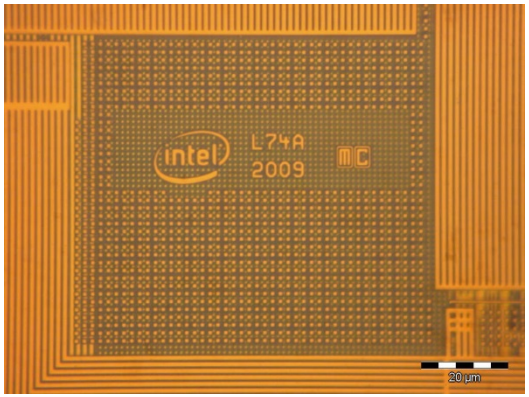
- Part type: MT29F128G08A
- Part description: 32Gbit Flash memory

(4 dies, 2 planes, 2048 blocks, 128 pages, 8640 x 8 bit)

- Manufacturer: Micron technology
- Package: 54-pin TSOP2
- Die dimensions: 17.2 x 9.6 mm
- SEE testing: RADEF, April and September 2014

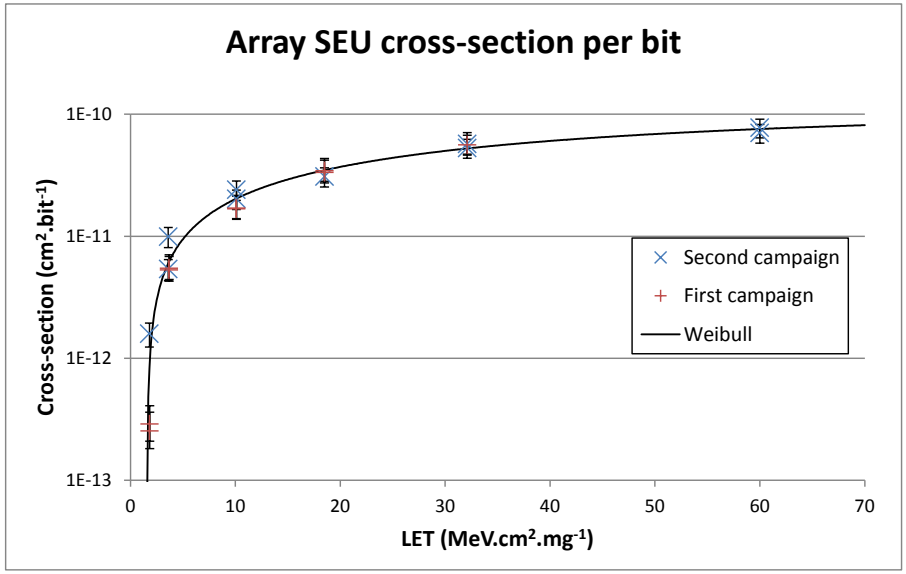






SEE - Flash: MT29F128G08A (2/2)

- 3 test sequences
  - Wait (no access while beam is on)
  - Read (read while beam is on)
  - Erase write (erase and write while beam is on)
- No SEL up to 60 MeV.mg^{-1}.cm^{-2} room temperature (fluence 1E7 cm^{-2})
- SEU starting at 1.8 MeV.mg^{-1}.cm^{-2}
  - Some last only 1 read
  - Some last few seconds / reads
  - Some stay (until erase)
- Large errors starting at 1.8 MeV.mg^{-1}.cm^{-2}
  - One address on many pages
  - One page
  - One block



TID - Flash: MT29F128G08A (1/8)

- TID source: GAMRAY, April and May 2014
- 11 samples tested (5xON, 5xOFF, 1xREF)
- High End digital tester used (800 Mbps pattern rate)
- Static biasing for ON parts
- Irradiation steps and dose rate :

Irradiation Steps	Dose rate	Annealing steps	Temperature
krad (Si)	rad(Si)/h	Hours	°C
0		-	Room
7	260	-	Room
12	260	-	Room
18	260	-	Room
24	260	-	Room
48	260	-	Room
70	260	-	Room
100	260	-	Room
-	-	24h	Room
-	-	168h	100°C

Serial Number	Allocation
11	Control
5	Biased ON
6	Biased ON
7	Biased ON
8	Biased ON
9	Biased ON
1	Biased OFF
2	Biased OFF
3	Biased OFF
4	Biased OFF
10	Biased OFF

- Results :
  - Biased ON samples:
    - ✓ First functional failure observed at 48kRad(Si) step for all samples.
    - ✓ No samples recovery observed after 24h and 168h annealing steps.
  - Biased OFF samples:
    - ✓ First functional failure observed at 48kRad(Si) step on 4 samples.
    - ✓ No samples recovery observed after 24h + 168h annealing steps.
    - ✓ Nevertheless out of the 5xOFF parts, 1 sample failed after 168h annealing step @ 100°C.

TID - Flash: MT29F128G08A (2/8)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN	MAX	UNITS
DC					
Continuity Neg	Cont_Neg	Iin=-100uA	-1.5	-0.2	V
Input Leakage Current Low	ILIL	Vin=0V , VCC= VCCmax (3.6V)	-40.0E-6	40.0E-6	A
Input Leakage Current High	ILIH	Vin= VCC= VCCmax (3.6V)	-40.0E-6	40.0E-6	A
Output Leakage Current Low	ILOL	Vout=0V , Vcc = 3.6V DQ are disabled	-40.0E-6	40.0E-6	A
Output Leakage Current High	ILOH	Vout=VCCmax, Vcc = 3.6V DQ are disabled	-40.0E-6	40.0E-6	A
Output Low Voltage	VOL	IOL=2.1mA, Vcc = 3.3V	0.99		V
Output High Voltage	VOH	IOH=-400uA Vcc = 3.3V		2.31	V
Input Low Voltage	VIL	Vcc = 3.3V	0.66		V
Input High Voltage	VIH	Vcc = 3.3V		2.64	V
Power supply (VCC =3.3V)					
Operating Current, Page Read with serial Access	ICC1	Read Active Current on Target 0, MODE5		100.0E-3	A
Operating Current, Program	ICC2	Program Active Current on Target 0 lun 0 & Target 1 Lun 0, MODE5		200.0E-3	A
Operating Current, Erase	ICC3	Erase Block 0 on Target 0 lun 0 & Target 1 Lun 0		200.0E-3	A
Standby Current	ISB	CE/=VCC-0.2V, WP/=0V/VCC, VCC & VCCQ common		200.0E-6	A

TID - Flash: MT29F128G08A (3/8)

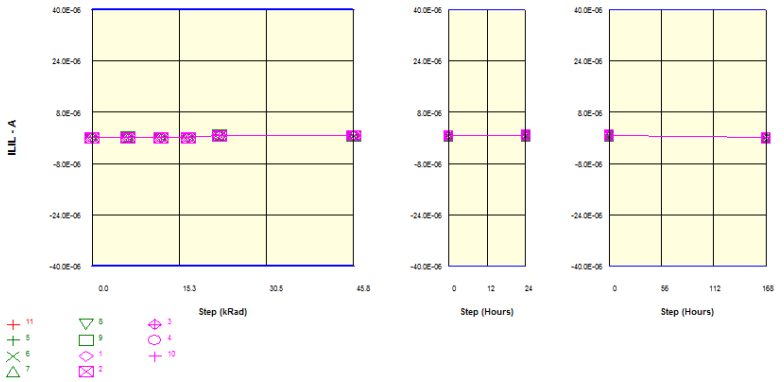
PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN	MAX	UNITS
AC (VCC=3.3V, Input Pulse Levels =0V to VCC , Input and Output Timing Levels=VCC/2, AC Measurements done on Block memory N°1) Mode 0					
Program Time	tProg	PROGRAM PAGE operation time GO NOGO		560.0E-6	s
Block Erase Time	tBers	BLOCK ERASE operation time , GO NOGO		7.0E-3	s
CLE Setup Time	tCLS			50.0E-9	s
CLE Hold Time	tCLH			20.0E-9	s
CE/ Setup Time	tCS			70.0E-9	s
CE/ Hold Time	tCH	GO NOGO		20.0E-9	s
WE/ Pulse Width	tWP	Note2		50.0E-9	s
ALE Setup Time	tALS			50.0E-9	s
ALE Hold Time	tALH			20.0E-9	s
Data Setup Time	tDS			40.0E-9	s
Data Hold Time	tDH			20.0E-9	s
Write Cycle Time	tWC	Note2		100.0E-9	s
WE/ High Hold Time	tWH	Note2, GONOGO		30.0E-9	s
ALE to RE/ Delay	tAR,	GO NOGO		25.0E-9	s
CLE to RE/ Delay	tCLR	GO NOGO		20.0E-9	s
RE/ Pulse Width	tRP			50.0E-9	s
Read Cycle Time	tRC			100.0E-9	s
RE/ Access Time	tREA			40.0E-9	s
WE High to Busy	tWB			200.0E-9	s
CE/ Access Time	tCEA			100.0E-9	s
RE/ High Hold Time	tREH	GO NOGO		30.0E-9	s
WP/ High to WE/ Low	tWW	GO NOGO		100.0E-9	s

TID - Flash: MT29F128G08A (4/8)

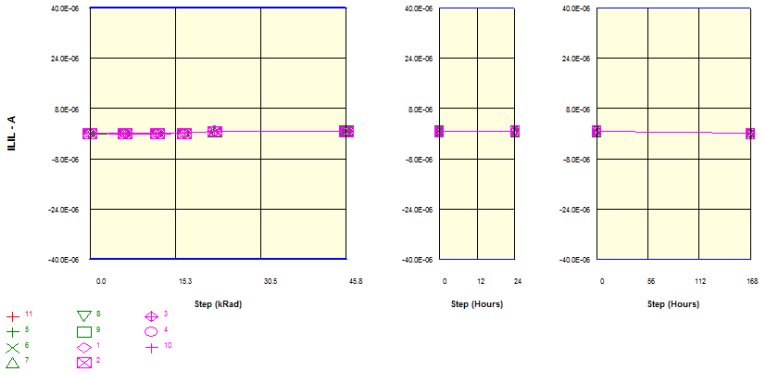
PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN	MAX	UNITS
Functionality (VCC =3.3V)					
Pattern FCT Checkerboard	Func_CHK	Erase Write , Read block 0 with pattern Checkerboard 0x55 & 0xAA	-	-	-
Pattern FCT /Checkerboard	Func_/CHK	Erase Write , Read block 0 with pattern invers Checkerboard 0xAA & 0x55	-	-	-

TID - Flash: MT29F128G08A (5/8)

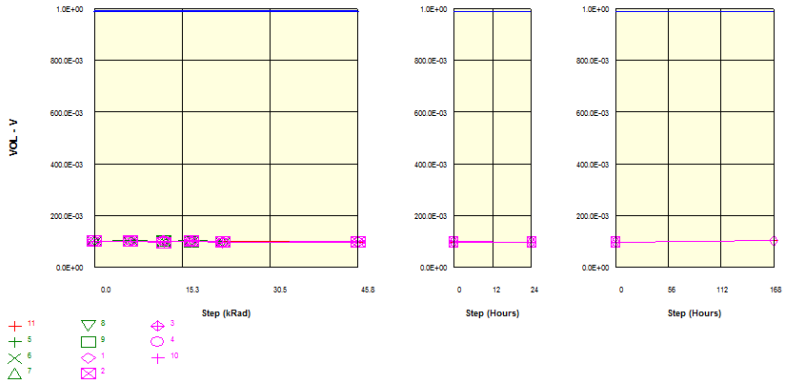
Parameter : Input Leakage Current Low : [ILILALE]
Test conditions : Vin=0V . VCC= VCCmax (3.6V)
Unit : A
Spec Limit Min : -40.0E-06
Spec Limit Max : 40.0E-06
Spec limits are represented in bold lines on the graphic.



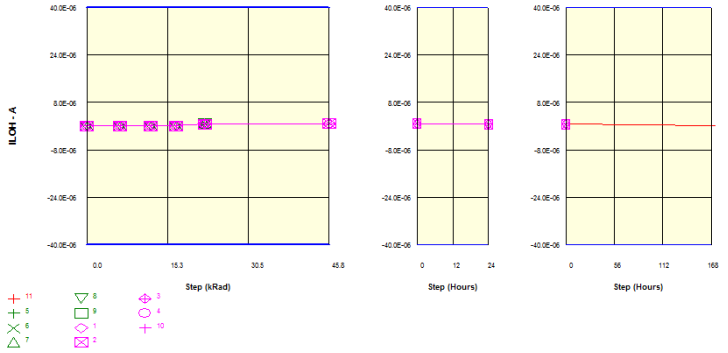
Parameter : Input Leakage Current Low : [ILILIO[0]
Test conditions : Vin=0V . VCC= VCCmax (3.6V)
Unit : A
Spec Limit Min : -40.0E-06
Spec Limit Max : 40.0E-06
Spec limits are represented in bold lines on the graphic.



Parameter : Output Low Voltage : [VOLIO[0]
Test conditions : IOL=2.1mA. Vcc = 3.3V
Unit : V
Spec Limit Max : 990.0E-03
Spec limits are represented in bold lines on the graphic.

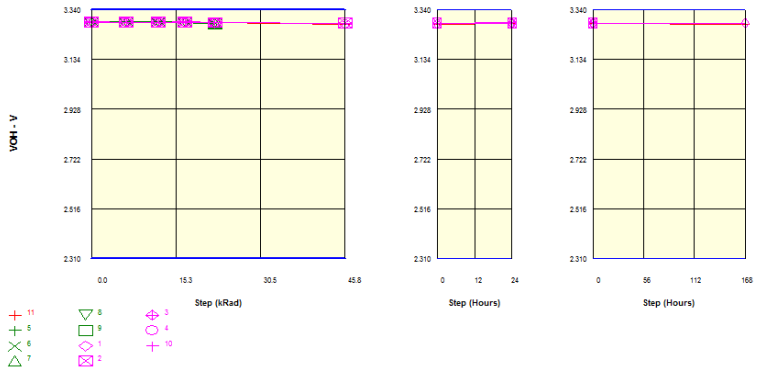


Parameter : Output Leakage Current High : [ILOHIO[0]
Test conditions : Vout=VCCmax. Vcc = 3.6V DQ are disabled
Unit : A
Spec Limit Min : -40.0E-06
Spec Limit Max : 40.0E-06
Spec limits are represented in bold lines on the graphic.

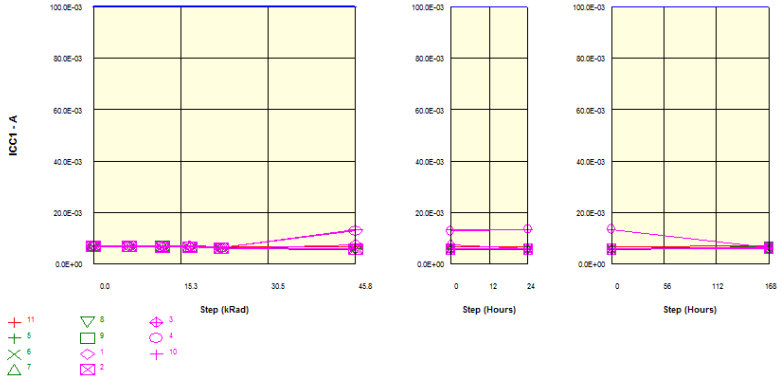


TID - Flash: MT29F128G08A (6/8)

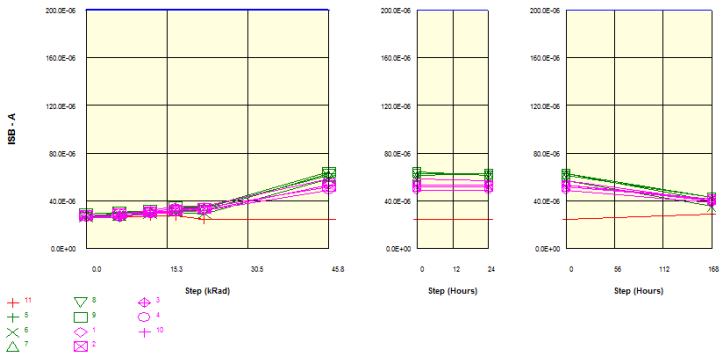
Parameter : Output High Voltage : [VOHIO[0]
Test conditions : IOH=-400uA Vcc = 3.3V
Unit : V
Spec Limit Min : 2.310
Spec Limit Max : 3.340
Spec limits are represented in bold lines on the graphic.



Parameter : Operating Current. Page Read with serial Access : [ICC1
Test conditions : Read Active Current on Target 0. MODE5
Unit : A
Spec Limit Max : 100.0E-03
Spec limits are represented in bold lines on the graphic.



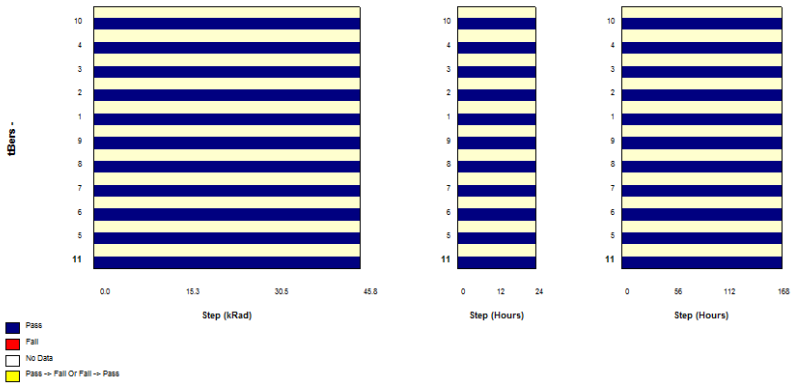
Parameter : Standby Current : [ISB]
Test conditions : CE/=VCC-0.2V. WP/=0V/VCC. VCC & VCCQ common
Unit : A
Spec Limit Max : 200.0E-06
Spec limits are represented in bold lines on the graphic.



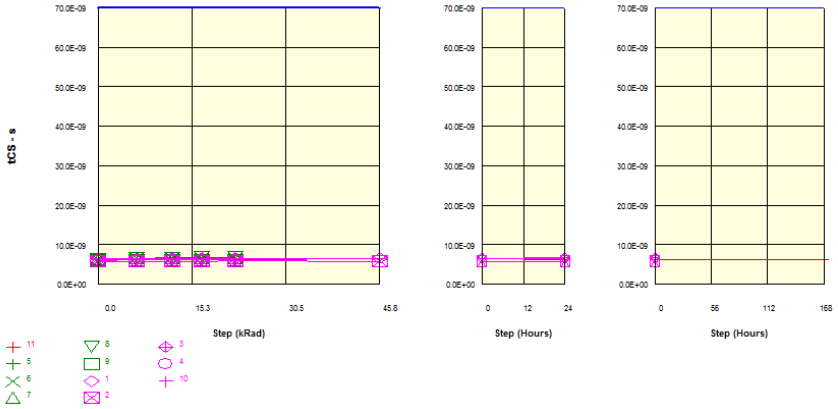
TID - Flash: MT29F128G08A (7/8)

Parameter : Program Time : [tProg]
Test conditions : PROGRAM PAGE operation time GO NOGO
Unit :
No spec limit specified.

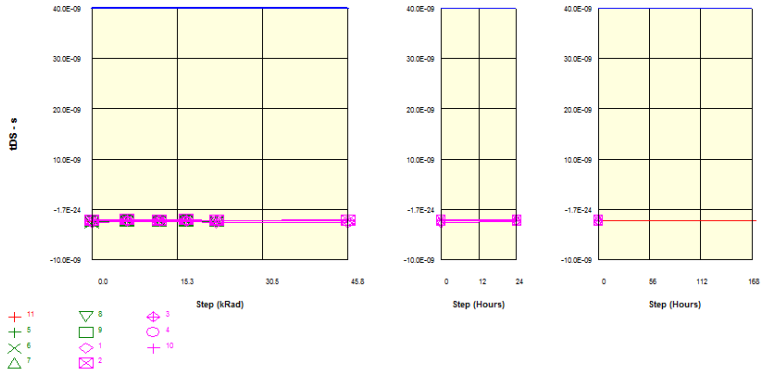
Parameter : Block Erase Time : [tBers]
Test conditions : BLOCK ERASE operation time . GO NOGO
Unit :
No spec limit specified.



Parameter : CE/ Setup Time : [tCS]
Test conditions :
Unit : s
Spec Limit Max : 70.0E-09
Spec limits are represented in bold lines on the graphic.

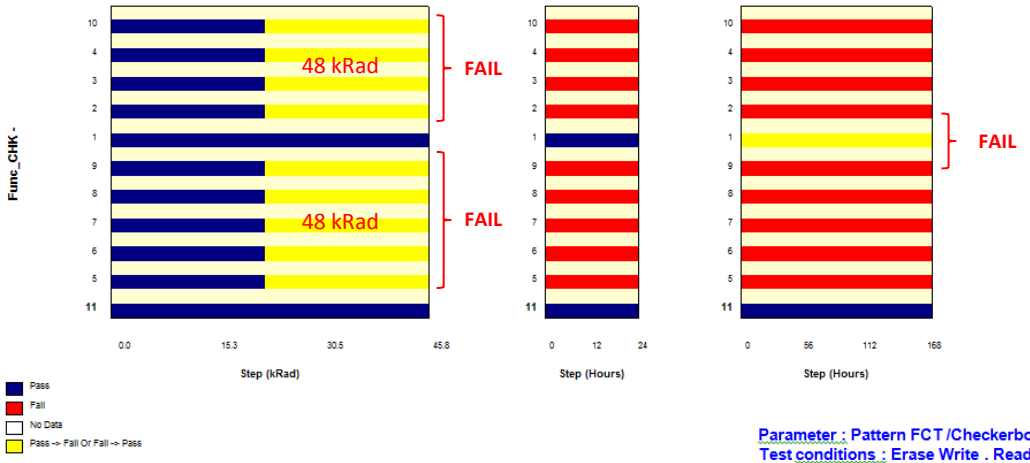


Parameter : Data Setup Time : [tDS]
Test conditions :
Unit : s
Spec Limit Max : 40.0E-09
Spec limits are represented in bold lines on the graphic.

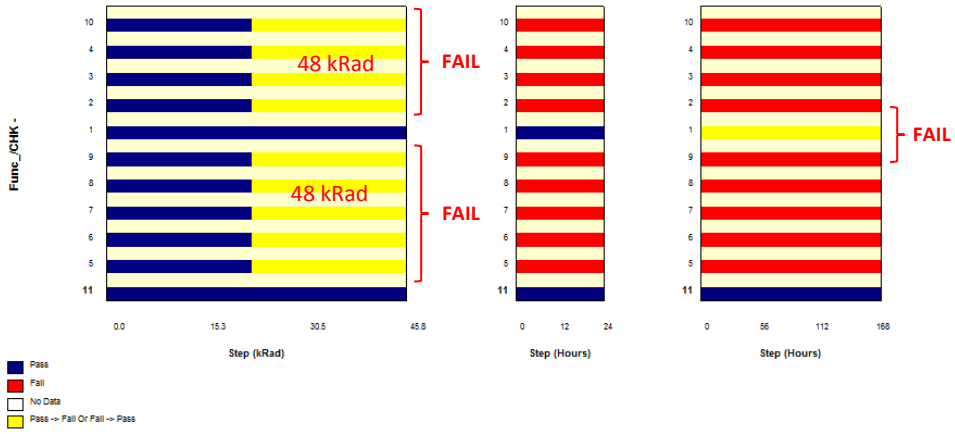


TID - Flash: MT29F128G08A (8/8)

Parameter : Pattern FCT Checkerboard : [Func_CHK]
Test conditions : Erase Write . Read block 0 with pattern Checkerboard 0x55 & 0xAA
Unit :
No spec limit specified.

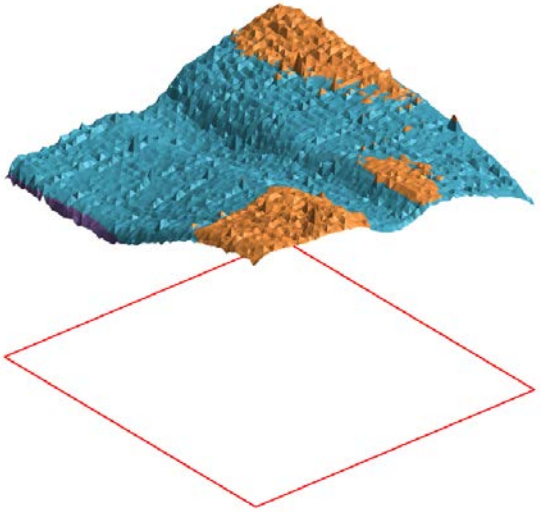


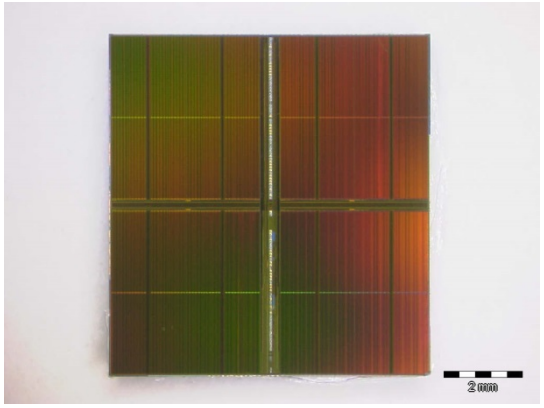
Parameter : Pattern FCT /Checkerboard : [Func_/CHK]
Test conditions : Erase Write . Read block 0 with pattern invers Checkerboard 0xAA & 0x55
Unit :
No spec limit specified.

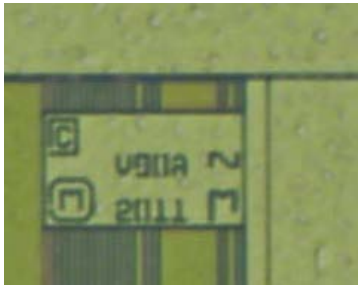


SEE - DDR3: IS46TR16256AL (1/4)

- Part type: IS46TR16256AL
- Part description: 4Gb DDR3 SDRAM
- Manufacturer: Integrated Silicon Solution, Inc
- Package: FBGA-96
- Die dimensions: 8.7 x 8.2 mm
- SEE testing:
  - TAMU, July 2014
- Irradiation performed in air exposure.







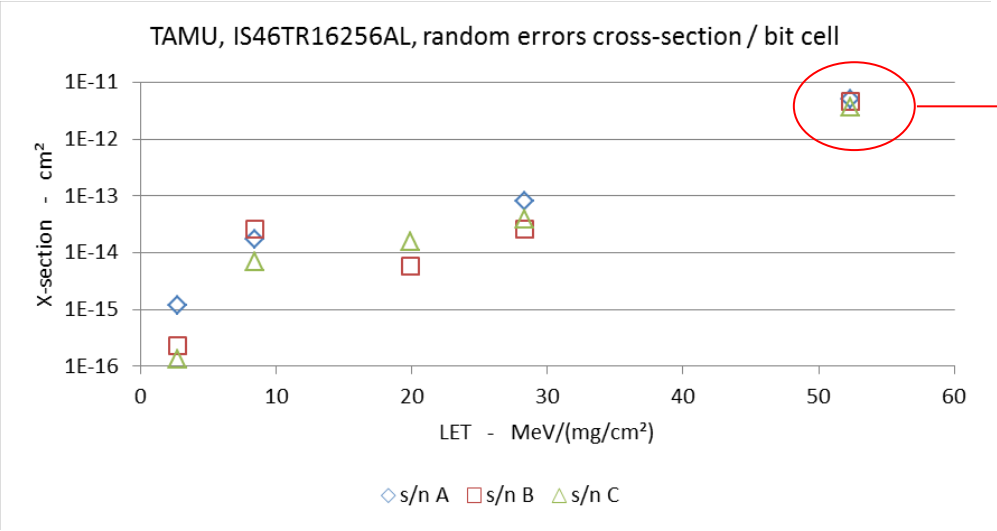
SEE - DDR3: IS46TR16256AL (2/4)

- One simple test sequence: 1 full array write followed by 2 full array reads, based on Xilinx “MIG 7 series” IP.
- Test done with a 800 MHz clock and 1.35 V.
  - Full array write is done in 200 µs.
  - Both full array read and compares are done in 1.5 s.

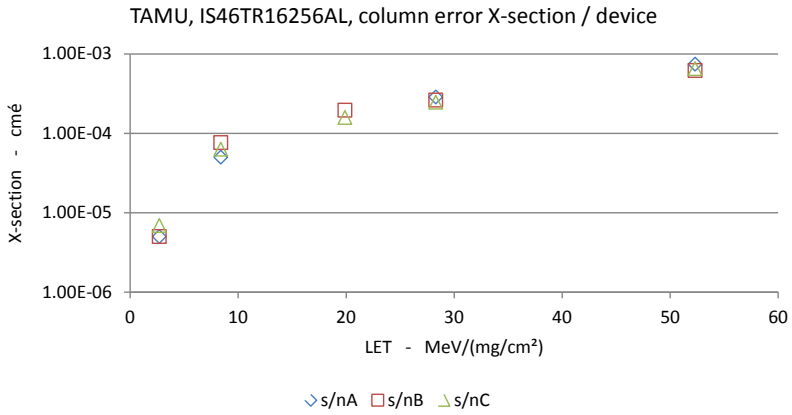
- No SEL up to 52.3 MeV.mg^{-1}.cm^{-2} (fluence 1E7 cm^{-2}) at room

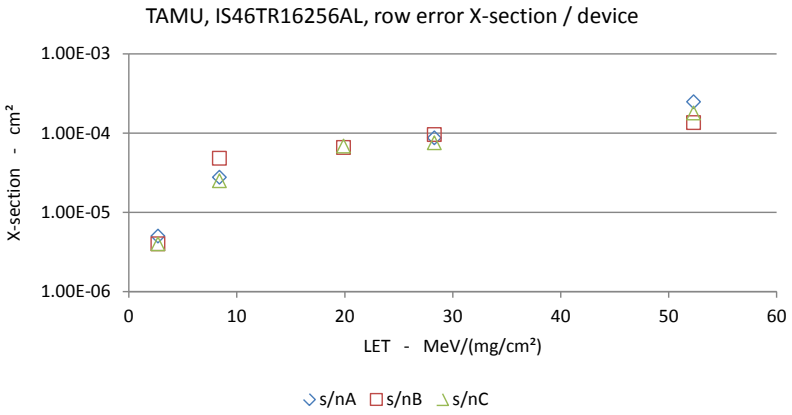
- SEU
  - Random errors, row errors and column errors starting at 2.7 MeV.mg^{-1}.cm^{-2}
  - Persistent errors (random single bit error) starting at 52.3 MeV.mg^{-1}.cm^{-2}
    - Further failure analysis will be performed by the CNES.
  - Most persistent errors cure after some time (annealing at 100 °C helps)
  - Large errors recover using power cycling (sole implemented SEFI counter-measure)

SEE - DDR3: IS46TR16256AL (3/4)



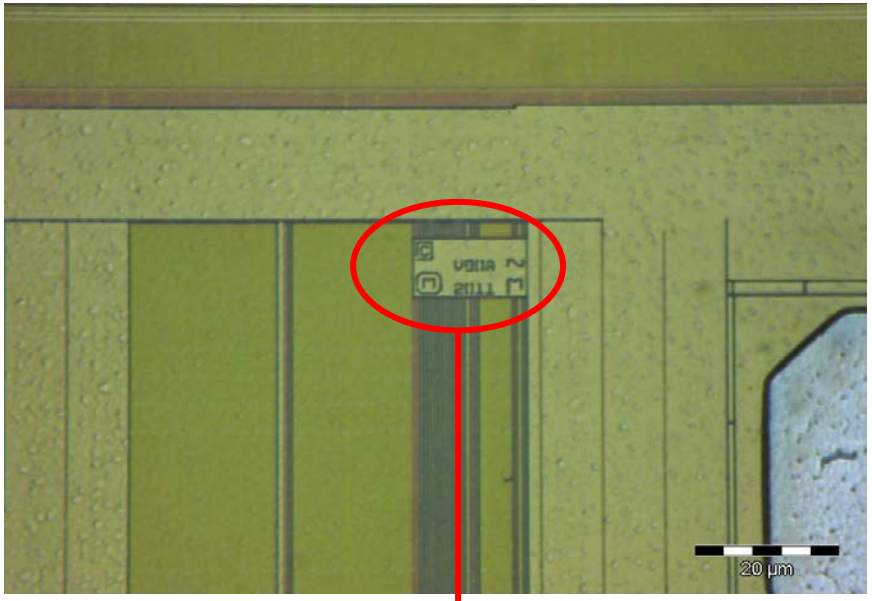
This point is not representative.
Most probably it's a combination of two phenomenon.
Either a different ion or a ion for which energy has been modified.



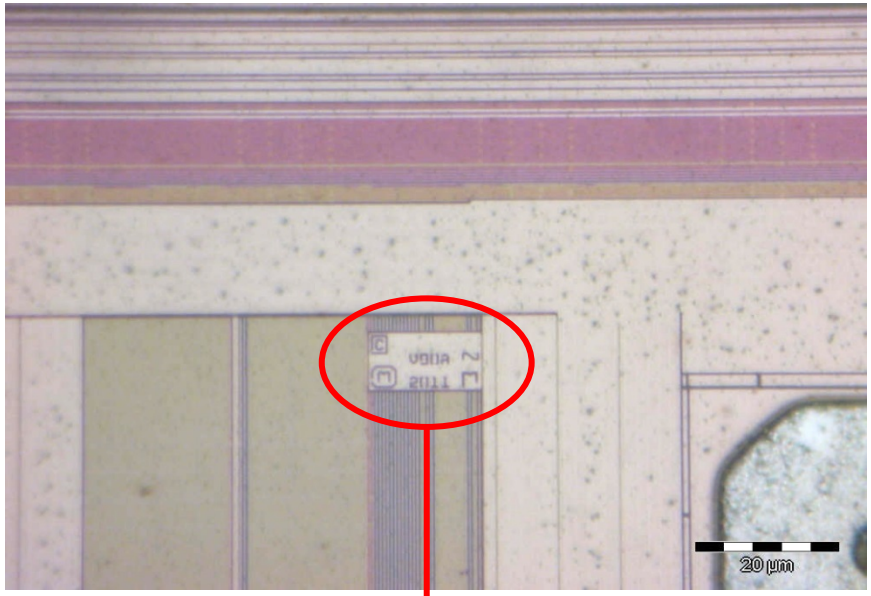


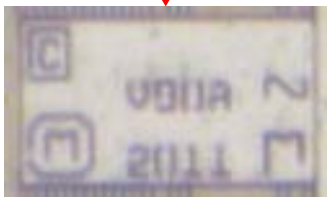
SEE - MT41K256M16HA DDR3 (4/4)

IS46TR16256AL



MT41K256M16HA-125AIT





Same mask die !

Radiation Final Presentation Days

Thank You !