Radiation Final Presentation Days

Tested parts
TID focus

In the scope of the ESA study:

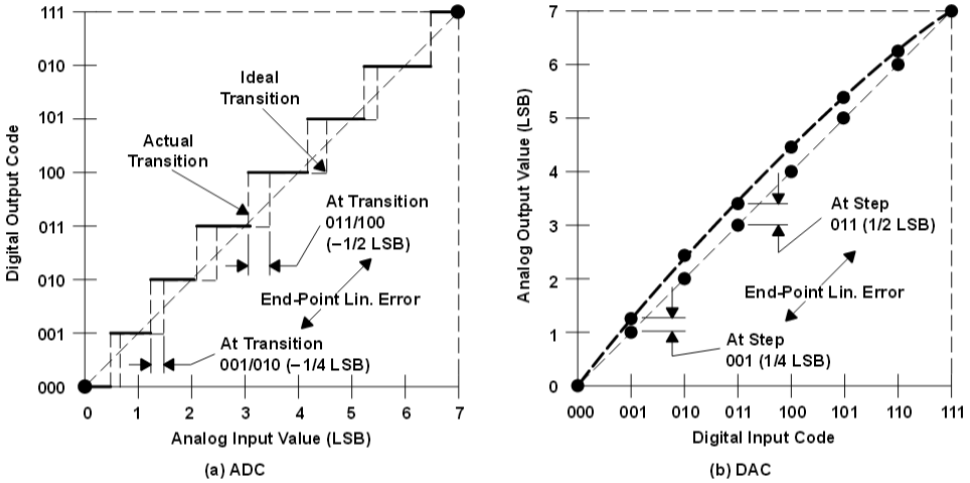
"Test Methods, Requirements, and Guidelines for Evaluation of Radiation Sensitivity of Analog to Digital Converters (ADC), Digital to Analog Converters (DAC) and Vertical Power MOSFETs".

A total dose radiation evaluation test of the following converters has been performed:

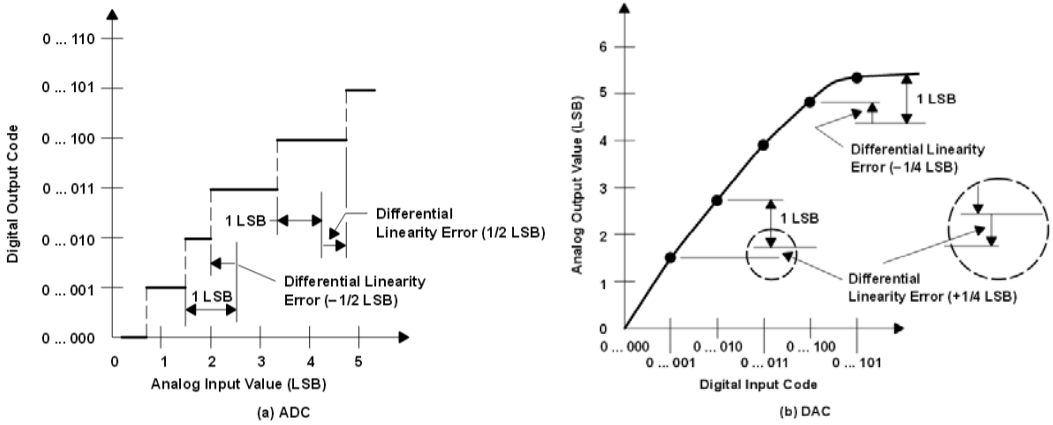
Part Type	Type	Manufacturer	Package	Function	Testing
AD976SD/883	ADC	Analog Device	DIL 28	16 bits 200 kSps	TID + SEE
ADC128S102	ADC	National Semiconductor	SO 16 WB	12 bits, 8 channel	TID + SEE
RHF1401KS01	ADC	STM	SO 48 WB	14 bits	TID + SEE
DAC5675AHFG	DAC	Texas Instruments	CQFP 52	14 bits 400 MSps with LVDS	TID + SEE

ADC and DAC glossary

- **INL: Integral Non linearity Error:** For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step.

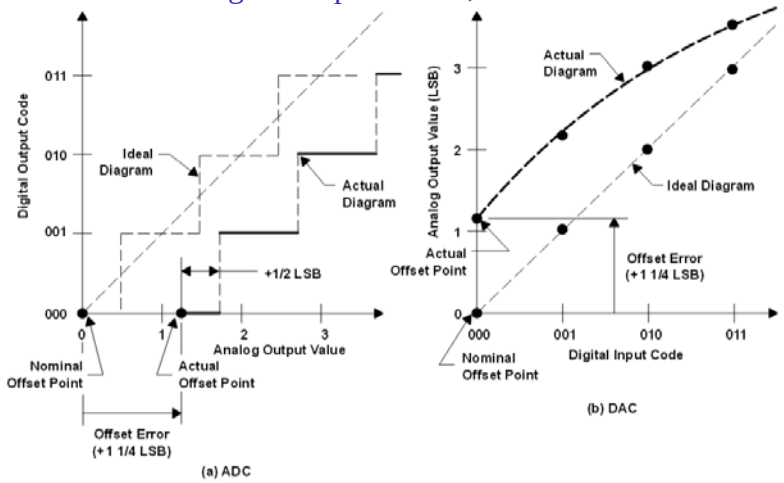


- **DNL: Differential Non linearity Error:** The differential nonlinearity error (sometimes seen as simply differential linearity) is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB.

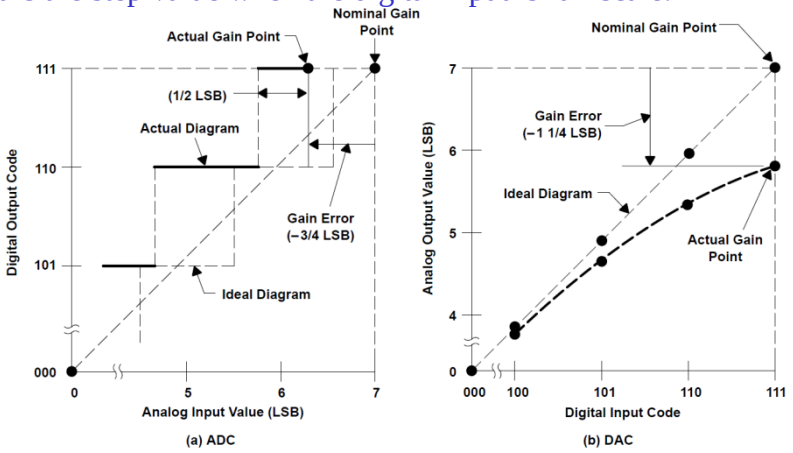


ADC and DAC glossary

- **OE: Offset Error:** The offset error is defined as the difference between the nominal and actual offset points. For an ADC, the offset point is the mid-step value when the digital output is zero, and for a DAC it is the step value when the digital input is zero.



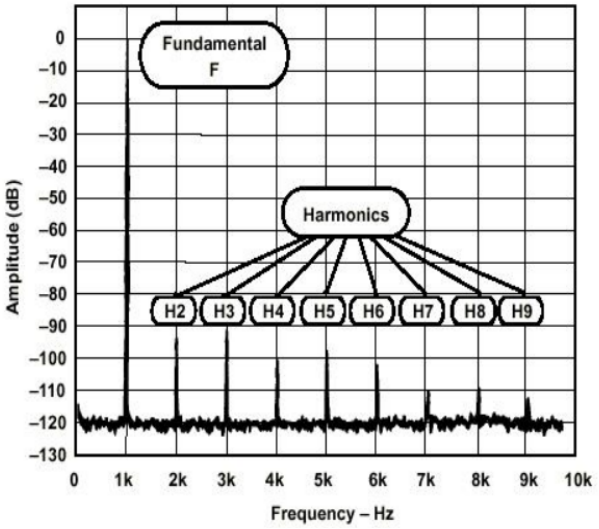
- **GE: Gain Error:** The gain error shown is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the mid-step value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale.



ADC and DAC glossary

- SNR: Signal to Noise Ration (without Harmonics).
- THD: Total Harmonic Distortion.
- SINAD: Signal to Noise And Distortion Ratio.

  Note: SINAD is often converted to effective number-of-bits (ENOB) using the relationship for the theoretical SNR of an ideal N-bit ADC



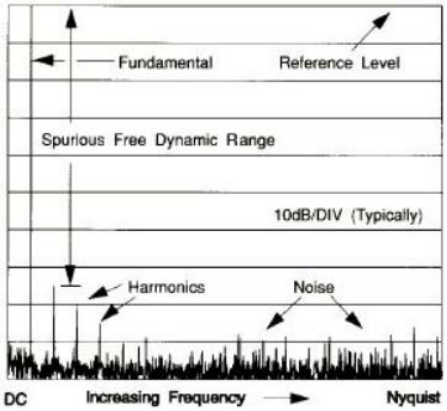
$$SNR\ (dB) = 20 \times \log \frac{E_F}{E_N}$$

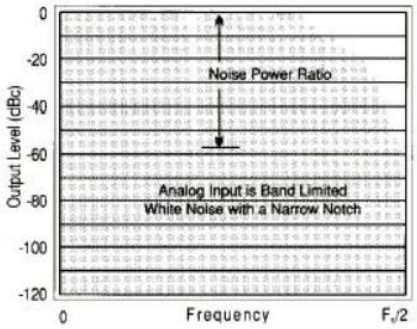
$$THD\ (dB) = 20 \times \log \frac{\sqrt{E_{H2}^2 + \ldots + E_{H9}^2}}{E_F}$$

$$THD+N\ (dB) = 20 \times \log \frac{\sqrt{E_{H2}^2 + \ldots + E_{H9}^2 + E_N^2}}{E_F}$$

$$SINAD = SNR + D = \frac{1}{THD + N}$$

- SFDR: Spurious Free Dynamic Range.





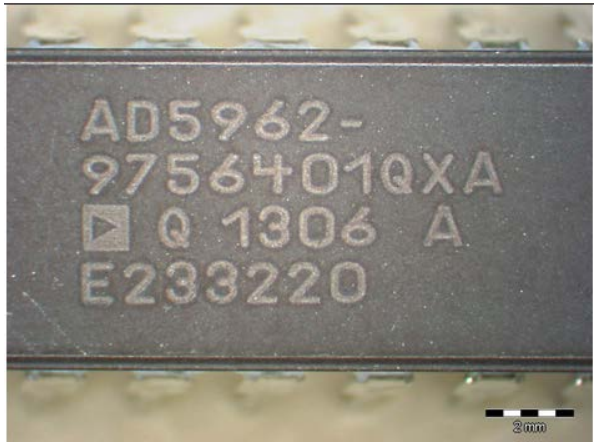
AD976SD/883 (1/10)

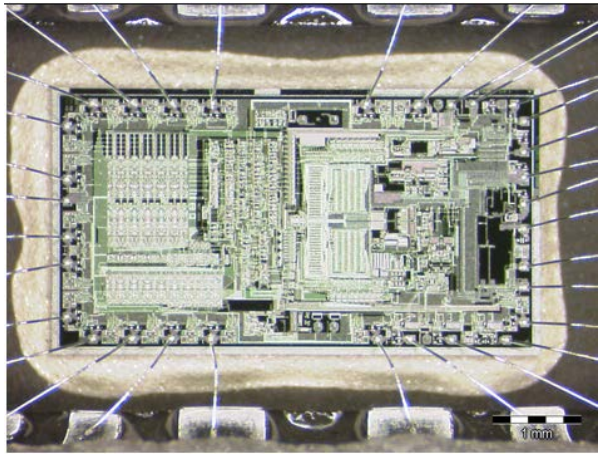
- Part type: AD976SD/883 (5962-9756401QXA)
- Part description: 16 bits 100kSps/200kSps BICMOS ADC
- Manufacturer: Analog Device
- Package: DIL 28
- Date code: 1306
- TID Testing: UCL, January and February 2012
- 11 samples tested (5xON, 5xOFF, 1xREF)
- Combining mixed mode tester and dedicated ADC/DAC tester
- Dynamic biasing for ON parts matching device applications scope
- Irradiation steps and dose rate (310 rad(Si)/hour):

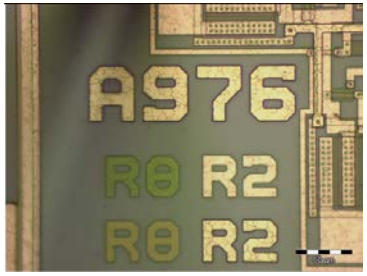
Serial Number (serialized by Hirex)	Allocation
1	Control
2	Biased ON
3	Biased ON
4	Biased ON
5	Biased ON
6	Biased ON
7	Biased OFF
8	Biased OFF
9	Biased OFF
10	Biased OFF
11	Biased OFF

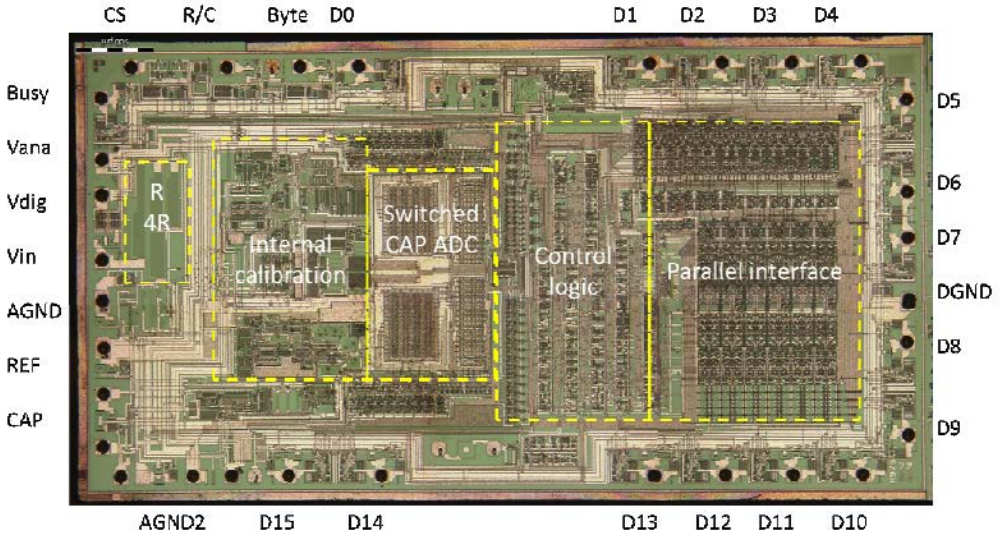
Irradiation Steps Requested	Dose rate	Annealing steps	Temperature
0 krad(Si)		-	Room
10 krad(Si)	310 rad(Si)/h	-	Room
20 krad(Si)	310 rad(Si)/h	-	Room
30 krad(Si)	310 rad(Si)/h	-	Room
50 krad(Si)	310 rad(Si)/h	-	Room
100 krad(Si)	310 rad(Si)/h	-	Room
-	-	24h	Room
-	-	+144h	Room
-	-	168h	100°C

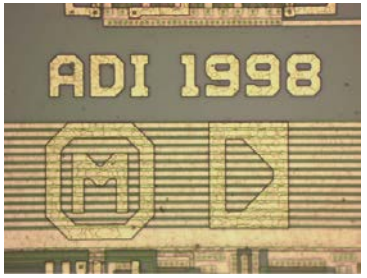
AD976SD/883 (2/10)











AD976SD/883 (3/10)

Results :

- **Biased ON samples:**
  - ✓ Electrical degradation starts at 20 kRad(Si) for bias ON parts only on ILINK/CS, BPZE, AP.
  - ✓ All bias ON parts are FAIL after 30 kRad(Si). Some devices have even lost their functionality.
  - ✓ Parts exhibit a positive recovery trend after annealing steps on almost all parameters except the dynamic ones such as INL, DNL, AP, SFDR, SINAD, THD etc. Nevertheless devices are still converting.

- **Biased OFF samples:**
  - ✓ Electrical degradation starts at 100 kRad(Si) for bias OFF parts on a few parameters mostly dynamic ones such as INL, SFDR and AN.
  - ✓ Bias OFF parts have recovered after annealing steps for AN parameters.
  - ✓ Bias OFF parts haven't recovered after annealing steps for INL and SFDR parameters.

AD976SD/883 (4/10)

PARAMETERS	SYMBOLS	TEST CONDITIONS VANA=5V, VDIG=5V, VREF=2.5V	MIN	MAX	UNITS
Logic input high Voltage	Vih			2	V
Logic input low Voltage	Vil		0.8		V
Logic Input current	ILINL	Vih=5V, Vil=0V	-10.0E-6	10.0E-6	A
Logic Input current	ILINH	Vih=5V, Vil=0V	-10.0E-6	10.0E-6	A
Logic output high voltage	VOH	IOH=0.5mA	4		V
logic output low voltage	VOL	IOL=1.6mA		0.4	V
Three state output leakage	IOLTL		-5.00E-06	5.00E-06	A
Three state output leakage	IOLTH		-5.00E-06	5.00E-06	A
Power dissipation	PD			0.1	W

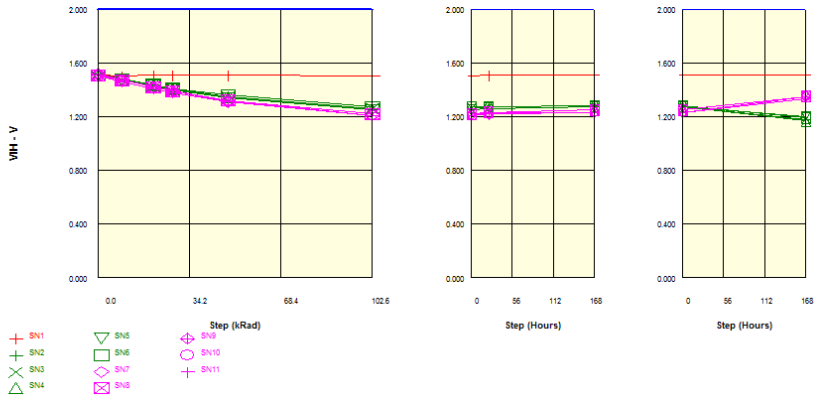
Note 1: Vin=-0.5dB, Fin=45 kHz, all measurement referred to a 0dB (20Vpp) input signal. THD includes first six harmonics, Bandwidth = 50 kHz.
Note 2: Iol=1.6mA; Ioh=500uA, Vcrossover 2.1V, Vol=0.4V, Voh=4V, Vil=0.8V, Vih=2V
Note 3: Measurement decomposed in t9_DV & t9_Z. t9_DV: all data valid. T9_Z: all data Z.
Note 4: Functionality tested at 2 extreme values of t13.
Note 5: Measurement decomposed in t14_DV & t14_Z. t14_DV: all data valid. T14_Z: all data Z.

AD976SD/883 (5/10)

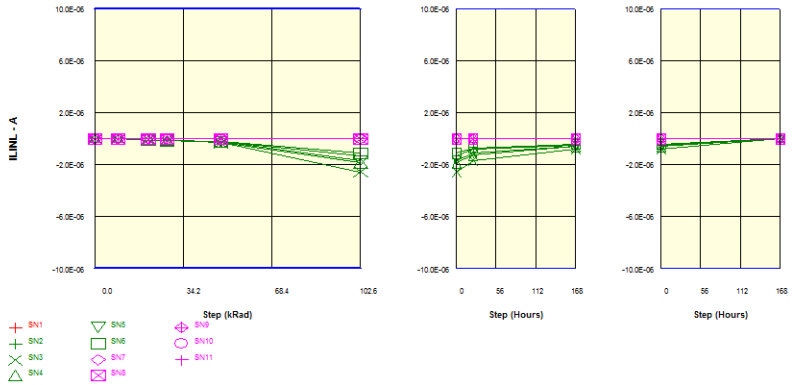
PARAMETERS	SYMBOLS	TEST CONDITIONS VANA=5V, VDIG=5V, VREF=2.5V	MIN	MAX	UNITS
Integral nonlinearity Positive	**INL_Positive**	All codes, fs=200ksps		2.5	LSB
Integral nonlinearity Negative	**INL_Negative**	All codes, fs=200ksps	-2.5		LSB
Differential nonlinearity	**DNL**	Go-noGo test, All codes, fs=200ksps, Minimum resolution for which "no missing codes" is guaranteed.	16 Bits		P/F
Bipolar zero error	**BPZE**	Code = 32767.5, Ta=+25°C, fs=200ksps	-0.01	0.01	V
Negative full scale error	**AN**	Code=0.5, Ta=+25°C, fs=200ksps	-0.25	0.25	%
Positive full scale error	**AP**	Code=65535.5, Ta=+25°C, fs=200ksps	-0.25	0.25	%
Signal-to-noise + distorsion	**S/(N+D)**	Fin=45KHz, fs=200ksps **Note 1**	84		dB
Total Harmonic Distorsion	**THD**	Fin=45KHz, fs=200ksps **Note 1**		-94	dB
Spurious free dynamic range	**SFDR**	Fin=45KHz, fs=200ksps	94		dB
Voltage reference output	**Vref**	Ta=+25°C	2.48	2.52	V
Power supply rejection	**PSR**	Vdig=Vana=5V □5%	-8	8	LSB
Convert pulse width	**t1**	**Note 2**		50.0E-9	s
Data valid after R//C low	**t2**	**Note 2**		4.0E-6	s
/BUSY low delay	**t3**	**Note 2**		100.0E-9	s
/BUSY low time	**t4**	**Note 2**		4.0E-6	s
Conversion time	**t7**	GO NOGO		4.0E-6	s
Acquisition time	**t8**	GO NOGO		1.0E-6	s
Bus relinquish	**t9**	**Note 2, Note 3**	10.0E-9	100.0E-9	s
Throughput time	**t11**	**Note 2**		5.0E-6	s
R//C to /CS setup	**t12**	**Note 2**		10.0E-9	s
Time between conversions	**t13**	GO NOGO, **Note 4**	5.0E-6	1.0E-3	s
Bus access and byte delay	**t14**	**Note 2, Note 5**	10.0E-9	100.0E-9	s

AD976SD/883 (6/10)

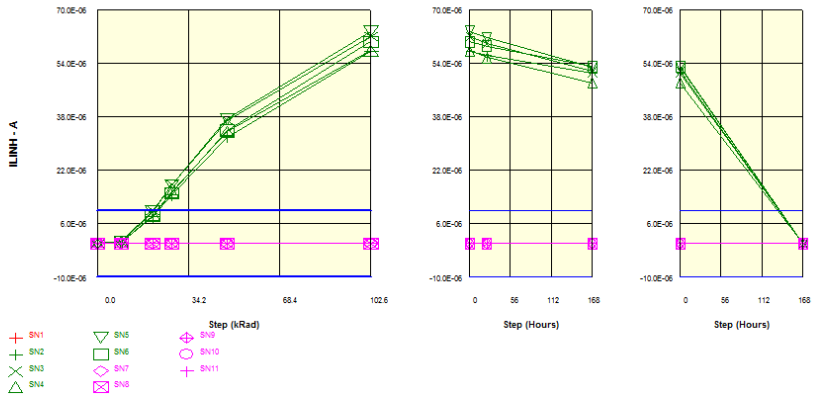
Parameter : Logic input high Voltage : [VIH/CS]
Test conditions :
Unit : V
Spec Limit Max : 2.000
Spec limits are represented in bold lines on the graphic.



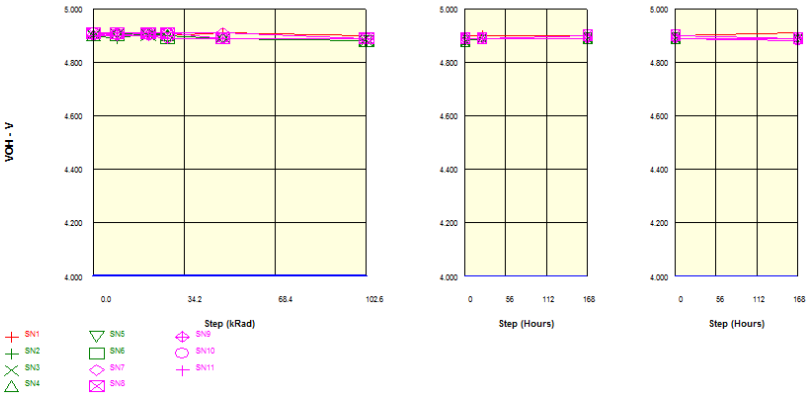
Parameter : Logic Input current : [ILINL/CS]
Test conditions : Vih=5V. Vil=0V
Unit : A
Spec Limit Min : -10.0E-06
Spec Limit Max : 10.0E-06
Spec limits are represented in bold lines on the graphic.



Parameter : Logic Input current : [ILINH/CS]
Test conditions : Vih=5V. Vil=0V
Unit : A
Spec Limit Min : -10.0E-06
Spec Limit Max : 10.0E-06
Spec limits are represented in bold lines on the graphic.

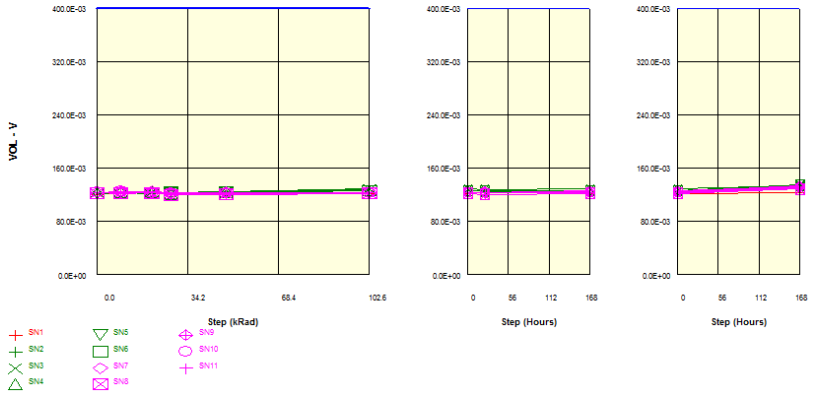


Parameter : Logic output high voltage : [VOHD15]
Test conditions : IOH=0.5mA
Unit : V
Spec Limit Min : 4.000
Spec limits are represented in bold lines on the graphic.

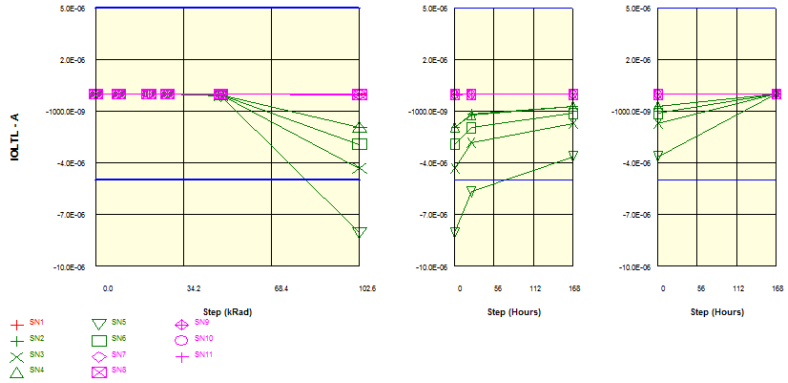


AD976SD/883 (7/10)

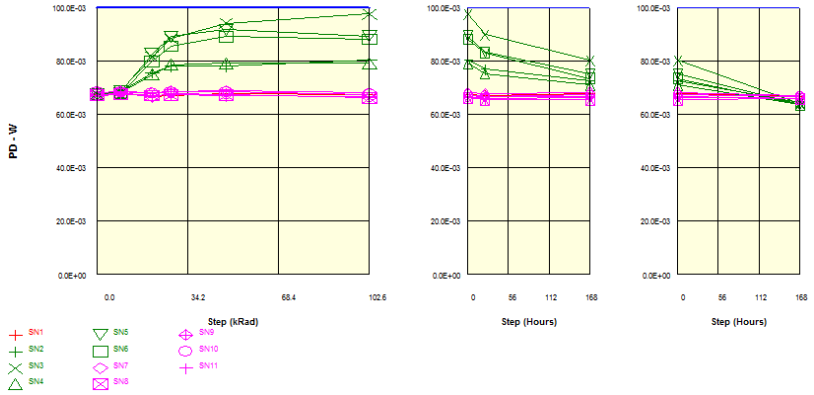
Parameter : logic output low voltage : VOLD
Test conditions : IOL=1.6mA
Unit : V
Spec Limit Max : 400.0E-03
Spec limits are represented in bold lines on the graphic.



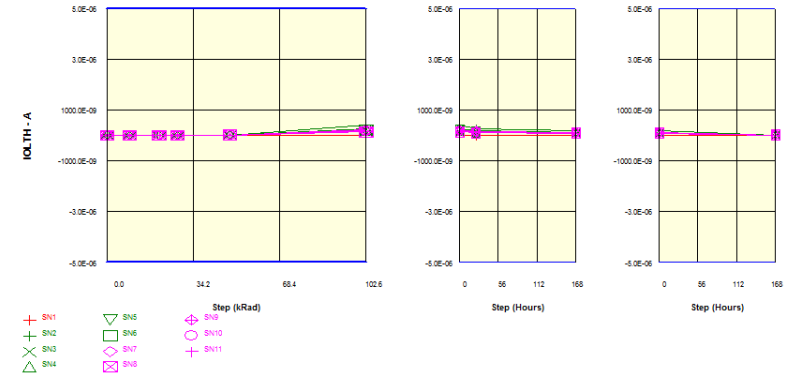
Parameter : Three state output leakage : IOLTLD1
Test conditions :
Unit : A
Spec Limit Min : -5.0E-06
Spec Limit Max : 5.0E-06
Spec limits are represented in bold lines on the graphic.



Parameter : Power dissipation : PD
Test conditions :
Unit : W
Spec Limit Max : 100.0E-03
Spec limits are represented in bold lines on the graphic.

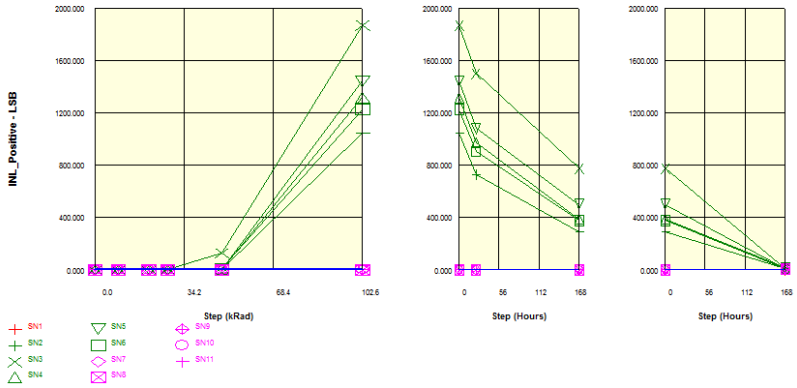


Parameter : Three state output leakage : IOLTHD
Test conditions :
Unit : A
Spec Limit Min : -5.0E-06
Spec Limit Max : 5.0E-06
Spec limits are represented in bold lines on the graphic.

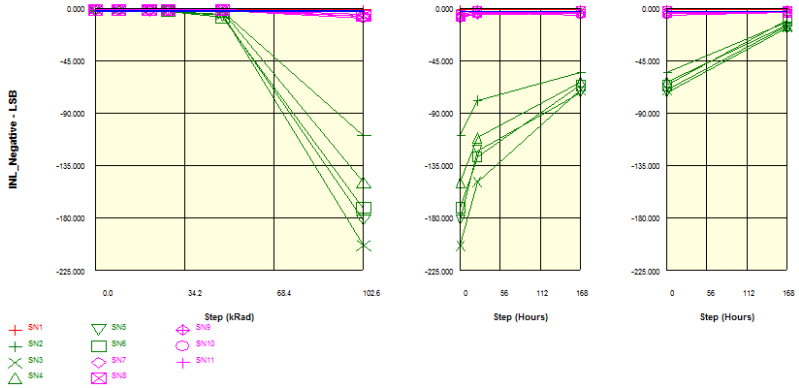


AD976SD/883 (8/10)

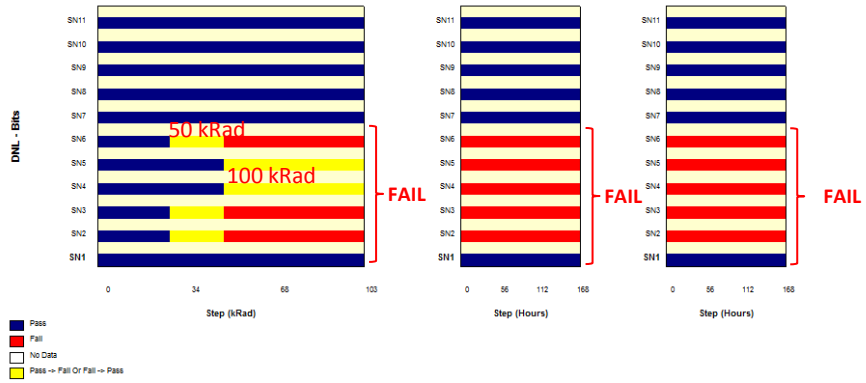
Parameter : Integral nonlinearity Positive : INL_Positive
Test conditions : All codes
Unit : LSB
Spec Limit Max : 2.500
Spec limits are represented in bold lines on the graphic.



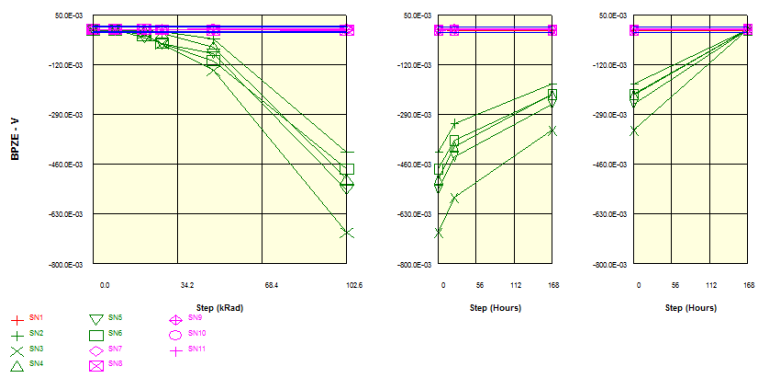
Parameter : Integral nonlinearity Negative : INL_Negative
Test conditions : All codes
Unit : LSB
Spec Limit Min : -2.500
Spec limits are represented in bold lines on the graphic.



Parameter : Differential nonlinearity : DNL
Test conditions : All codes? Minimum resolution for which "no missing codes" is guaranteed.
Unit : Bits
Spec Limit Min : 16
Spec limits are represented in bold lines on the graphic.

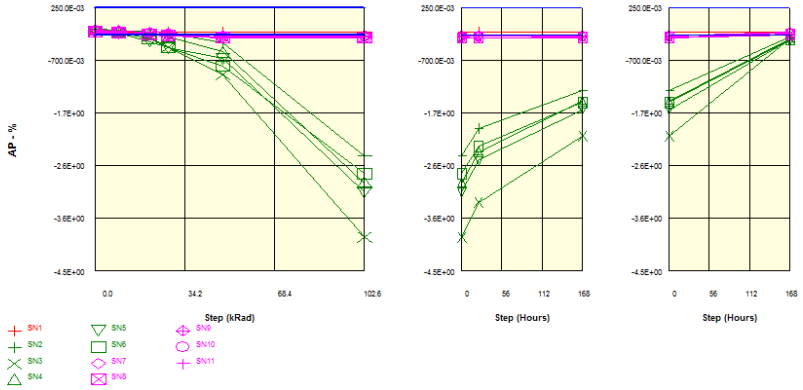


Parameter : Bipolar zero error : BPZE
Test conditions : Code = 32767.5. Ta=+25°C
Unit : V
Spec Limit Min : -10.0E-03
Spec Limit Max : 10.0E-03
Spec limits are represented in bold lines on the graphic.

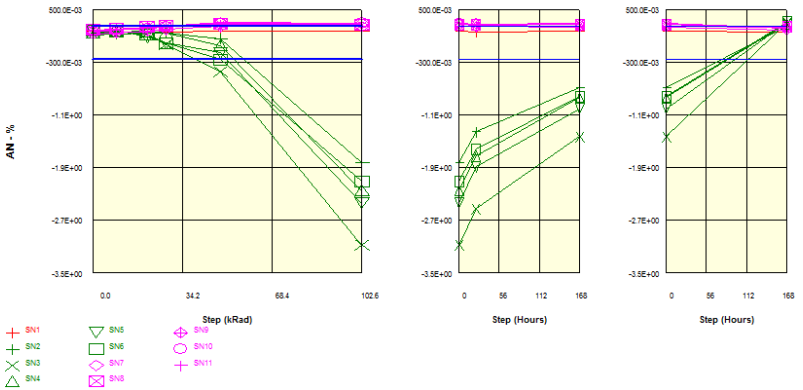


AD976SD/883 (9/10)

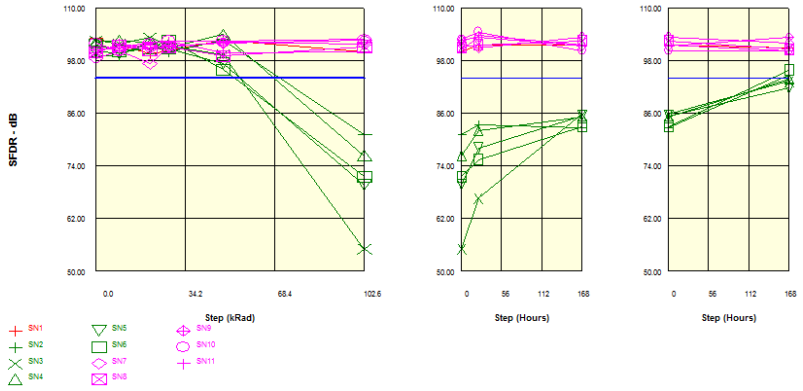
Parameter : Positive full scale error : [AP]
Test conditions : Code=65535.5. Ta=+25°C
Unit : %
Spec Limit Min : -250.0E-03
Spec Limit Max : 250.0E-03
Spec limits are represented in bold lines on the graphic.



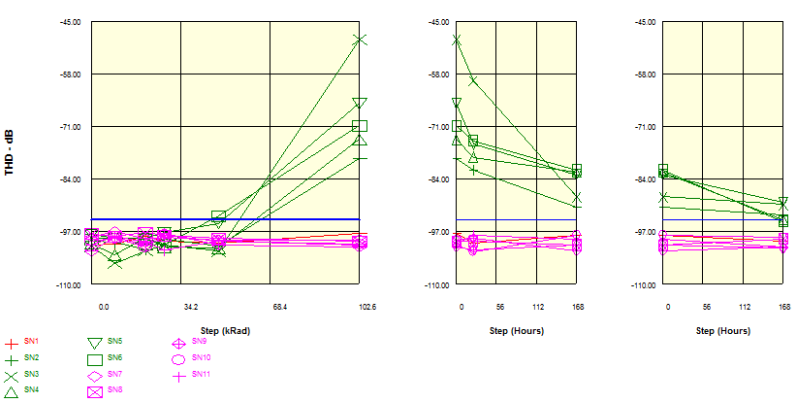
Parameter : Negative full scale error : [AN]
Test conditions : Code=0.5. Ta=+25°C
Unit : %
Spec Limit Min : -250.0E-03
Spec Limit Max : 250.0E-03
Spec limits are represented in bold lines on the graphic.



Parameter : Spurious free dynamic range : [SFDR]
Test conditions : Fin=45KHz
Unit : dB
Spec Limit Min : 94.00
Spec limits are represented in bold lines on the graphic.

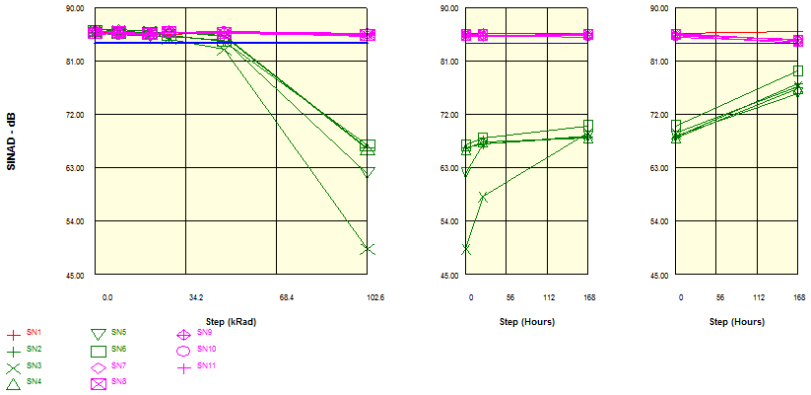


Parameter : Total Harmonic Distorsion : [THD]
Test conditions : Fin=45KHz. Vin=-0.5dB. Fin=45KHz. all measurement referred to a 0dB (20Vpp) input signal. THD includes firs harmonics. Bandwidth =50kHz
Unit : dB
Spec Limit Max : -94.00
Spec limits are represented in bold lines on the graphic.

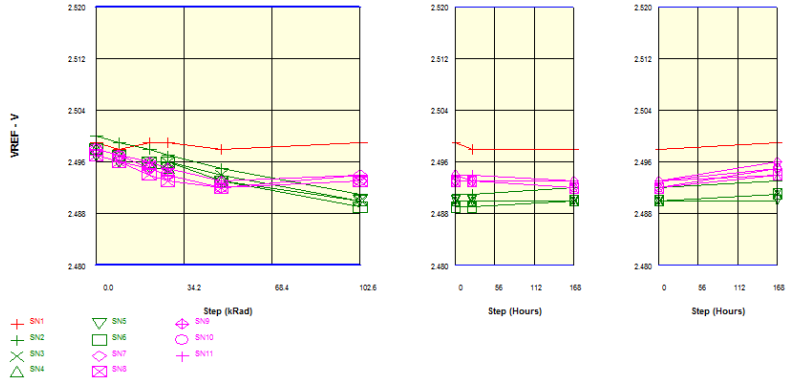


AD976SD/883 (10/10)

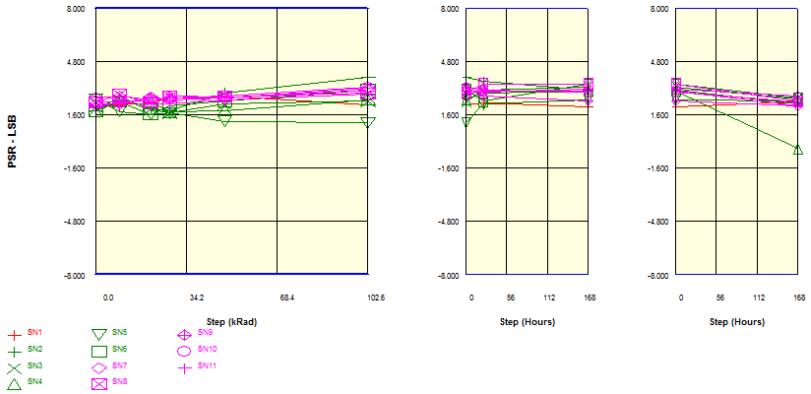
Parameter : Signal-to-noise + distorsion : [SINAD]
Test conditions : Fin=45KHz. Vin=-0.5dB. Fin=45KHz. all measurement referred to a 0dB (20Vpp) input signal
Unit : dB
Spec Limit Min : 84.00
Spec limits are represented in bold lines on the graphic.



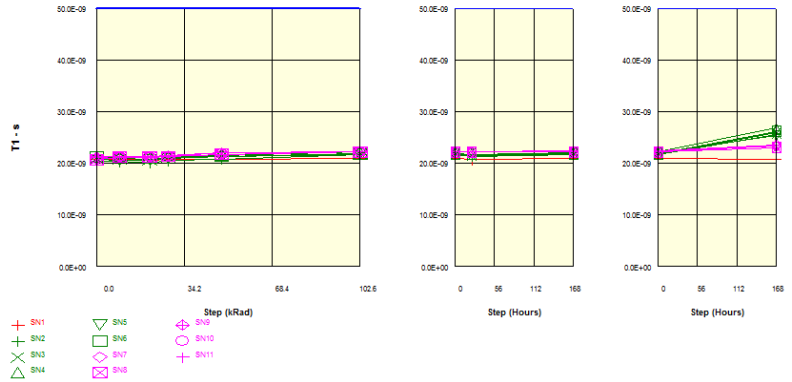
Parameter : Voltage reference output : [VREF]
Test conditions : Ta=+25°C
Unit : V
Spec Limit Min : 2.480
Spec Limit Max : 2.520
Spec limits are represented in bold lines on the graphic.



Parameter : Power supply rejection : [PSR]
Test conditions : Vdig=Vana=5V +/-5%
Unit : LSB
Spec Limit Min : -8.000
Spec Limit Max : 8.000
Spec limits are represented in bold lines on the graphic.



Parameter : Convert pulse width : [T1]
Test conditions : Iol=1.6mA; Ioh=500uA. Vcrossover 2.1V. Vol=0.4V. Voh=4V
Unit : s
Spec Limit Max : 50.0E-09
Spec limits are represented in bold lines on the graphic.



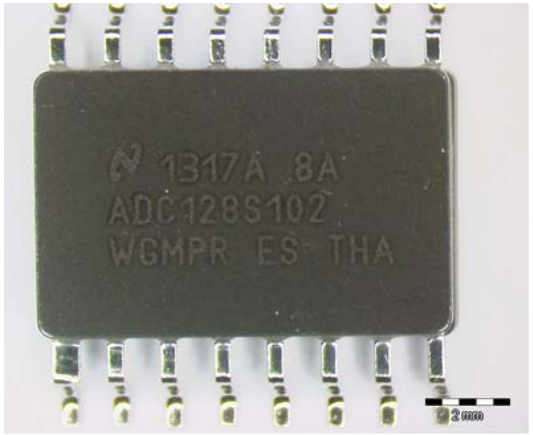
ADC128S102 (1/8)

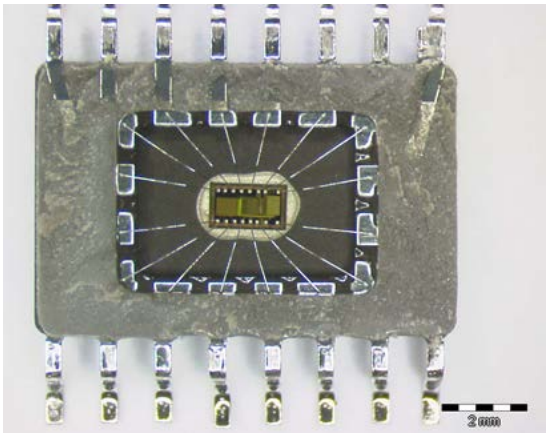
- Part type: ADC128S102WGMPR
- Part description: 12 bits 8 channels ADC
- Manufacturer: National Semiconductor
- Package: SO 16 WB
- Date code: 1317A
- TID Testing: UCL, May and June 2014
- 11 samples tested (5xON, 5xOFF, 1xREF)
- Combining mixed mode tester and dedicated ADC/DAC tester
- Dynamic biasing for ON parts matching device applications scope
- Irradiation steps and dose rate (310 rad(Si)/hour):

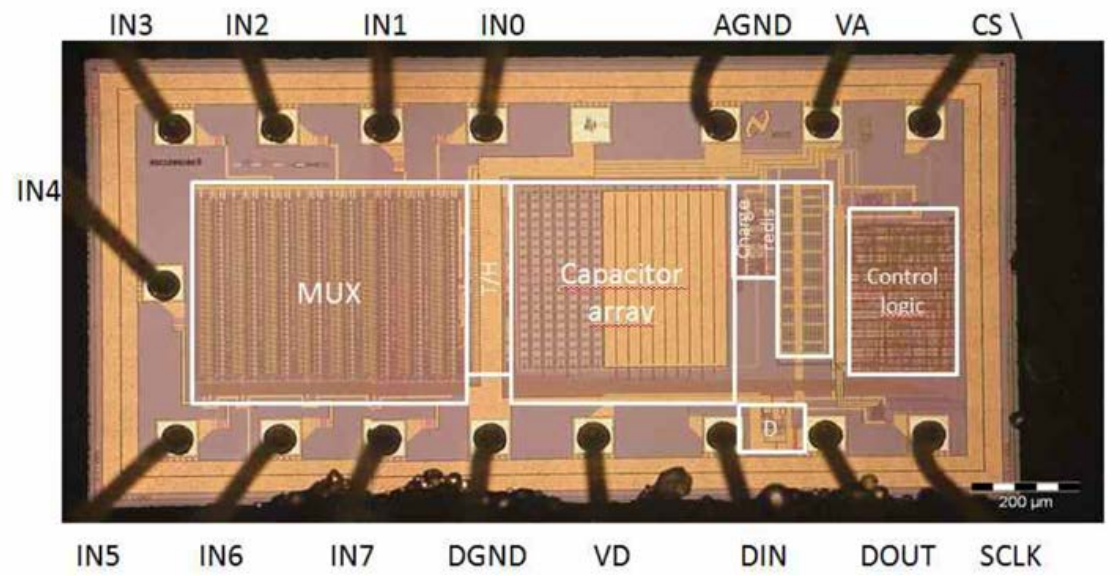
Serial Number (serialized by Hirex)	Allocation
1	Control
2	Biased ON
3	Biased ON
4	Biased ON
5	Biased ON
6	Biased ON
7	Biased OFF
8	Biased OFF
9	Biased OFF
10	Biased OFF
11	Biased OFF

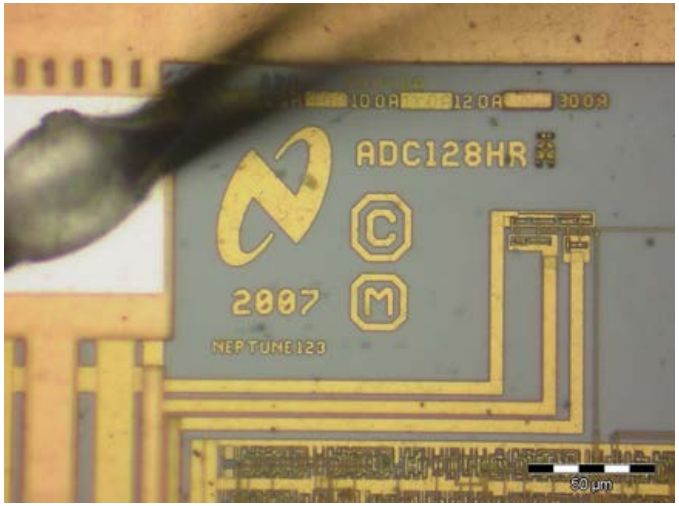
Irradiation Steps Requested	Dose rate	Annealing steps	Temperature
0 krad(Si)		-	Room
10 krad(Si)	310 rad(Si)/h	-	Room
20 krad(Si)	310 rad(Si)/h	-	Room
30 krad(Si)	310 rad(Si)/h	-	Room
50 krad(Si)	310 rad(Si)/h	-	Room
100 krad(Si)	310 rad(Si)/h	-	Room
-	-	24h	Room
-	-	+144h	Room
-	-	168h	100°C

ADC128S102 (2/8)









ADC128S102 (3/8)

Results :

- **Biased ON samples:**
  - ✓ Dynamic parameters seems to be more sensitive with a 3V PSU than 5V.
  - ✓ Static parameters, especially current and power consumption are more sensitive with a 5V PSU than 3V.
    - o Two FAIL parts (SN4 and 5) observed at 100 kRad(Si) step on DNL and IOZH @ 3V PSU
    - o Same FAIL parts (SN4 and SN5) observed at 50 kRad(Si) step on Supply current IA and Power consumption (PC) in IDDLE mode @ 3V PSU.
    - o Same FAIL parts (SN4 and SN5) observed at 50 kRad(Si) step on current an power consumption in IDDLE MODE @ 5V PSU.
    - o Same FAIL parts (SN4 and SN5) observed at 100 kRad(Si) step on current an power consumption in NORMAL MODE @ 5V PSU.
    - o Almost all FAIL parts have recovered after annealing except on Power consumption, nevertheless final value is very close from the limits.

- **Biased OFF samples:**
  - ✓ No failure for the bias OFF parts observed.

ADC128S102 (4/8)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN	MAX	UNITS
		fsclk=16MHz, fsample=1MSPS, VA=VD=3V			
Integral Non linearity	INL_3V+_INX	Note 1	-1	1.1	LSB
Integral Non linearity	INL_3V-_INX	Note 1	-1	1.1	LSB
Differential Non linearity	DNL_3V+_INX	Note 1	-0.7	0.9	LSB
Differential Non linearity	DNL-_3V_INX	Note 1	-0.7	0.9	LSB
Offset Error	Voff_3V_INX	Note 1	-2.3	2.3	LSB
Full Scale Error	FSE_3V_INX	Note 1	-2	2	LSB
Signal to noise ratio	SNR_3V_INX	fIN=40.2kHz, -0.02dBFS Note 1	69		dB
Signal to noise + distorsion	SINAD_3V_INX	fIN=40.2kHz, -0.02dBFS Note 1	68		dB
Total Harmonic Distorsion	THD_3V_INX	fIN=40.2kHz, -0.02dBFS Note 1		-74	dB
Peak Harmonic or spurious noise	SFDR_3V_INX	fIN=40.2kHz, -0.02dBFS Note 1	75		dB
Effective Number of bit	ENOB_3V_INX	fIN=40.2kHz, -0.02dBFS Note 1	11.1		bits
Input Leakage Current Low	IIL_3V	Vin=0V	-1.0E-6	1.0E-6	A
Input Leakage Current High	IIH_3V	Vin=3V	-1.0E-6	1.0E-6	A
Input Leakage Current Low	Ileak_INX_3V	VIN_X= 3V Note 1	-1.0E-6	1.0E-6	A
Output Low Voltage	VOL_3V	Isink=1mA		0.4	V
Output High Voltage	VOH_3V	Isource=200µA	2.5		V
Input Low /High Voltage	VIL/VIH_3V	GO NOGO Test, VIL=0.8V, VIH=2.1V			P/F
Ouptut Leakage Current Z	IOZL_3V		-10.0E-6	10.0E-6	A
Ouptut Leakage Current Z	IOZH_3V		-10.0E-6	10.0E-6	A
Total supply Current Normal	IA_ID_NORM_3V	fSample=1MSPS, fIN=40kHz VIL=0V VIH=3V		1.5E-3	A
Total supply Current Shutdown	IA_ID_IDLE_3V	fSCLK=0kSPS		30.0E-6	A
Power Consumption Normal	PC_NORM_3V	fSample=1MSPS, fIN=40kHz		4.5E-3	W
Power Consumption Shutdown	PC_IDLE_3V	fSCLK=0kSPS		90.0E-6	W

Note 1: these measurements are done on each channel: X suffix indicates channel number => INX with X= 0 to 7

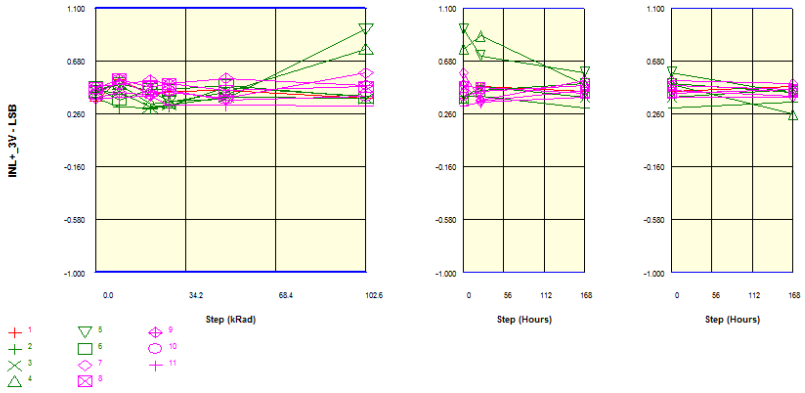
ADC128S102 (5/8)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN	MAX	UNITS
		fsclk=16MHz, fsample=1MSPS, VA=VD=5V			
Integral Non linearity	INL+_5V_INX	Note 2	-1.25	1.4	LSB
Integral Non linearity	INL-_5V_INX	Note 2	-1.25	1.4	LSB
Differential Non linearity	DNL+_5V_INX	Note 2	-0.9	1.5	LSB
Differential Non linearity	DNL-_5V_INX	Note 2	-0.9	1.5	LSB
Offset Error	Voff_5V_INX	Note 2	-2.3	2.3	LSB
Full Scale Error	FSE_5V_INX	Note 2	-2	2	LSB
Signal to noise ratio	SNR_5V_INX	fIN=40.2kHz, -0.02dBFS Note 2	68.5		dB
Signal to noise + distorsion	SINAD_5V_INX	fIN=40.2kHz, -0.02dBFS Note 2	68		dB
Total Harmonic Distorsion	THD_5V_INX	fIN=40.2kHz, -0.02dBFS Note 2		-74	dB
Peak Harmonic or spurious noise	SFDR_5V_INX	fIN=40.2kHz, -0.02dBFS Note 2	75		dB
Effective Number of bit	ENOB_5V_INX	fIN=40.2kHz, -0.02dBFS Note 2	11.1		bits
Input Leakage Current Low	IIL_5V	Vin=0V	-1.0E-6	1.0E-6	A
Input Leakage Current High	IIH_5V	Vin=5V	-1.0E-6	1.0E-6	A
Input Leakage Current Low	Ileak_INX_5V	VIN_X= 5V Note 2	-1.0E-6	1.0E-6	A
Output Low Voltage	VOL_5V	Isink=1mA		0.4	V
Output High Voltage	VOH_5V	Isource=200µA	4.5		V
Input Low /High Voltage	VIL/VIH_5V	GO NOGO Test, VIL=0.8V, VIH=2.4V			P/F
Ouptut Leakage Current Z	IOZL_5V		-10.0E-6	10.0E-6	A
Ouptut Leakage Current Z	IOZH_5V		-10.0E-6	10.0E-6	A
Total Sypply Current Normal	IA_ID_NORM_5V	fSample=1MSPS, fIN=40kHz, VIL=0V VIH=3.3V		3.1E-3	A
Total supply Current Shutdown	IA_ID_IDLE_5V	fSCLK=0kSPS		100.0E-6	A
Power Consumption Normal	PC_NORM_5V	fSample=1MSPS, fIN=40kHz		15.5E-3	W
Power Consumption Shutdown	PC_IDLE_5V	fSCLK=0kSPS		500.0E-6	W

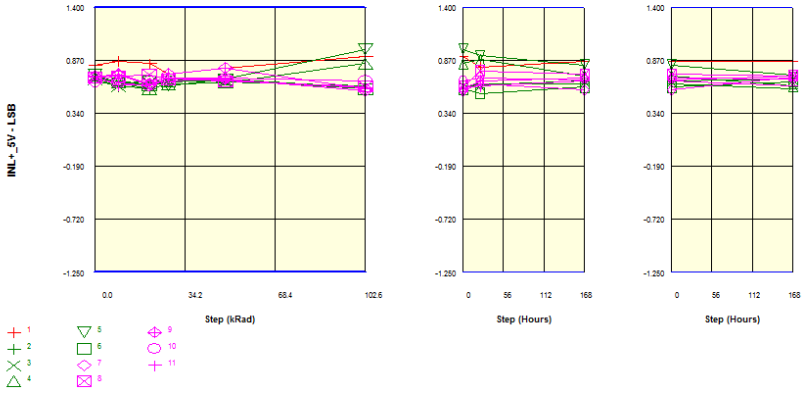
Note 2: these measurements are done on each channel: X suffix indicates channel number => INX with X= 0 to 7

ADC128S102 (6/8)

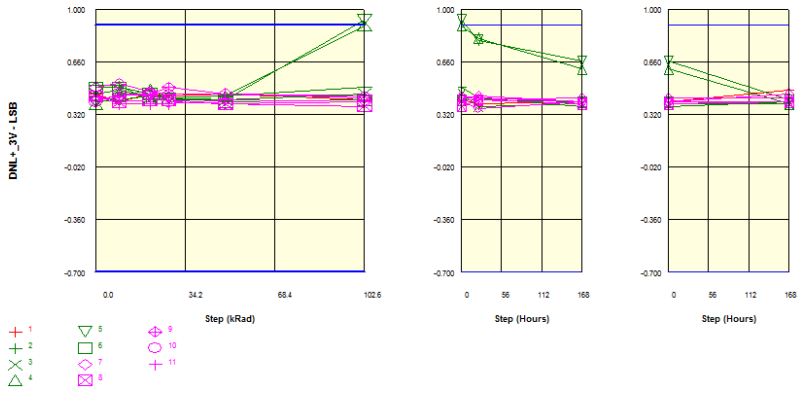
Parameter : Integral Non linearity : INL+_3VIN
Test conditions : INX => X= 0 to 7
Unit : LSB
Spec Limit Min : -1.000
Spec Limit Max : 1.100
Spec limits are represented in bold lines on the graphic.



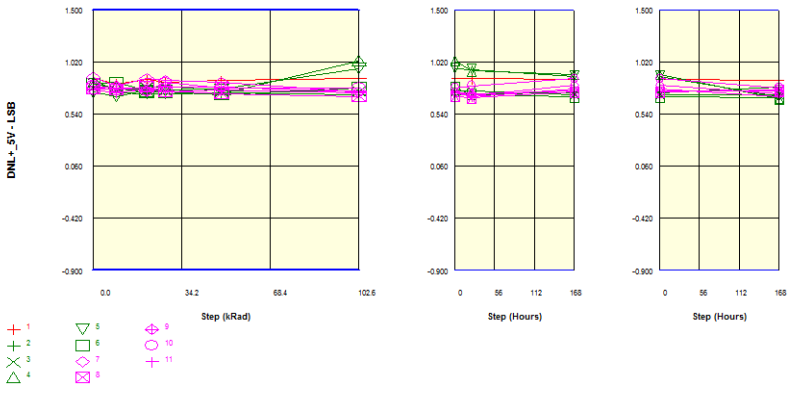
Parameter : Integral Non linearity : INL+_5VIN
Test conditions : INX => X= 0 to 7
Unit : LSB
Spec Limit Min : -1.250
Spec Limit Max : 1.400
Spec limits are represented in bold lines on the graphic.



Parameter : Differential Non linearity : DNL+_3VIN
Test conditions : INX => X= 0 to 7
Unit : LSB
Spec Limit Min : -0.700
Spec Limit Max : 0.900
Spec limits are represented in bold lines on the graphic.

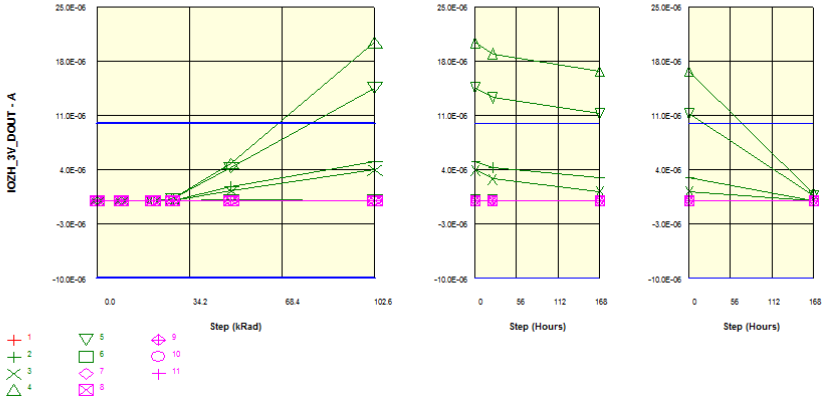


Parameter : Differential Non linearity : DNL+_5VIN
Test conditions : INX => X= 0 to 7
Unit : LSB
Spec Limit Min : -0.900
Spec Limit Max : 1.500
Spec limits are represented in bold lines on the graphic.

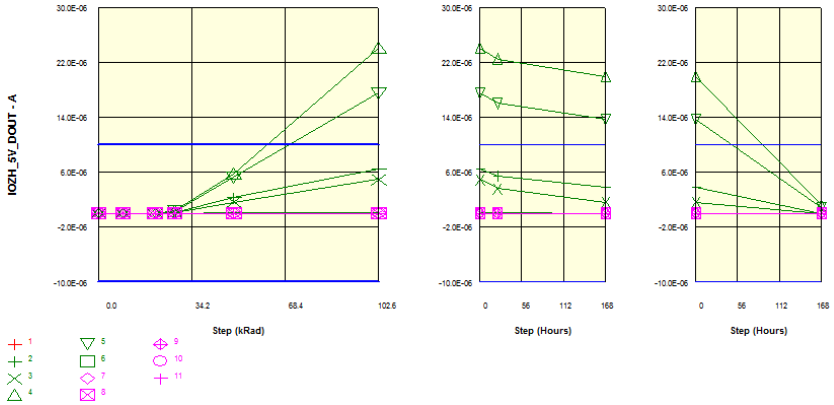


ADC128S102 (7/8)

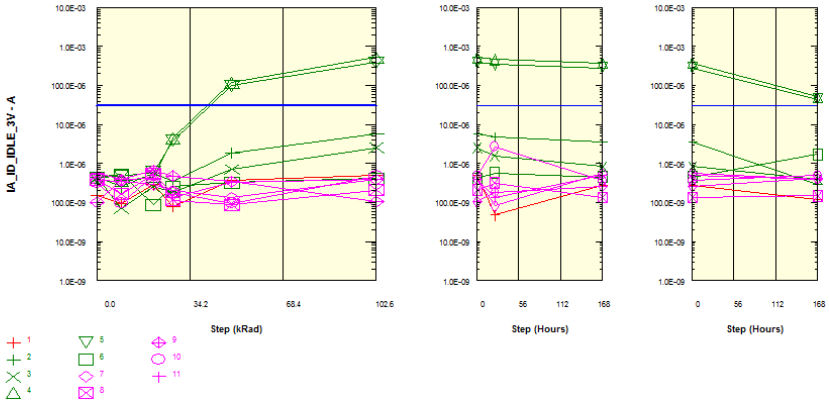
Parameter : Ouptut Leakage Current Z : IOZH_3V_DOUT
Test conditions :
Unit : A
Spec Limit Min : -10.0E-06
Spec Limit Max : 10.0E-06
Spec limits are represented in bold lines on the graphic.



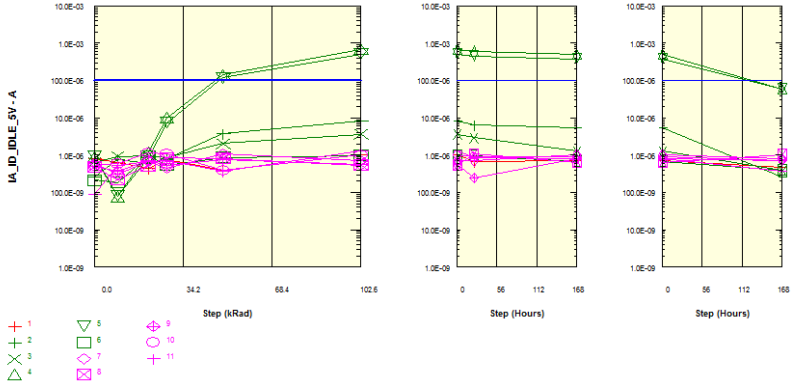
Parameter : Ouptut Leakage Current Z : IOZH_5V_DOUT
Test conditions :
Unit : A
Spec Limit Min : -10.0E-06
Spec Limit Max : 10.0E-06
Spec limits are represented in bold lines on the graphic.



Parameter : Total supply Current Shutdown : IA_ID_IDLE_3V
Test conditions : fSCLK=0kSPS
Unit : A
Spec Limit Max : 30.0E-06
Spec limits are represented in bold lines on the graphic.

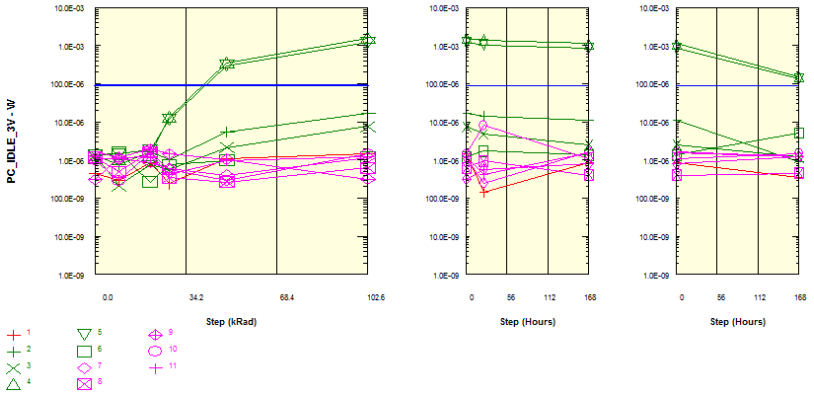


Parameter : Total supply Current Shutdown : IA_ID_IDLE_5V
Test conditions : fSCLK=0kSPS
Unit : A
Spec Limit Max : 100.0E-06
Spec limits are represented in bold lines on the graphic.

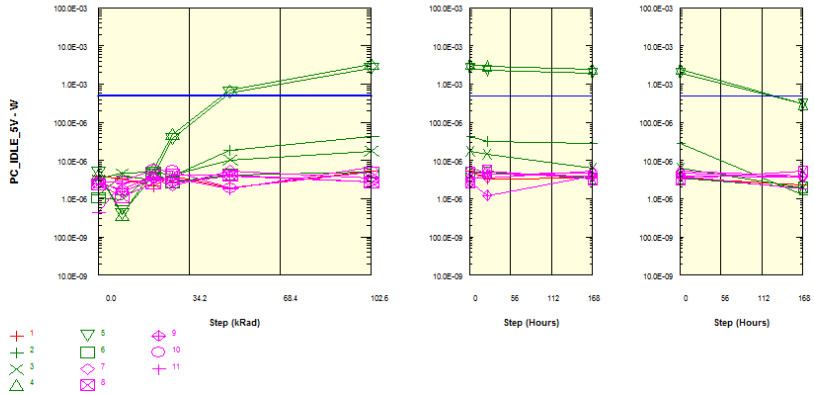


ADC128S102 (8/8)

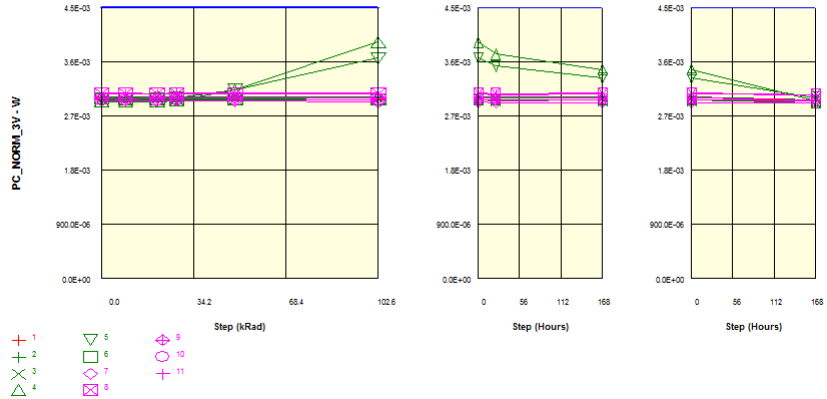
Parameter : Power Consumption Shutdown : PC_IDLE_3V
Test conditions : fSCLK=0kSPS
Unit : W
Spec Limit Max : 90.0E-06
Spec limits are represented in bold lines on the graphic.



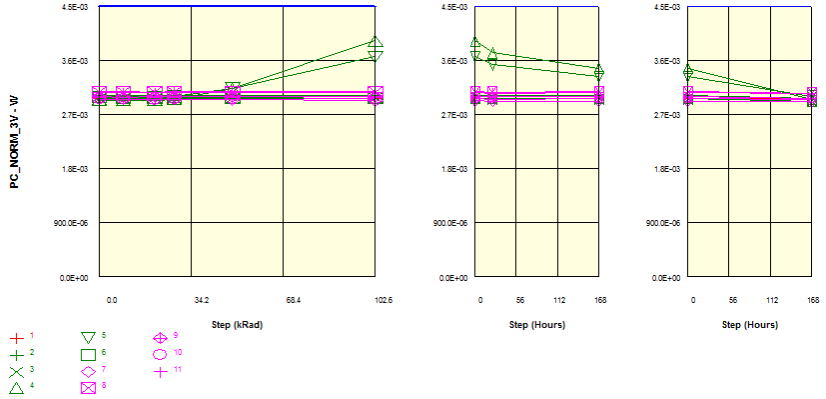
Parameter : Power Consumption Shutdown : PC_IDLE_5V
Test conditions : fSCLK=0kSPS
Unit : W
Spec Limit Max : 500.0E-06
Spec limits are represented in bold lines on the graphic.



Parameter : Power Consumption Normal : PC_NORM_3V
Test conditions : fSample=1MSPS. fIN=40kHz
Unit : W
Spec Limit Max : 4.5E-03
Spec limits are represented in bold lines on the graphic.



Parameter : Power Consumption Normal : PC_NORM_3V
Test conditions : fSample=1MSPS. fIN=40kHz
Unit : W
Spec Limit Max : 4.5E-03
Spec limits are represented in bold lines on the graphic.



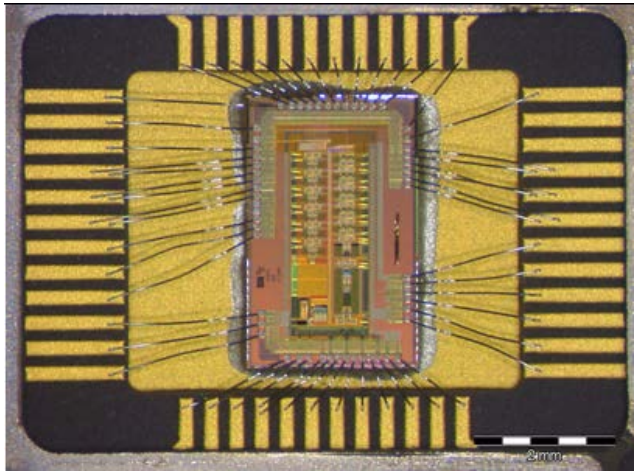
RHF1401KS01 (1/12)

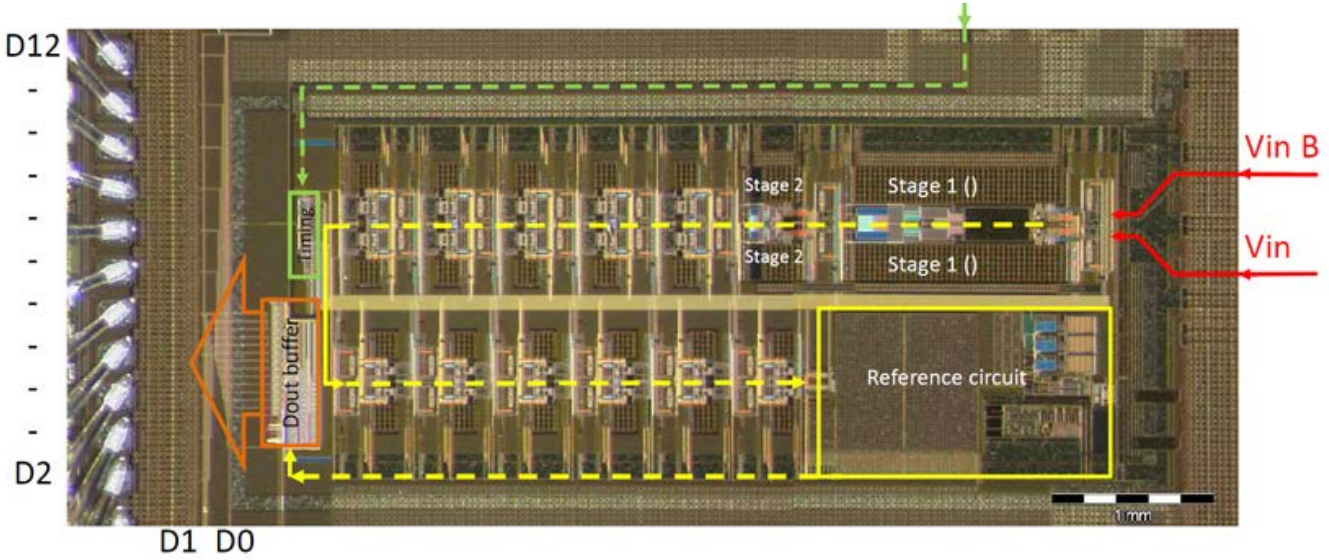
- Part type: RHF1401KS01
- Part description: 14 bits 20 MSps radiation hardened ADC
- Manufacturer: STMicroelectronics
- Package: SO 48 WB
- Date code: 31228A
- TID Testing: UCL, June and July 2013
- 11 samples tested (5xON, 5xOFF, 1xREF)
- Combining mixed mode tester and dedicated ADC/DAC tester
- Dynamic biasing for ON parts matching device applications scope
- Irradiation steps and dose rate (200 rad(Si)/hour):

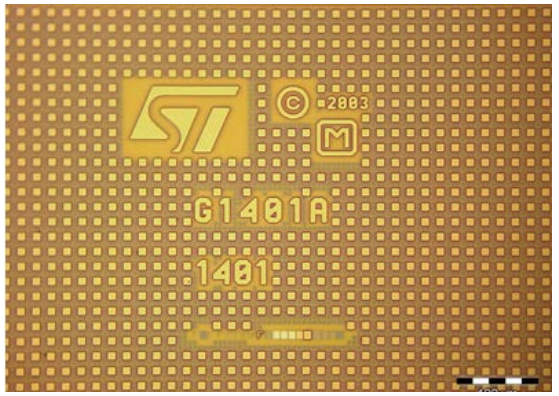
Serial Number	Allocation
11	Control
1	Biased ON
12	Biased ON
13	Biased ON
14	Biased ON
15	Biased ON
16	Biased OFF
17	Biased OFF
18	Biased OFF
19	Biased OFF
20	Biased OFF

Irradiation Steps Requested	Dose rate	Annealing steps	Temperature
krad (Si)	rad(Si)/h	Hours	°C
0		-	Room
10	200	-	Room
20	200	-	Room
30	200	-	Room
50	200	-	Room
100	200	-	Room
-	-	24	Room
-	-	168	100

RHF1401KS01 (2/12)







RHF1401KS01 (3/12)

Results :

- **Biased ON samples:**
  - ✓ All parameters both STATICS, DYNAMICS and AC remain within the limits.
  - ✓ No rebound after annealing.

- **Biased OFF samples:**
  - ✓ All parameters both STATICS, DYNAMICS and AC remain within the limits.
  - ✓ No rebound after annealing.

RHF1401KS01 (4/12)

PARAMETERS	SYMBOLS	TEST CONDITIONS (See note)	MIN	MAX	UNITS
Analog supply current	Aicc	Fs = 20Msps. Fin = 10MHz			A
Digital supply current	Dicc	Fs = 20Msps. Fin = 10MHz			A
Digital buffer supply current	Iccbi	Fs = 20Msps. Fin = 10MHz. OEB set to Vil			A
Digital buffer supply current	Iccbe	Fs = 20Msps. Fin = 10MHz. OEB set to Vil			A
Digital buffer supply current	Iccbez	Fs = 20Msps. Fin = 10MHz. OEB set to Vih			A
Digital buffer supply current	Iccbiz	Fs = 20Msps. Fin = 10MHz. OEB set to Vih			A
Polarization Voltage	Vpol	Fs = 20Msps. Fin = 10MHz			V
Input Common Mode Voltage	Vincm	Fs = 20Msps. Fin = 10MHz	400.0	500.0	mV
Top internal reference voltage	Vrefp	Fs = 20Msps. Fin = 10MHz. Vrefm = GND	760.0	950.0	mV
Logic "1" voltage	Voh_OR	Fs = 20Msps. Fin = 10MHz. OEB set to Vil & IOL = 10µA	2.250		V
Logic "1" voltage	Voh	Fs = 20Msps. Fin = 10MHz. OEB set to Vil & IOL = 10µA	2.250		V
Logic "1" voltage	Voh_DR	Fs = 20Msps. Fin = 10MHz. OEB set to Vil & IOL = 10µA	2.250		V
Logic "0" voltage	Vol_OR	Fs = 20Msps. Fin = 10MHz. OEB set to Vil & IOL = -10µA		250.0	mV
Logic "0" voltage	Vol	Fs = 20Msps. Fin = 10MHz. OEB set to Vil & IOL = -10µA		250.0	mV
Logic "0" voltage	Vol_DR	Fs = 20Msps. Fin = 10MHz. OEB set to Vil & IOL = -10µA		250.0	mV
High impedance leakage current	Iozh_OR	Fin = 0MHz. Rpol = 45kOhms. OEB set to Vih	-15.0	15.0	µA
High impedance leakage current	Iozh	Fin = 0MHz. Rpol = 45kOhms. OEB set to Vih	-15.0	15.0	µA
High impedance leakage current	Iozh_DR	Fin = 0MHz. Rpol = 45kOhms. OEB set to Vih	-15.0	15.0	µA
High impedance leakage current	Iozl_OR	Fin = 0MHz. Rpol = 45kOhms. OEB set to Vih	-15.0	15.0	µA
High impedance leakage current	Iozl	Fin = 0MHz. Rpol = 45kOhms. OEB set to Vih	-15.0	15.0	µA
High impedance leakage current	Iozl_DR	Fin = 0MHz. Rpol = 45kOhms. OEB set to Vih	-15.0	15.0	µA

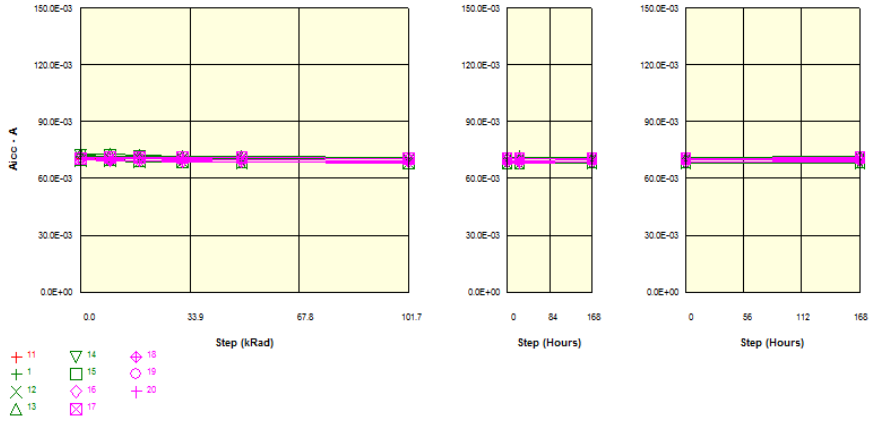
RHF1401KS01 (5/12)

PARAMETERS	SYMBOLS	TEST CONDITIONS (See note)	MIN	MAX	UNITS
Offset error @ Vin = -1dBFS	OE	Fs = 20Msps. Fin = 15MHz			%
Gain error @ Vin = 1.9V	GE	Fs = 20Msps. Fin = 15MHz			%
Differential non linearity	DNLP	Fs = 20Msps. Fin = 15MHz			LSB
Differential non linearity	DNLM	Fs = 20Msps. Fin = 15MHz			LSB
Integral non linearity	INLP	Fs = 20Msps. Fin = 15MHz			LSB
Integral non linearity	INLM	Fs = 20Msps. Fin = 15MHz			LSB
Spurious free dynamic range	SFDR	Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS			dBc
Signal to noise ratio	SNR	Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS			dBFS
Total harmonics distortion	THD	Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS			dB
Signal to noise and distortion ratio	SINAD	Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS			dB
Effective number of bits	ENOB	Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS			bits

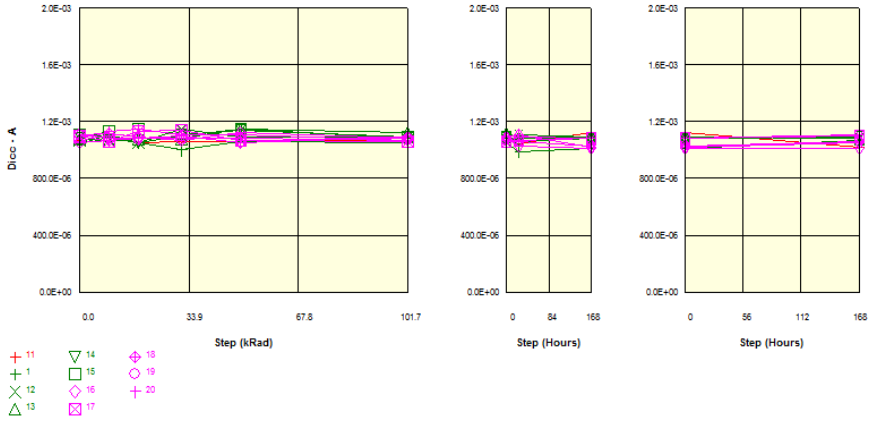
Note:
Internal REFP (REFMODE=0) & INCM, Rpol = 45 kOhm, AVcc = DVcc = Vccbe = Vccbi = 2.5V unless otherwise specified

RHF1401KS01 (6/12)

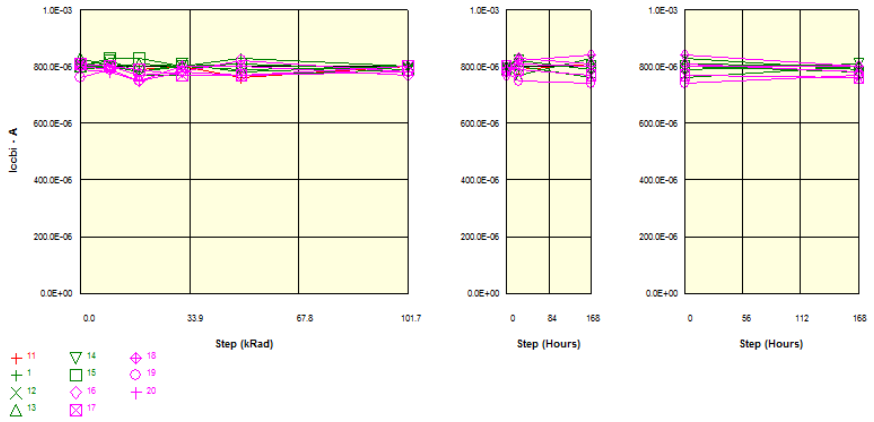
Parameter : Analog supply current : Aicc
Test conditions : Fs = 20Msps. Fin = 10MHz
Unit : A
No spec limit specified.



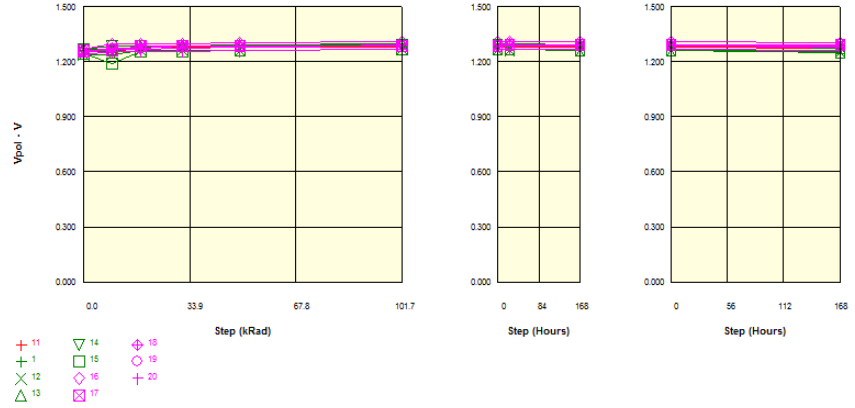
Parameter : Digital supply current : Dicc
Test conditions : Fs = 20Msps. Fin = 10MHz
Unit : A
No spec limit specified.



Parameter : Digital buffer supply current : Iccb
Test conditions : Fs = 20Msps. Fin = 10MHz. OEB set to Vil
Unit : A
No spec limit specified.

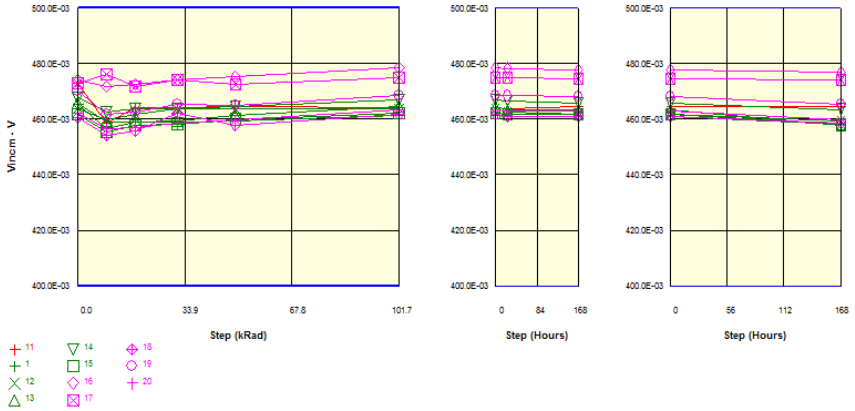


Parameter : Polarization Voltage : Vpo
Test conditions : Fs = 20Msps. Fin = 10MHz
Unit : V
No spec limit specified.

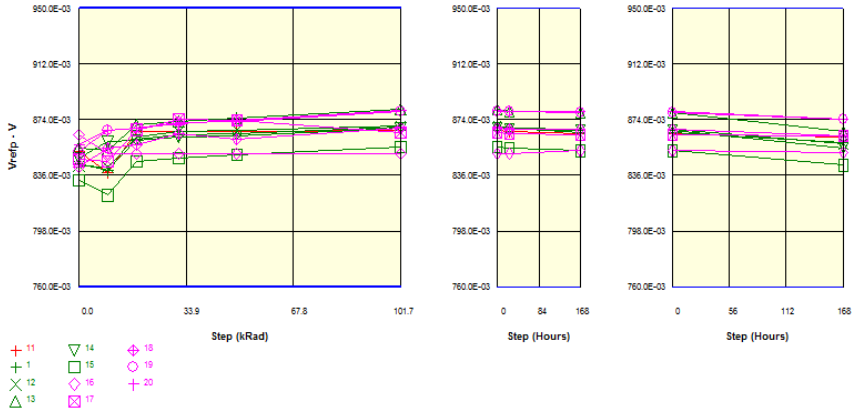


RHF1401KS01 (7/12)

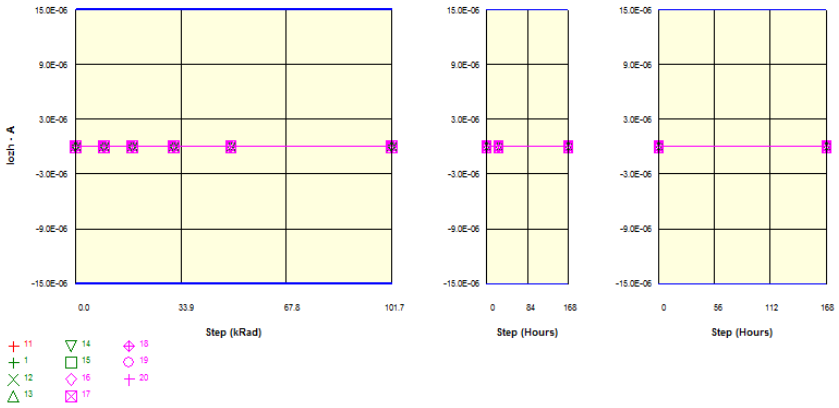
Parameter : Input Common Mode Voltage : [Vincm]
Test conditions : Fs = 20Msps. Fin = 10MHz
Unit : V
Spec Limit Min : 400.0E-03
Spec Limit Max : 500.0E-03
Spec limits are represented in bold lines on the graphic.



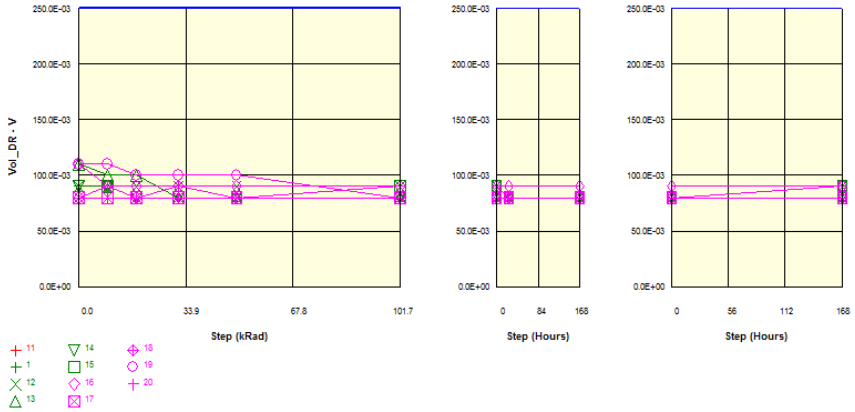
Parameter : Top internal reference voltage : [Vrefp]
Test conditions : Fs = 20Msps. Fin = 10MHz. Vrefm = GND
Unit : V
Spec Limit Min : 760.0E-03
Spec Limit Max : 950.0E-03
Spec limits are represented in bold lines on the graphic.



Parameter : High impedance leakage current : [IozhD8]
Test conditions : Fin = 0MHz. Rpol = 45kOhms. OEB set to Vih
Unit : A
Spec Limit Min : -15.0E-06
Spec Limit Max : 15.0E-06
Spec limits are represented in bold lines on the graphic.

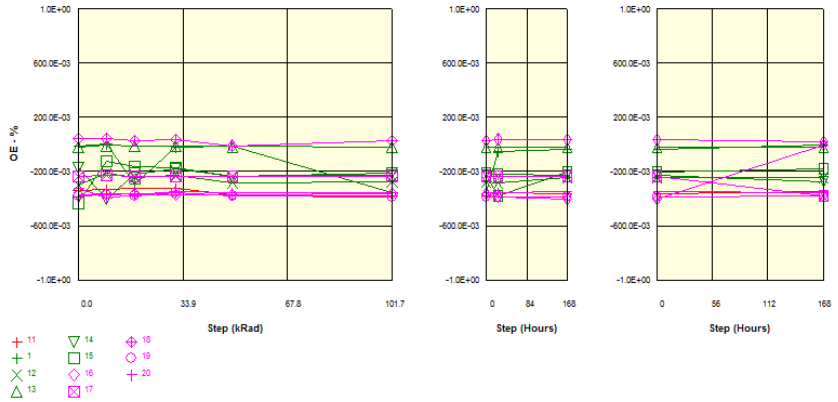


Parameter : Logic "0" voltage : [Vol_DR]
Test conditions : Fs = 20Msps. Fin = 10MHz. OEB set to Vil & IOL = -10µA
Unit : V
Spec Limit Max : 250.0E-03
Spec limits are represented in bold lines on the graphic.

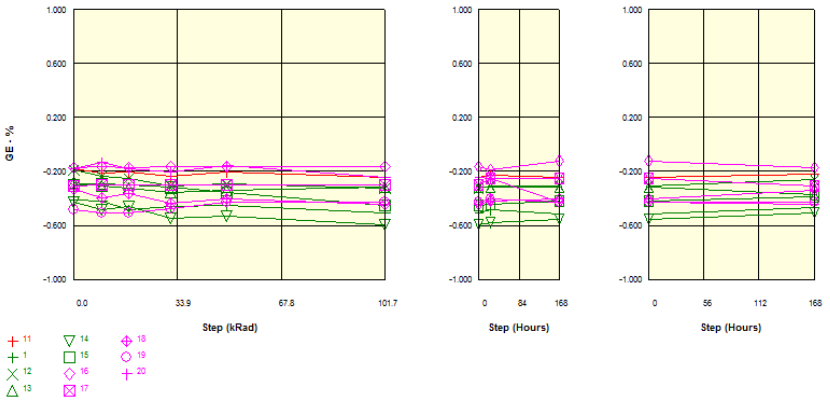


RHF1401KS01 (8/12)

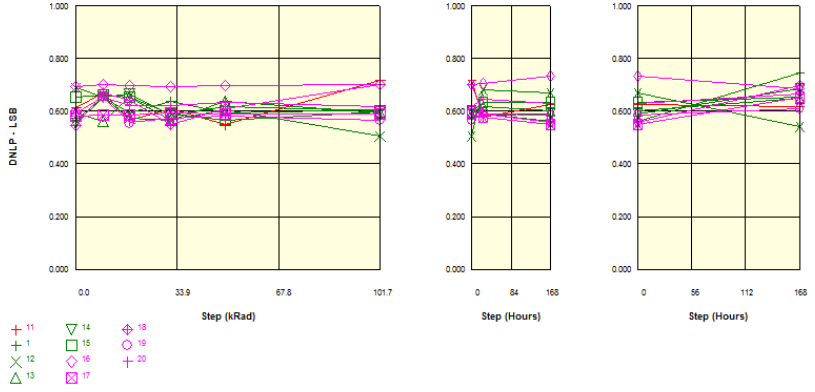
Parameter : Offset error @ Vin = -1dBFS : [OE]
Test conditions : Fs = 20Msps. Fin = 15MHz
Unit : %
No spec limit specified.



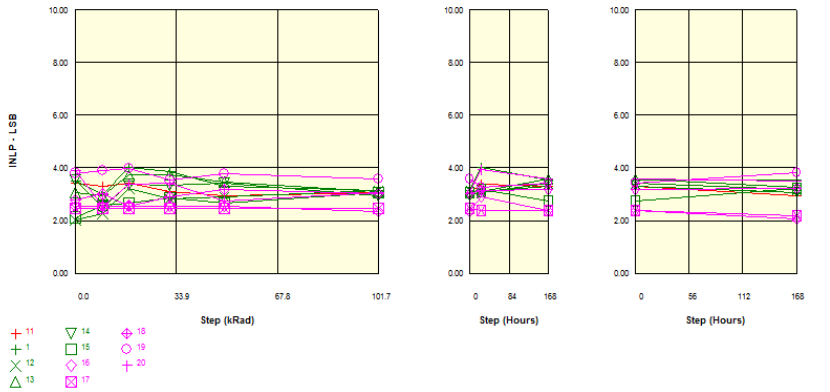
Parameter : Gain error @ Vin = 1.9V : [GE]
Test conditions : Fs = 20Msps. Fin = 15MHz
Unit : %
No spec limit specified.



Parameter : Differential non linearity : [DNLP]
Test conditions : Fs = 20Msps. Fin = 15MHz
Unit : LSB
No spec limit specified.

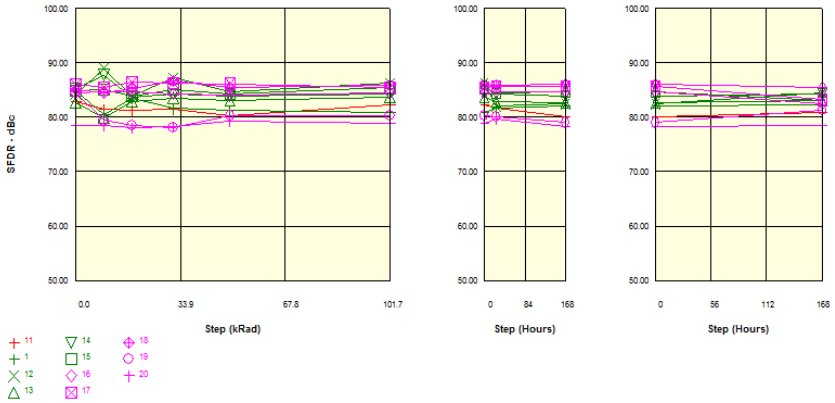


Parameter : Integral non linearity : [INLP]
Test conditions : Fs = 20Msps. Fin = 15MHz
Unit : LSB
No spec limit specified.

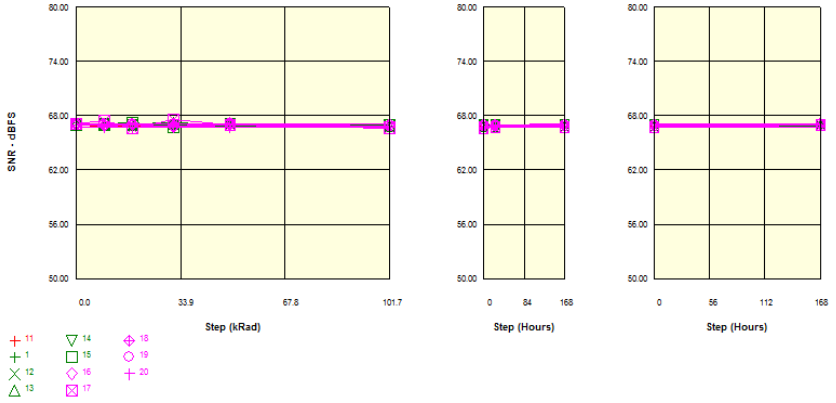


RHF1401KS01 (9/12)

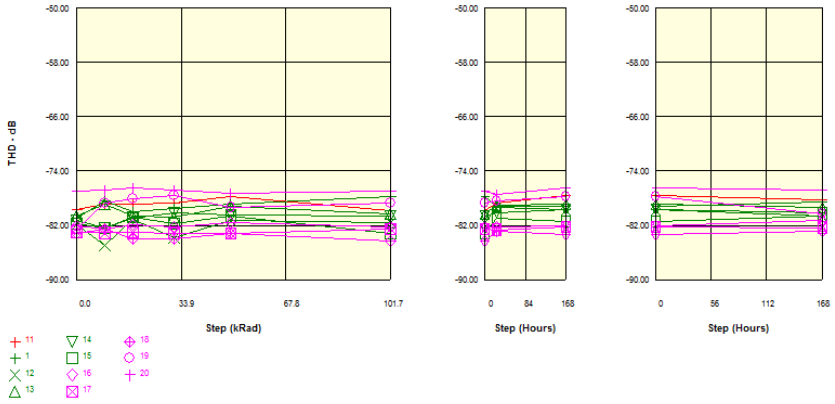
Parameter : Spurious free dynamic range : [SFDR]
Test conditions : Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS
Unit : dBc
No spec limit specified.



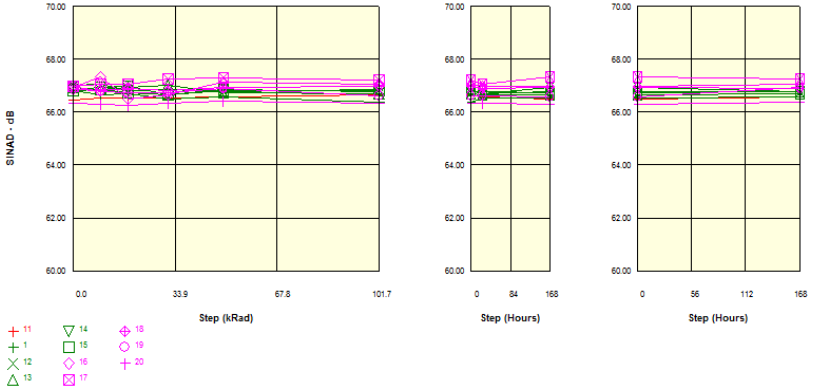
Parameter : Signal to noise ratio : [SNR]
Test conditions : Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS
Unit : dBFS
No spec limit specified.



Parameter : Total harmonics distortion : [THD]
Test conditions : Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS
Unit : dB
No spec limit specified.

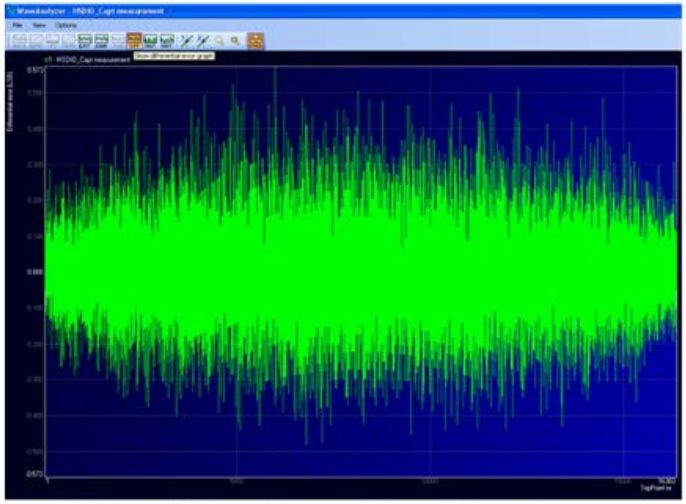


Parameter : Signal to noise and distortion ratio : [SINAD]
Test conditions : Fs = 20Msps. Fin = 15MHz. Vin = -1dBFS
Unit : dB
No spec limit specified.

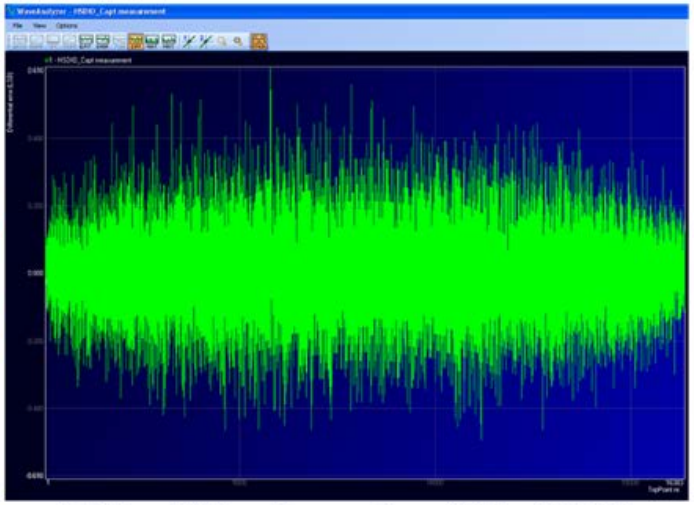


RHF1401KS01 (10/12)

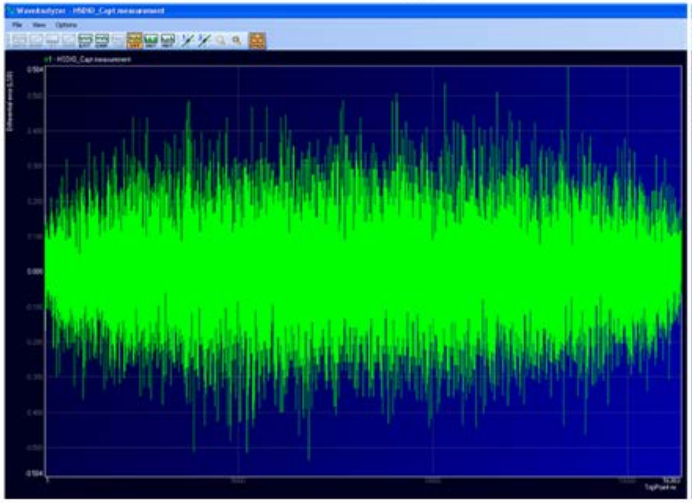
DNL – SN1 - Init



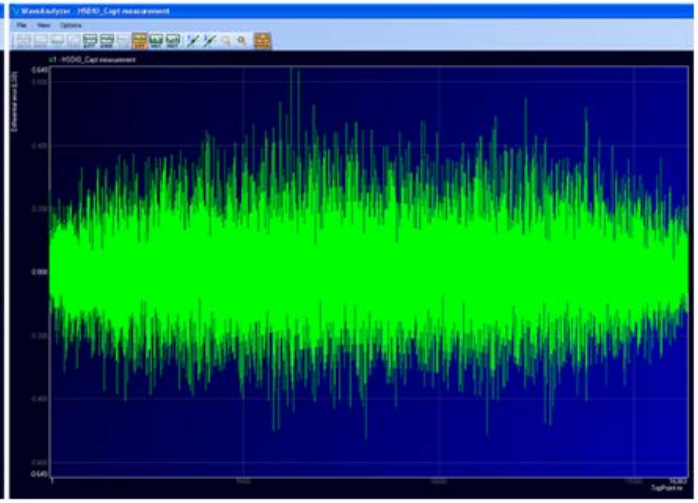
DNL – SN1 – 100 kRad



DNL – SN1 – Annealing 168h Room

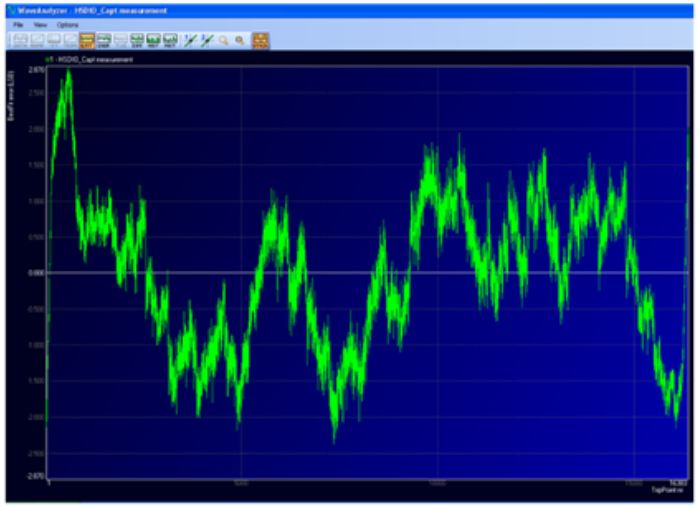


DNL – SN1 – Annealing 168h 100°C

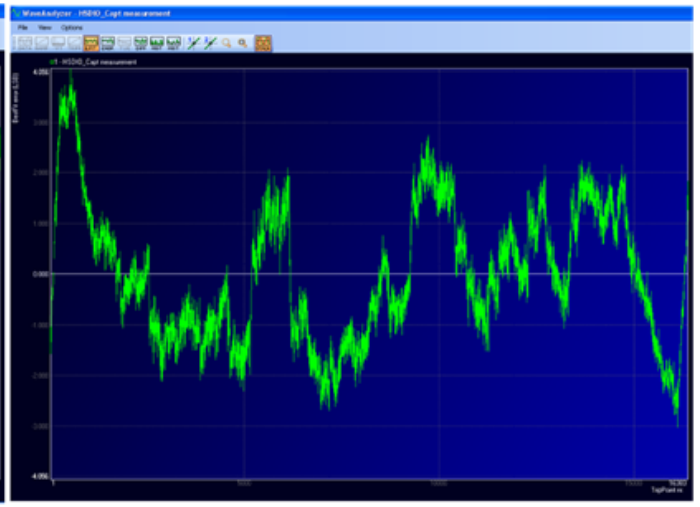


RHF1401KS01 (11/12)

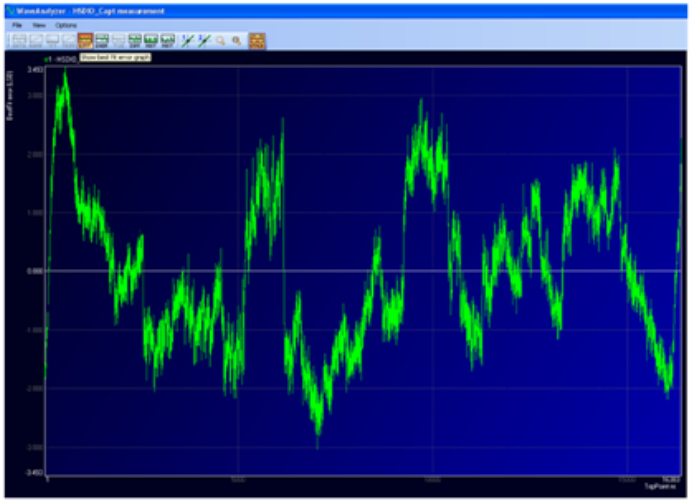
INL – SN1 - Init



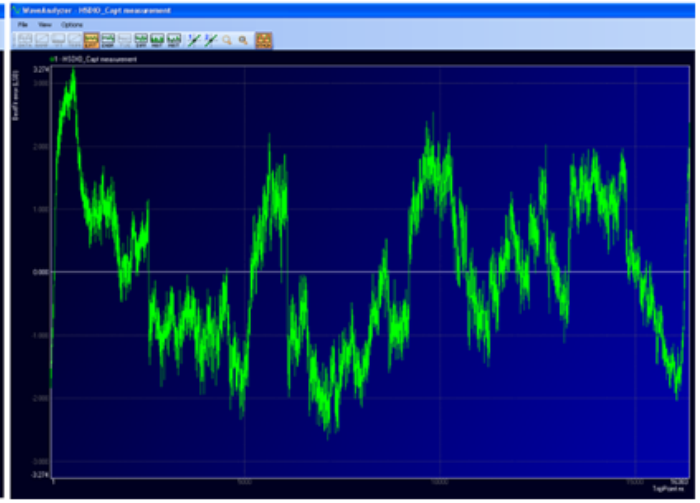
INL – SN1 – 100 kRad



INL – SN1 – Annealing 168h Room

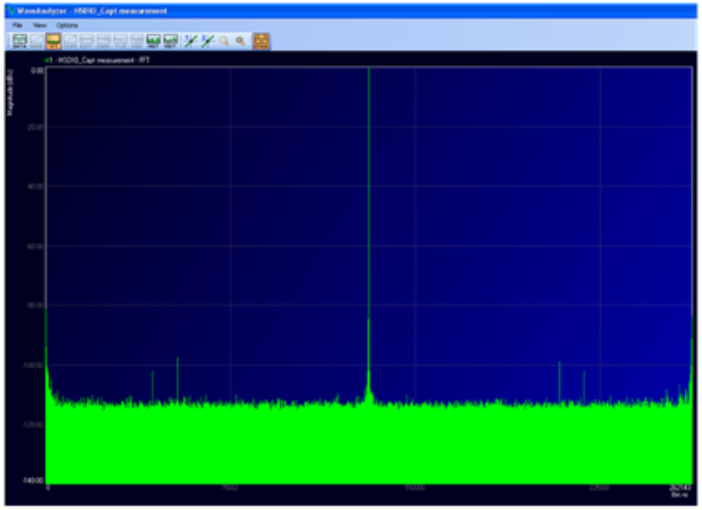


INL – SN1 – Annealing 168h 100°C

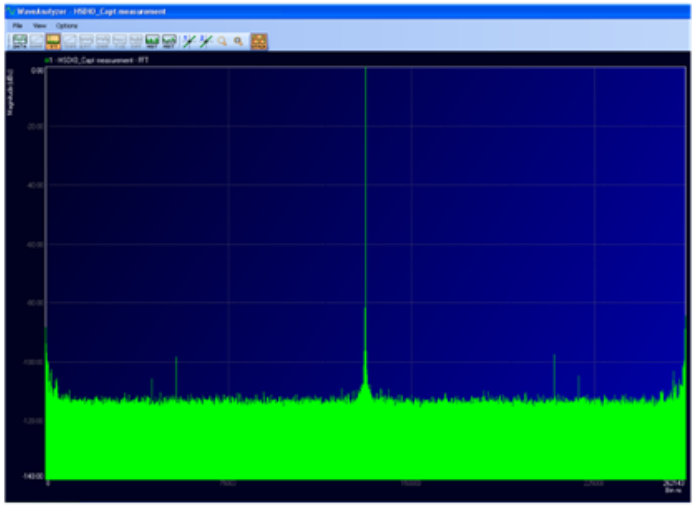


RHF1401KS01 (12/12)

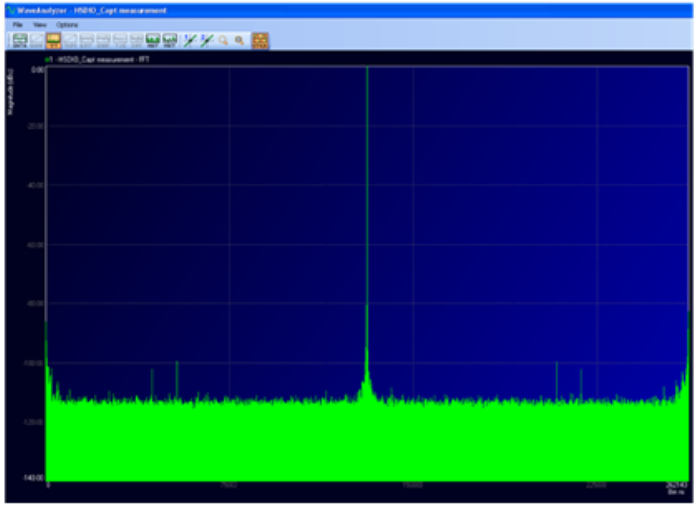
Dynamic Tests – SN1 - Init



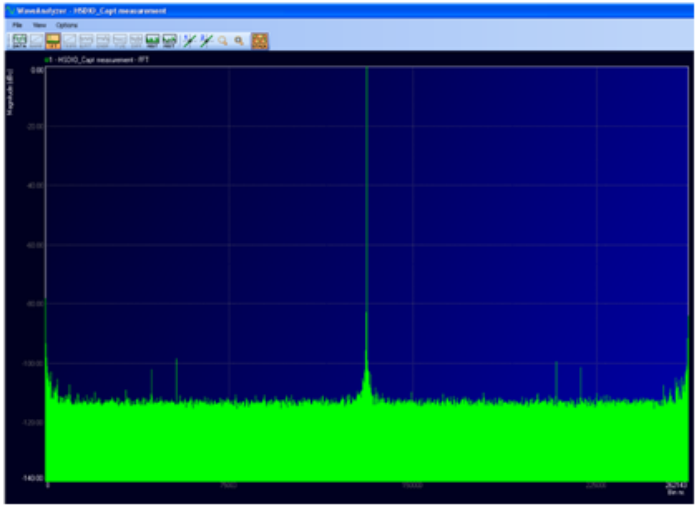
Dynamic Tests – SN1 – 100 kRad



Dynamic Tests – SN1 – Annealing 168h Room



Dynamic Tests – SN1 – Annealing 168h 100°C



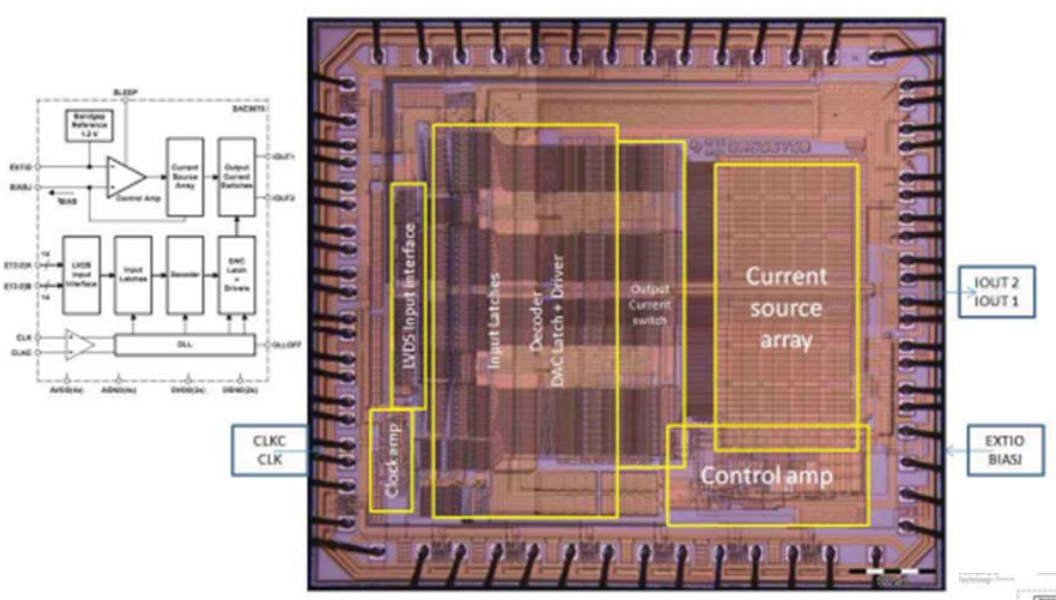
DAC5675AHFG (1/x)

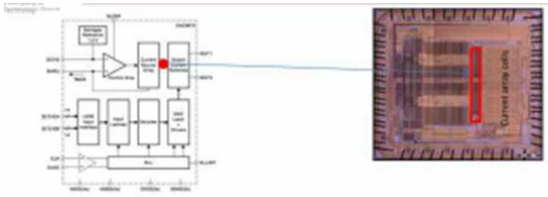
- Part type: DAC5675AHFG
- Part description: 14 bits 400 MSps with LVDS DAC
- Manufacturer: Texas Instruments
- Package: CQFP 52
- Date code: 1233A
- TID Testing: UCL, November and December 2014
- 11 samples tested (5xON, 5xOFF, 1xREF)
- Combining mixed mode tester and dedicated ADC/DAC tester
- Dynamic biasing for ON parts matching device applications scope
- Irradiation steps and dose rate (310 rad(Si)/hour):

Serial Number (serialized by Hirex)	Allocation
1	Control
2	Biased ON
3	Biased ON
4	Biased ON
5	Biased ON
6	Biased ON
7	Biased OFF
8	Biased OFF
9	Biased OFF
10	Biased OFF
11	Biased OFF

Irradiation Steps Requested	Dose rate	Annealing steps	Temperature
krad (Si)	rad(Si)/h	Hours	°C
0	-	-	Room
10	310	-	Room
20	310	-	Room
30	310	-	Room
50	310	-	Room
100	310		Room
-	-	24h	Room
-	-	144h	Room
-	-	168h	100°C

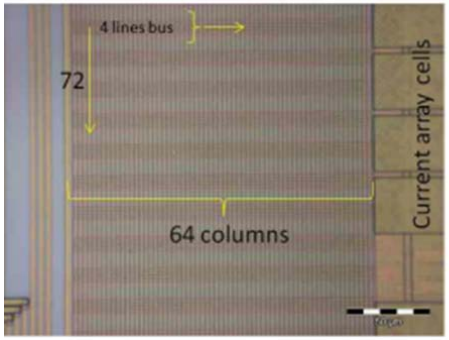
DAC5675AHFG (2/x)

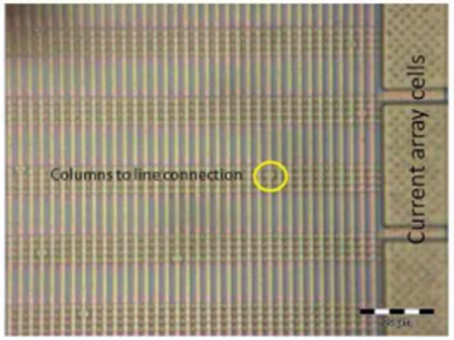




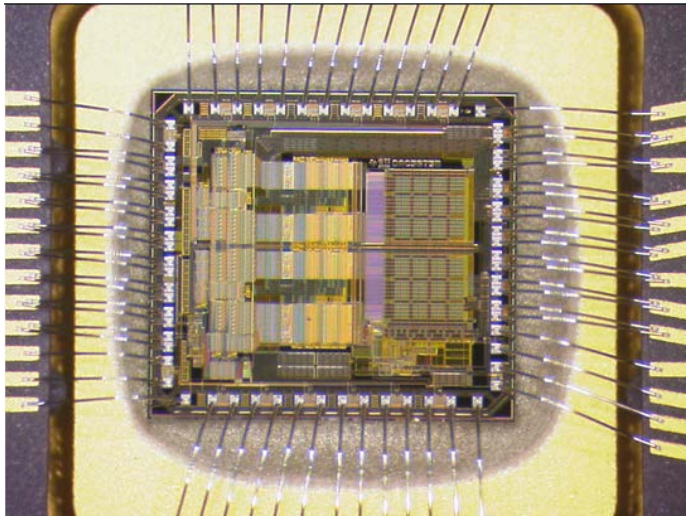
- 4 lines bus*72
- 64 columns

16384 (4*64*64)





DAC5675AHFG (3/x)



DAC5675AHFG (4/x)

Results :

- **Biased ON samples:**
  - ✓ All parameters both STATICS, DYNAMICS and AC remain within the limits.
  - ✓ No rebound after annealing.

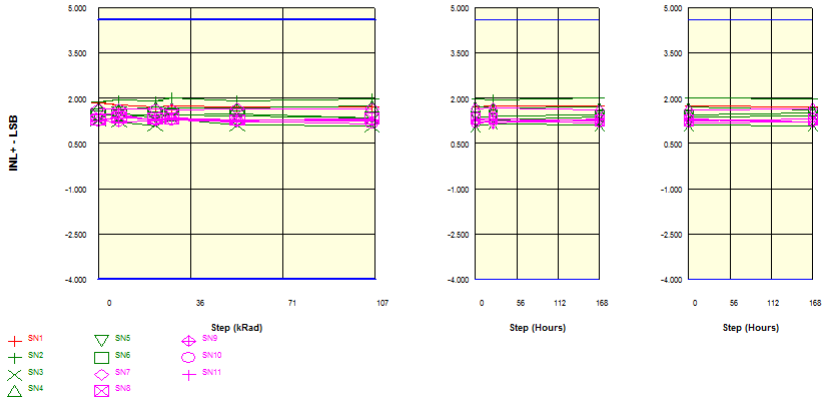
- **Biased OFF samples:**
  - ✓ All parameters both STATICS, DYNAMICS and AC remain within the limits.
  - ✓ No rebound after annealing.

DAC5675AHFG (5/x)

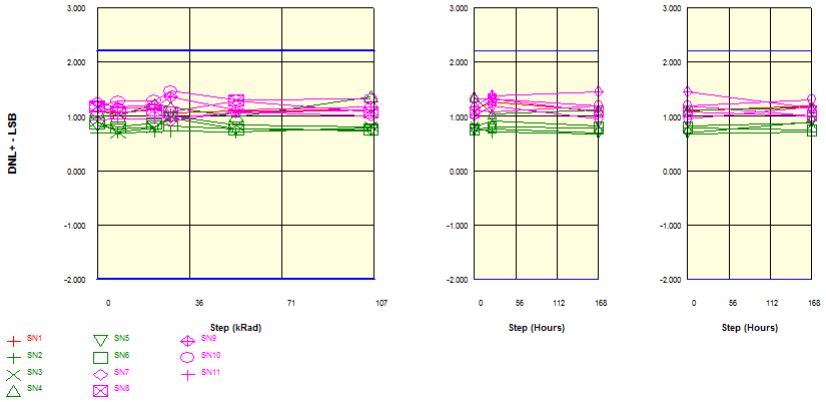
PARAMETERS	SYMBOLS	TEST CONDITIONS	Limits		UNITS
			MIN	MAX	
Linear Electrical specifications (Dvdd=Avdd=3.3V, 50 MSPS, $I_{O(FS)}$= 20 mA unless otherwise specified)					
Integral Non Linearity Positive	INL+	EXTIO Intern	-4	4.6	LSB
Integral Non Linearity Negative	INL-	EXTIO Intern	-4	4.6	LSB
Differential Non Linearity Positive	DNL+	EXTIO Intern	-2	2.2	LSB
Differential Non Linearity Negative	DNL-	EXTIO Intern	-2	2.2	LSB
Gain Error	Eg	EXTIO Extern	-10	10	%FSR
AC Electrical specifications (Dvdd=Avdd=3.3V, $I_{O(FS)}$= 20 mA, 50MSPS)					
Total harmonic distortion	THD	EXTIO Intern			dBc
Spurious free dynamic range	SFDR	EXTIO Intern			dBc
Signal to noise ratio	SNR	EXTIO Intern			dBc
DC Electrical specifications (Dvdd=Avdd=3.3V, 50 MSPS, $I_{O(FS)}$= 20 mA unless otherwise specified)					
Analog Supply Current	Iavdd	EXTIO Intern, Square @1Mhz		148	mA
Digital Supply Current	Idvdd	EXTIO Intern, Square @1Mhz		130	mA
Reference Voltage	VEXTIO	EXTIO Intern, Square @1Mhz	1.17	1.3	V
Digtal specifications (Dvdd=Avdd=3.3V unless otherwise specified)					
High-level input current	I_{IH}	Sleep input	-100	100	µA
Low-level input current	I_{IL}	Sleep input	-10	10	µA

DAC5675AHFG (6/x)

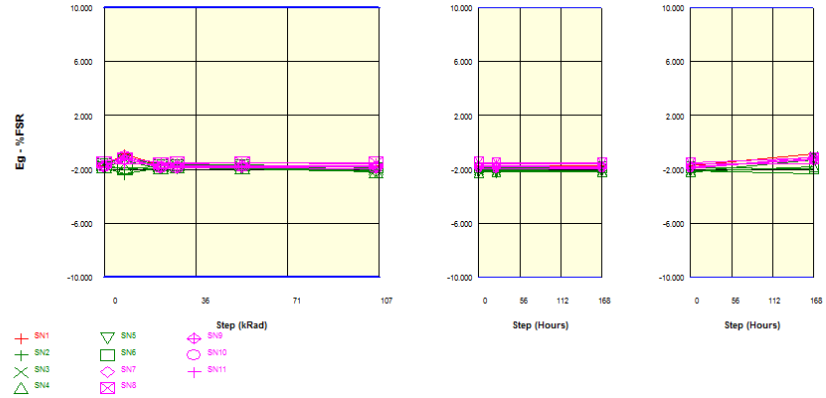
Parameter : Integral Non Linearity Positive : [INL+]
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Intern
Unit : LSB
Spec Limit Min : -4.000
Spec Limit Max : 4.600
Spec limits are represented in bold lines on the graphic.



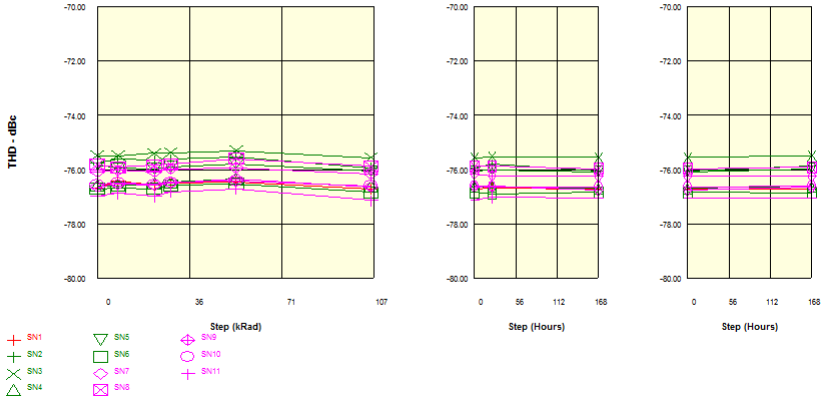
Parameter : Differential Non Linearity Positive : [DNL+]
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Intern
Unit : LSB
Spec Limit Min : -2.000
Spec Limit Max : 2.200
Spec limits are represented in bold lines on the graphic.



Parameter : Gain Error : [Eg]
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Extern
Unit : %FSR
Spec Limit Min : -10.000
Spec Limit Max : 10.000
Spec limits are represented in bold lines on the graphic.

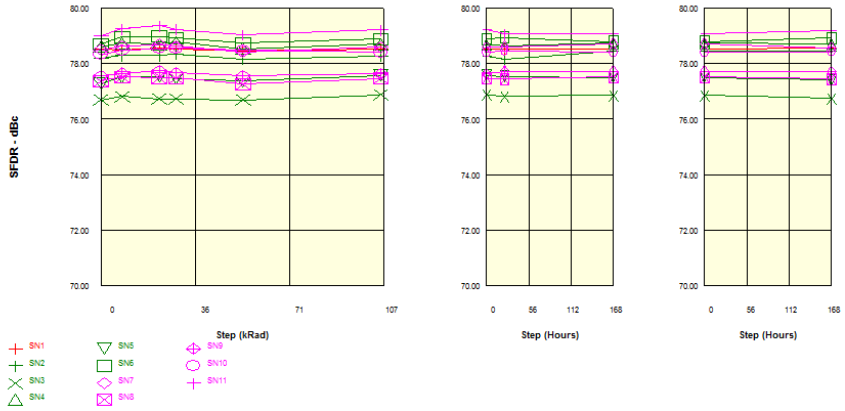


Parameter : Total harmonic distortion : [THD]
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Intern
Unit : dBc
No spec limit specified.

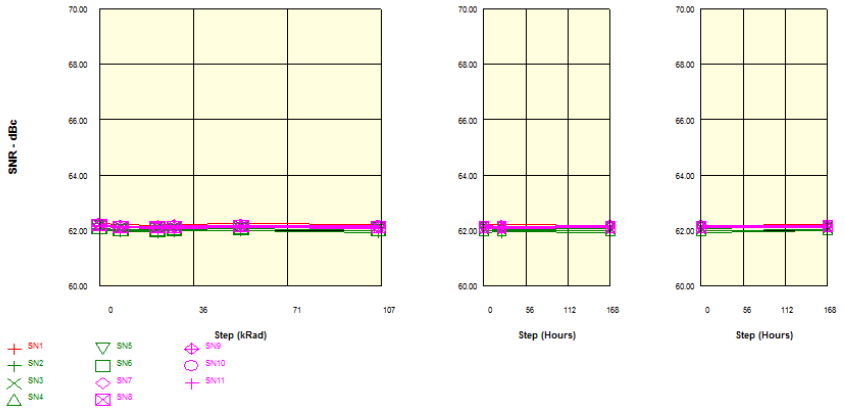


DAC5675AHFG (7/x)

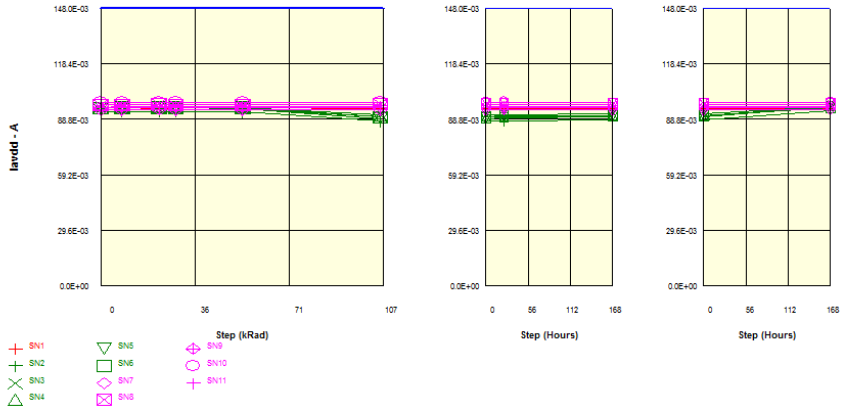
Parameter : Spurious free dynamic range : [SFDR]
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Intern
Unit : dBc
No spec limit specified.



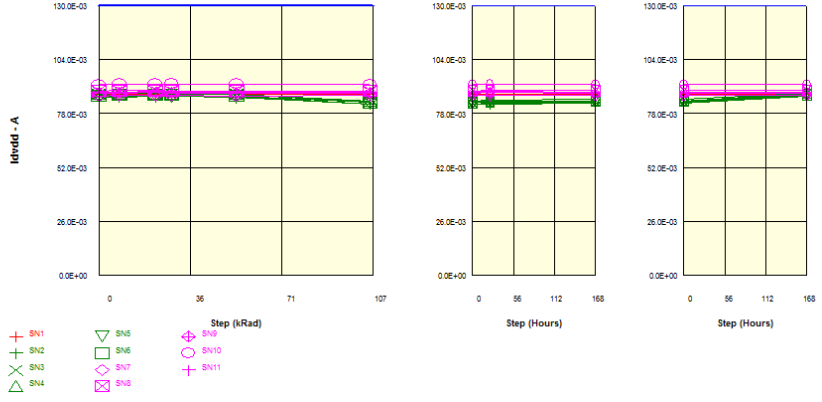
Parameter : Signal to noise ratio : [SNR]
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Intern
Unit : dBc
No spec limit specified.



Parameter : Analog Supply Current : [Iavdd]
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Intern
Unit : A
Spec Limit Max : 148.0E-03
Spec limits are represented in bold lines on the graphic.

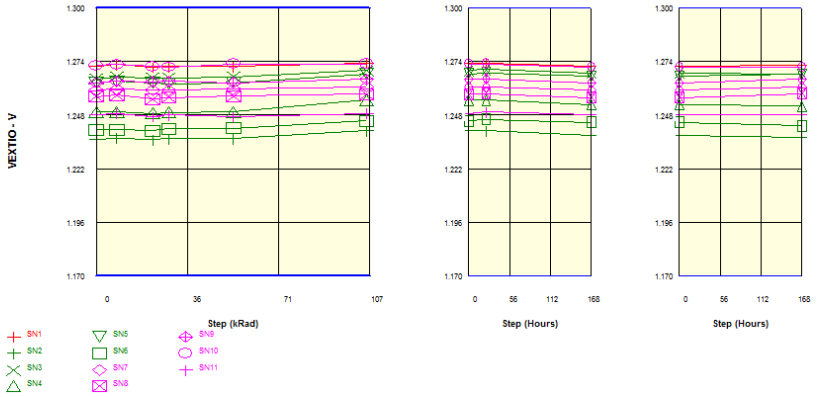


Parameter : Digital Supply Current : [Idvdd]
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Intern
Unit : A
Spec Limit Max : 130.0E-03
Spec limits are represented in bold lines on the graphic.

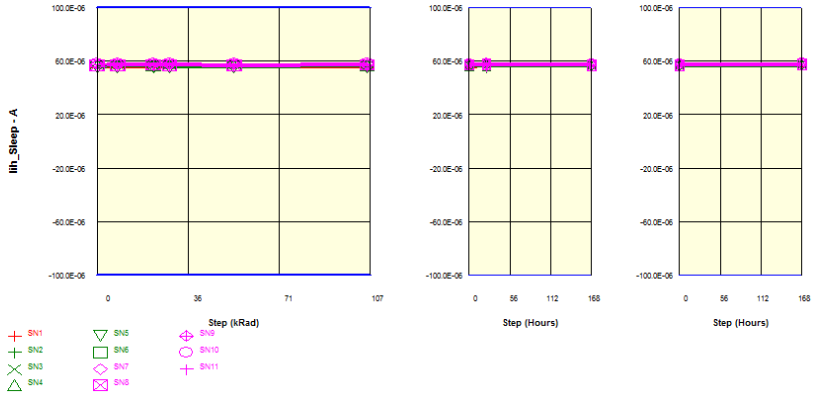


DAC5675AHFG (8/x)

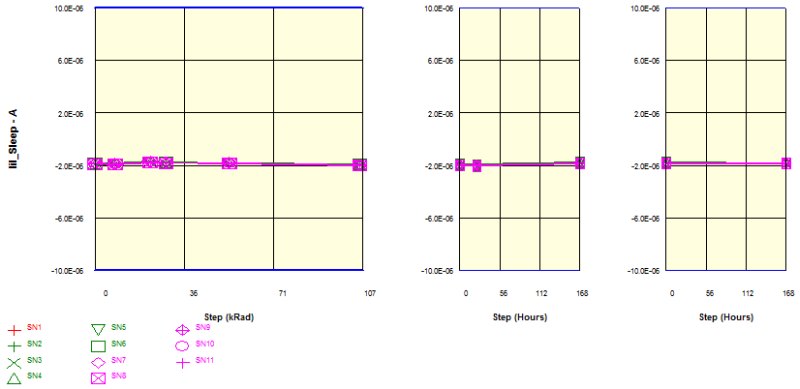
Parameter : Reference Voltage : VEXTIO
Test conditions : Dvdd=Avdd=3.3V. 50 MSPS. IO(FS)= 20 mA. EXTIO Intern
Unit : V
Spec Limit Min : 1.170
Spec Limit Max : 1.300
Spec limits are represented in bold lines on the graphic.



Parameter : High-level input current : Iih_Sleep
Test conditions : Dvdd=Avdd=3.3V
Unit : A
Spec Limit Min : -100.0E-06
Spec Limit Max : 100.0E-06
Spec limits are represented in bold lines on the graphic.



Parameter : Low-level input current : Iil_Sleep
Test conditions : Dvdd=Avdd=3.3V
Unit : A
Spec Limit Min : -10.0E-06
Spec Limit Max : 10.0E-06
Spec limits are represented in bold lines on the graphic.



Radiation Final Presentation Days

Thank You !