

SEE Testing of ADC and DAC

Christian POIVEY¹, Francois Xavier Guerre²

¹ESA ESTEC

² HIREX Engineering

1. Introduction
2. Component tested
3. SEE Test method investigated

1. Different test methods can be used to perform a SEE test on ADC/DAC device
 - a. Static test
 - b. ADC/DAC
 - c. Golden chip
 - d. Compare DUT output to previous conversion cycles
 - Beat Frequency
 - 4 points
 - other

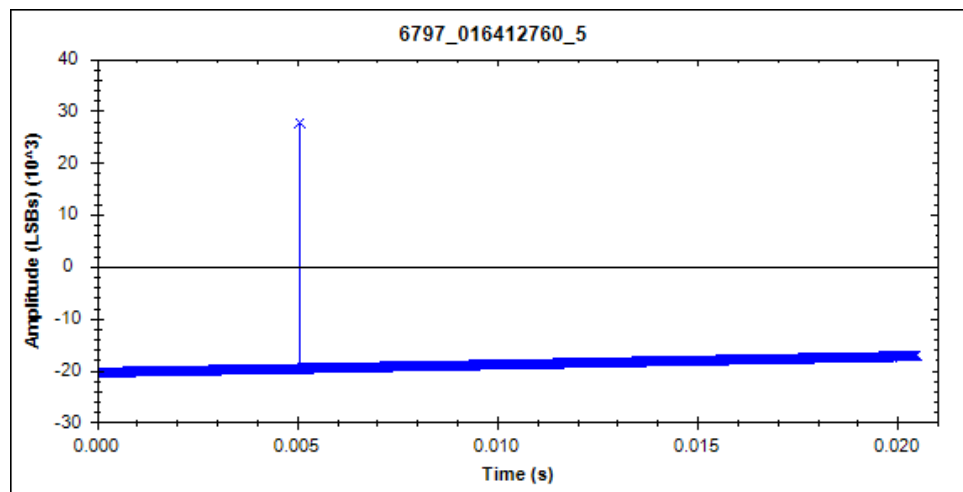
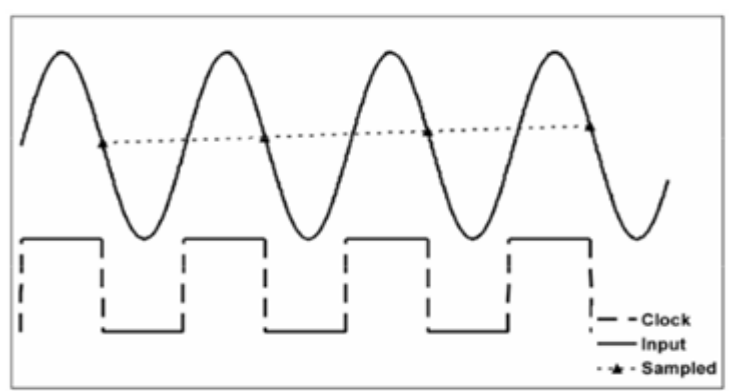
Types Tested



Type	Manufacturer	Function
AD976	Analog Devices	ADC 16 bits
RHF1401	ST Micro	ADC 14 bits
ADC128S102	TI	ADC 12 bits 8 channels
DAC5675	TI	DAC 14 bits

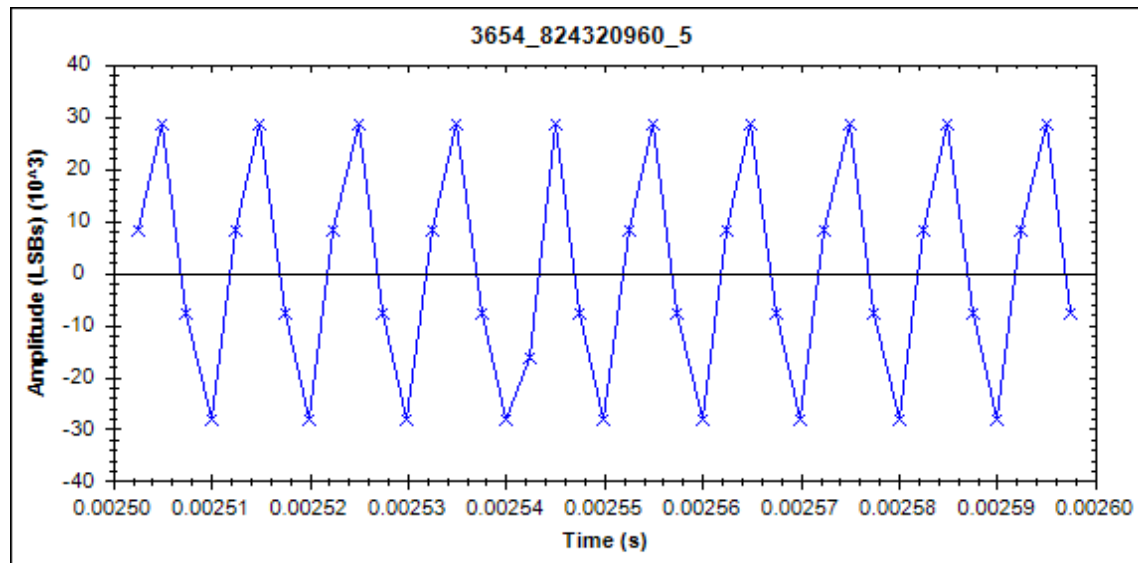
Beat Frequency Test Method

1. With the input frequency f_{in} set very close to the sampling frequency, the output code of the ADC is a slow moving sine wave, changing at a rate of 1 LSB per clock cycle.
 - a. Input sine frequency f_{in} and sampling frequency f_s must repond to:
 - $f_{in} = f_s / (2^N \cdot \pi)$ with $N=16$
 - b. SEE detection: compare DUT output with previous conversion cycle output

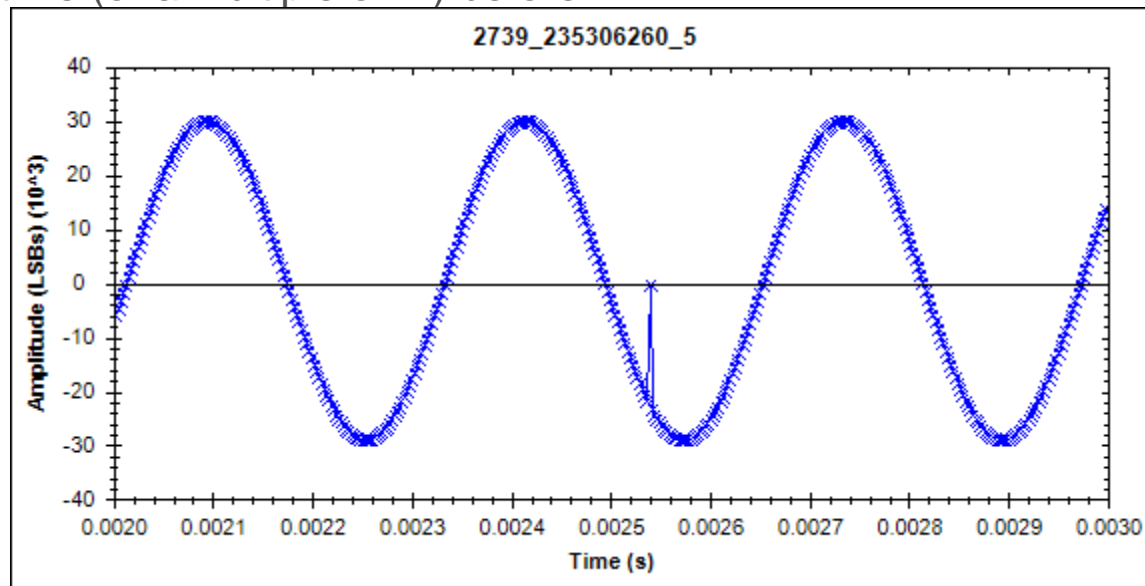


4-point method

1. DUT sampling frequency being fixed, the selected frequency of the sinewave input is such that only 4 points of the sine output are converted continuously.
 - a. Input sinewave frequency f_{in} and sampling frequency f_s must repond to:
 - $f_{in}=f_s/4$
 - b. SEE detection: compare DUT output with output of 4 clock cycles before (or a multiple of 4)



1. DUT sampling frequency being fixed, input frequency is set to a much lower value than f_s and f_s is? a multiple of f_{in} , leading to a significant number of points converted by sinewave input period.
 - a. Input sinewave frequency f_{in} and sampling frequency f_s must repond to:
 - $f_{in}=f_s/m$ with m integer ($m=128$)
 - b. SEE detection: compare DUT output with previous output m clock time (or a multiple of m) before



- 1. A conversion is considered in error when the output comparison with the reference exhibits a difference greater than a set threshold**
 - 1. Threshold set is the minimum error value for which no detection occurs in the absence of beam**
 - 1. Typically 4LSBs for 14 and 16 bits (1 LSB ~ 100 μ V)**
- 2. 2048 conversions values before the detection trigger and 2048 after are recorded**
 - 1. allows for checking the occurrence of successive conversions in error if any.**

DUT Clock and Input Generation

- Excellent accuracy
- Control of phase shift

