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MEMO

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To	PCB/SMT WG	**Copy**	

Subject: IST test procedure for PCB coupons

1 SCOPE

This memo has been defined in frame of the ongoing Working Group on ECSS-Q-ST-70-10/11.

The first objective of this memo is to provide a recommended baseline test procedure and motivation for this.

The second objective is to specify the perimeter when IST is recommended to be performed. These requirements are intended to be made applicable through the ECSS.

The appendix includes further information and preliminary observations. This procedure is subject to an IST study to be performed under supervision of the ECSS WG.

2 PERIMETER

2.1 Procurement

IST shall be performed for procurement in case any of the following technological conditions are met:

1) Any PCB with ≥ 0.3 mm (in z-direction) of resin with a high CTE (in z-direction below Tg) as specified in Table 1. (This includes 85NT and all no-flow prepreg.)

2) Rigid FR4 PCB with ≥ 12 Cu layers

3) Rigid-flex PCB with
   a) ≥ 12 Cu layers, or
   b) ≥ 2 flex laminates, or
   c) asymmetric build-up or asymmetric lamination

4) HDI PCB with microvias and/or aspect ratio > 7 (not including aspect ratio 7 which is standard)

At least one coupon shall be included per panel and submitted to IST testing. However, assessing all drill sequences may require multiple coupons, as described in §3.1.

2.2 Qualification

IST shall be performed on all technology for qualification, for qualification renewal and for delta qualification.

IST shall be performed to EoL (end of life) to provide information, with acceptance criteria as specified in §5.3.

For qualification renewal or delta qualification (not for initial qualification) IST may be limited to 1500 cycles instead of EoL.

2.3 Process control

The PCB manufacturer shall establish an “IST control procedure” that describes the use of IST for process control.

IST testing shall be done until EoL using a more stressing method, since testing without failure does not provide a discriminative test method and does not provide a quantification of reliability.

3 COUPON

3.1 Design

The coupon design shall be type “X” (TVX, SLX, ...), which indicates the presence of an internal and external heating circuit.

IST feature size for pads, drill diameter, pitch and copper foil thickness shall be representative of the PCB.

Coupon design shall accommodate IST to assess the reliability of the barrel (e.g. through a sense circuit) on all drilling sequences (including e.g. PTH, blind via, buried via in the core of an HDI PCB) except for a buried via between two copper layers in a single laminate (which is considered to be very robust). If applicable, microvias shall be assessed by IST.

3.2 Surface finish

Tin-lead finish should be stripped off from the coupon by the PCB manufacturer, prior to IST testing. The effect of the stripping on the representativity of the coupon needs to be considered.

Tin-lead finish may be included on coupons provided that the IST endurance has significant margin to the acceptance criteria to account for any possible masking effect. In case tin-lead is included on the IST coupon, the absence of tin-lead in barrel cracks shall be verified by microsectioning.

4 PREPARATION

4.1 Electrical pre-screening

Electrical pre-screening and possible down selection should be performed in accordance with reference PWB-150316 (from PWB Corp) in case multiple coupons are available.

After soldering of connectors it is recommended to measure the resistance of coupons once more to ensure adequate assembly.

4.2 Bake out

1) Bake out at 120°C for 6h for all materials
2) Solder connectors to coupon
3) It is recommended that measures are taken to prevent re-absorption of humidity (e.g. using a desiccator) after baking.
4) In uncontrolled conditions samples shall be submitted to IST within 12 hours after baking. In case re-absorption of humidity is mitigated as per point 3, this period may be longer.

4.3 Preconditioning temperature

All technology shall be submitted to 6 preconditioning cycles to 230°C.

5 IST CYCLES

5.1 Temperature limit

The following temperature limits shall be used for IST cycles:
Polyimide: 170°C
HTg FR4: 150°C
Microvias on polyimide: 210°C

5.2 Control parameters

Failure threshold of resistance change shall be 10% for standard circuits.
Failure threshold of resistance change shall be 4% for microvia circuits.

"Compensation" shall be "Calculated" for standard tests.
"Compensation" shall be "None" for microvia testing and for testing standard vias with a pitch of ≥ 2.5 mm.

"Sense Fail Type" shall be "A or B"

The power circuit for preconditioning shall be the "superheat" circuit (identified on new coupon designs by "H").
The power circuit for IST cycling (the first few IST cycles before preconditioning and all IST cycles after preconditioning) shall be the standard power circuit (identified by "P").

For testing single level microvias, the power cable shall be connected directly to the microvias sense circuit. The sense cable is connected to a power or sense circuit that has previously demonstrated to be robust (e.g. the superheat circuit). The measured sense data is not considered important and any failure or variation measured can be disregarded.

5.3 Requirement for IST endurance

Any coupon shall have an IST endurance of ≥ 400 cycles for standard vias and PTH (based on standard test method to 150°C for HTg FR4 or 170°C for polyimide).

It is recommended to implement an IST endurance of ≥ 400 cycles for microvias (based on the standard method to 210°C for polyimide) either on a separate coupon or subsequent of the standard IST cycles.

Any coupon with endurance below this threshold shall be documented as a major non-conformance in a non-conformance report (NCR). The NRB may evaluate the PCB acceptable after early IST failure, based on a) materials evaluation without IST heritage, b) passed group 6 test, c) passed traditional outgoing inspection.

6 MICROSECTIONING

Microsection the coupon should be performed, preferably on the location determined by IR thermography.

The purpose is to get a visual confirmation of the failure mechanism in the metallisation. Barrel crack and innerlayer separation should be the main focus of this inspection.

In case tin-lead is included on the IST coupon, the absence of tin-lead in barrel cracks shall be verified by microsectioning, as this may impact the measured IST endurance, as indicated in §3.2.

7 REPORTING

Reports should include the following:

- Summary of test parameters, referred to within the present procedure.
- The coupon design drawing which includes sample description and assignment of circuits
- Graph of resistance change as function of IST cycles
- Representative microsection showing failure mechanism, if applicable
- Compliance to acceptance criteria

8 INFORMATIVE APPENDIX

8.1 Introduction

Interconnect Stress Test (IST) is a novel test method that performs rapid thermal cycling on coupons of Printed Circuit Boards (PCB). The coupons are daisy-chained vias with power circuits through which a current is applied to heat the coupon and sense circuits that are used to monitor the resistance change as function of thermal cycling. This test method is efficient at assessing the quality of the metallisation. It will test until a set failure threshold. The failure mechanism is typically barrel cracks or innerlayer separation.

8.2 Perimeter for procurement

The technological parameters specified in §2.1 decrease via reliability and IST endurance. Therefore these critical parameters shall be screened by IST for procurement. It is estimated that this perimeter includes about 10-20% of space PCBs. Other technologies (e.g. rigid polyimide PCBs) are screened by in-process IST as specified in §2.3.

Table 1: Thermal expansion in Z-direction below glass transition temperature for some commonly used materials

Material	z-CTE <Tg [ppm/K]	IST required according to point 1 of §2.1
Arlon 37N low-flow prepreg	76	Y
Arlon 38N low-flow prepreg	54	Y
Arlon 49N low-flow prepreg	56	Y
Thermount 85NT	93	Y
Ventec VT-901 low flow prepreg	60	Y
Isola PCL-FRP-370HR low-flow prepreg	45	Y
Isola DE104 (not in use)	70	
Rogers RT/duroid 5880 (not used for multilayers)	237	
Arlon 33N	53	
Arlon 35N	51	
Arlon 84N	48	
Arlon 85N	55	
Arlon 44N	55	
Arlon 45N	55	
Arlon CLTE	34	
Arlon CLTE-XT	20	
Isola P96	55	
Isola PCL370HR	45	
Ventec VT-901	50	
Isola IS420	38	
Hitatchi MCL-E-700G type R	25	
Rogers RT/Duroid 6002	24	
Rogers RO4003	46	

The coupon should be located as close as possible to the PCB to be representative of Cu coverage. In case of more PCBs per panel, the coupon should be located as close as possible near the centre of the panel. The coupon should not be located in the corner of the panel. More coupons can be added as preferred. For complex PCBs it may be needed to implement a second coupon to asses more than 2 via types, as described in Table 2.

The PCB manufacturer shall give an identification to the coupon ensuring full traceability.

Note that the procuring authority may specify further requirements for technology to be screened by IST (e.g. on polyimide rigid) to mitigate the risk of assembling a critical component (such as an expensive area array device or long lead time items).

It is acceptable to limit the test duration to cover the acceptance criteria specified in §5.3. However, testing to EoL is preferable as it provides more information.

No microsection is needed when no SnPb is present on the coupon and when the IST results are acceptable. A single microsection is needed when SnPb is present on the coupon and when the IST results are acceptable. This is specified to determine the presence or absence of SnPb in the cracks.

8.3 **Perimeter for qualification**

IST coupons can be placed as for procurement, specified in §2.1

For acceleration studies, it is recommended to use 3 temperatures for IST cycling and to use as a minimum 12 coupons per temperature. The methodology and analysis of data for an acceleration study needs to be developed by an experienced operator (e.g. PWB Corp). The acceleration model is only valid for failure mechanisms involving fatigue.

8.4 **Perimeter for process control**

To ensure consistent and comparative methodology:

- IST coupons should be of identical technology (build-up),
- IST test parameters should be identical,
- The frequency of testing should be once per two weeks as a minimum, with the aim to perform it weekly.

The IST control procedure shall define:

- Test vehicle
- Test moment and frequency (e.g. one day after start-up, or replenish of bath) Coupons should be manufactured as the worst-case parameters (e.g. for TOC total organic contamination)
- Test parameters
- Statistical Process Control (SPC) limits
- Coupon could be designed with 2 circuits 0.3 mm drill iaw PID and 0.2 mm drill.
- Treatment of nonconformances and corrective actions

To reduce testing time, it is acceptable to modify the test method to provide more stress and, thus, to achieve EoL faster. This is acceptable since this in-process test is intended to be a comparative monitoring of the process.

8.5 **Coupon design**

It is recommended that PWB Corp (Canada) is requested to design the coupon. This can be done by completing the "IST design work sheet", available through the following weblink. http://www.pwbcorp.com/EN/Coupons.php

It is recommended to select the minimum drill size of vias to be represented in the IST coupon. In case a slightly larger via diameter is used much more frequently than the minimum diameter, it is recommended to select the more frequent one.

The sense circuit is typically designed to be sensitive to barrel crack. The power circuit applies heat to the coupon and in addition it is typically designed to be sensitive to interconnect defect. The standard power circuit is applied through interconnects on 4 internal layers. These will therefore be assessed by IST, whilst other layers remain unassessed. In case the need arises for more comprehensive assessment of interconnections of all layers, PWB Corp can be requested to design specific coupons. Because of practical limitations, it is not required to assess interconnections on all via types.

To accommodate the need to assess the barrel and the interconnection of specified via types, it may be necessary to implement one coupon with one or two sense circuits or two coupons with multiple sense circuits. This is summarised in the following tables. Alternatively, it may be possible to combine several via types on a single sense circuit to avoid a second coupon. The configuration of PTH+blind+buried can be treated as PTH+blind+microvia.

Table 2: Single and two coupon test circuit selection strategy

Single Coupon Test Circuit Selection Strategy								
Structures	PTH		Buried Via		Blind Via		Single-level Microvia	Multi-level Microvia
Circuits to test	Barrel	Interconnect	Barrel	Interconnect	Barrel	Interconnect		
PTH Only	S1	P						
PTH+Counter-bored via	S1+S2	P						
PTH+Buried	S1	P	S2					
PTH+Buried+Microvia	S1 or S2	P	S1 or S2				S1 or S2	
PTH+Blind	S1	P			S2			
PTH+Blind+Microvia	S1 or S2	P			S1 or S2		S1 or S2	
Buried+Microvia			S1	P			S2	
Blind+Microvia					S1	P	S2	
Microvia							S1 & P	
Multi-level Microvia							S2 & P	S1

Two Coupon Test Circuit Selection Strategy								
Structures	PTH		Buried Via		Blind Via		Single-level Microvia	Multi-level Microvia
Circuits to test	Barrel	Interconnect	Barrel	Interconnect	Barrel	Interconnect	Via to Pad	Via to Via
PTH+Buried+Microvia	C1-S1	C1-P	C1-C2-S2	C2-P			C2-S1	
PTH+Blind+Microvia	C1-S1	C1-P			C1-C2-S2	C2-P	C2-S1	
PTH+Buried+ Multi-level Microvia	C1-S1	C1-P	C1-S2	C2-P				C2-S1+S2
PTH+Microvia+ Multi-level Microvia	C1-S1	C1-P					C1-S2	C2-S1+S2
Microvia+ Multi-level Microvia							C1-C2-P	C1-C2-S1+S2

8.6 Coupon surface finish

Surface finish for space application typically comprise of reflowed tin-lead. It has been observed that tin-lead reflows or diffuses into the crack initiations in the copper hole wall. The tin-lead inside the cracks may exacerbate the crack growth due to CTE differences and at the same time it might mask the resistance change.

8.7 Determining preconditioning parameters

The current used during preconditioning is specific for the coupon design. The software will make adjustments to the set current to optimise the heat cycle. However a first approximation of the current needs to be entered in the software. To determine this current, the following options are available:

1) In case the coupon design is known by PWB Corp, they may be contacted to request the current parameter for the design.
2) In case the required current is not known by PWB Corp, a sacrificial coupon should be used to determine the current.
3) An experienced operator may be able to estimate the current parameter based on similar designs. This is only recommended in case previous options are not possible.

Note that more preconditioning cycles can be used for robust technology such as polyimide. However, this is likely to only affect the number of IST cycles to failure; it does not create a new failure mechanism. For comparative analysis and consistency it is recommended to use 5 cycles to 230°C.

8.8 IST temperature limit

The temperature of 170°C for polyimide has been chosen to prevent tin-lead surface finish from reflowing. In case the sample has been prepared with tin-lead stripped, PWB recommend for polyimide to test until 210°C. However, present heritage is based on 170°C. The temperature limit should not change the failure mechanism, it should just lead to reaching the resistance threshold with less cycles. For comparative analysis a temperature of 170°C is currently recommended on all via types (PTH, blind and buried via), except microvias.

Microvia polyimide circuits can be tested at 210°C on a separate coupon. In case microvias are combined on a single coupon with other vias on the second sense circuit, it is recommended to first perform standard IST on the other circuit followed by IST on the microvia circuit.

PWB recommend testing microvias on HTg FR4 at 190°C. However, these are not used for space.

8.9 IST control parameters

The 10% resistance threshold is commonly referred to as “failure”. However, since IST performs cycling to failure by definition, the term “failure” does not indicate acceptability, which is specified in §5.3.

New coupon designs may have a second power circuit named “superheat” (identified by “H”) with the purpose to be more representative of reflow processes during preconditioning by applying the heat externally. However, switching power connectors between preconditioning and IST requires manipulation and thorough understanding of the software. Full representativity is not a driver if it adds significant complexity to the practical execution of the test.

Compensation set to “none” ensures that the test temperature is measured on the power circuit (not on the sense circuit). This prevents higher temperatures on any of the circuits than the one selected for the test. This is valid for standard via circuits and of specific importance for microvia circuits.

Sense fail type set to “A or B” ensures that the IST cycles stop after either Sense A or Sense B fails, instead of continuing the test until both fail.

8.10 **IST endurance**

PWB Corp proposes to test microvias only until 100 cycles. The rationale is that the failure mode of microvias is associated with interconnection defect to the capture pad, which either occurs quickly or not at all. Hence, this proposal could save test time.

It may be acceptable to use technology that has an IST endurance below the specified threshold due to inherent weaknesses of materials or processes (e.g. complex rigid-flex technology). An non-conformance review board (NRB) shall be organised with the final customer to review the acceptability, which may be substantiated by performing an acceleration study covering mission requirements and/or by acceptable group 6 test results.

8.11 **IR thermography**

Gradual increase of the resistance during IST cycling indicates that degradation of the coupon occurs generally and, therefore, no single location may appear by IR imaging. Abrupt increase of resistance during IST cycling indicates that degradation of the coupon occurs on one or few locations and, therefore, IR imaging is an efficient method to determine the failed via(s) for subsequent microsectioning.

The following optional investigation is recommended to be performed for fault finding after IST testing on a coupon that has reached the 10% threshold for resistance change.

- Apply a thin masking tape over the coupon to remove reflection from the metallisation
- Inject a current on the failed circuit (likely to be a sense circuit) or on the failed microvia circuit.
- Observe the heating of the coupon with an IR camera.
- Increase current gradually.
- When the failure location becomes apparent, mark the relative location on coupon.
- Immediately disconnect the current.

At all stages during this test, the current shall be carefully controlled so as not to overheat the coupon locally.

8.12 **Capacitance**

Capacitance measurements can be added to investigate the quality of the dielectric with another equipment named DELAM tester.