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TITLE
Radiation Pre-Evaluation of FPGA Influence of TID Test Condition on Actel A1425A

EUROPEAN SPACE AGENCY
CONTRACT REPORT

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SUMMARY

The impact of static versus dynamic operation during Total Dose Testing (TID) of commercially manufactured FPGA has been performed using the Actel FPGA A1425A as test vehicle. The samples, manufactured by Matsushita (MEC), were biased at 5V and irradiated using a Cobalt-60 source at a dose rate of 1300 rad(Si)/hour. In dynamic conditions, the devices were clocked at 20 MHz resulting in a case temperature of about 40 °C

For the TID tested non-hardened commercial FPGA's, it has been shown that the total dose induced leakage current is decreased by a factor of two by irradiation in 100% clocked condition compared to static mode. The Voltage Output Low was practically not affected in 100% dynamic test condition while it was non-functioning in the static case.

DOCUMENT CHANGE RECORD

Changes between issues are marked with a left-bar.

Issue	Date	Paragraphs affected	Change information
1	12 Oct 1999	All	New document
2	19 Jan 2000	5	Some text and figures
		4.1	Table 4.1

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1. ABSTRACT

The impact of static versus dynamic operation during Total Dose Testing (TID) of commercially manufactured FPGA has been performed using the Actel FPGA A1425A as test vehicle. The samples, manufactured by Matsushita (MEC), were biased at 5V and irradiated using a Cobalt-60 source at a dose rate of 1300 rad(Si)/hour. In dynamic conditions, the devices were clocked at 20 MHz resulting in a case temperature of about 40 °C
TID testing in dynamic condition seem to indicate in faster annealing of radiation damage resulting in higher cumulated dose tolerance than in static condition.

2. INTRODUCTION

The standard method to assure the hardness-assurance screening requirements for spacecraft has been to perform total dose tests for the worst case conditions rather than in the anticipated application conditions. For devices originating from commercial processes this may result in non-relevant irradiation data and exclusion of many potentially good commercial devices.

The time dependent growth and annealing of irradiation induced defects in VLSI circuits are very complex and highly dependent upon oxide processing. For non-hardened commercial processes the radiation response in practical dose rate regimes are generally dominated by field-oxide parasitic leakage, which normally exhibit a rapid recovery with annealing time and temperature. In a very low-dose rate environment the irradiation response will likely be controlled by the gate-oxide leakage.
For FPGA, the most application like test mode would likely be 100% dynamic test at high clock frequency.

In order characterise the irradiation response of commercially manufactured FPGA and the influence of the operation condition, the Actel A1425 has been used as a test vehicle. Four samples have been irradiated to a cumulated dose of 26.5 krad(Si) for each of the three different operation modes.

1) static,
2) 100% dynamic at 20 MHz
3) 50% static / 50% dynamic at 20 MHz

In-situ measurements of function and the standby current were performed. Pre- and post electrical measurements of the input/output voltage and leakage were also performed. The different operation modes indicate large differences in the measured total dose tolerance.

3. TEST SAMPLES

The A1425A is the third generation FPGA (ACT3) from Actel. The die of the tested devices was manufactured by MEC in 0.8u technology. The devices employ antifuse technology implemented in ONO gate 0.8 um 2 level metal CMOS. This device is a 2500 gate FPGA with 310 logic modules (160 S-modules and 150 C-modules) and maximum 100 user I/O's.
The samples tested have been package in 132 pin CQFP screened to Mil-883 quality level. Two date codes have been used.

Marking / *Top side*	Marking / *Bottom Side*
Delta C Actel Logo A1425A CQ132B 9704	 UCJ014 UCJ014 Philippines

Marking / *Top side*	Marking / *Bottom Side*
Delta C Actel Logo A1425A CQ132B 9719	 UCJ014 UCJ014 Philippines

4. TEST TECHNIQUES

4.1 Methods

Total dose tests have been performed by load data into the DUT's, wait for a pre-set of time and check for errors. To test for start-up problems, the bias to the DUT's was always turned off/on before function test. The supply current to the DUT was monitored continuously. The following test cycle was performed on four samples for each test mode:

1) DUT turned off during 10 seconds
2) DUT turned on
3) DUT tested for functionality at 20 MHz
4) DUT biased for 30 minutes
5) DUT biased for 1 minute in static mode for measurements of standby current

During step 4, three different test conditions have been used.
- Static mode – where the test samples have been left in bias conditions un-clocked.
- 50% Dynamic mode – where the test samples have been left in bias conditions toggled in a un-clock / clock sequence for equivalent 64 clock pulses at 20 MHz.
- 100% Dynamic mode – where the test samples have been left in bias conditions clocked at 20 MHz during the full test.

The DUT's are tested using a "virtual golden chip" test method. The principal of the technique is to compare each output from the DUT with the correct data stored and controlled by a monitor board closely connected to the DUT-board.
The layout of the DUT's have been individually controlled 64-bit shift registers (ring counters) with a bit pattern consisting of consecutive 0 1 0 1 etc. The DUTs have been programmed with one ring counter for each logical module.

Pre- and post irradiation electrical measurements have been performed on the parameters shown in Table 4.1. Due to problems with the test equipment is some test conditions not the same as for the specified the limits.

Table 4.1 Electrical parameters and conditions

TEST PARAMETER	TEST CONDITIONS	LIMITS from Actel	
		Min	Max
I_{CC}	V_{CC} = 5,0 V		2 mA
Functionality	f_{CLK} =20 MHz		
Input current low , I_{il} [1]	V_I = 0,3 V	-10µA	+10µA
Input current high , I_{ih}	V_I = 5,0 V	-10µA	+10µA
Voltage output low, $V_{OL\ (CMOS)}$ [2]	V_{CC} = 5,0 V Output current = 6.0 mA		0.33 V
Voltage output high, $V_{OH\ (CMOS)}$ [2]	V_{CC} = 5,0 V Output current = -6.0 mA	3.84V	
Timing = delay of signal between two I/O pins	V_{CC} = 5,0 V Threshold = 1,5 V		

[1] Limits is specified with V_I = GND
[2] Limits is specified with VCC = min (4.75V)

4.2 Facility

The total dose tests were performed at the hospital of Borås. This facility has a Cobalt-60 source suitable for low dose rate testing.
Staff from Department of Sjukhusfysik at Borås hospital calibrated the exposition rate. The source is calibrated for dose rate to water and then calculated for expected dose rate to Silicon. The determined dose is correct within 10%.

5. RESULTS

The standby current from the three different test modes is presented in Figure 5-1. For each test modes, four samples have been irradiated. The typical variation in standby current for the different samples is shown in Figure 5-2 for the static test. The results are representative for the other test modes as well. Up to the tested cumulated dose, no significant difference in spread of current values was observed for the two date codes. In 100% dynamic mode, a mix of the two date codes have been used. For static mode dc 9719 was used, and for 50% dynamic the dc 9704 was used.

Due to the large increase in standby current in static test mode, the test was interrupted before the planned cumulated total dose in order to have functioning devices for the post electrical measurements. The two dynamic tests were pursued to the same total dose in order to have proper comparison.

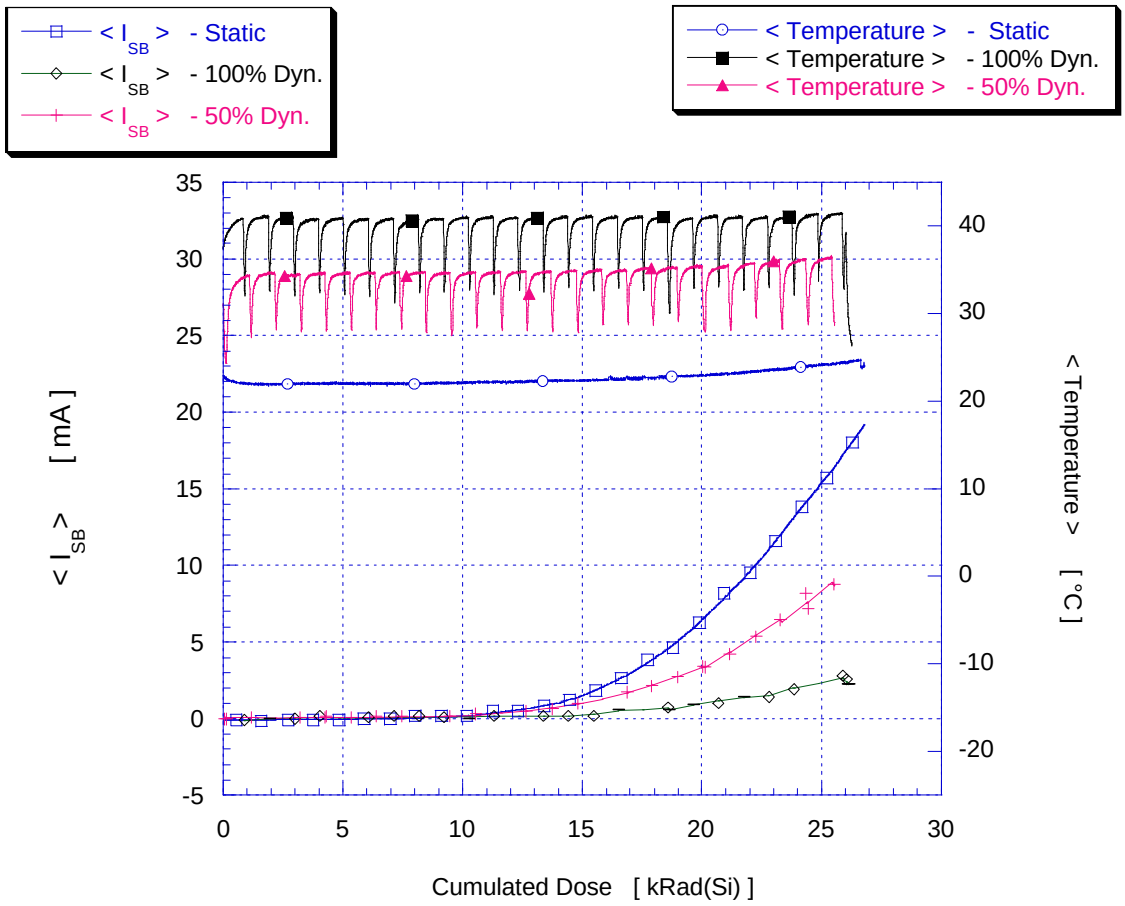

Figure 5-1. Supply current as a function of total dose for the different test conditions. Data for each condition represents the average value of four test sample. The upper part of the figure shows the case temperature for the three test conditions. The "dips" in the temperature curves for 50%- and 100% dynamic tests shows the decrease of case temperature in connection with the power off/on functional test (every 30 minutes) where the bias is off for about 2 minutes.

The maximum limit for the standby current according to data specification is 2 mA. From Fig 5-1, it could be seen that the supply current passed the limit around 15 krad(Si) for Static mode, around 18 krad(Si) for 50% dynamic and around 25 krad(Si) for 100% dynamic.
By operating the FPGA in 100% dynamic mode at 20 MHz, the total dose tolerance concerning the leakage current could almost be increased with a factor of 2.

In Figure 5-1 are also shown the case temperatures monitored in-situ for the three test modes. In static mode the temperature is around 25 °C, while at 50% dynamic it has increase to an average temperature of 35°C and at 100% dynamic the case temperature is around 40 °C.

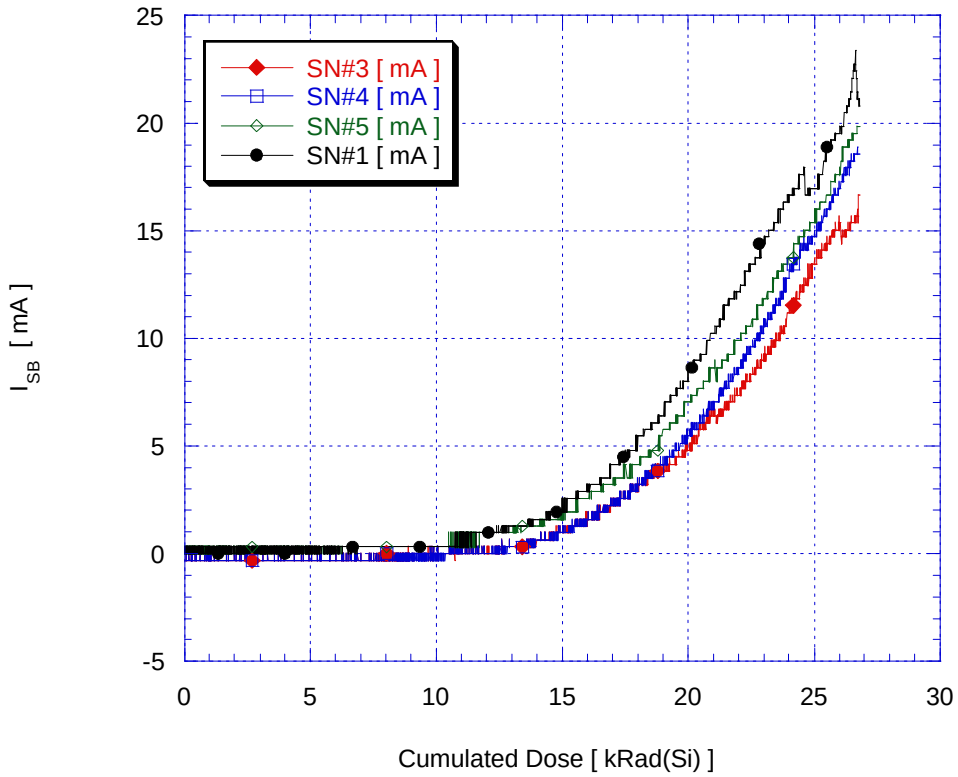

Figure 5-2. Standby current as a function of total dose for the four samples irradiated in static condition. The spread in current values between the samples is representative for all test conditions and the two date codes used. The spread in standby current values tends to increase with increasing leakage current. The leakage for the other two test conditions was never above 10 mA. Functional error was detected in sample SN#1 at about 25 krad(Si).

Post electrical measurements on samples in static mode indicated severe problems in the drive capability of the Voltage Output Low (Vol). The results for the three test conditions are shown in Fig 5-3. In static mode the internal logic indicated no functional failure, but the Vol failed when it was loaded according to specification. Even in 50% dynamic mode the Vol specification limit of 0,5 V was exceeded.

The other electrical measurements are shown in Figs 5-4 to 5-6. The difference between the various test methods is much less pronounced here.

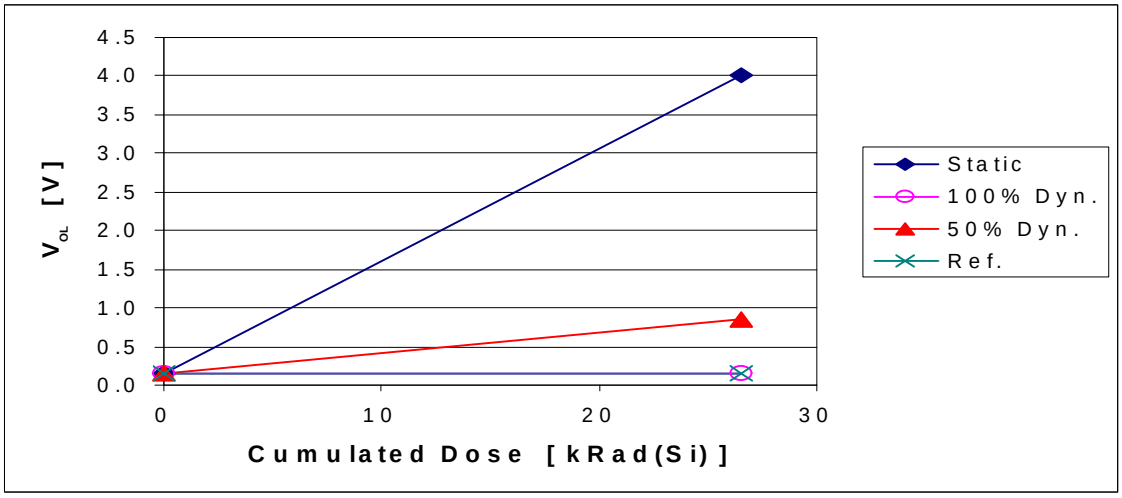

Figure 5-3. Pre- and post irradiation measurements of Voltage Output Low (Vol) for the three test conditions. The specification limit is 0,5 V with test conditions Supply voltage = 5V and Output current = 6 mA. With the selected scale, data for 100% dynamic test are shown superimposed on data for the Ref. Data specification limit is 0,33 V.

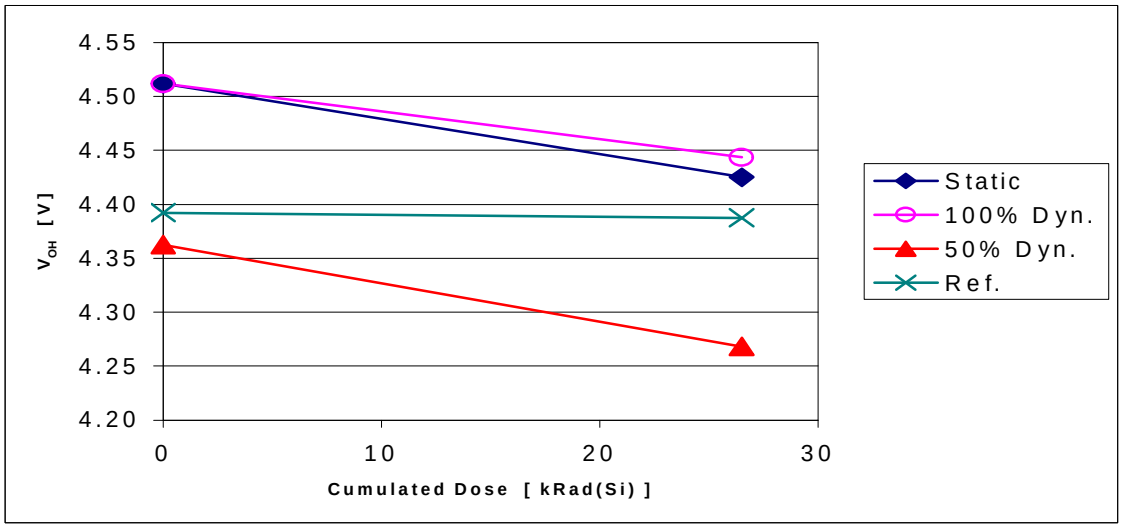

Figure 5-4. Pre- and post irradiation measurements of Output voltage high (Voh) for the three test conditions. The specification limit is 5 mA with test conditions Supply voltage = 5 V and output current = -6 mA. Data specification limit is 3,84 V.

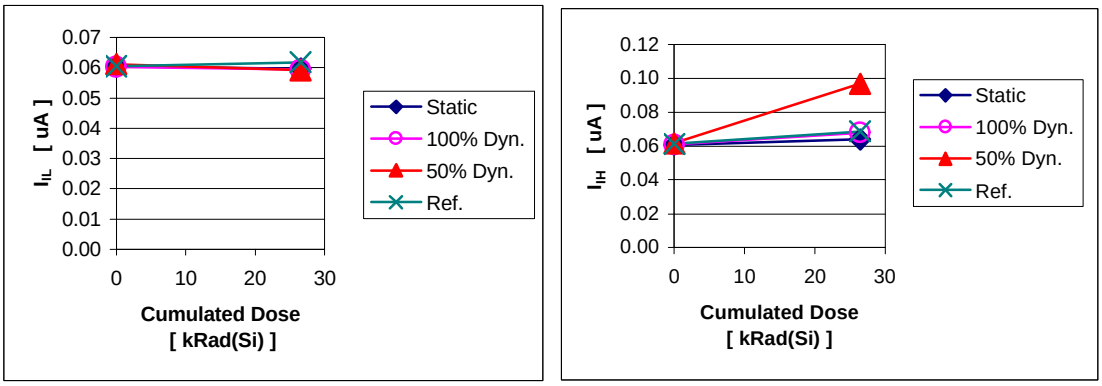

Figure 5-5. Pre- and post irradiation measurements of Input current low (Iil) and Input current high (Iih) for the three test conditions. The specification limit is 10 µA. Data shown in this figure are mean values of clocked I/O's used in the test area. Data for all static and manufacturer specific IO's have been excluded. Data specification limit is ± 10 µA for $V_I = V_{CC}$ or GND.

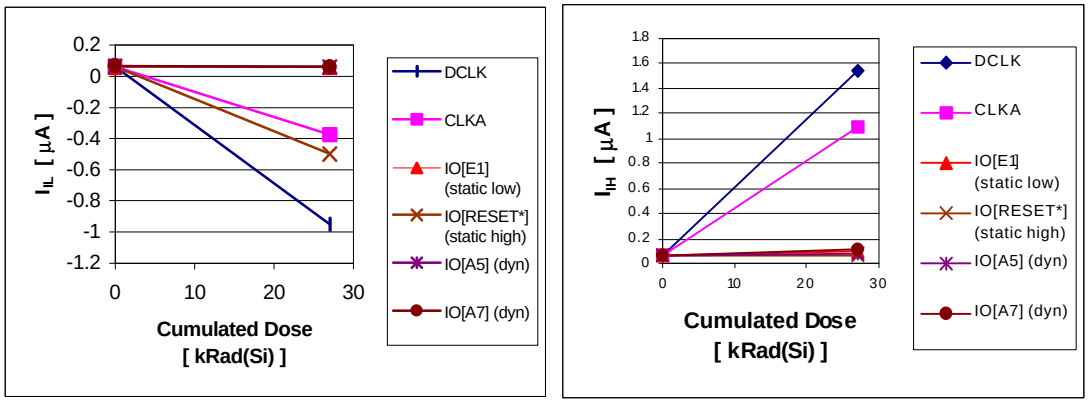

Figure 5-6. Pre- and post irradiation measurements of Input current low (Iil) and Input current high (Iih) for different I/O's. The data are taken from 50% dynamic test mode. Shown in the graphs are 6 different I/O', where DCLK and CLKA are predefined from the manufacturer and the other are user defined. The IO (Reset) and IO(E1) have been in static mode during irradiation, while IO(A5) and IO(A7) are examples of IO's which have been clocked during irradiation (see Fig 5-5). For the IO(Reset) the CLKB pin has been used as an IO.

Measurements of timing changes due to irradiation has been implemented in the design for both I/O and internal logic building blocks. Post irradiation timing measurements of internal logic in static mode gave inconsistent values and no stable measuring points could be achieved due to the high degree of total dose damage and the very fast annealing process taking place as soon as the devices were in clocked condition. Therefore, this test was not repeated for the other two test conditions.
Timing measurements of the I/O function indicated very little damage with total dose. The results are shown in Figs 5-7 and 5-8.

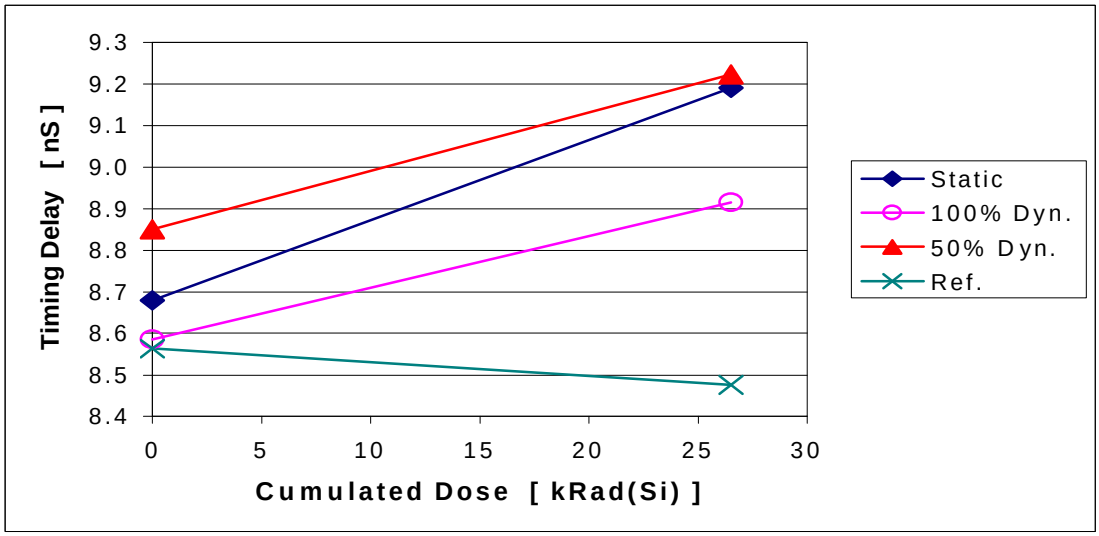

Figure 5-7. Pre- and post irradiation measurements of timing delay between two I/O pins. Average values over four samples for each test condition. The measurements are very critical for the power supply setting and temperature.

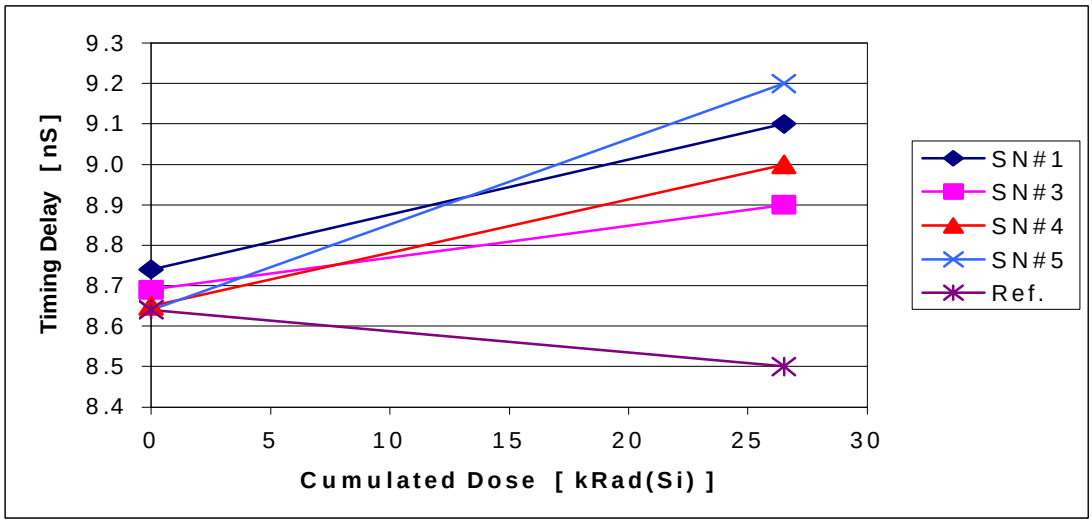

Figure 5-8. Pre- and post irradiation measurements of timing delay between two I/O pins. Individual samples for the static test. The start-delay value showed a spread among all tested samples of about 0.3 ns centred around 8.7 ns. The measurements are very critical for the power supply setting and the temperature.

6. CONCLUSION

For the TID tested non-hardened commercial FPGA's, it has been shown that the total dose induced leakage current is decreased by a factor of two by irradiation in 100% clocked condition compared to static mode. The Voltage Output Low was practically not affected in 100% dynamic test condition while it was non-functioning in the static case.

The 100% clocked condition is likely the normal condition for space application. Since the operating condition has such an influence on the total dose tolerance, radiation characterisation of commercial FPGA's should be performed at application like conditions. The present study indicate that irradiation in static condition represents very much of a worst case condition, likely too much for a majority of applications.

The time dependent growth and annealing of irradiation induced defects in commercial FPGA circuits seem to be highly dependent upon bias and operating condition. Very likely, the radiation response is dominated by field-oxide parasitic leakage, which normally exhibit a rapid recovery with annealing time and temperature.

An open question is still the importance of the operating frequency versus the temperature for the radiation response. For 100% operating test, would the results be the same for 20 and 10 MHz or would 10 MHz 100% dynamic be the same as the 50% static- 50% dynamic at 20 MHz? Could the temperature be the dominating annealing driver?
The case temperature difference between 50% dynamic and 100% dynamic was only 5 degree. The case temperature was measured to be at maximum around 40 degree. In many applications the case temperature would likely by around 60 degree.

The present results found for Actel A1425A are very likely highly dependent on device technology and FPGA program. The general result that static conditions are leading to worse radiation response is probably true for a majority of commercial devices. To verify the importance of frequency versus temperature for supply current and other parameters, a new set of test experiments will be designed