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MEMO

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To	ECSS WG, PCB/SMT WG, PCB manufacturers	**Copy**	

Subject: Approach for pad lift and associated laminate cracks

1 BACKGROUND

Pad lift (or: lifted lands) and associated laminate cracks under the pad have been observed recently during qualification renewal of epoxy PCB technology after thermal stress. Pass/fail criteria for this defect are not clearly described in ECSS-Q-ST-70-10C. Nevertheless, this has traditionally been evaluated by ESA as a major non-conformance.

Several industrial members of the working group for the revision of ECSS-Q-ST-70-10/11 have proposed acceptance of pad lift within certain limitations, because it is considered to be a non-critical defect and unavoidable for some technology.

This memo describes the investigation on acceptability for the future revised ECSS standards, as well as an intermediate approach until revision of the ECSS is finalised.

2 CRITICALITY OF PAD LIFT

According to its definition, pad lift is an adhesive separation between the copper pad and the dielectric material. In addition, cracks in the dielectric material (cohesive separation) under the pad can occur as a result of the same thermomechanical stress. For the purpose of this memo, such associated dielectric cracks are included within the definition of pad lift. Examples of pad lift and associated laminate cracks are shown in figure 1.

Among other things, the following elements are considered to contribute to pad lift: low Tg, CTE in Z-direction above Tg, duration above Tg, size of annular ring (pad diameter), diameter of hole, thickness of PCB, thickness of copper, dielectric thickness to second layer, component lead thickness and presence of stress relief. Dielectric materials with a Tg below the melting temperature of solder (183°C for eutectic SnPb) are prone to pad lift because the solder solidifies upon cooling and imposes strain on the pad, while the dielectric continues to shrink extensively until its temperature drops below Tg.

Thermal stress tests (solder bath floating test and, in particular, rework simulation) on coupons are considered representative of an assembled PCB. Therefore the pass/fail criteria for pad lift shall be identical. However, rework simulation comprises of 5x solder/de-solder cycles. The amount of rework or repair permitted on technology prone to pad lift could be limited as a risk mitigation.

ESA's concern with pad lift after thermal stress is the possible propagation of the defect as a result of mechanical vibrations, thermal cycling and CTE mismatch between component and PCB.

In the current ECSS-Q-ST-70-10C, pad lift is specified as a major non-conformance based on visual inspection after (1x) solder bath floating test or after vapour phase simulation, in accordance with clause 7.4.2.2/h.4+5. Pad lift is not specified to be evaluated in a microsection after solder bath floating test or after rework simulation.

As a reference, pad lift after thermal stress is acceptable according to IPC-6012DS for space applications until the height of the surface copper. The same requirement applies in IPC-J-STD-001ES for component holes on electronic assemblies in space applications.

On the as delivered PCB, without thermal stress test, pad lift is not considered acceptable. This is not a subject of discussion and not within the scope of this memo.

3 INVESTIGATE ACCEPTABILITY IN ECSS WG

The following tasks are proposed to the WG on ECSS-Q-ST-70-10/11:

1) Demonstrate by testing that the propagation of the defect beyond specified pass/fail criteria does not occur. The test shall envelop worst-case assembly configuration and space environment.

2) Demonstrate by heritage that technology prone to pad lift is performing adequately in space projects. The technology and the space environment shall envelop the future needs.

3) Advice shall be sought from IPC and NASA on their justification for accepting pad lift on assemblies in space applications.

4 INTERMEDIATE APPROACH TAKING IMMEDIATE EFFECT

For qualification renewal of any material, ESA shall evaluate pad lift taking into account the exact requirements of the current ECSS-Q-ST-70-10C, the newly proposed requirements for the document under revision and the requirements of IPC-6012DS. This means that PCB technology showing pad lift shall not a priori fail the qualification or the renewal.

For procurement, the occurrence of pad lift after thermal stress seen in microsections of the coupon within the limitations defined in IPC-6012DS and the ECSS under revision

shall be reported in the CoC. The customer shall be notified by the PCB manufacturer about ESA’s concerns for the electronic assembly as outlined in this memo. However, the CoC may still declare full compliance to the PID, in accordance with QT/2013/725/SH.

Furthermore, a specific review of the coupon design shall be performed during MRR on affected technology. The coupon shall discriminate a number of representative component holes and via holes, in accordance with ECSS-Q-ST-70-12C clause 15.2.d bullet 5a, 5b, 6, 7 and 8. Three times solder bath floating test shall be performed on component holes as well as via holes, as standard. Rework simulation shall be performed on component holes, as standard. Rework simulation shall not be performed on via holes.

To mitigate the risk of pad lift, the PID of the PCB manufacturer defines further design restrictions for component holes with respect to pad and hole diameters.

In case pad lift occurs on the coupon, the concern can be mitigated by the customer by implementing stress relief and by heritage with assembly of the technology. In case pad lift occurs and no stress relief is present, the customer shall demonstrate the non-criticality of pad lift to the ESA project. As a further mitigation for pad lift, the customer is recommended to limit the amount of repair or rework.

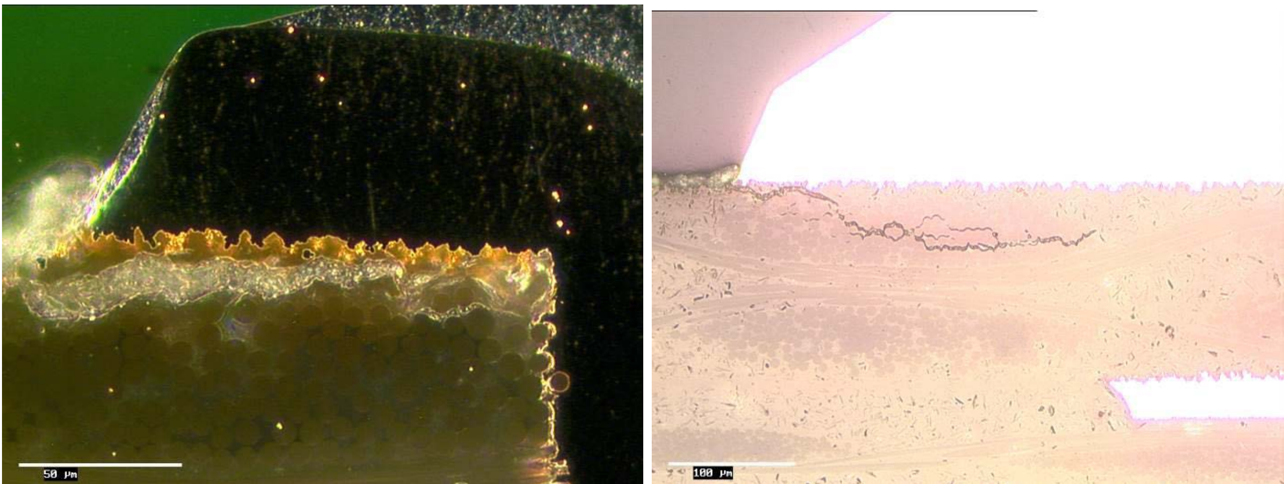

Figure 1: Examples of pad lift and associated laminate cracks in bright and dark field microscopy.