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MEMO

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From	Carole Villette	**Visa**	T. Ghidini
To	Companies having ESA Approved Summary Tables or under verification programme, ESA skills training school, ESA recommended outsourcing companies, ESA PA Managers,	**Copy**	G. Corocher, J. Hokka, R. de Marino, A. Pesce, L. Marchand, Th. Battault

Subject: Devices that have shown anomalies during assembly on laminates or during verification programme as per ECSS-Q-ST-70-38

This memo is the update of the TEC-QT/2012/206/CV and the ESA-TECQTM-MO-1143.

The changes between the different issues are highlighted in blue.

During the past years some failures on solder joints or in devices have been identified at the completion of the environmental testing performed in compliance with the ECSS-Q-ST-70-38C.

The intention of this memo is to allow all parties to be aware of the possible anomalies. This memo can be considered as informative. The objective is that each company will compile and maintain its own list of sensitive devices.

The assembly of the devices is considered sensitive when:

-The crack in the solder joint is longer than 75% of acceptable crack or when other anomalies have been identified after assembly and/or at the completion of the verification programme.

-The failure in the solder joints and/or in the devices has been noticed in many occasions by different end users.

Some of these listed sensitive devices may require higher number of devices to be verification tested as identified in the TEC-QT/2013/398/CV Memo.

The list of the devices is not exhaustive. This list may be updated once new anomalies are identified. The list of devices for which anomalies have been observed is uploaded on the escies website (www.escies.org).

Component	Package type	Type of failure	Possible cause of the failure	Possible preventive action
Chip Resistor	R1206, R2010, R2512	Cracks in the solder joint	CTE mismatch between PCB and component	- To increase the stand off. Such corrective action may not be sufficient.
Chip resistor network	Resistor network	Cracks in the solder joint	CTE mismatch between PCB and component	- To increase the stand off. Such corrective action may not be sufficient.
Chip Capacitors	Any of ceramic of type 2	Crack in the ceramic initiated at the end termination	-Thermal shock that may be caused during pretinning and or assembly, - Assembled part having been reworked	-Preparation and assembly procedures to be compliant to component manufacturer recommendations (preheating of the board, device and limited delta temperature between iron tip and component), -Pretinning is not recommended. - Due to the sensitivity to thermal shock ESA does not accept rework to be performed on such devices. Therefore in case of non conform solder joint the device is changed.
Chip capacitors	Size C1825 type 1 and type 2 and bigger	Cracks in the solder joint	-CTE mismatch	To increase the solder stand off when possible.
Active components	LCCs	Crack in the solder joint	CTE mismatch between PCB and component	-Degolding/ pretinning and soldering temperature used need to be compliant to the component manufacturer datasheet to avoid damage of the device, - To increase the stand off -Increase of stand off may not be sufficient (risk of poor wetting due to high thermal dissipation), -another possible alternative is to solder the device upside down and add gull wing terminations

				(need of verification in compliance with ECSS). In this case the change of solder footprint is needed. - To solder upside down and have long wiring implemented.
Tantalum capacitors	CWR06	Crack in the device. Crack in the epoxy between the tantalum and the terminal.	Component technology	-It is recommended to use TAJ/ CWR packages as these parts are less sensitive to package damage. - To avoid not needed thermal stress on the device (e.g. pretinning)
	SMDs (SMD0.5, SMD1, SMD2, SMD5C)	Crack in the ceramic	CTE mismatch between PCB and component	-Procurement of package with leaded terminations. - Assembly upside down using thermal adhesive and addition of wires or ribbons. This alternative needs to be verification tested in compliance with ECSS . This configuration may not be adapted for high thermal dissipation need.
	SMDs with ribbons assembled upside down	Crack in the ceramic	Component construction	-Minimum degolding and pretinning temperature to be applied -Soldering with hot air the ribbons onto the terminals.
Oscillator	JLCC4 with bottom brazed terminals	Crack in the solder joint	CTE mismatch/ component design Failure due to excessive stiffeness in the leads that does allow any stress relief during environmental test	-To wire the connection (functional impact shall be evaluated) -Use of an alternative package
Stacked	SOP from	-Crack in the	CTE	-The parts can be procured

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devices	3D+	solder joint -Unacceptable solder height at heel when hand soldering	mismatch/ component design	with shortened leads that allow better solder flow and allow proper solder at heel fillet.
Stacked capacitors	CNCXX	- poor wetting due to finish type 10 (Ag 98%)	Component technology	- To pre-tin the device
Photo transistor	Pill from micropac	- Cracks in the solder joint of the two small terminals	CTE mismatch between PCB and component	- To degold and pretin at temperature compliant to the component manufacturer recommendations. - Not to solder the bottom part on the PCB but to make a wiring connection.
Inductor	Coilcraft inductor AE235 type	Poor wetting of the terminals	Component technology	-To request coilcraft for additional cleaning of the terminal to remove the contamination from the enamel present on the terminal.
	Enamel wire	Short due to damaged enamel		-To inspect the wire to ensure absence of any damage in the insulation, -Procurement of a double enamel layer is recommended to reduce the risk of short, -Another alternative is to add an insulation (kapton, brady label, filled varnish…) between the wire and the metallic part to avoid direct contact with metallic traces.
Bottom terminated chip device	QFN	Cracks in the solder joint	CTE mismatch between PCB and component	-To increase stand off

Table 1: List of devices that have shown anomalies during the assembly verification as per ECSS-Q-ST-70-38 on PCB laminates.