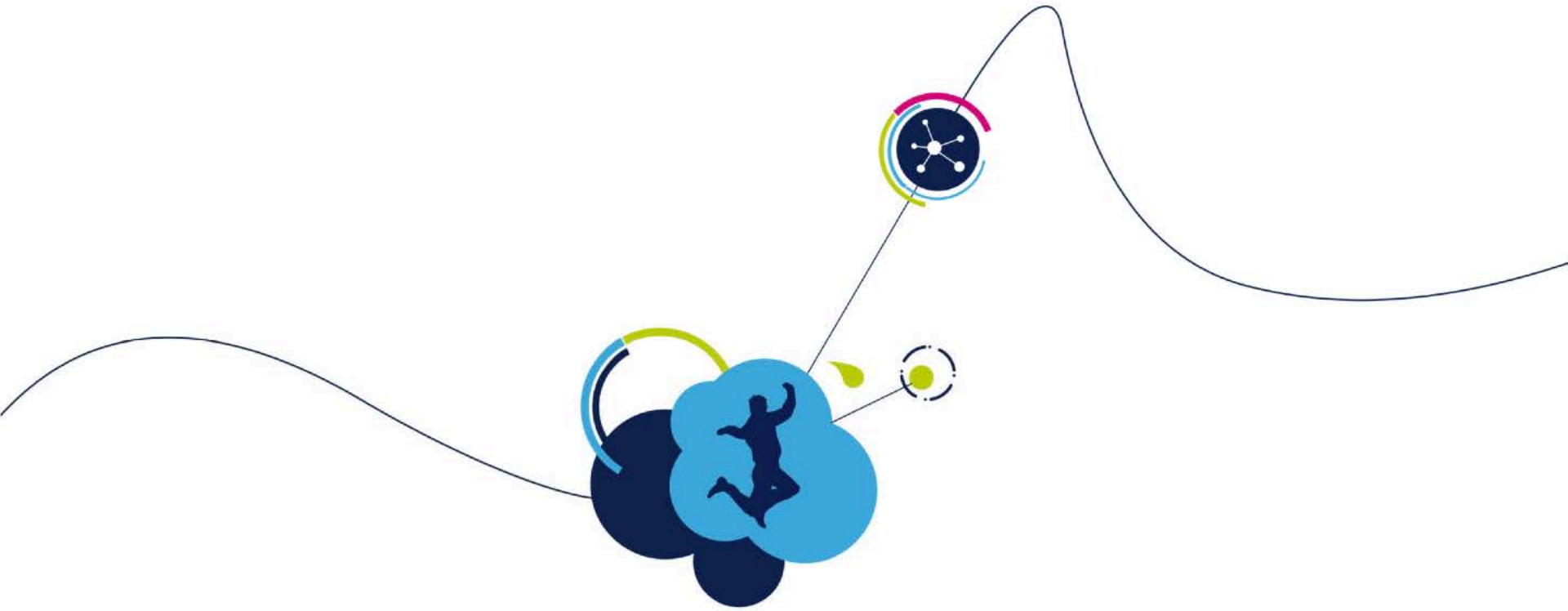

C65SPACE Hardened Design Platform

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Microelectronics section (TEC-EDM)

C65 Space at a glance

Faster, Denser, Space grade HiRel 65nm platform

- C65Space gate density better than 90nm alternatives
- Based on mature and HiVolume C65LP process
- Hi-Rel and RadHard Space mission profile validated through 10 test chips
- Outstanding immunity against high energy radiations

Extended design options

- Extended corners for space (20 yrs @125°C)
- Three VT flavors Rad-hard Ios *(2 standard Cells, 1 Memory)*
- Rad-hard PLL 1.2 GHz
- High performance standard cells
- ECC-protected HD/HS SRAM and ROM : *choice open left to designer for ST ECC solution or not*

Mature process & ecosystem

- Based on mature C65LP process and several test chips: wafer supply, design and manufacturing
- Design Environment and Extended IP offer
- Technology CMOS65LP selected by ESA for future space telecom applications & Earth Observation

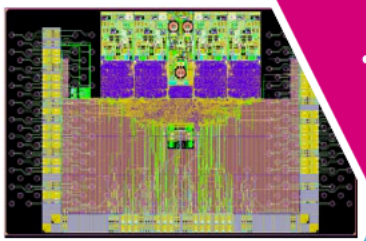
ST C65SPACE technology overview

Main Features

Process
7 copper metallization with 5 thin and 2 thick
Compatible with flip-chip and wire bounding packages
> 1200 Cells #110 clk network, #866 GP, #92 skyrob, #154 P&R
Radiation
No single event latch-up up to LET=60Mev/mg/cm2 at 125C and Vdd at 1.3V
TID @300kRAD
Reliability
Mission profile: 20 years at 110C with Vdd at 1.3V

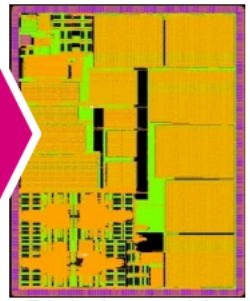
Rad-hard IO offer
- BIDIR
- I2C
- LVDS
- cold spare supported

Enabling High Speed design
- PLL 6 phases 200MHz – 1.2GHz
- HSSL IP up to 6.25Gbits/s (under Hardening)



HSSL test-chip

Rad-hard Digital offer
- Std-cells
- SRAM
- DPRAM (1R + 1W)
- ROM



Digital test-chip

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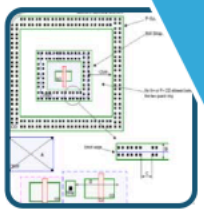
C65SPACE

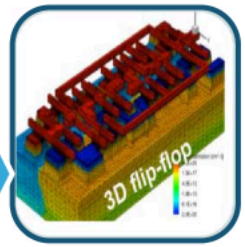
ESCC evaluated

Rad-hard process
- Space PDK
- Enhanced reliability



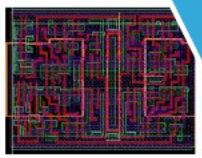
DRC rules for Space

Modeling capabilities
- 3D TCAD
- Fault injection
- Design in Reliability (DiR)

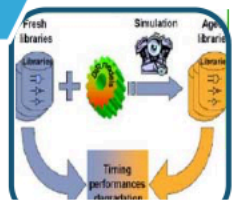


3D TCAD simulation

Rad-hard design techniques
- Rad-hard schematics
- Rad-hard layout
- DNW script



Rad-hard flip-flop



Extended Radiation Hardened IP offer C65SPACE

Standard cells

- 3.3V IO gate oxide GO2 (5nm)
- 1.2V core gate oxide, 1.8nm triple VT transistors
- 7 copper metallization
- Low-K intermetallic dielectrics

Memories

- Low voltage ROM Single port / Dual port
- BIST library, EDAC library
- High density SRAMs

Specific

- Process monitoring C65SPACE root process
- SKYROB65LP LVT/SVT SEE rad-hard performances

Analog IPs

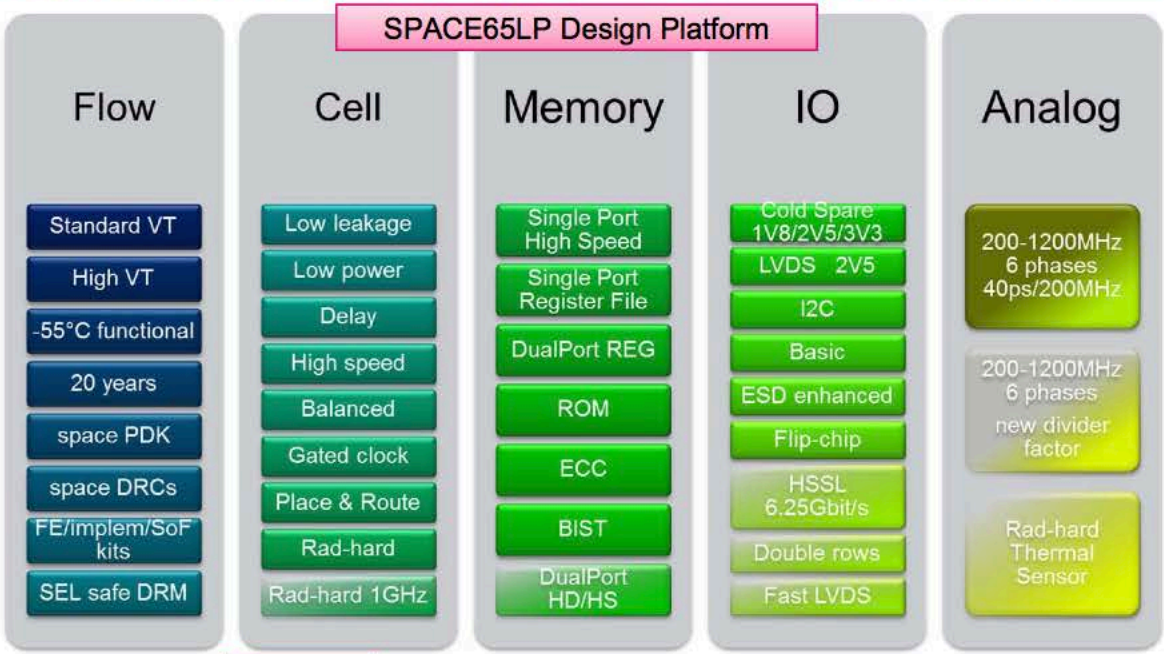
- Bandgaps
- Cold Sparing IOs
- Thermal sensor LVDS 600Mhz
- 6 phases, 200-1200MHz PLL

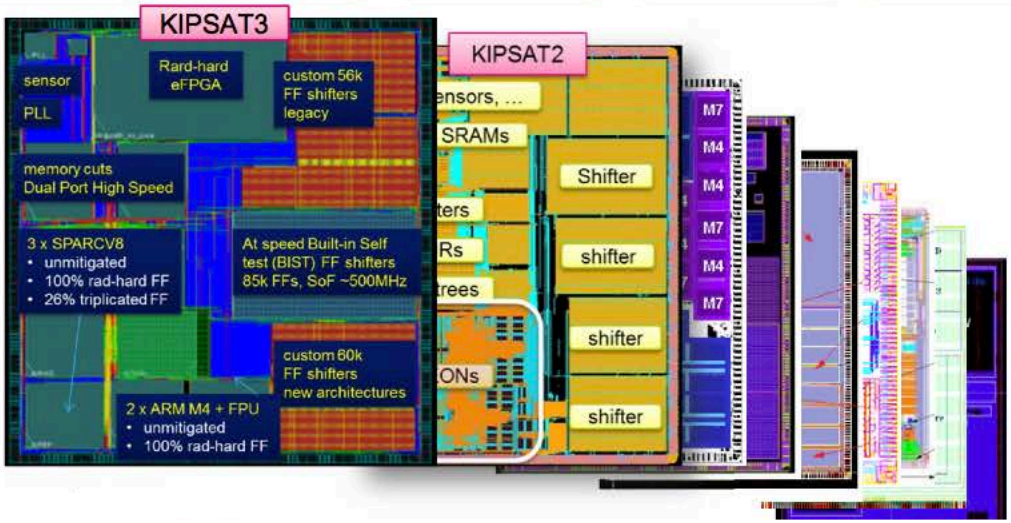
Advanced Ips (under qualification and/or in development or in plan)

- 6.2Gbit/s SerDes
- LVDS1.2Ghz
- DDR2/3 IO+ PHY + CTL
- eFPGA/ FPGA
- High speed ADC / DAC
- NetworkOnChip NOC
- Voltage regulators Vbias generators
- Oscillators

Key features 65nm SPACE ASIC platform

- **30+ space IPs/libraries created**
  - withstand space ions, protons, X-rays
  - sustain -55°C and 125°C/20yrs
    - vs. typical -40°C/10yrs
  - specific DRM against SEL
  - CAD flow upgraded
- **12 qualification circuits tested**
  - technology assessment
  - qualification of digital/analog IPs
  - space SPARC/ARM demonstrators
- **ASIC deployment since 2013**

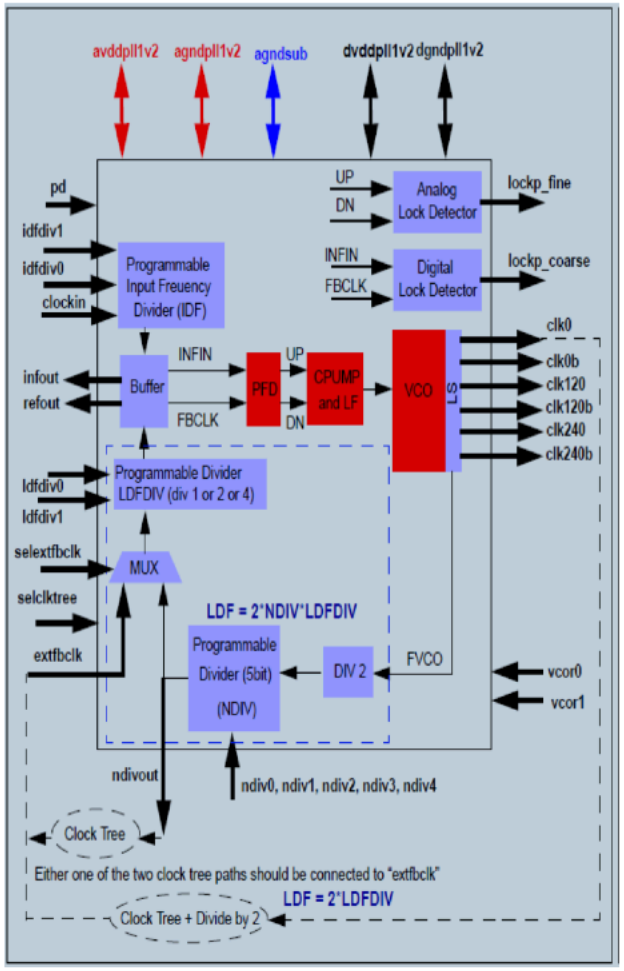




C65SPACE Memories SP/DP Offer

Memory Config for Space Platform	Word Count	Mux Range	Voltage Range Supported	Transistor Devices
C65LP_ST_DPHS_SPACE	64-8K	8	1.1V - 1.35V	Core full SVT,Periphery is SVT except few LVT devices
C65LP_ST_DPHD_SPACE	80-8K	4,8,16	1.1V - 1.35V	Core & Periphery full SVT
C65LP_ST_SPREG_SPACE	16-2048	2,4,8	1.1V - 1.35V (without debug)	Almost full SVT, few LVT used to optimize speed
C65LP_ST_DPREG_SPACE	16 - 4096	2,4,8	1.1V - 1.35V	Full SVT
C65LP_ST_ROMHS_SPACE	128 - 131072	16,32,64	1.1V - 1.35V	Almost full SVT, few HVT devices in periphery

C65SPACE Radiation Hardened 1.2GHz PLL



Highlights

- 1.2V PLL (for both analog and digital supplies)
- Programmable VCO frequency with very wide VCO frequency range
- 6 equidistance output clock phases
- Supports clock de-skew (with delay up to 8ns)
- Digital lock detection for coarse frequency lock
- Analog lock detection for fine phase lock

Technology Options	65nm, 50A GO2, LPSVT, 7M
Area	0.33514 mm^2
Maximum Power	29.25 mW
Analog Supply	1.1V – 1.3V
Digital Supply	1.1V – 1.3V
Input Frequency	20MHz - 400MHz
PFD Frequency	20MHz - 100MHz
VCO Frequency	200MHz - 1200MHz
Output Phases	6 (60 degrees apart)
Pk-pk Period jitter	+/-60ps@200MHz output

C65SPACE Radiation Hardened 6.25Gbps SERDES

SERDES Datasheet

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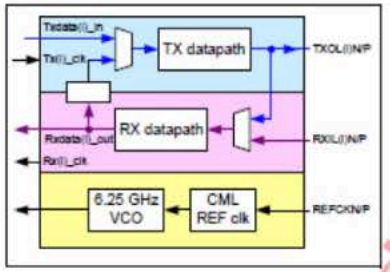
C65SPACE-HSSL

6.25 Gbps multi-rate, multi-lane, SerDes macro IP

Product preview



Features

- ST CMOS065LP low-power 65 nm CMOS technology
- 1.5625, 3.125 and 6.25 Gbps operation
- BER < 10^{-14}
- 20 bit TX and RX parallel data interface width / sub-rate mode
- Global power down and per link TX & RX power downs
- Compact form factor: 3040u x 1600u (tbc)
- Flip chip only layout
- Full immunity to single event latch-up (SEL) failures with a LET up to 60MeVcm2/mg
- No single event functional interrupts (SEFIs), up to 60MeVcm2/mg
- 1.2V power supply

Description

The ST 65 nm HSSL IP is a radiation hardened high-performance SERDES developed in ST CMOS065LP Low Power 65 nanometer CMOS technology and is provided as Flip chip only layout with build-in 2KV ESD protection. It features 8 channels (4Tx + 4 Rx) and is supplied by 1.2 volt.

It embeds a PLL and four identical data slices. Each data slice is composed of a data transmission lane and a data reception lane. The PLL provides very stable 6.25 GHz internal bit clock which is synthesized from a lower frequency input reference clock. This bit clock is used to generate each transmission bit clock and to recover each received bit clock.

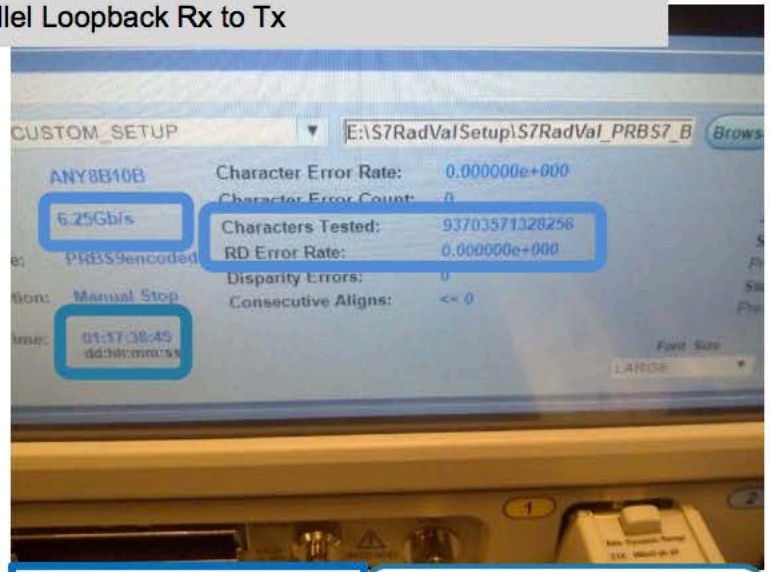
Each data slice is running independently to each other. In each data slice, the transmitter and receiver are running independently to each other and may have different bit rate.

A +/-100ppm plesiochronous operation is guaranteed by design in each data lane individually and independently (Tx data lane and Rx data lane).

Each data slice embeds one BIST which contains: a PRBS generator, a BER monitor, an internal data lane loopback TX -> RX (in each data slice) and a TX clock jitter generator.

BER Silicon measurement

Parallel Loopback Rx to Tx



BER=1e-14
CL =99,99 %

After 6 days, 0 errors@6.25Ghz
BER=1e-15, CL=96%

IP SoC Integration Application Note

HSSL Integration Note — ST Restricted

HSSL SerDes

HSSL SerDes Macro Integration Note

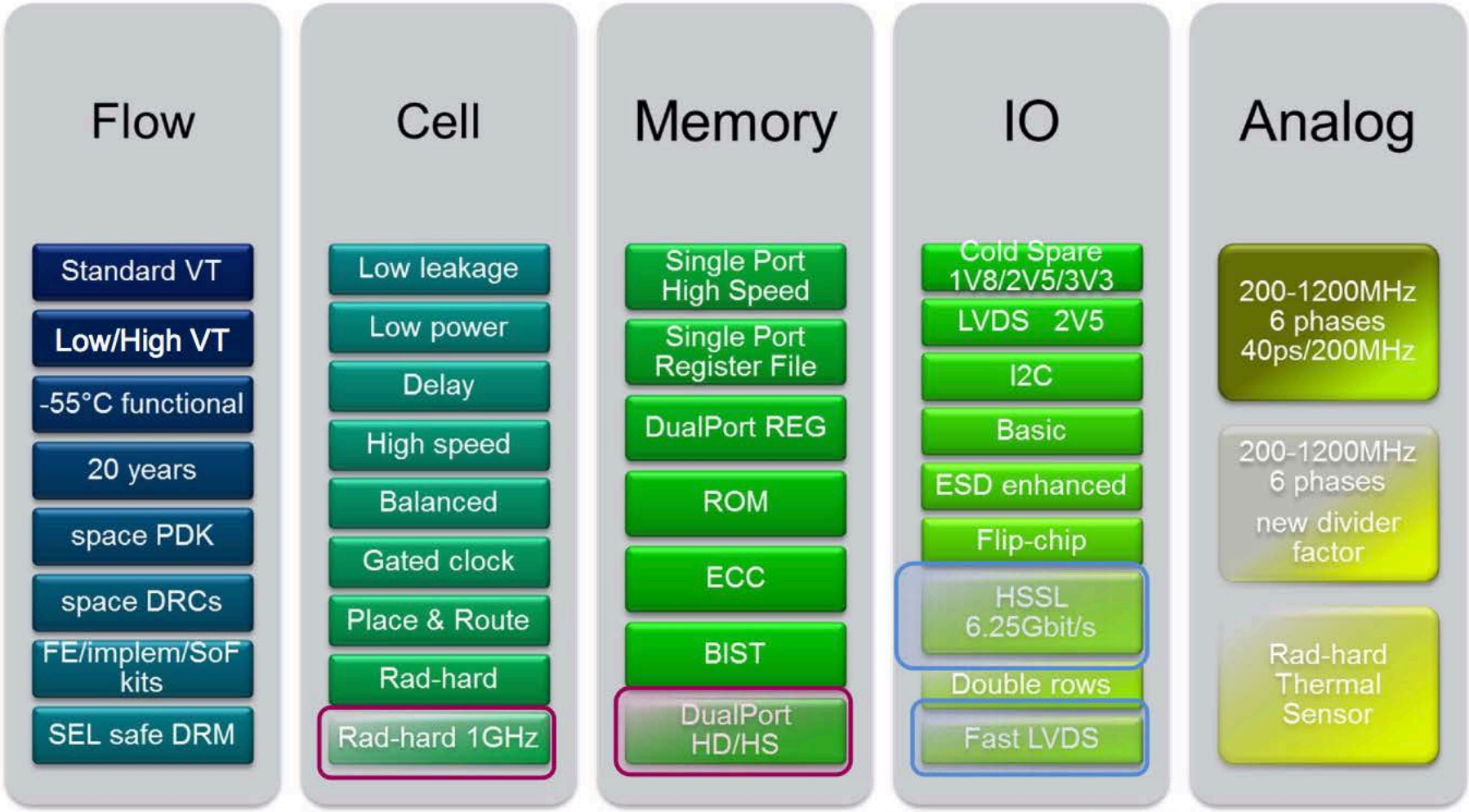
Rev. 0.7

C65SPACE Product Databook

Section	Subsections	Subparts content	# of pages
Catalog	1	Rad hard 65nm CMOS technology platform for space applications (description of main features)	22
Datasheets	5	Standard Cell Radiation Hardened Cell IO Library PLLs Sensors	1930
Radiation Test Report	4	Heavy Ions High Energy Protons	106
MAT20 Qualification Reports	11	Electrical Characterization report on LVDS Electrical Characterization report on I2C Electrical Characterization report on PLL PIRADVAL EWS test report ../..	302
MAT30 Qualification Reports	1	65nm Spatial Electrical Reliability Analysis Report	24
Certifications	1	CMOS065LP SPACE MAT30 Certificate (ST production milestone)	6
IEEE Publications	2	presented at NSREC 2013	14

C65SPACE Design Platform
Last upgrades

C65SPACE Design Platform Content

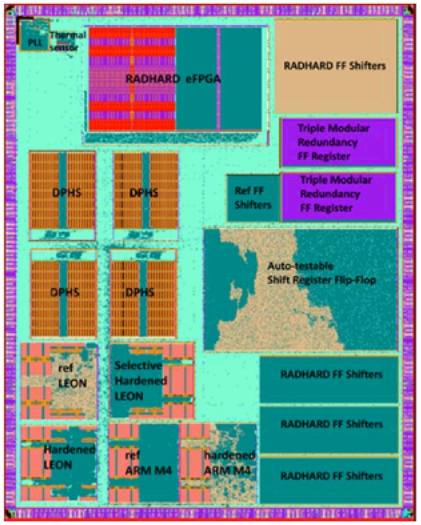


Electrical characterisation & successful Radiation test Completion Q4 2015

Design Done Q4 2015

Qualifying latest DIGITAL space IPs

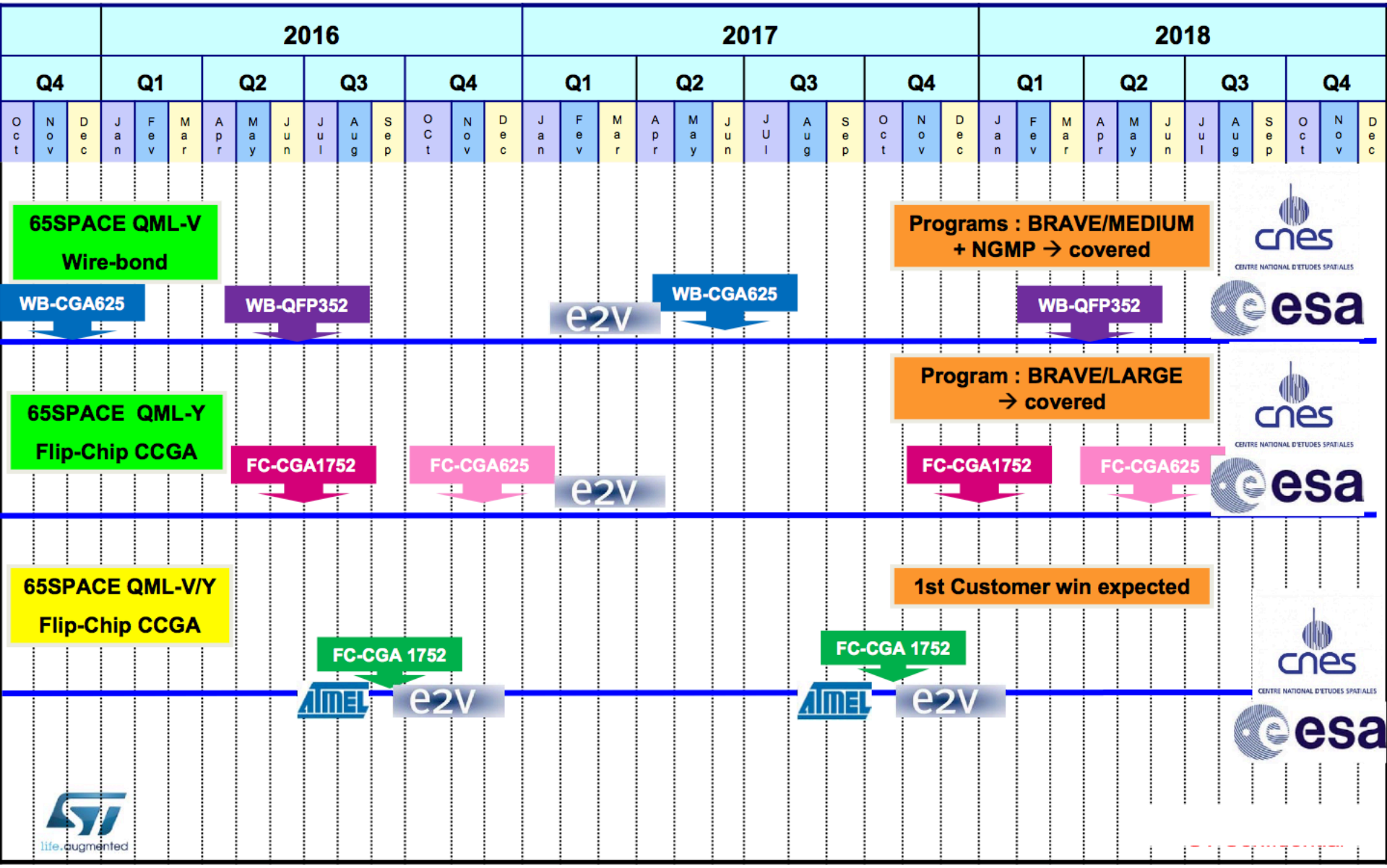
- **KIPSAT3 circuit with latest space digital IPs & CAD tools**
  - innovative test capabilities (at-speed BIST for flops)
  - rad-hard CPU/MCU prototypes (NGMP)
  - eFPGA macrocells (BRAVE)
- **Status on functional and radiation tests :**
  - 20+ blocks tested
  - 5+ reports issued showing successful radiations robustness (SEU & SEL)



Category	IP	Functional	Heavy ions	Heavy ions#2	Protons	Protons#2
Memories	Dual Port SRAM	done	done	W31	done	W31
	Reference FlipFlops	done	done	W31	done	W31
	Triplicated FlipFlops	done	done	W31	done	W31
	Redundant FlipFlops	done	done	W31	done	W31
	BIST Flip-Flop GHz	done	done	W31	done	W31
Microcontroller prototypes	Reference ARM M4	done	done	W31	done	W31
	Hardened ARM M4	done	done	W31	done	W31
Microprocessor prototypes	Reference LEON3	done	done	W44	done	W31
	Hardened LEON3	done	done	W44	done	W31
	Optimized LEON3	done	done	W44	done	W31
eFPGA macrocells	eFPGA	done	done	W31	done	W31
	Hardened eFPGA	done	done	W31	done	W31
Analog	Thermal Sensor	done	done	W31	done	W31
	Hardened PLL V1	done	done	W31	done	W31

QML-V, QML-Y C65SPACE Qualifications

C65SPACE ASICs QML-V, QML-Y Qualification Plan schedule



Thanks