EU FP7 MERLIN Research Project

Overview – Objectives – First results

Mikko Karppinen, VTT

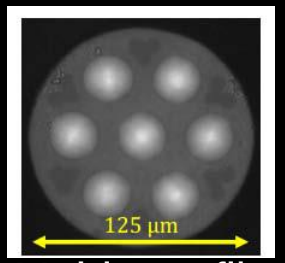
Intra-satellite Fibre Optic Links Workshop,
at ESTEC, 10 Dec 2015

Multi-gigabit, energy-efficient, ruggedized Lightwave engines for advanced on-board digital processors

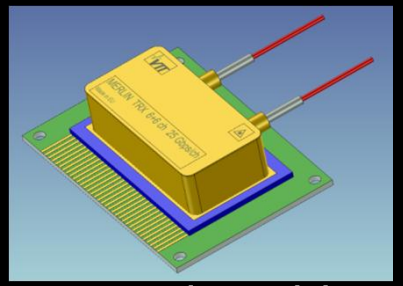
MERLIN project in a nutshell

Title: *Multi-Gigabit, Scalable & Energy Efficient on-board Digital Processors Employing Multicore, Vertical, Embedded Optoelectronic Engines*

- EU FP7 Space project grant for 2013–2016
- Objectives include:
  - Ruggedized optical transceiver "engines" with
    - record-high data rate of 150 Gb/s, in single fibre
    - record wide temp range; rad hard; low power
  - Very dense integration by the use of:
    - Novel multicore fibers
    - Custom VCSEL & PD arrays
    - Custom multi-channel ASICs



Multicore fiber (©OFS)


Transceiver Vision

Project coordinator: Leontios Stampoulidis, G&H

Project Objectives

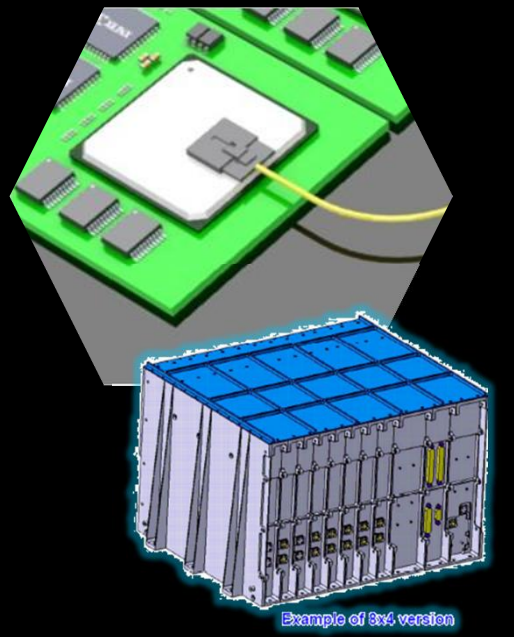
- Space transceivers for optical interconnects on board Tb/s satellite payloads
- Board level optical interconnection of digital transparent processors with the integration of:
  - 1. 850 nm circular VCSEL/PDs
  - 2. Rad-hard MM MC fibers
  - 3. Rad-hard electronics

Targets:

Power
- *<10mW / Gb/s*

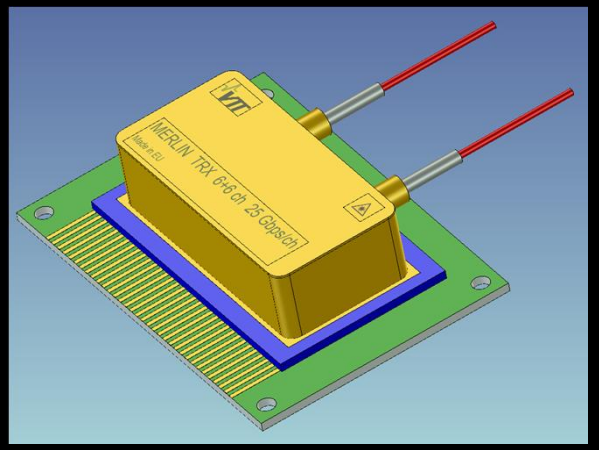
Speed
- *10-25 Gb/s line-rates*
- *150 Gb/s (6x 25 Gb/s) aggregate*

Packaging
- *Hermetic*
- *10x fiber count decrease*



Transceiver integration & packaging baseline targets

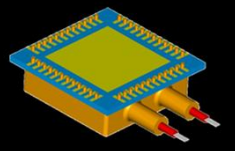
- VCSEL & PD arrays coupled to 6-core multimode fibers
- Fibre input/output parallel to PCB plane
- Radiation-resistant
- Hermetically sealed
- $T_{stor.}$ = –55…+125 °C
- $T_{oper.}$ = –40…+85 °C or up to +100 °C
  - MERLIN targeting state-of-the-art
- Small footprint and mass
- Surface-mountable on PCB at 25 Gb/s/channel



Project development phases

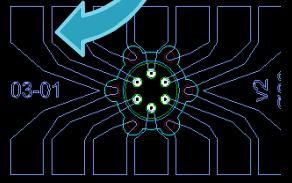
1st year:

- Define mission scenarios
- Define system requirements & module specifications
- Develop device & system level modeling toolkit
- Define component blueprint & fabrication methodology



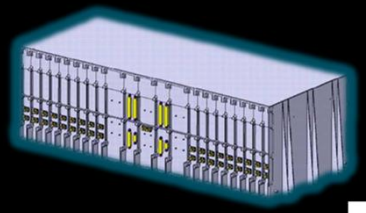
2nd year:

- Fabricate gen-1 components (VCSEL, PD, fibers & Electronics)
- Evaluate gen-1 components address 10-25 Gb/s
- Define gen-2
- Define test plan



3rd year:

- Fabricate & test gen-2
- Package & module integrate components
- System integration
- Functional & environmental trials



MERLIN Work Packages

WP2

LEADER: TAS
SPECIFICATIONS: Application – System – Module –Component – Integration method

WP3

LEADER: CHALMERS
OPTO-ELECTRONICS: VCSELs, PDs, BiCMOS ICs

WP4

LEADER: OFS
FIBERS: MM, MC FIBER & FANOUT

WP5

LEADER: VTT
MODULES & INTEGRATION: Transmitter & Transceiver module, prototype system development, testing

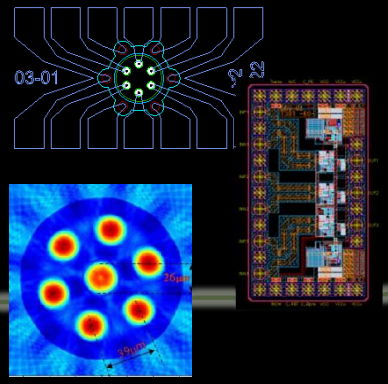
Some Key Achievement so far

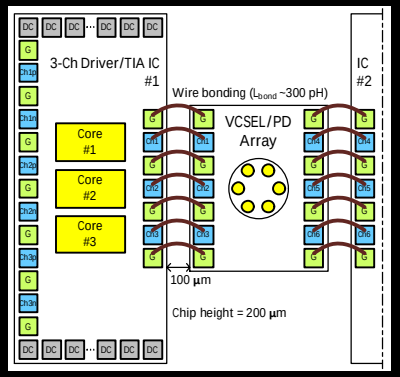
- VCSELs demonstrated up to 25 Gb/s @ 100 degC and 40Gb/s @ 85 degC
- PDs up to 25 Gb/s
- 1st Gen Driver and TIA chips up to 25 Gb/s
- 6-ch Tx and Rx Optical Engines demonstrated using the aforementioned devices

MERLIN evolution

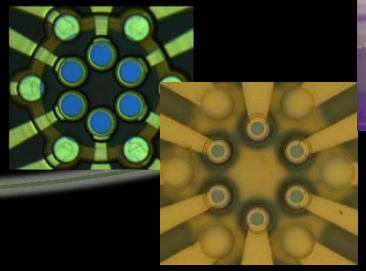
Integration
Functionality

Component design
Integration design

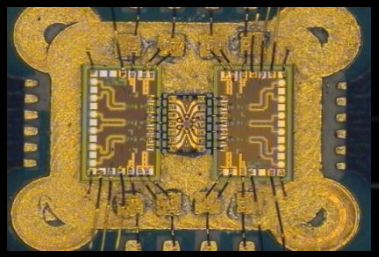




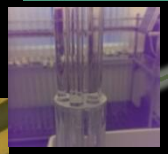
Gen-1

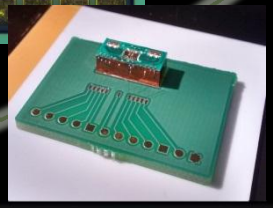


Integration concept
TOSA/ROSA



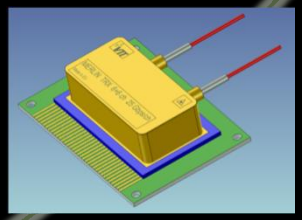
Gen-2



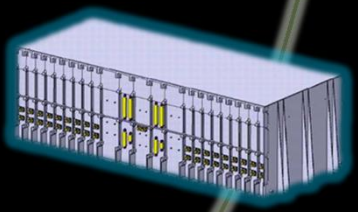


Engines

Module assembly



System concept



M12 **M24** **M36**

VCSELs

Specification	MERLIN high-speed HE-VCSELs Gen 1	MERLIN high-speed HE-VCSELs Gen 2	MERLIN Gen-1	MERLIN Gen-2
Technology platform	GaAs	GaAs	GaAs	GaAs
Operating wavelength (nm)	850	850	850	850
Bandwidth @ maximum operating temperature (GHz)	≥ 15	≥ 23	**19**	>25 GHz @ RT >20 GHz @ 100 degC
Modulation speed @ maximum operating temperature (Gb/s)	25	Up to 40	25 & 40 G demonstrated	Up to 40 G demonstrated
Maximum operating temperature (ºC)	100	85	85 demonstrated	100 degC demonstrated @ 25 Gb/s 85 degC demonstrated @ 40 Gb/s
Dissipated electrical energy per bit @ RT (fJ/bit)	≤ 200	<300	245	<200
Array & module integration	Circular 6-VCSEL array	Circular 6-VCSEL array	Circular 6-VCSEL array	Circular 6-VCSEL array Integration with drivers demonstrated