TOTAL DOSE RADIATION TEST REPORT

Part Type : MTW32N20E

Package : TO-247AE

N-Channel Power MOSFET

Motorola Semiconductors

Report Reference : ESA_QCA990904T_C

Issue : 01

Date : July 1st 1999

ESA Contract No 13413/98/NL/MV dated 25/01/99

ESTEC Technical Officer: R. Harboe Sorensen

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Written by :	J.F. PASCAL		Date :	
Approved by :	F.X GUERRE		Date :	

TOTAL DOSE RADIATION TEST REPORT
on
Motorola Semiconductors MTW32N20E N-Channel Power Mosfet.

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1 Abstract

Under ESA/ESTEC contract n° 13413/98/NL/MV covering "Radiation Evaluation of Power MOSFET Devices from Different European Manufacturers", a large number of commercial Power MOSFET device types were radiation assessed. Results from these assessments, primarily focused on the radiation sensitivity of the MOSFETs to Total Ionizing Dose (TID) and Single Event Effects (SEE), are reported in individual TID and SEE reports. Below summary table list manufacturer and evaluated types, and give references to the various reports issued.

Manufacturer	Type	TID Report	SEE Report
Philips	PHP50N06T	ESA_QCA990901T_C	ESA_QCA990901S_C
Philips	BUK456-200A	ESA_QCA990902T_C	ESA_QCA990902S_C
Motorola	MTP50N06VL	ESA_QCA990903T_C	
Motorola	MTW32N20E	ESA_QCA990904T_C	
Motorola	MTP50N06V	ESA_QCA990905T_C	
Siemens	BUZ100S	ESA_QCA990906T_C	ESA_QCA990906S_C
Siemens	BUZ100SL	ESA_QCA990907T_C	ESA_QCA990907S_C
Siemens	BUZ341	ESA_QCA990908T_C	ESA_QCA990908S_C
SGS-Thomson	SP60	ESA_QCA990909T_C	ESA_QCA990909S_C
SGS-Thomson	SP100V	ESA_QCA9909010T_C	ESA_QCA9909010S_C
SGS-Thomson	SP200V	ESA_QCA9909011T_C	ESA_QCA9909011S_C
Siemens	SPP1N60S5	ESA_QCA9909012T_C	ESA_QCA9909012S_C
Philips	BUK7508-55	ESA_QCA9909013T_C	ESA_QCA9909013S_C
Harris	HUF75639P3	ESA_QCA9909014T_C	ESA_QCA9909014S_C

2 Introduction

A total dose radiation evaluation test of the Motorola Semiconductors MTW32N20E N-Channel Power Mosfet has been performed with an accumulated dose of about 37 Krad(Si) at a dose rate of 75 rad(Si)/hour, in response to European Space Agency contract reference : 13413/98/NL/MV.

The purpose of this test was to evaluate total dose withstanding of this component, to investigate its suitability for being used in space applications. This test was conducted on commercial samples provided by ESTEC.
Test has been performed in accordance with Hirex proposal HRX/98.3475 issue 01.

A complete set of electrical measurements together with graphical representation of measured parameters with respect to total dose received, are provided for all samples.

3 Applicable and Reference Documents

3.1 Applicable Documents

- ESA/SCC Basic specification N° 22900 issue 4
- Motorola Semiconductors datasheet (See Annex)
- Hirex Engineering proposal: HRX/98.3475 issue 01.

3.2 Reference Documents

- MIL-STD-883: test methods and procedures for microcircuits

4 Test Samples

11 samples of the MTW32N20E device were tested (2 groups of 5 + 1 control sample). The samples were serialized before the radiation test as indicated in the following table.

Serial Number	Allocation
1	Control
2	Bias 1
3	Bias 1
4	Bias 1
5	Bias 1
6	Bias 1
7	Bias 2
8	Bias 2
9	Bias 2
10	Bias 2
11	Bias 2

Identification of the MTW32N20E is given below:

Part Number:	MTW32N20E	**Mask Set:**	NA
Top Marking:	DE9734 MTW32N20E	**Chip Marking:**	NA
Diffusion Lot:	NA	**Wafer #:**	NA
Date Code:	9734	**Project:**	Not defined

5 Experimental Conditions

5.1 Radiation Source Dose Rate and Annealing

The dose exposures were performed at CERT-ONERA. In this irradiation facility, a Cobalt 60 source is used with the possibility to vary the dose rate by simply adjusting the distance to the source.
The irradiation conditions used for this test are provided in the following table:

Irradiation Steps	Dose rate	Annealing steps	Temperature
krads	krads/h	hours	°C
0			
3.85	0,075		25
7.35	0,075		25
13.95	0,075		25
19.65	0,075		25
24.65	0,075		25
29.85	0,075		25
36.85	0,075	0	25
		24	25
		192	100

5.2 Bias during Dose Exposures and Measurements conditions

5.2.1 Bias conditions

During exposures dedicated test boards were used mounted on a special board-holder made for irradiation. The test board allowed to bias the devices in accordance with the electrical circuit provided in Figure 1. Two bias conditions were used so called Bias 1 and Bias 2.
Bias 1 corresponds to a gate stress of VGSS equals 12 Volts. Bias 2 corresponds to drain to source stress equals 80% of BVDSS.
During annealing steps the same stress conditions were applied at room and 100°C temperatures respectively.

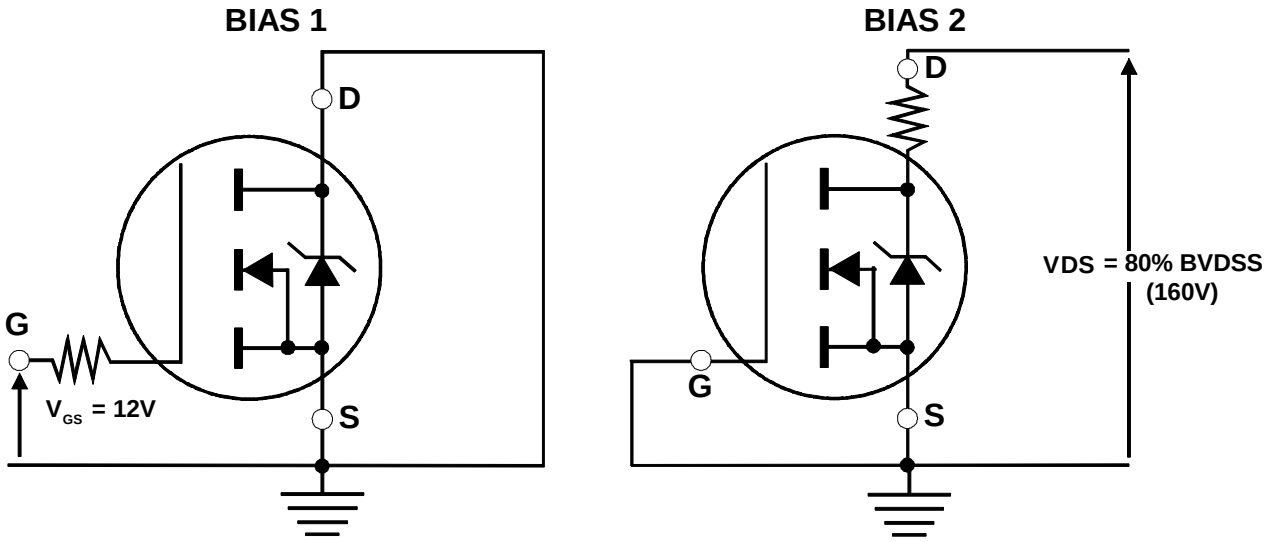


Figure 1 : Bias Conditions during Irradiation Exposures and Annealing

5.2.2 Electrical Measurements

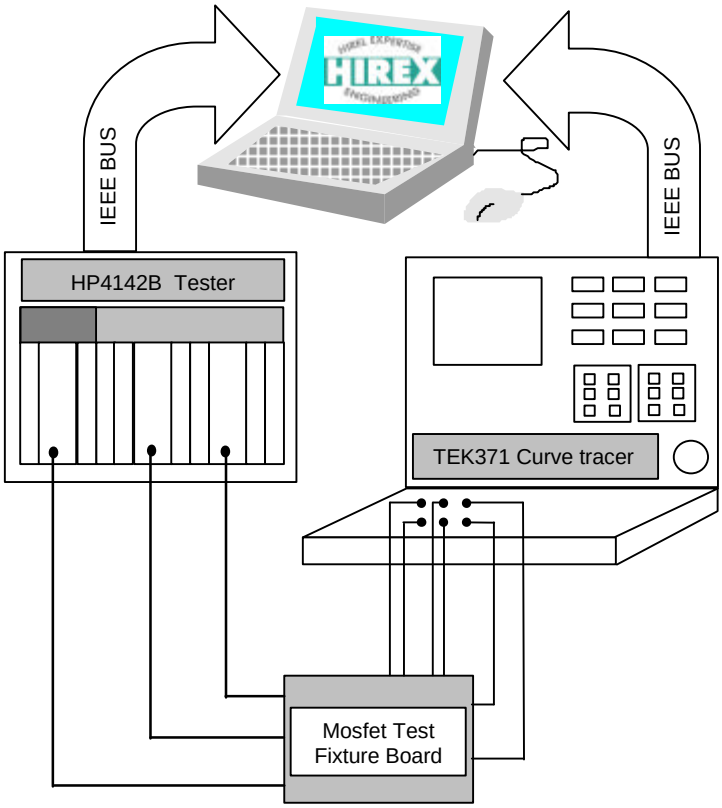
Mosfet transistor test program principle is provided in Figure 2. Due to the great number of samples to be measured (test campaign was conducted on 14 part types at the same time) and the time interval constraints required for performing measurements after each exposure and annealing step, It was decided to automate low power and high power measurements.

Two instruments were used to cover low power and high power measurements respectively.
HP4142B was used for breakdown voltage, gate and drain leakage currents, and threshold voltage measurements.
Tektronix TEK371 high power curve tracer was used for R_{DSON} measurements.

A dedicated test fixture was designed to ensure proper switching of instruments. In addition a faraday cup was used to ensure optimum conditions for low level measurements.

Test program has been written in Visual Basic on a PC computer. HPIB commands were sent to each instrument via IEEE bus, in order to measure a given parameter with specified conditions.
Results were automatically loaded in an Excel worksheet and compared in real time to specification limits. This allowed for real time data analysis in particular when failures were recorded.

Figure 2 : Mosfet transistor test program principle



Electrical parameters test conditions and limits used for performing this test are given in the following table.

Symbol	Test Parameter	Test Conditions	Min limit	Max limit	Unit
BVDSS	Drain to Source breakdown voltage	VGS=0V, ID=0.25mA	200		V
VGSTH	Gate to Source threshold voltage	VDS>=VGS, ID=0.25mA	2	4	V
+IGSS	Positive Gate Source leakage current	VGS=+20V, VDS=0V		100	nA
-IGSS	Negative Gate Source leakage current	VGS=-20V, VDS=0V		100	nA
IDSS	Drain current	VGS=0V, VDS=200V		250	µA
RDSON	Static drain to source on-state resistance	VGS=10V, ID=16A		0.075	Ohm

Table 1 : Measured electrical parameters

6 Test Summary

A Total Ionizing Dose assessment was carried out by Hirex Engineering under ESA contract on the Motorola MTW32N20E N-Channel Power Mosfet.
2 groups of 5 samples each plus one control sample were used during testing. The first group was exposed to radiation using Bias 1 conditions corresponding to a gate stress of the devices. The second group of 5 samples was exposed to radiation using Bias 2 conditions corresponding to drain to source stress of the devices, equals 80% of BVDSS (160 Volts).

Based on the analysis of the results, the tolerances of this component and main conclusion are provided below.

Parametric Tolerance Level (>=Krad) - Bias 1:	13.95
Parametric Tolerance Level (>=Krad) - Bias 2:	3.85

Parametric tolerance level represents the last cumulative exposure at which no samples failed any test

Main conclusion:

Most samples exhibited high drain to source leakage currents and consequently very low breakdown voltages, at 24.65 Krad(Si) and 19.65 Krad(Si) dose respectively, under Bias 2 conditions.
Threshold voltage is out of specification at 19.65 Krad(Si) under Bias 1 conditionsThreshold voltage is out of specification at 7.35 Krad(Si) under Bias 2 conditions. In addition this parameter becomes negative after 24.65 Krad(Si) exposure.

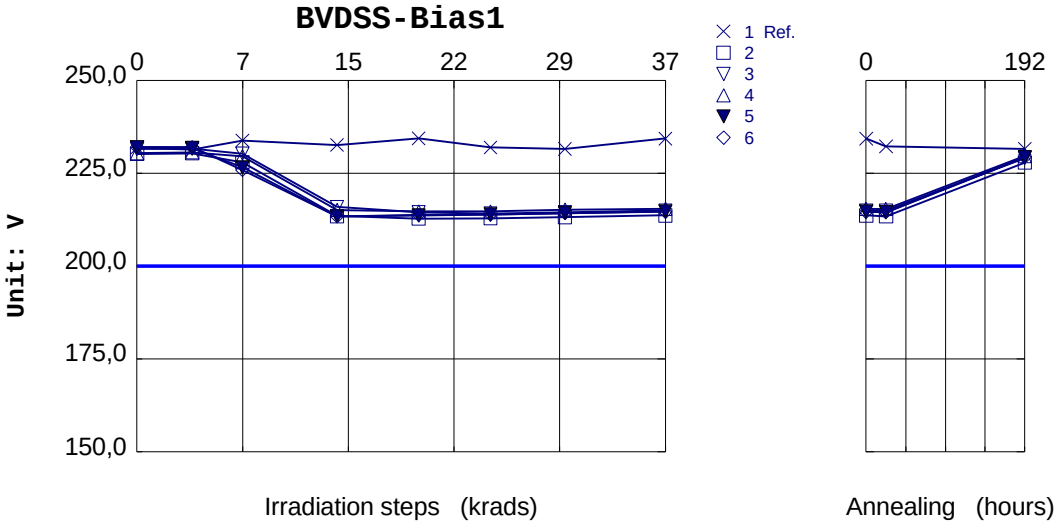
7 Test Results

Test results including tables and graphics are provided in this section for each measured parameter. To allow easy reading of data, each parameter is plotted twice, one for the first bias condition: Bias 1 and one for the second condition: Bias 2.

Parameter: Drain to source breakdown voltage: BVDSS-Bias1 **VGS=0V, ID=0.25mA**
Unit= V
Spec limit min: 200
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,318E +02	2,314E +02	2,338E +02	2,326E +02	2,344E +02	2,319E +02	2,315E +02
2	2,302E +02	2,304E +02	2,279E +02	2,135E +02	2,128E +02	2,129E +02	2,132E +02
3	2,315E +02	2,316E +02	2,303E +02	2,159E +02	2,144E +02	2,142E +02	2,144E +02
4	2,304E +02	2,306E +02	2,296E +02	2,151E +02	2,147E +02	2,147E +02	2,152E +02
5	2,320E +02	2,317E +02	2,265E +02	2,133E +02	2,136E +02	2,139E +02	2,142E +02
6	2,320E +02	2,320E +02	2,259E +02	2,133E +02	2,138E +02	2,138E +02	2,143E +02
Statistics							
Min	2,302E +02	2,304E +02	2,259E +02	2,133E +02	2,128E +02	2,129E +02	2,132E +02
Max	2,320E +02	2,320E +02	2,303E +02	2,159E +02	2,147E +02	2,147E +02	2,152E +02
Mean	2,312E +02	2,313E +02	2,280E +02	2,142E +02	2,139E +02	2,139E +02	2,143E +02
Sigma	8,721E -01	7,453E -01	1,890E +00	1,198E +00	7,444E -01	6,491E -01	7,288E -01

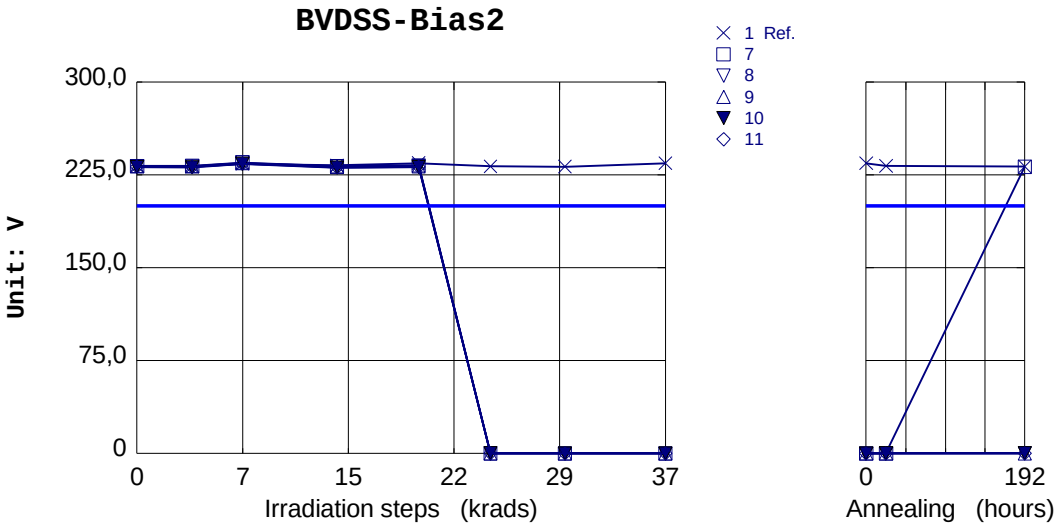
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	2,343E +02	2,322E +02	2,316E +02
2	2,136E +02	2,134E +02	2,279E +02
3	2,149E +02	2,149E +02	2,291E +02
4	2,154E +02	2,153E +02	2,296E +02
5	2,147E +02	2,144E +02	2,293E +02
6	2,146E +02	2,145E +02	2,293E +02
Statistics			
Min	2,136E +02	2,134E +02	2,279E +02
Max	2,154E +02	2,153E +02	2,296E +02
Mean	2,146E +02	2,145E +02	2,290E +02
Sigma	6,414E -01	7,330E -01	6,817E -01



Parameter: Drain to source breakdown voltage: BVDSS-Bias2 **VGS=0V, ID=0.25mA**
Unit= V
Spec limit min: 200
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,318E +02	2,314E +02	2,338E +02	2,326E +02	2,344E +02	2,319E +02	2,315E +02
7	2,322E +02	2,322E +02	2,349E +02	2,320E +02	2,327E +02	4,000E -02	1,000E -02
8	2,319E +02	2,319E +02	2,346E +02	2,316E +02	2,321E +02	2,000E -02	1,000E -02
9	2,317E +02	2,316E +02	2,343E +02	2,312E +02	2,319E +02	1,000E -02	1,000E -02
10	2,311E +02	2,310E +02	2,338E +02	2,307E +02	2,312E +02	2,000E -02	1,000E -02
11	2,314E +02	2,313E +02	2,341E +02	2,310E +02	2,315E +02	2,000E -02	1,000E -02
Statistics							
Min	2,311E +02	2,310E +02	2,338E +02	2,307E +02	2,312E +02	1,000E -02	1,000E -02
Max	2,322E +02	2,322E +02	2,349E +02	2,320E +02	2,327E +02	4,000E -02	1,000E -02
Mean	2,317E +02	2,316E +02	2,343E +02	2,313E +02	2,319E +02	2,200E -02	1,000E -02
Sigma	4,214E -01	4,828E -01	4,445E -01	5,174E -01	5,820E -01	1,095E -02	0,000E +00

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	2,343E +02	2,322E +02	2,316E +02
7	1,000E -02	1,000E -02	2,313E +02
8	1,000E -02	1,000E -02	1,400E -01
9	1,000E -02	1,000E -02	6,000E -02
10	0,000E +00	2,000E -02	7,000E -02
11	1,000E -02	1,000E -02	5,000E -02
Statistics			
Min	0,000E +00	1,000E -02	5,000E -02
Max	1,000E -02	2,000E -02	2,313E +02
Mean	8,000E -03	1,200E -02	4,633E +01
Sigma	4,472E -03	4,472E -03	1,034E +02

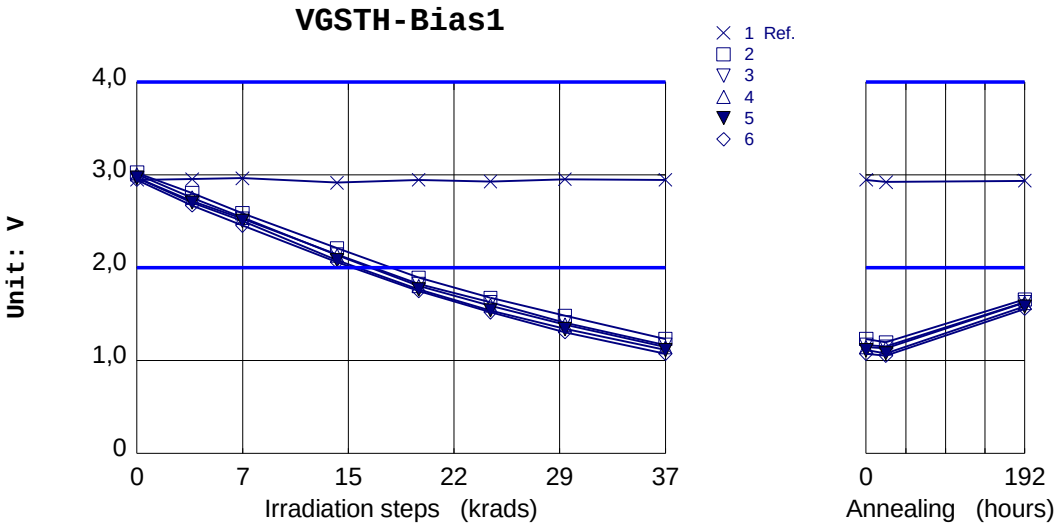


Parameter: Gate to source threshold voltage: VGSTH-Bias1 **VDS>=VGS, ID=0.25mA**

Unit= V
Spec limit max: 4
Spec limit min: 2
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,946E +00	2,953E +00	2,962E +00	2,914E +00	2,944E +00	2,927E +00	2,952E +00
2	3,023E +00	2,803E +00	2,587E +00	2,208E +00	1,893E +00	1,674E +00	1,482E +00
3	2,965E +00	2,716E +00	2,526E +00	2,142E +00	1,824E +00	1,629E +00	1,409E +00
4	3,006E +00	2,753E +00	2,539E +00	2,131E +00	1,803E +00	1,592E +00	1,387E +00
5	2,968E +00	2,701E +00	2,503E +00	2,079E +00	1,765E +00	1,539E +00	1,339E +00
6	2,945E +00	2,670E +00	2,453E +00	2,059E +00	1,746E +00	1,518E +00	1,306E +00
Statistics							
Min	2,945E +00	2,670E +00	2,453E +00	2,059E +00	1,746E +00	1,518E +00	1,306E +00
Max	3,023E +00	2,803E +00	2,586E +00	2,208E +00	1,893E +00	1,674E +00	1,482E +00
Mean	2,981E +00	2,728E +00	2,521E +00	2,124E +00	1,806E +00	1,591E +00	1,385E +00
Sigma	3,200E -02	5,119E -02	4,906E -02	5,847E -02	5,721E -02	6,397E -02	6,775E -02

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	2,945E +00	2,921E +00	2,936E +00
2	1,231E +00	1,196E +00	1,658E +00
3	1,168E +00	1,150E +00	1,629E +00
4	1,143E +00	1,130E +00	1,622E +00
5	1,111E +00	1,077E +00	1,581E +00
6	1,072E +00	1,052E +00	1,556E +00
Statistics			
Min	1,072E +00	1,052E +00	1,556E +00
Max	1,231E +00	1,196E +00	1,658E +00
Mean	1,145E +00	1,121E +00	1,609E +00
Sigma	6,017E -02	5,757E -02	4,062E -02

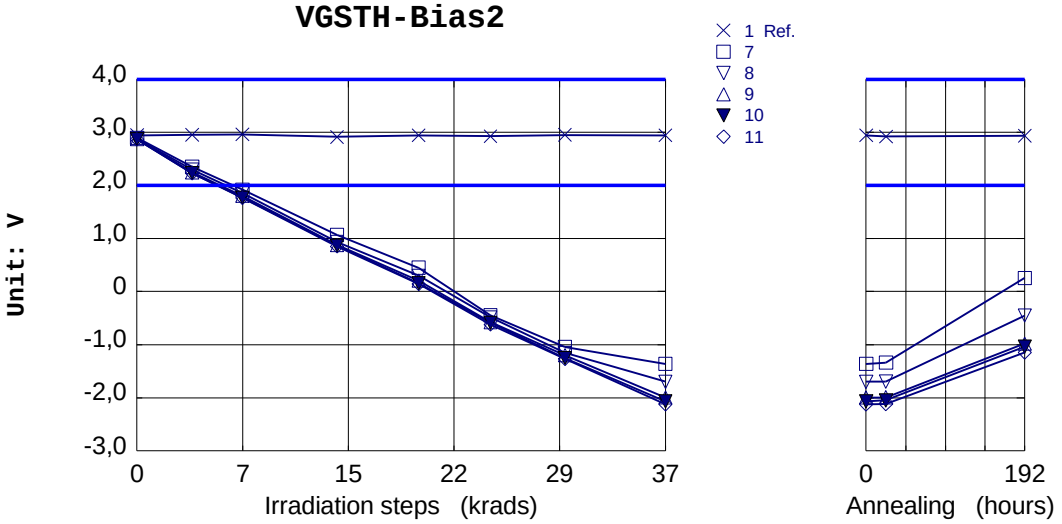


Parameter: Gate to source threshold voltage: VGSTH-Bias2 **VDS>=VGS, ID=0.25mA**

Unit= V
Spec limit max: 4
Spec limit min: 2
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,946E +00	2,953E +00	2,962E +00	2,914E +00	2,944E +00	2,927E +00	2,952E +00
7	2,899E +00	2,351E +00	1,921E +00	1,066E +00	4,477E -01	-4,480E -01	-1,045E +00
8	2,883E +00	2,298E +00	1,854E +00	9,327E -01	3,006E -01	-4,870E -01	-1,154E +00
9	2,875E +00	2,248E +00	1,807E +00	8,776E -01	2,045E -01	-5,740E -01	-1,198E +00
10	2,872E +00	2,230E +00	1,770E +00	8,653E -01	1,559E -01	-5,870E -01	-1,254E +00
11	2,869E +00	2,229E +00	1,766E +00	8,502E -01	1,447E -01	-6,220E -01	-1,268E +00
Statistics							
Min	2,869E +00	2,229E +00	1,766E +00	8,502E -01	1,447E -01	-6,220E -01	-1,268E +00
Max	2,899E +00	2,351E +00	1,921E +00	1,066E +00	4,477E -01	-4,480E -01	-1,045E +00
Mean	2,880E +00	2,271E +00	1,824E +00	9,184E -01	2,507E -01	-5,436E -01	-1,184E +00
Sigma	1,174E -02	5,275E -02	6,515E -02	8,835E -02	1,262E -01	7,297E -02	8,996E -02

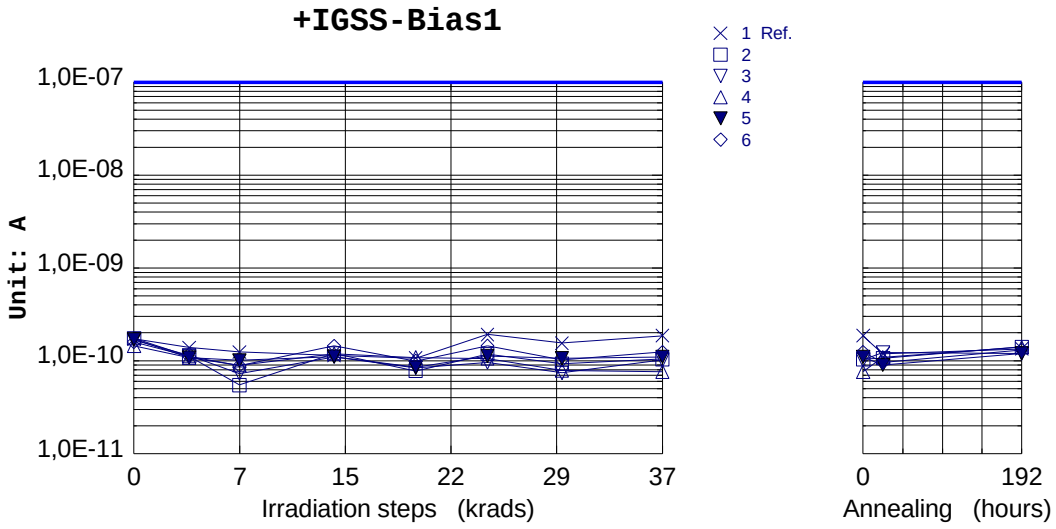
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	2,945E +00	2,921E +00	2,936E +00
7	-1,362E +00	-1,340E +00	2,563E -01
8	-1,701E +00	-1,697E +00	-4,521E -01
9	-1,997E +00	-1,994E +00	-9,799E -01
10	-2,072E +00	-2,049E +00	-1,038E +00
11	-2,124E +00	-2,118E +00	-1,147E +00
Statistics			
Min	-2,124E +00	-2,118E +00	-1,147E +00
Max	-1,362E +00	-1,340E +00	2,563E -01
Mean	-1,851E +00	-1,840E +00	-6,721E -01
Sigma	3,187E -01	3,221E -01	5,841E -01



Parameter: Positive Gate source leakage current: +IGSS-Bias1 **VGS=+20V, VDS=0V**
Unit= A
Spec limit max: 100E-9
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	1,723E -10	1,396E -10	1,250E -10	1,143E -10	1,073E -10	1,927E -10	1,556E -10
2	1,755E -10	1,121E -10	5,488E -11	1,204E -10	7,790E -11	1,188E -10	9,312E -11
3	1,677E -10	1,146E -10	7,308E -11	1,100E -10	8,396E -11	9,616E -11	7,422E -11
4	1,455E -10	1,082E -10	8,942E -11	1,193E -10	1,089E -10	1,065E -10	7,874E -11
5	1,717E -10	1,086E -10	1,013E -10	1,108E -10	8,518E -11	1,130E -10	1,067E -10
6	1,597E -10	1,115E -10	8,904E -11	1,448E -10	9,960E -11	1,460E -10	1,020E -10
Statistics							
Min	1,455E -10	1,082E -10	5,488E -11	1,100E -10	7,790E -11	9,616E -11	7,422E -11
Max	1,755E -10	1,146E -10	1,013E -10	1,448E -10	1,089E -10	1,460E -10	1,067E -10
Mean	1,640E -10	1,110E -10	8,154E -11	1,211E -10	9,110E -11	1,161E -10	9,096E -11
Sigma	1,190E -11	2,652E -12	1,796E -11	1,410E -11	1,273E -11	1,872E -11	1,418E -11

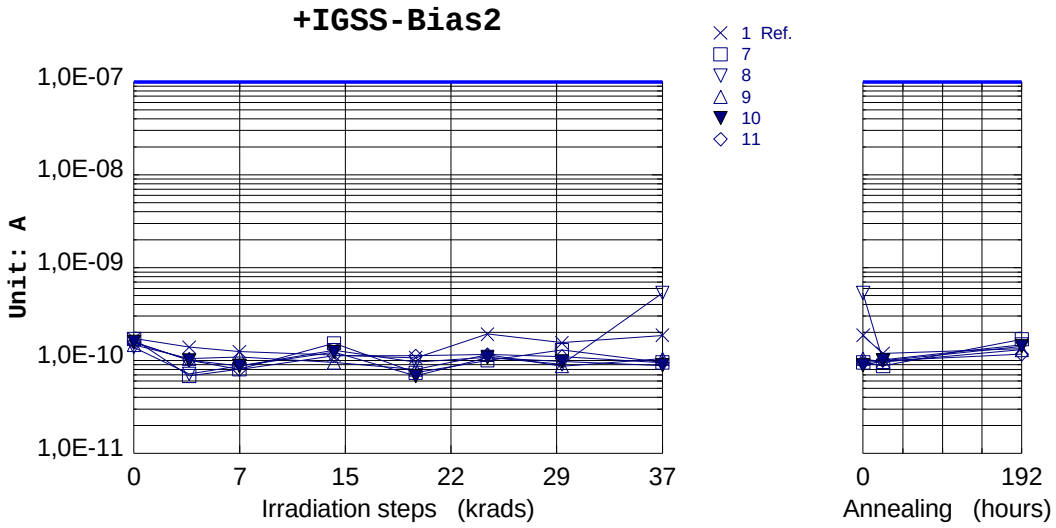
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	1,867E -10	1,196E -10	1,347E -10
2	1,042E -10	1,069E -10	1,412E -10
3	1,020E -10	1,227E -10	1,200E -10
4	7,634E -11	1,091E -10	1,407E -10
5	1,100E -10	9,014E -11	1,203E -10
6	1,245E -10	9,622E -11	1,312E -10
Statistics			
Min	7,634E -11	9,014E -11	1,200E -10
Max	1,245E -10	1,227E -10	1,412E -10
Mean	1,034E -10	1,050E -10	1,307E -10
Sigma	1,749E -11	1,256E -11	1,042E -11



Parameter: Positive Gate source leakage current: +IGSS-Bias2 **VGS=+20V, VDS=0V**
Unit= A
Spec limit max: 100E-9
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	1,723E -10	1,396E -10	1,250E -10	1,143E -10	1,073E -10	1,927E -10	1,556E -10
7	1,701E -10	6,806E -11	8,048E -11	1,538E -10	7,384E -11	1,000E -10	1,294E -10
8	1,387E -10	7,158E -11	8,744E -11	1,290E -10	9,616E -11	1,087E -10	9,070E -11
9	1,477E -10	1,047E -10	1,095E -10	9,536E -11	8,002E -11	1,154E -10	8,694E -11
10	1,588E -10	1,009E -10	8,734E -11	1,229E -10	6,802E -11	1,077E -10	9,752E -11
11	1,573E -10	1,011E -10	7,994E -11	1,126E -10	1,126E -10	1,158E -10	1,105E -10
Statistics							
Min	1,387E -10	6,806E -11	7,994E -11	9,536E -11	6,802E -11	1,000E -10	8,694E -11
Max	1,701E -10	1,047E -10	1,095E -10	1,538E -10	1,126E -10	1,158E -10	1,294E -10
Mean	1,545E -10	8,926E -11	8,894E -11	1,227E -10	8,613E -11	1,095E -10	1,030E -10
Sigma	1,190E -11	1,785E -11	1,205E -11	2,154E -11	1,816E -11	6,461E -12	1,726E -11

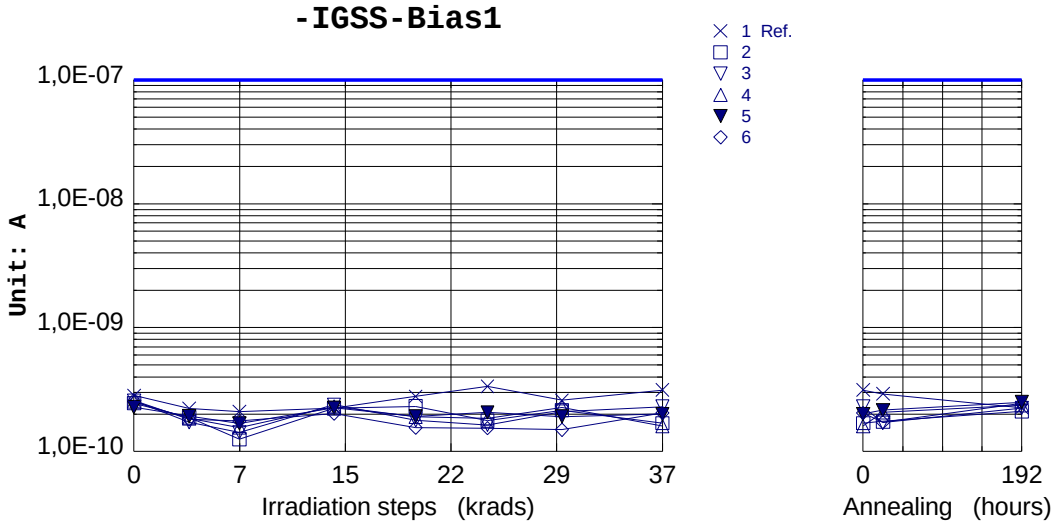
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	1,867E -10	1,196E -10	1,347E -10
7	9,550E -11	8,740E -11	1,691E -10
8	5,340E -10	1,014E -10	1,483E -10
9	1,045E -10	9,644E -11	1,303E -10
10	8,852E -11	9,958E -11	1,420E -10
11	9,434E -11	9,954E -11	1,164E -10
Statistics			
Min	8,852E -11	8,740E -11	1,164E -10
Max	5,340E -10	1,014E -10	1,691E -10
Mean	1,834E -10	9,686E -11	1,412E -10
Sigma	1,961E -10	5,579E -12	1,977E -11



Parameter: Negative Gate source leakage current: -IGSS-Bias1 VGS=-20V, VDS=0V
Unit= A
Spec limit max: 100E-9
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,825E -10	2,224E -10	2,100E -10	2,244E -10	2,784E -10	3,350E -10	2,586E -10
2	2,449E -10	1,882E -10	1,256E -10	2,225E -10	2,312E -10	1,774E -10	2,146E -10
3	2,566E -10	1,722E -10	1,426E -10	2,380E -10	1,785E -10	1,637E -10	2,100E -10
4	2,519E -10	1,845E -10	1,556E -10	2,304E -10	1,899E -10	1,850E -10	2,274E -10
5	2,275E -10	1,927E -10	1,683E -10	2,249E -10	1,920E -10	2,066E -10	1,914E -10
6	2,581E -10	1,815E -10	1,762E -10	2,019E -10	1,553E -10	1,540E -10	1,494E -10
Statistics							
Min	2,275E -10	1,722E -10	1,256E -10	2,019E -10	1,553E -10	1,540E -10	1,494E -10
Max	2,581E -10	1,927E -10	1,762E -10	2,380E -10	2,312E -10	2,066E -10	2,274E -10
Mean	2,478E -10	1,838E -10	1,537E -10	2,236E -10	1,894E -10	1,773E -10	1,986E -10
Sigma	1,245E -11	7,733E -12	2,024E -11	1,349E -11	2,755E -11	2,027E -11	3,037E -11

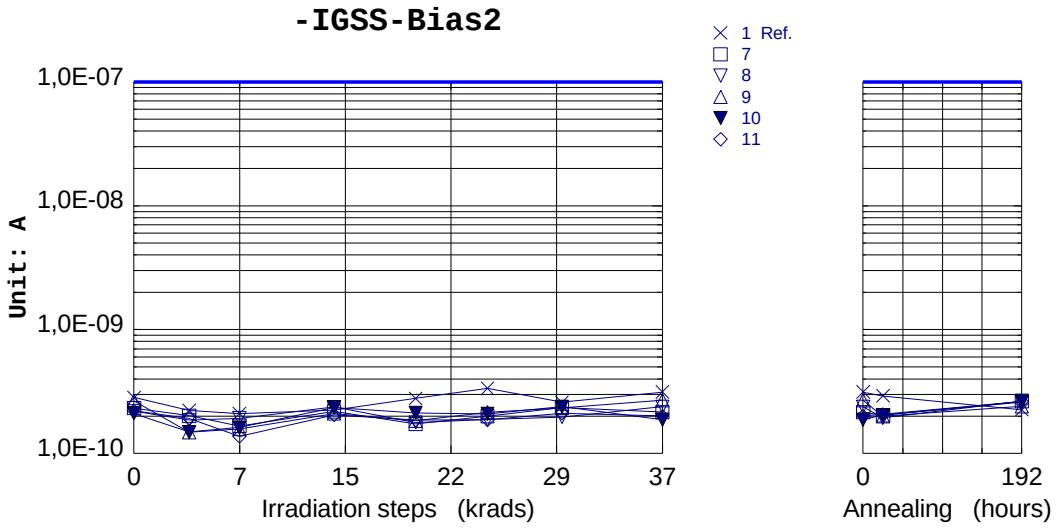
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	3,132E -10	2,918E -10	2,258E -10
2	1,690E -10	1,744E -10	2,105E -10
3	2,299E -10	1,706E -10	2,241E -10
4	1,602E -10	2,066E -10	2,358E -10
5	2,005E -10	2,152E -10	2,498E -10
6	2,041E -10	1,723E -10	2,450E -10
Statistics			
Min	1,602E -10	1,706E -10	2,105E -10
Max	2,299E -10	2,152E -10	2,498E -10
Mean	1,928E -10	1,878E -10	2,331E -10
Sigma	2,824E -11	2,132E -11	1,597E -11



Parameter: Negative Gate source leakage current: -IGSS-Bias2 VGS=-20V, VDS=0V
Unit= A
Spec limit max: 100E-9
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,825E -10	2,224E -10	2,100E -10	2,244E -10	2,784E -10	3,350E -10	2,586E -10
7	2,320E -10	2,016E -10	1,666E -10	2,182E -10	1,731E -10	2,001E -10	2,338E -10
8	2,196E -10	1,855E -10	1,926E -10	2,366E -10	1,776E -10	1,876E -10	1,968E -10
9	2,659E -10	1,479E -10	1,574E -10	2,102E -10	1,834E -10	2,144E -10	2,334E -10
10	2,104E -10	1,485E -10	1,615E -10	2,345E -10	2,121E -10	2,090E -10	2,384E -10
11	2,203E -10	1,922E -10	1,369E -10	2,047E -10	1,859E -10	1,864E -10	2,116E -10
Statistics							
Min	2,104E -10	1,479E -10	1,369E -10	2,047E -10	1,731E -10	1,864E -10	1,968E -10
Max	2,659E -10	2,016E -10	1,926E -10	2,366E -10	2,121E -10	2,144E -10	2,384E -10
Mean	2,297E -10	1,752E -10	1,630E -10	2,208E -10	1,864E -10	1,995E -10	2,228E -10
Sigma	2,166E -11	2,525E -11	2,001E -11	1,429E -11	1,520E -11	1,249E -11	1,788E -11

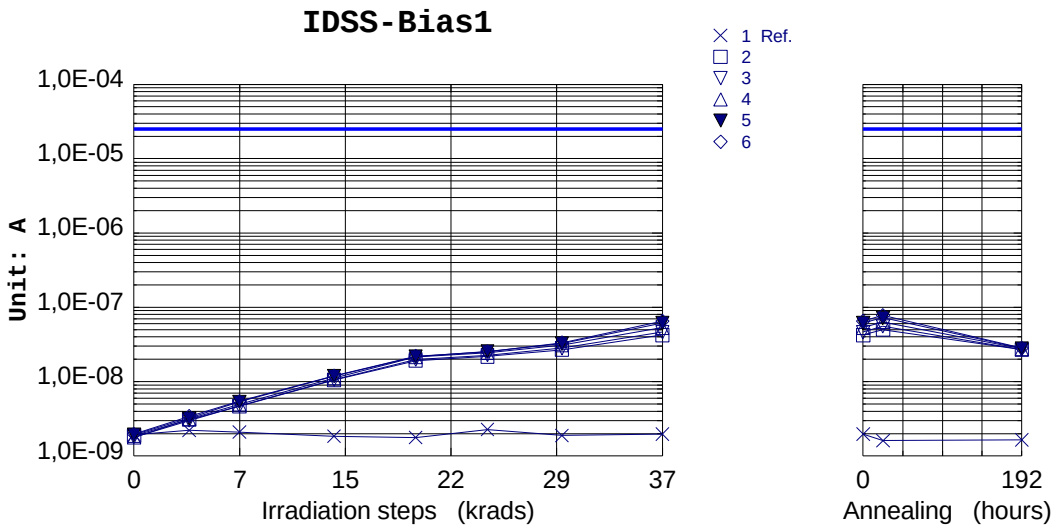
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	3,132E -10	2,918E -10	2,258E -10
7	2,153E -10	2,030E -10	2,632E -10
8	2,386E -10	1,939E -10	2,654E -10
9	2,688E -10	1,993E -10	2,394E -10
10	1,871E -10	2,036E -10	2,597E -10
11	2,006E -10	2,063E -10	2,632E -10
Statistics			
Min	1,871E -10	1,939E -10	2,394E -10
Max	2,688E -10	2,063E -10	2,654E -10
Mean	2,221E -10	2,012E -10	2,582E -10
Sigma	3,236E -11	4,798E -12	1,069E -11



Parameter: Drain current: IDSS-Bias1 VGS=0V, VDS=200V
Unit= A
Spec limit max: 250E-6
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	1,927E -09	2,204E -09	2,093E -09	1,841E -09	1,770E -09	2,268E -09	1,891E -09
2	1,867E -09	3,093E -09	4,649E -09	1,055E -08	1,916E -08	2,173E -08	2,670E -08
3	1,787E -09	3,004E -09	4,694E -09	1,062E -08	1,983E -08	2,258E -08	2,817E -08
4	1,767E -09	3,128E -09	4,923E -09	1,110E -08	2,140E -08	2,432E -08	3,109E -08
5	1,931E -09	3,226E -09	5,352E -09	1,184E -08	2,169E -08	2,556E -08	3,261E -08
6	1,978E -09	3,418E -09	5,469E -09	1,199E -08	2,209E -08	2,538E -08	3,347E -08
Statistics							
Min	1,767E -09	3,004E -09	4,649E -09	1,055E -08	1,916E -08	2,173E -08	2,670E -08
Max	1,978E -09	3,418E -09	5,469E -09	1,199E -08	2,209E -08	2,556E -08	3,347E -08
Mean	1,866E -09	3,174E -09	5,017E -09	1,122E -08	2,083E -08	2,391E -08	3,041E -08
Sigma	9,053E -11	1,578E -10	3,759E -10	6,710E -10	1,269E -09	1,702E -09	2,892E -09

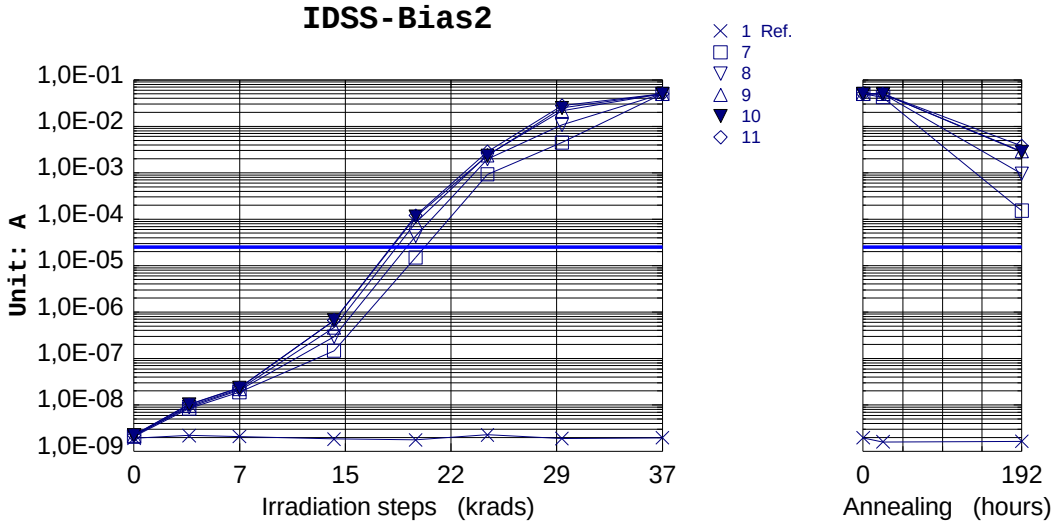
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	1,963E -09	1,609E -09	1,651E -09
2	4,226E -08	5,011E -08	2,685E -08
3	4,628E -08	5,539E -08	2,697E -08
4	5,318E -08	6,375E -08	2,765E -08
5	6,149E -08	7,221E -08	2,799E -08
6	6,514E -08	7,831E -08	2,841E -08
Statistics			
Min	4,226E -08	5,011E -08	2,685E -08
Max	6,514E -08	7,831E -08	2,841E -08
Mean	5,367E -08	6,395E -08	2,757E -08
Sigma	9,717E -09	1,161E -08	6,653E -10



Parameter: Drain current: IDSS-Bias2 VGS=0V, VDS=200V
Unit= A
Spec limit max: 250E-6
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	1,927E -09	2,204E -09	2,093E -09	1,841E -09	1,770E -09	2,268E -09	1,891E -09
7	2,075E -09	8,363E -09	1,900E -08	1,475E -07	1,498E -05	9,236E -04	4,498E -03
8	2,169E -09	8,956E -09	2,097E -08	2,966E -07	4,336E -05	1,963E -03	1,073E -02
9	2,157E -09	9,516E -09	2,202E -08	4,655E -07	8,380E -05	2,400E -03	2,156E -02
10	2,234E -09	1,032E -08	2,360E -08	6,591E -07	1,137E -04	2,334E -03	2,500E -02
11	2,215E -09	1,018E -08	2,311E -08	6,660E -07	1,202E -04	2,821E -03	2,814E -02
Statistics							
Min	2,075E -09	8,363E -09	1,900E -08	1,475E -07	1,498E -05	9,236E -04	4,498E -03
Max	2,234E -09	1,032E -08	2,360E -08	6,660E -07	1,202E -04	2,821E -03	2,814E -02
Mean	2,170E -09	9,467E -09	2,174E -08	4,469E -07	7,521E -05	2,088E -03	1,798E -02
Sigma	6,190E -11	8,244E -10	1,840E -09	2,267E -07	4,533E -05	7,187E -04	9,994E -03

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	1,963E -09	1,609E -09	1,651E -09
7	4,998E -02	4,267E -02	1,530E -04
8	4,999E -02	5,000E -02	9,547E -04
9	5,000E -02	4,999E -02	2,901E -03
10	4,999E -02	5,000E -02	2,792E -03
11	4,999E -02	5,000E -02	3,786E -03
Statistics			
Min	4,998E -02	4,267E -02	1,530E -04
Max	5,000E -02	5,000E -02	3,786E -03
Mean	4,999E -02	4,853E -02	2,118E -03
Sigma	9,100E -06	3,275E -03	1,505E -03



Parameter: Static drain to source on-state resistance: RDSON-Bias1 **VGS=10V, ID=16A**

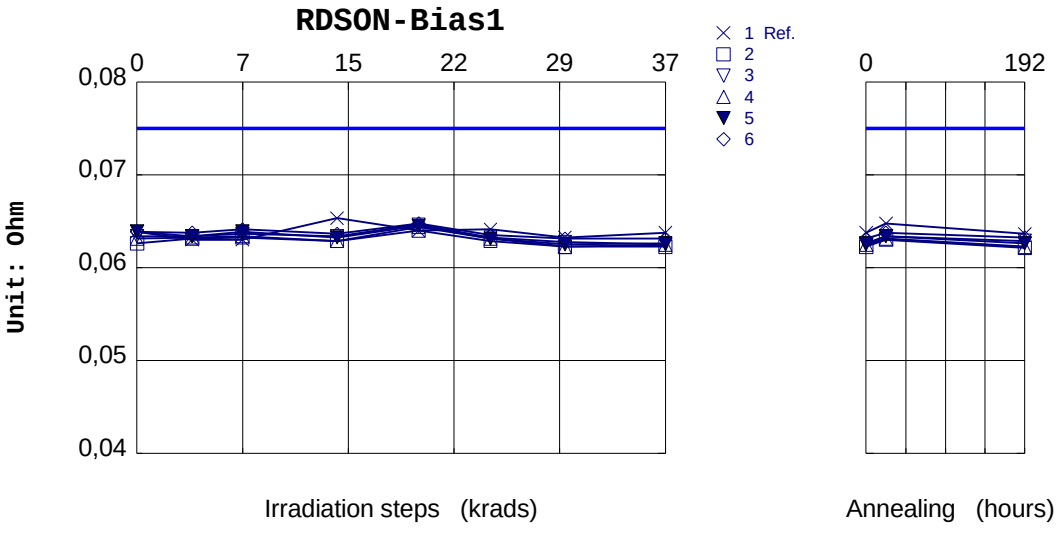
Unit= Ohm

Spec limit max: 0.075

Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	6,387E -02	6,300E -02	6,300E -02	6,533E -02	6,400E -02	6,413E -02	6,325E -02
2	6,262E -02	6,312E -02	6,325E -02	6,288E -02	6,400E -02	6,288E -02	6,225E -02
3	6,338E -02	6,338E -02	6,363E -02	6,338E -02	6,463E -02	6,325E -02	6,275E -02
4	6,312E -02	6,325E -02	6,338E -02	6,288E -02	6,437E -02	6,312E -02	6,225E -02
5	6,387E -02	6,338E -02	6,387E -02	6,325E -02	6,450E -02	6,312E -02	6,250E -02
6	6,387E -02	6,375E -02	6,413E -02	6,363E -02	6,475E -02	6,350E -02	6,312E -02
Statistics							
Min	6,262E -02	6,312E -02	6,325E -02	6,288E -02	6,400E -02	6,288E -02	6,225E -02
Max	6,387E -02	6,375E -02	6,413E -02	6,363E -02	6,475E -02	6,350E -02	6,312E -02
Mean	6,337E -02	6,338E -02	6,365E -02	6,320E -02	6,445E -02	6,318E -02	6,257E -02
Sigma	5,303E -04	2,339E -04	3,579E -04	3,260E -04	2,878E -04	2,271E -04	3,708E -04

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	6,375E -02	6,475E -02	6,363E -02
2	6,225E -02	6,300E -02	6,213E -02
3	6,250E -02	6,338E -02	6,288E -02
4	6,245E -02	6,312E -02	6,225E -02
5	6,262E -02	6,338E -02	6,262E -02
6	6,312E -02	6,375E -02	6,325E -02
Statistics			
Min	6,225E -02	6,300E -02	6,213E -02
Max	6,312E -02	6,375E -02	6,325E -02
Mean	6,259E -02	6,333E -02	6,262E -02
Sigma	3,287E -04	2,878E -04	4,593E -04



Parameter: Static drain to source on-state resistance: RDSON-Bias2 **VGS=10V, ID=16A**

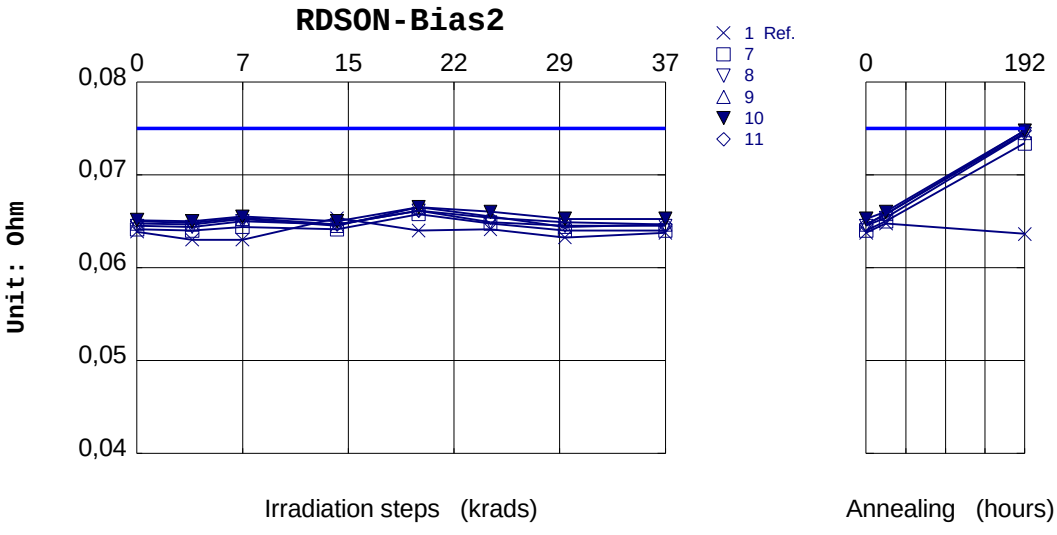
Unit= Ohm

Spec limit max: 0.075

Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	6,387E -02	6,300E -02	6,300E -02	6,533E -02	6,400E -02	6,413E -02	6,325E -02
7	6,413E -02	6,400E -02	6,437E -02	6,413E -02	6,575E -02	6,475E -02	6,400E -02
8	6,450E -02	6,437E -02	6,500E -02	6,463E -02	6,612E -02	6,487E -02	6,450E -02
9	6,475E -02	6,463E -02	6,525E -02	6,450E -02	6,650E -02	6,550E -02	6,437E -02
10	6,513E -02	6,500E -02	6,550E -02	6,500E -02	6,650E -02	6,600E -02	6,525E -02
11	6,500E -02	6,483E -02	6,538E -02	6,463E -02	6,612E -02	6,538E -02	6,487E -02
Statistics							
Min	6,413E -02	6,400E -02	6,437E -02	6,413E -02	6,575E -02	6,475E -02	6,400E -02
Max	6,513E -02	6,500E -02	6,550E -02	6,500E -02	6,650E -02	6,600E -02	6,525E -02
Mean	6,470E -02	6,457E -02	6,510E -02	6,458E -02	6,620E -02	6,530E -02	6,460E -02
Sigma	4,012E -04	3,928E -04	4,455E -04	3,137E -04	3,137E -04	5,047E -04	4,793E -04

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	6,375E -02	6,475E -02	6,363E -02
7	6,400E -02	6,500E -02	7,338E -02
8	6,450E -02	6,538E -02	7,438E -02
9	6,463E -02	6,575E -02	7,450E -02
10	6,525E -02	6,600E -02	7,475E -02
11	6,463E -02	6,575E -02	7,475E -02
Statistics			
Min	6,400E -02	6,500E -02	7,338E -02
Max	6,525E -02	6,600E -02	7,475E -02
Mean	6,460E -02	6,558E -02	7,435E -02
Sigma	4,455E -04	3,913E -04	5,687E -04



8 Conclusion

A total dose radiation verification test has been performed on MTW32N20E N-Channel Power Mosfet from Motorola Semiconductors up to 36.85 Krad(Si) accumulated dose.

Most samples exhibited high drain to source leakage currents and consequently very low breakdown voltages, at 24.65 Krad(Si) and 19.65 Krad(Si) dose respectively, under Bias 2 conditions.
These drain leakage currents are very high (up to the compliance value of 50mA).

Threshold voltage is out of specification at 19.65 Krad(Si) under Bias 1 conditions, a small recovery is observed after 168H annealing step but not sufficient to meet specification limit.
Threshold voltage is out of specification at 7.35 Krad(Si) under Bias 2 conditions. In addition this parameter becomes negative after 24.65 Krad(Si) exposure.

This device has shown a high susceptibility to radiation induced effects.

ANNEX 1 : MTW32N20E DATA SHEET

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

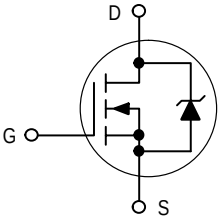
MTW32N20E

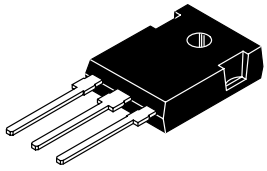
Motorola Preferred Device

TMOS POWER FET
32 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.075 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole





CASE 340K–01, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \leq 10$ μs)	I_D I_D I_{DM}	32 19 128	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.44	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vpk, I_L = 32 Apk, L = 1.58 mH, R_G = 25 Ω)	E_{AS}	810	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.7 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μAdc)		$V_{(BR)DSS}$	200	—	—	Vdc
Temperature Coefficient (Positive)			—	247	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0)		I_{DSS}	—	—	250	μAdc
(V_{DS} = 200 Vdc, V_{GS} = 0, T_J = 125°C)			—	—	1000	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	—	4.0	Vdc
Temperature Coefficient (Negative)			—	8.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$R_{DS(on)}$	—	0.064	0.075	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 32 Adc)		$V_{DS(on)}$	—	—	3.0	Vdc
(I_D = 16 Adc, T_J = 125°C)			—	—	2.7	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 16 Adc)		g_{FS}	12	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3600	5000	pF
Output Capacitance		C_{oss}	—	130	250	
Reverse Transfer Capacitance		C_{rss}	—	690	1000	
SWITCHING CHARACTERISTICS*†						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc, R_G = 6.2 Ω)	$t_{d(on)}$	—	25	50	ns
Rise Time		t_r	—	120	240	
Turn–Off Delay Time		$t_{d(off)}$	—	75	150	
Fall Time		t_f	—	91	182	
Gate Charge	(V_{DS} = 160 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc)	Q_T	—	85	120	nC
		Q_1	—	12	—	
		Q_2	—	40	—	
		Q_3	—	30	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*						
Forward On–Voltage	(I_S = 32 Adc, V_{GS} = 0)	V_{SD}	—	1.1	2.0	Vdc
	(I_S = 16 Adc, V_{GS} = 0, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 32 Adc, V_{GS} = 0, dI_S/dt = 100 A/μs)	t_{rr}	—	280	—	ns
		t_a	—	195	—	
		t_b	—	85	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.94	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

† Switching characteristics are independent of operating junction temperature.

YPICAL ELECTRICAL CHARACTERISTICS

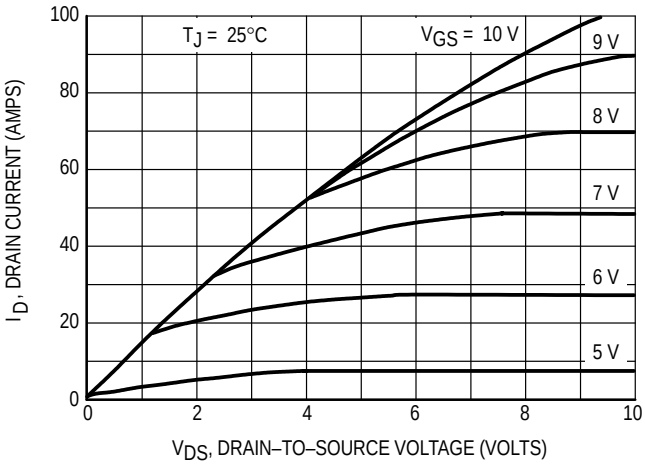


Figure 1. On–Region Characteristics

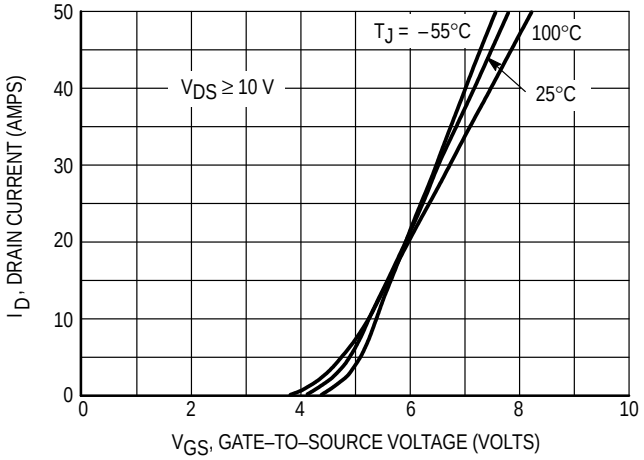


Figure 2. Transfer Characteristics

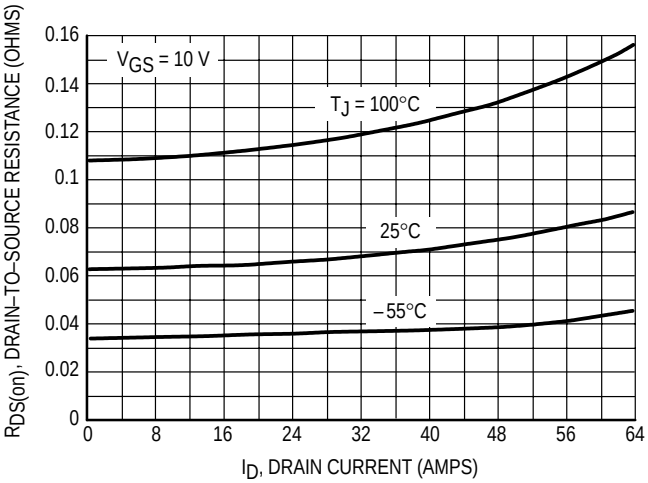


Figure 3. On–Resistance versus Drain Current and Temperature

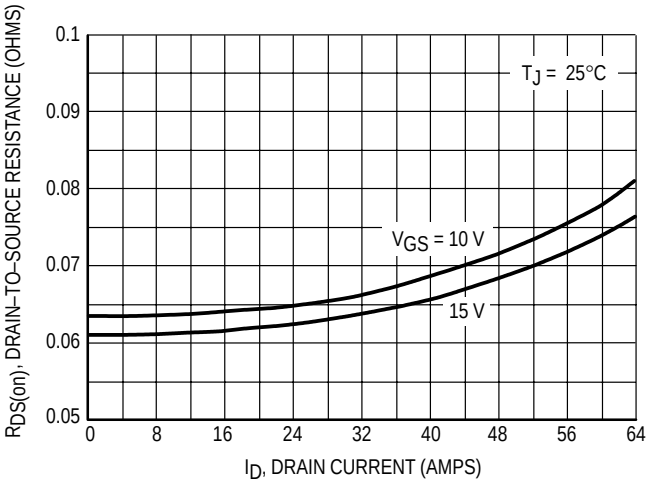


Figure 4. On–Resistance versus Drain Current and Gate Voltage

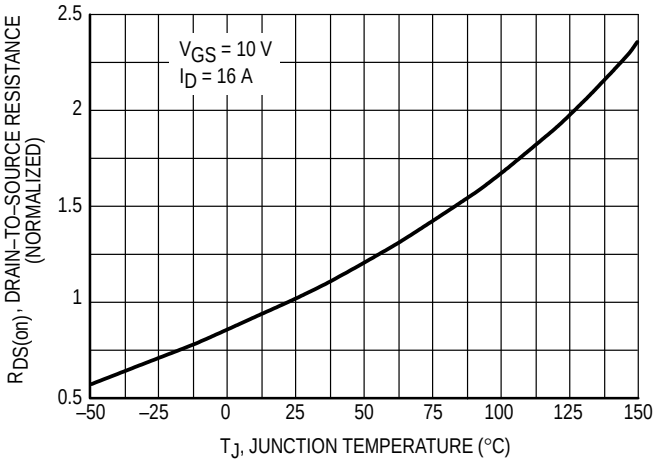


Figure 5. On–Resistance Variation with Temperature

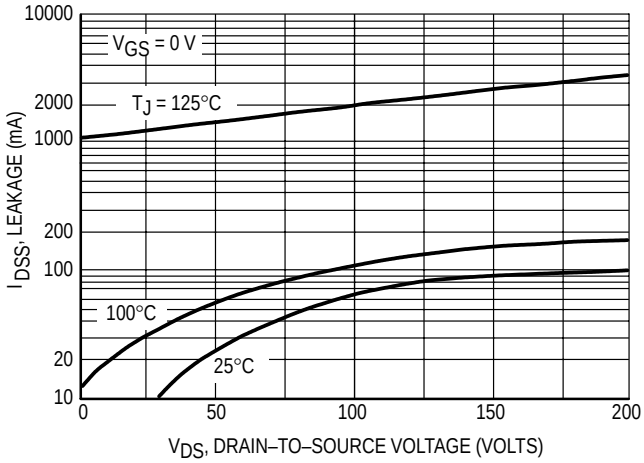


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by L di/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

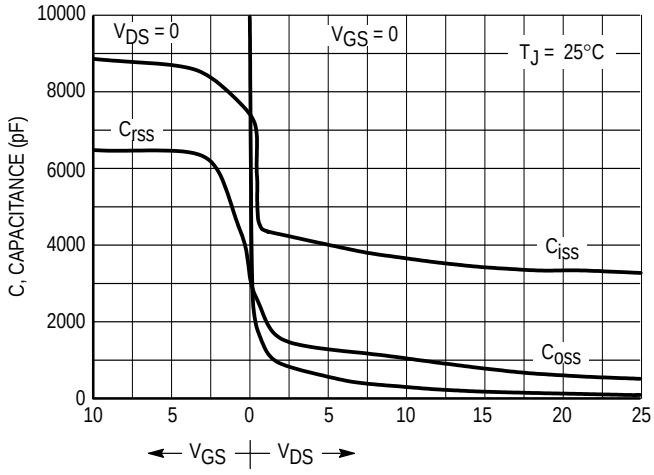


Figure 7. Capacitance Variation

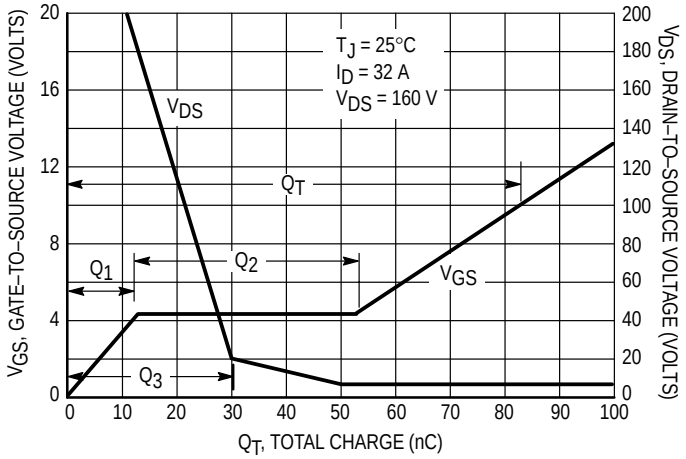


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

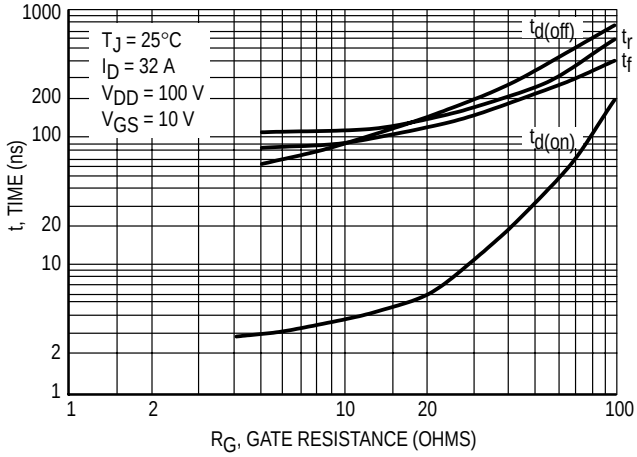


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

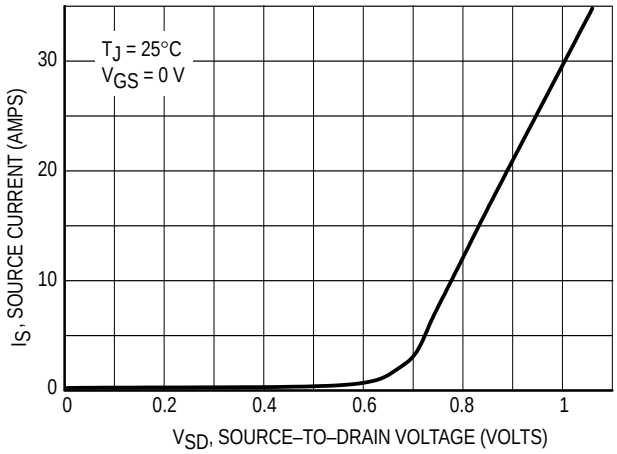


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} – T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

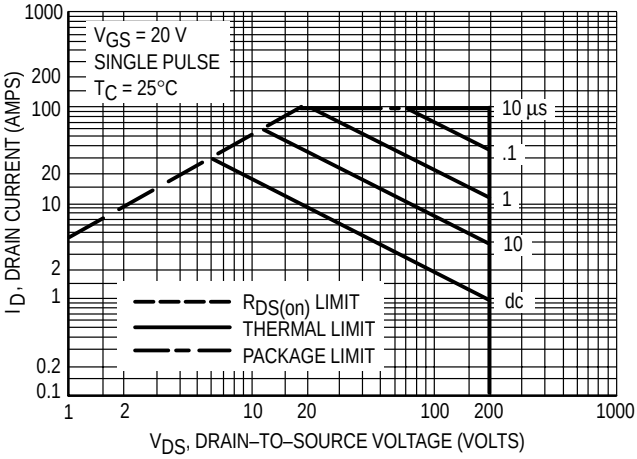


Figure 11. Maximum Rated Forward Biased Safe Operating Area

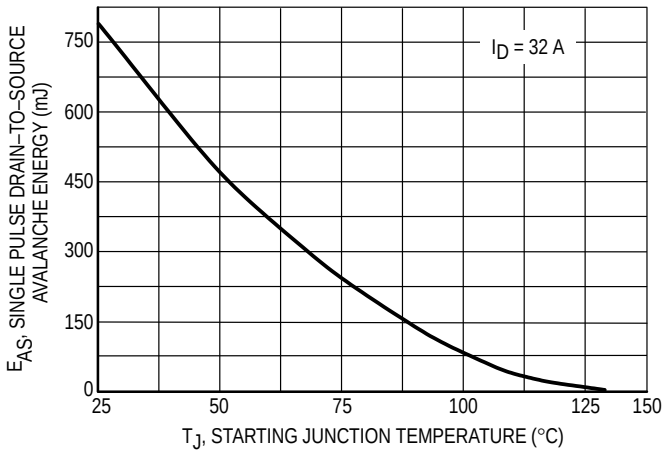


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

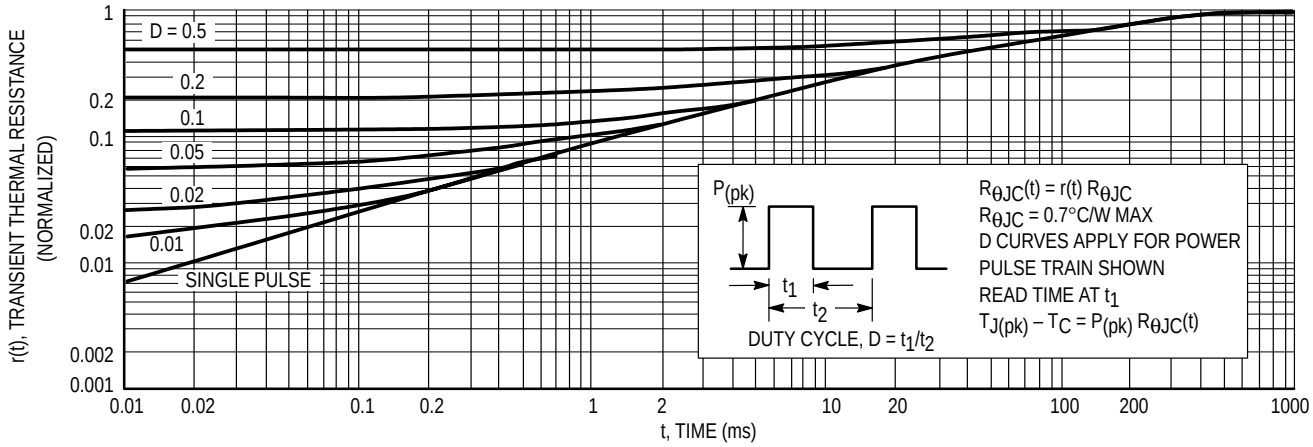
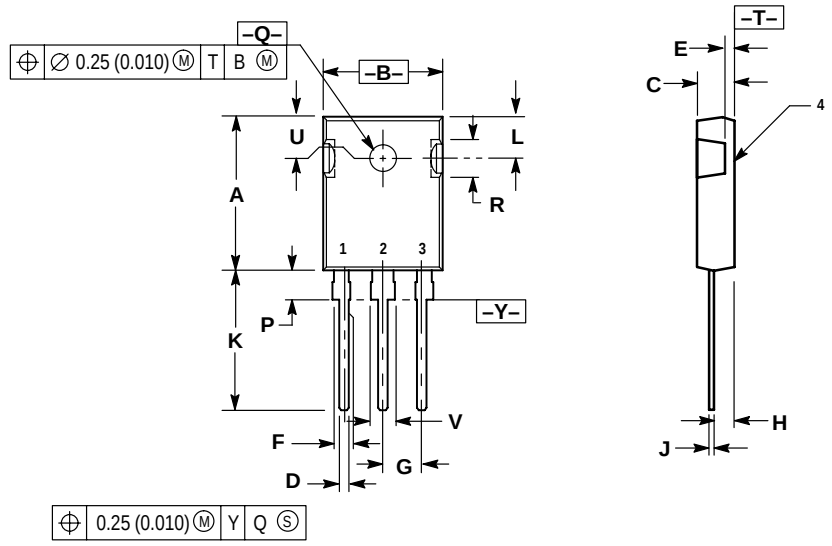


Figure 13. Thermal Response

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 340K–01
ISSUE O

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JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298