ST 65nm a Hardened ASIC Technology for Space Applications

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Agenda

- **Motivation for DSM program**
- ST C65SPACE radiation hardened ASIC technology
- ST C65SPACE qualification status / roadmap
- Conclusion

On board processors trend

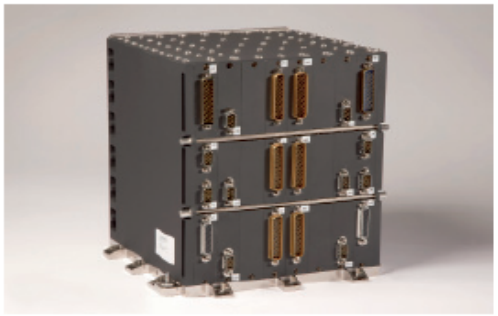
Reduction of power consumption, mass and dimensions achievable with silicon evolution and introduction of the SoC technology are significant:

GOCE (2009) CDMU
TAS-I *ERC32*

Power consumption = < **90 W** average (excluding external loads)

Mass = 21kg

Dimensions = 470(L)x272(H)x332(D) mm

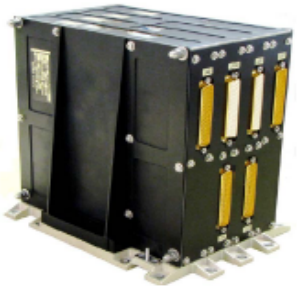


GAIA (2013) CDMU
RUAG-S *AT697F*

Power consumption = < **40W** average (excluding external loads)

Mass = 16kg

Dimensions = 420(L)x270(H)x(276(D) mm



SEOSAT (2014) OBC
ASTRIUM-E *SCOC3*

Power consumption = **15W** peak (excluding external loads)

Mass = 5.2kg

Dimensions = 250(L)x150(H)x216(D) mm

European microprocessors roadmap

History of ESA Microprocessor Developments

MA 31750 (Dynex Semiconductor)

- MIL-STD-1750A architecture
- GEC-Plessey 1.5 µm

SPARC V7 ERC32 chipset

- 3-chips: IU, FPU, MEC
- Temic 0.8 µm

SPARC V7 ERC32 single chip

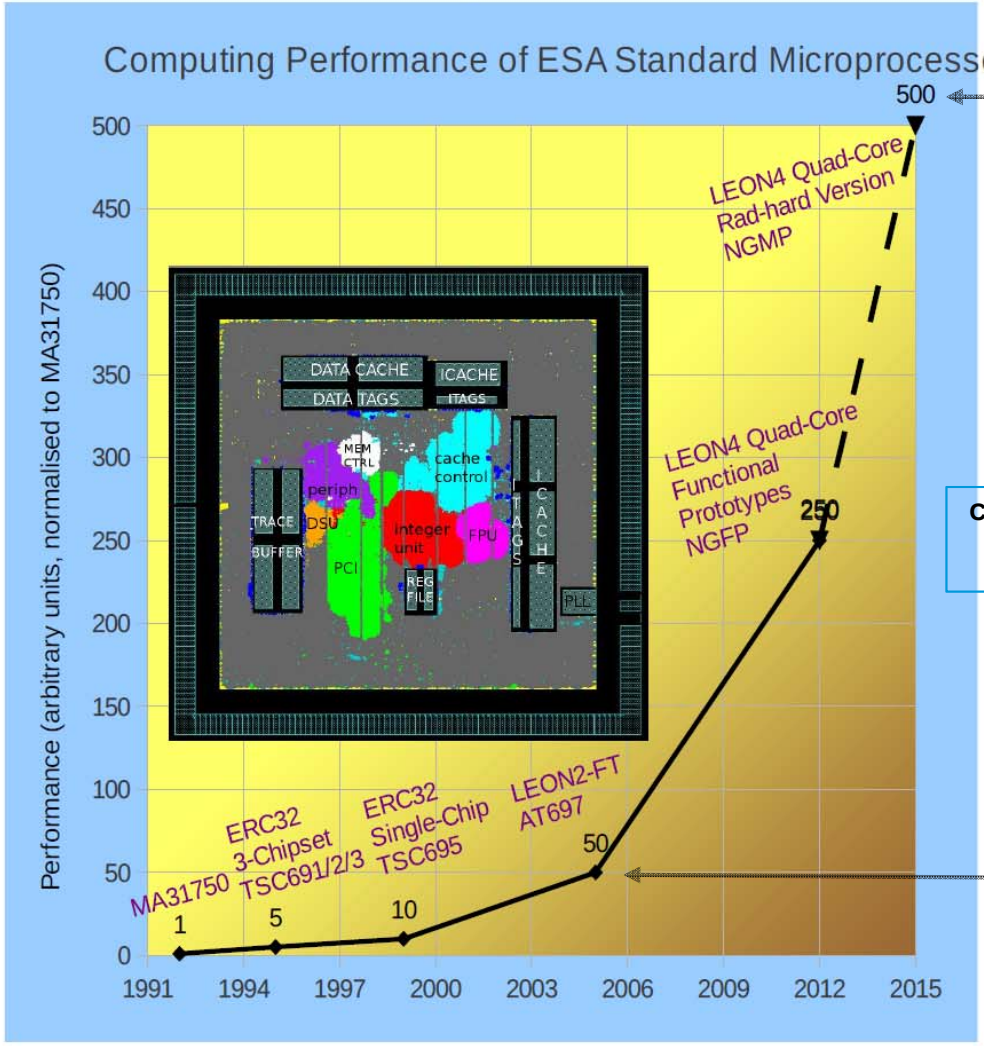
- Temic 0.5 µm

SPARC V8 LEON2/AT697

- Atmel 0.18 µm

SPARC V8 LEON4/NGMP

- Goal: 10x AT697 performance



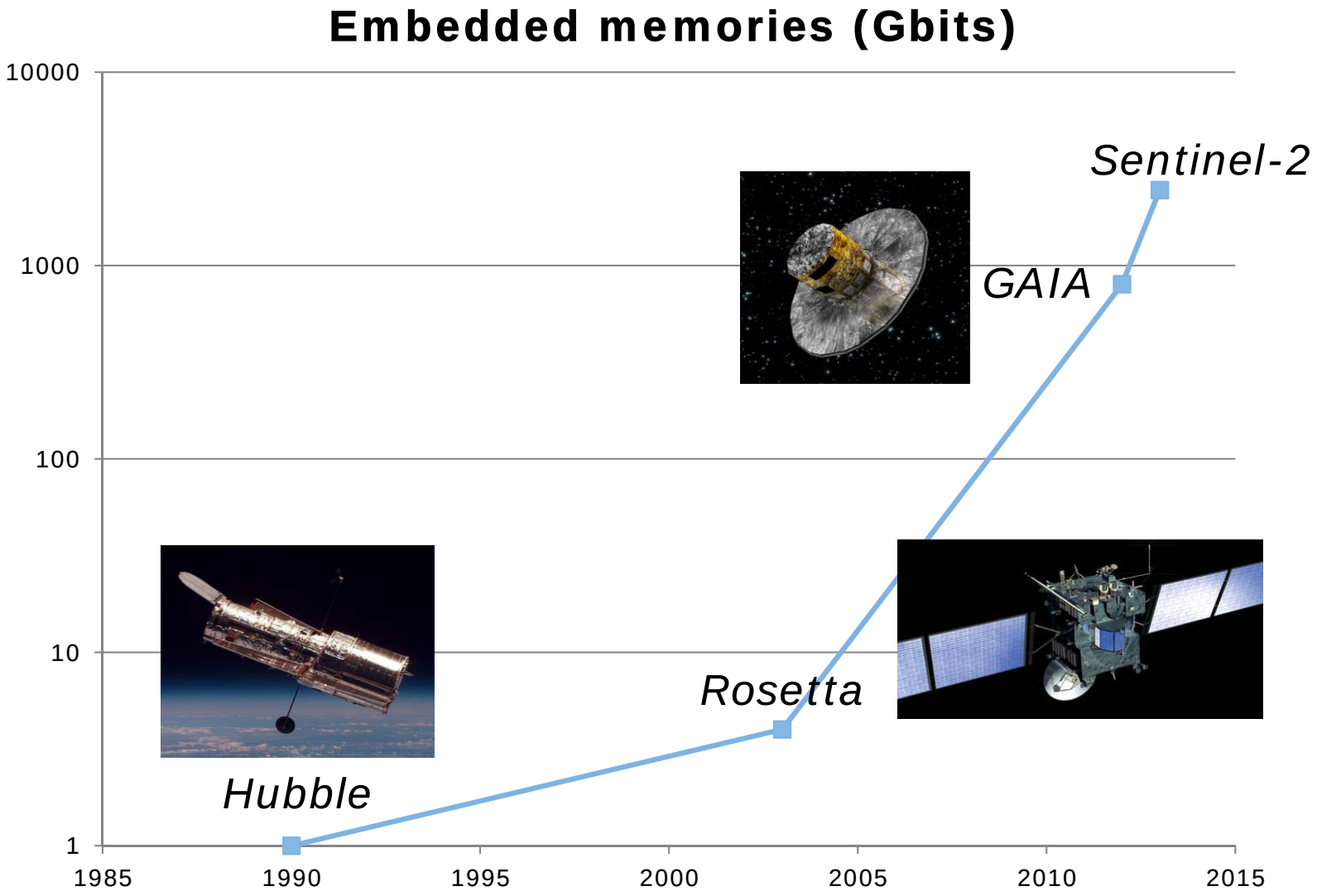
ST C65SPACE
65nm ASIC technology

Computing performances improvement
x 10 times

ATMEL ATC18RHA
180nm ASIC technology

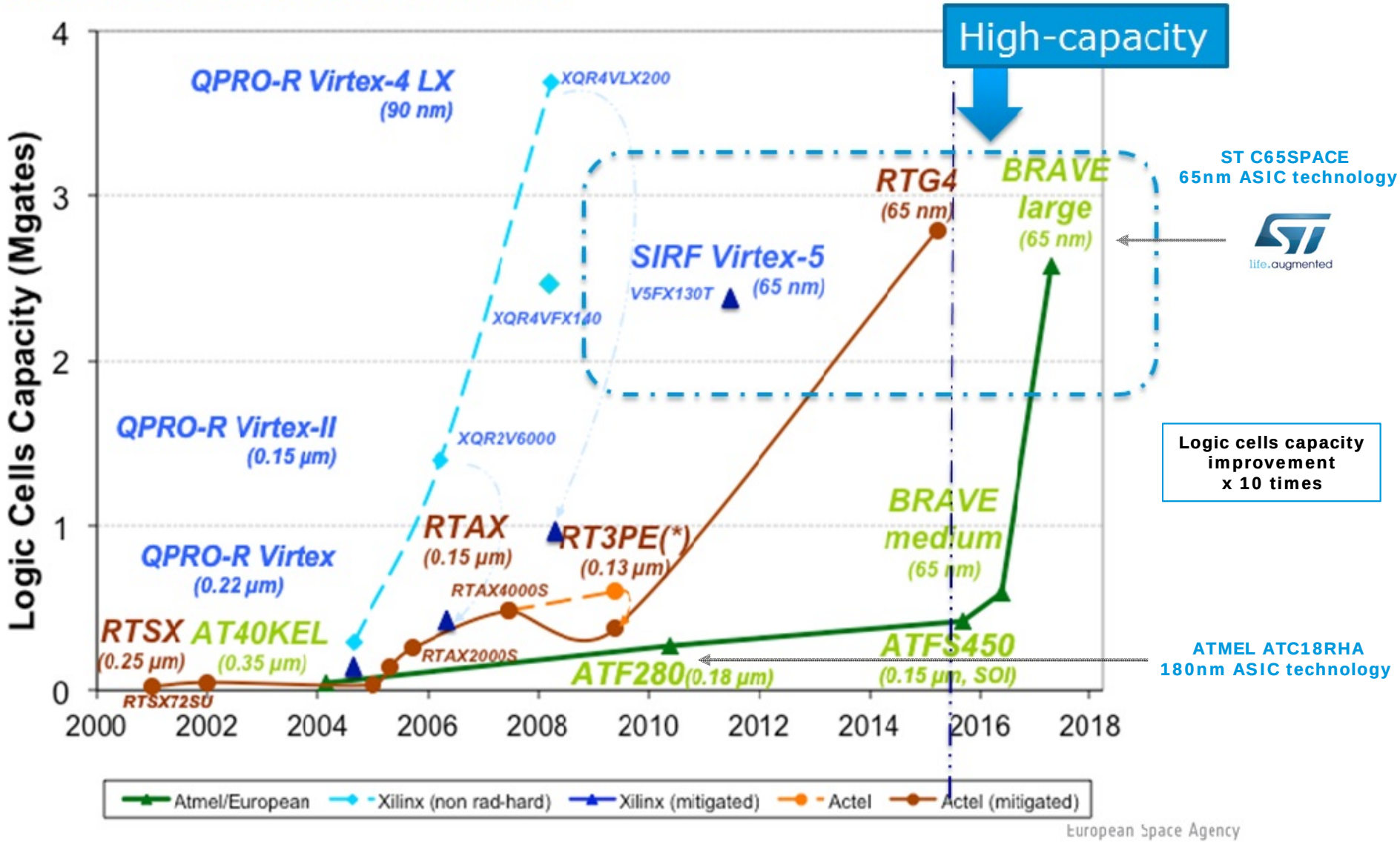
Source: Roland Weigand ESA Microelectronics section

On board memories trend



European FPGA roadmap

Note: RTG4, ATFS450 and BRAVE dates are for Engineering Samples



Source: David Merodio ESA Microelectronics section

Digital telecom processors roadmap

Bandwidth
input / output port
in MHz

500
250
120
30
20
10

Bandwidth per port improvement X 4 times

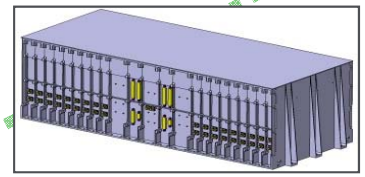
350 nm

DTP 1G
8 x 8 x 40 MHz

650 nm

INMARSAT4
120 x 27MHz

180 nm



DTP 2G
20 x 20 x 125MHz

ATMEL ATC18RHA
180nm ASIC technology

180 nm

Small GEO
4 x 4 x 36 MHz

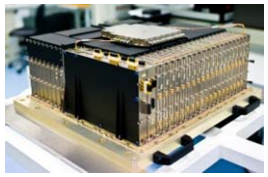
180 nm

ALPHASAT
14 x 14 x 250 MHz

90 nm

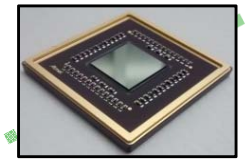
SMP
4 x 4 x 500 MHz
scalable 128 x 128

180 nm



Spaceflex5
20 x 20 x 250 MHz

65 nm



Spaceflex
48 x 48 x 500MHz
Scalable
96 x 96
144 x 144

28 nm
14 nm

ST C65SPACE
65nm ASIC
technology

Courtesy: Airbus Defense Space (UK)
Courtesy: Thales Alenia Space (France)

2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017+

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Hardened ASIC technology top level requirements

- ✓ Reach Space required functionalities
  - ✓ 30 Mgates capacity
  - ✓ Hardened standard-cells and memories
  - ✓ Support for cold-spare IOs
  - ✓ Hardened High speed link (HSSL) up to 6.25Gbit/s
  - ✓ Hardened PLL
- ✓ Reliability
  - ✓ Insure long term reliability during the 20 years operating time of the satellite
  - ✓ Std-cell, RAMs, IOs, high speed link, very low FIT (< 100ppm) over 20 years for temperature range from -55 … +125 degrees (junction temperature / Tj)
- ✓ Radiation
  - ✓ SEL free up to 60 MeV/mg/cm2 (in worst case conditions VDD / temperature)
  - ✓ TID = 300krad (in worst case conditions VDD / temperature)
  - ✓ Insure that all the offer (std-cells, IOs, memories, PLL, HSSL) is radiation robust
- ✓ Compliance with space qualification (ESCC)
  - ✓ Wafer level
  - ✓ Product level
- ✓ Process
  - ✓ Assure stable performances along the C65SPACE manufacturing duration
  - ✓ space process route frozen, specific process step, 10+ years supply guaranteed

Starting point ST65nm commercial process

- 65nm-LP CMOS from ST France : European technology, ITAR free
- 65nm CMOS commercially qualified in 2007
- 65nm CMOS Bulk Process :
  - Dual / Triple Gate Oxides
  - Dual / Triple Threshold Voltages for MOS Transistors
  - 7-9 Full Copper Dual Interconnect Levels
  - Low K

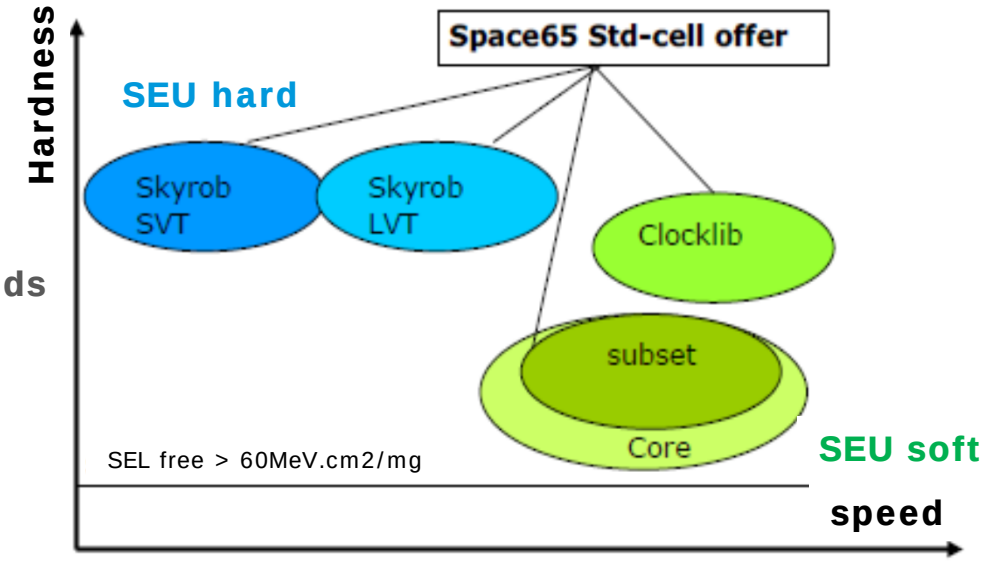
- performances:
  - 750 kgates/mm2
  - 2GHz stdcells
  - 5.7nW/(MHz x gates)
  - 1.25-7.5GBit/s HSSL modules

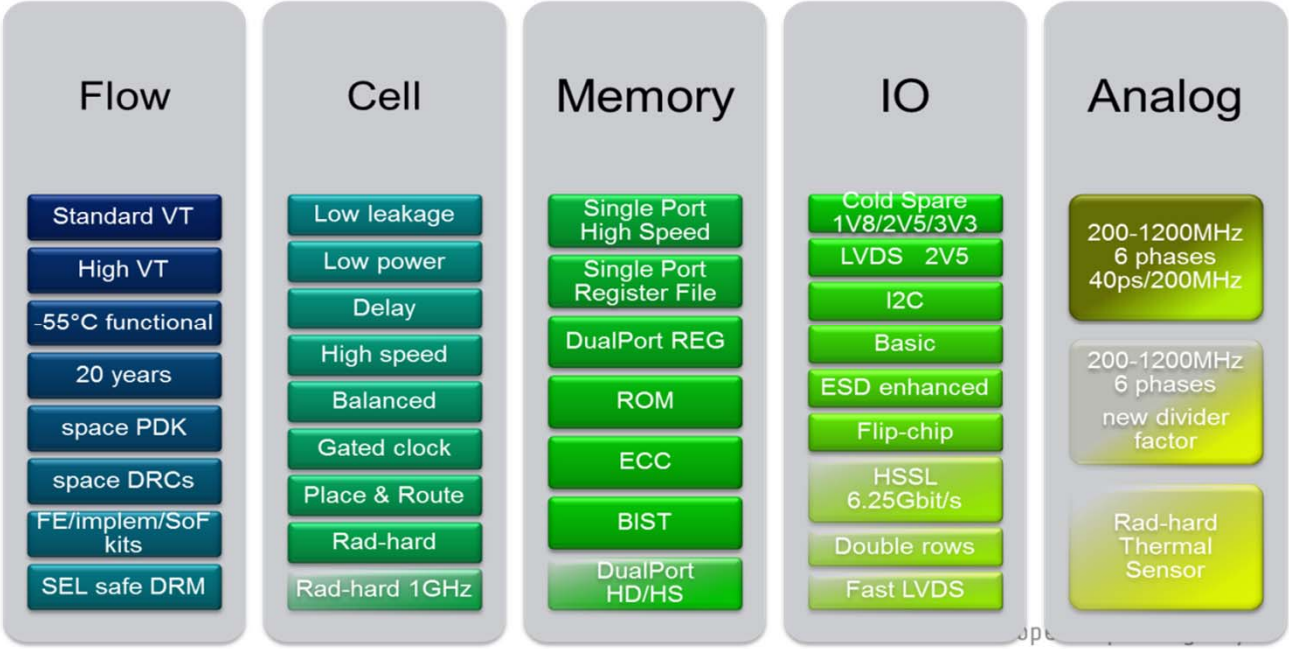
❖ ST Rad Hard offer based on CMOS 65nm-LP commercial process
❖ Reliability and Radiation maximisation performed at design stages

C65SPACE hardened process derived from ST65nm low power commercial process

C65SPACE offer

- **Libraries allowing best design trade off between speed, area, power and radiation hardening**
  - SEL immune by layout techniques
  - SEU performance adjusted according local design needs
- **C65SPACE flow adapted to specific radiation hardening needs**
  - Extended corner cases
  - Extended design rule checks
- **A full rad hard IP offer SEL free > 60MeV**
  - memory compilers SRAM, ROM
    - ECC RTL wrappers, BIST
  - Cold spare IOs
    - Compatible with wire bond / flip chip
    - CMOS 1.8v, 2.5v, 3.3v
    - I2C
    - LVDS 2.6Gbps
  - High Speed Serial Link 6.25Gbps
  - PLL 200MHz … 1.2 GHz
  - Robust flip-flops > 1GHz
  - Robust combinatorial cells
    - Clock gating, NAND2, IV
    - Clock tree buffers
  - Robust thermal sensors





C65SPACE offer

Qualification domain

- No single event latch-up up to LET=60Mev/mg/cm2 at 125C and Vdd at 1.3V
- No significant parametric drifts up to TID = 300 kradSiO2
- SEU: ultra low fail rates by design and technology (SEU rate divided by 500)
- Extended reliability corners over 20 years at VDD max = 1.3V (nominal + 10%)
  - Std-cell, RAMs, IOs → -55 … +125 degrees (Tj)
  - High speed serial link → -55 … + 110 degrees (Tj)

Operational domain

- Mission profile: 20 years at Tj=110 degrees and VDD nom = 1.2V

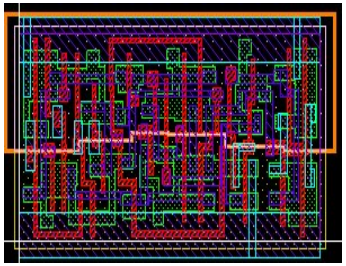
Features summary

- 7 copper metallization with 5 thin and 2 thick

- Corelib (performance = speed + density + power)
  - 1000+ general purpose cells (high density / non SEU hardened)
  - Standard speed grade cells → Standard Voltage Threshold (SVT)
  - High speed grade cells → Low Voltage Threshold (LVT)

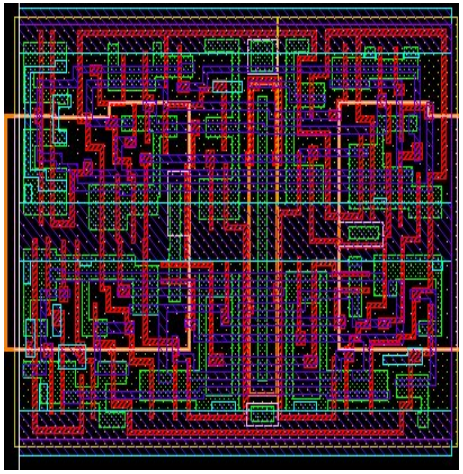
- Skyrob (performance = SEU / SET mitigation)
  - 100+ hardened cells SVT → optimised for leakage current
  - 100+ hardened cells LVT → optimised for speed

- Clocklib (performance = SET mitigation)
  - 100+ hardened cells SVT
  - 100+ hardened cells LVT



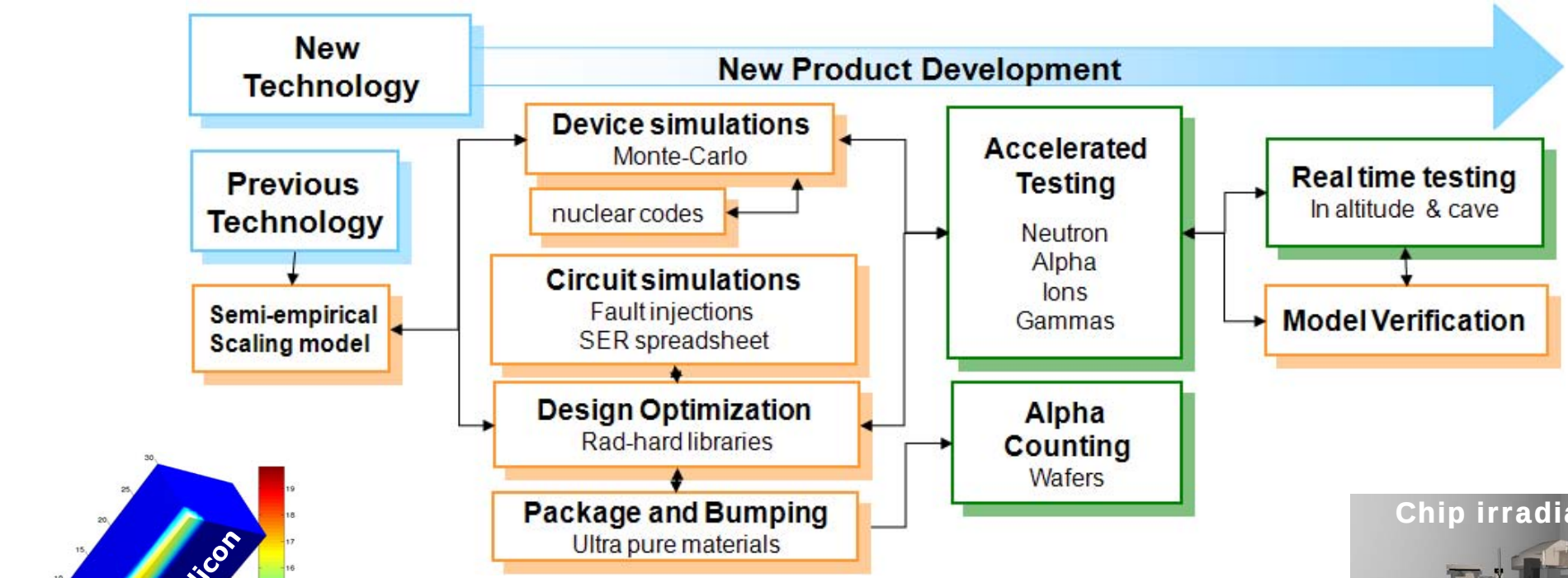
CoreLib Regular Flip-flop

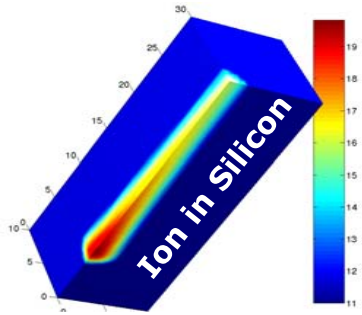
SEU
/100 … /500

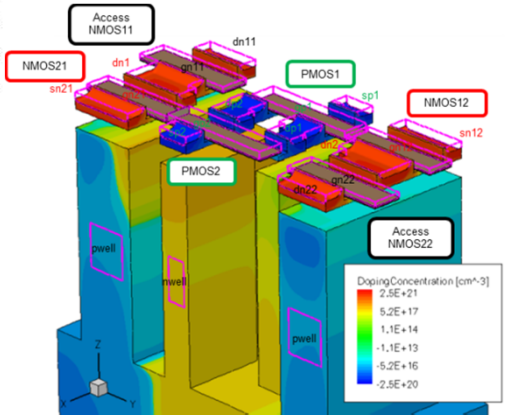


SkyRob Rad-hard Flip-flop

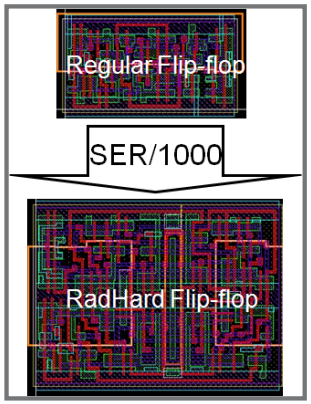
C65SPACE radiation hardening flow



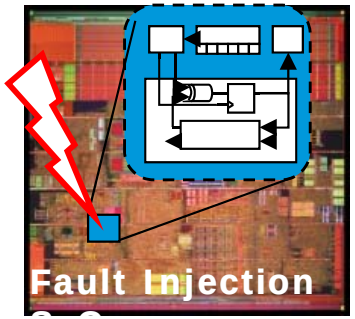


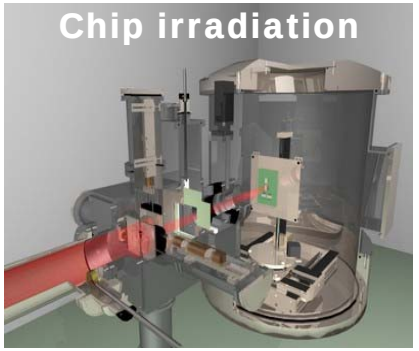


modelling



simulating





characterising

C65SPACE hardened DFF characterisation

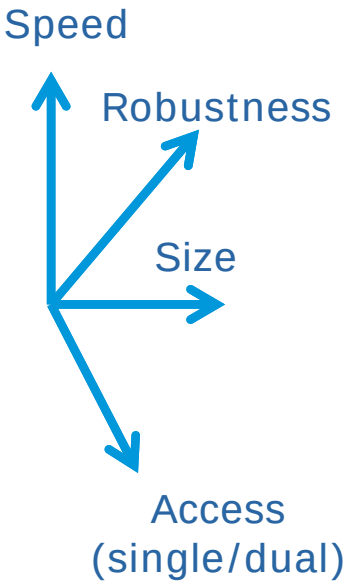
“SEU rate improvement factor with SKYROB ranging from 80 to 500”

Cell type	library	Upset rate in GEO (SEU / bit / day)	Improvement factor compared to standard commercial DFF		description
			best	worst	
Standard DFF from CORELIB with latchup protection (DNW)	CORE65LPSVT (Standard Vt = Slow)	1.6E-7 (best)	x	x	Reference DFF (commercial lib - CORELIB)
Standard DFF from CORELIB with latchup protection (DNW)	CORE65LPLVT (Low Vt = fast)	4.1E-7 (worst)	x	x	Reference DFF (commercial lib - CORELIB)
SKYROB65_LSDGURFD12_DFPQX6	SKYROB65LPSVT (Standard Vt)	0.812E-9	197	**504**	Harden DFF with drive 6. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
SKYROB_LSDGFD12S_SDFPRQTX10	SKYROB65LPSVT (Standard Vt)	1.23E-9	130	333	Harden DFF with drive 10. Scan-out D flip-flop with 1 phase positive edge clock, reset active low, Q and TQ outputs
SKYROB_LSDGFD12S_DFPQX18	SKYROB65LPSVT (Standard Vt)	1.82 E-9	87	225	Harden DFF with drive 18. D-type flip-flop with 1 phase positive edge triggered clock, Q output only

Data computed with tool web based CREME96

- GEO orbit @ solar quiet
- Shielding 100mils Aluminium
- ions up to element Z=92
- Weibull fit from experimental results at RADEF (December 2010)

C65SPACE hardened memories offer



Memory model	Word Count	Mux Range	Voltage Range Supported	Reliability	Radiations
Dual port high speed C65LP_ST_DPHS_SPACE **Large memory block**	64-8K	8	1.1V - 1.35V	**Sustain 20 years, worst case operations**	**Full immune with ECC against GEO harsh radiations**
Dual port high density C65LP_ST_DPHD_SPACE	80-8K	4,8,16	1.1V - 1.35V		
Single port register file C65LP_ST_SPREG_SPACE **Small memory block**	16-2048	2,4,8	1.1V - 1.35V		
Dual port register file C65LP_ST_DPREG_SPACE	16 - 4096	2,4,8	1.1V - 1.35V		
Read only memory C65LP_ST_ROMHS_SPACE	128 - 131072	16,32,64	1.1V - 1.35V		

Comprehensive **Rad Hard** SRAMs offer
single or dual port memory optimised for density or speed

C65SPACE High Speed Serial Link 6.25Gbps

HSSL IP datasheet

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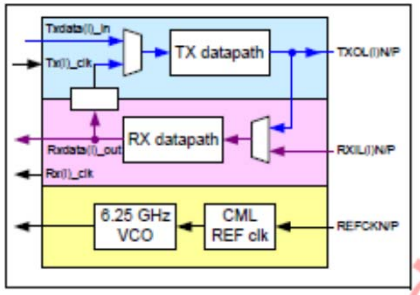
life.augmented

C65SPACE-HSSL

6.25 Gbps multi-rate, multi-lane, SerDes macro IP

Product preview



Features

- ST CMOS065LP low-power 65 nm CMOS technology
- 1.5625, 3.125 and 6.25 Gbps operation
- BER < 10^{-14}
- 20 bit TX and RX parallel data interface width / sub-rate mode
- Global power down and per link TX & RX power downs
- Compact form factor: 3040u x 1600u (tbc)
- Flip chip only layout
- Full immunity to single event latch-up (SEL) failures with a LET up to 60MeVcm2/mg
- No single event functional interrupts (SEFIs), up to 60MeVcm2/mg
- 1.2V power supply

Description

The ST 65 nm HSSL IP is a radiation hardened high-performance SERDES developed in ST CMOS065LP Low Power 65 nanometer CMOS technology and is provided as Flip chip only layout with build-in 2KV ESD protection. It features 8 channels (4Tx + 4 Rx) and is supplied by 1.2 volt.

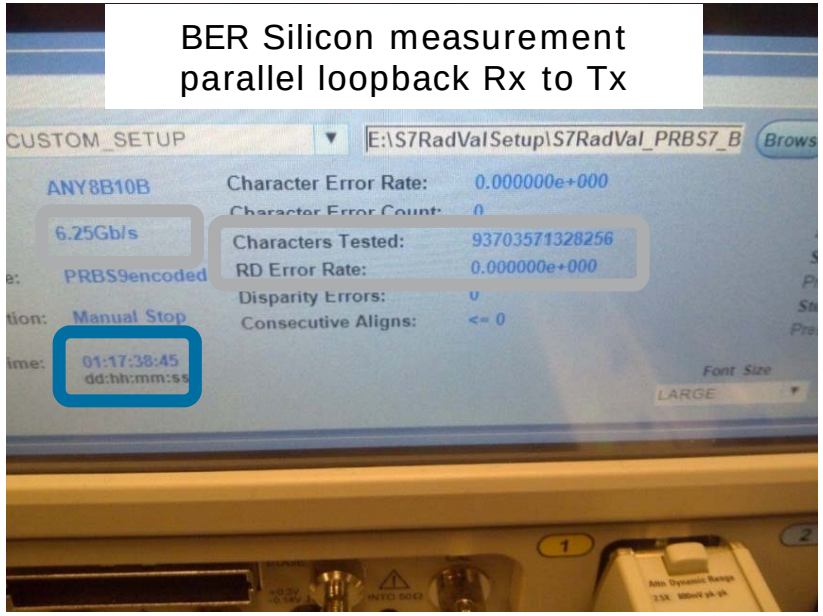
It embeds a PLL and four identical data slices. Each data slice is composed of a data transmission lane and a data reception lane. The PLL provides very stable 6.25 GHz internal bit clock which is synthesized from a lower frequency input reference clock. This bit clock is used to generate each transmission bit clock and to recover each received bit clock.

Each data slice is running independently to each other. In each data slice, the transmitter and receiver are running independently to each other and may have different bit rate.

A +/-100ppm plesiochronous operation is guaranteed by design in each data lane individually and independently (Tx data lane and Rx data lane).

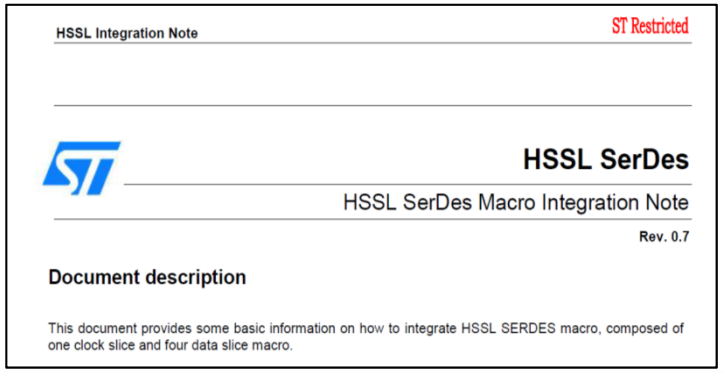
Each data slice embeds one BIST which contains: a PRBS generator, a BER monitor, an internal data lane loopback TX -> RX (in each data slice) and a TX clock jitter generator.

BER Silicon measurement parallel loopback Rx to Tx



After 6 days
0 errors @ 6.25Ghz
BER=1^{e}-15, CL=96%

HSSL IP integration note



HSSL Integration Note — ST Restricted

HSSL SerDes

HSSL SerDes Macro Integration Note

Rev. 0.7

Document description

This document provides some basic information on how to integrate HSSL SERDES macro, composed of one clock slice and four data slice macro.

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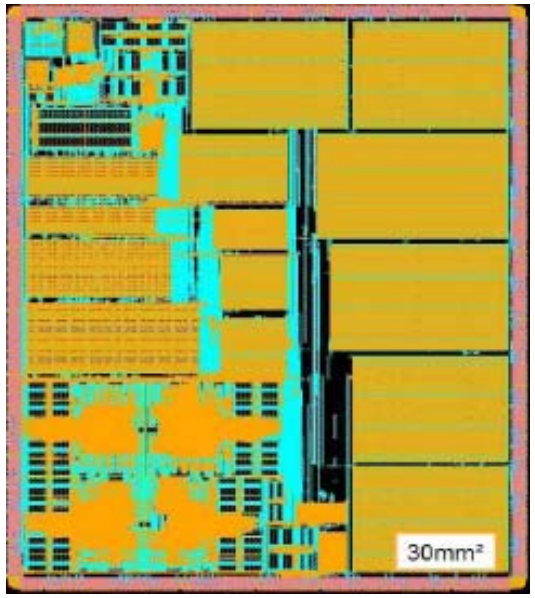
C65SPACE characterisations
4 different test vehicles families

TC1 (rad hard digital library):

- SKYROB65 ALLCELL blocks
- SKYROB65/CORE65 ROs
- FF shifters SKYROB65LP
- SRAM compilers
- Application digital blocks

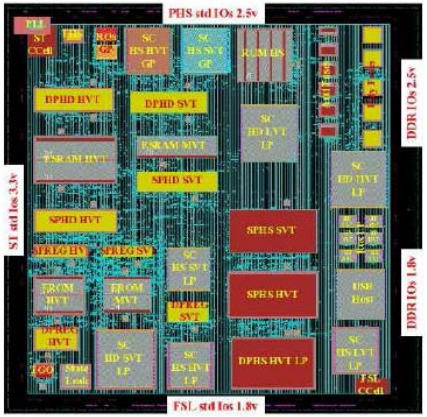


TC2 (rad hard analog library):

- high performance multiphase hardened PLL covering frequency range from 50MHz … 1.2 GHz (6 phases)
- special IOs
  - cold spare CMOS
  - cold spare LVDS
  - Signal
  - I2C

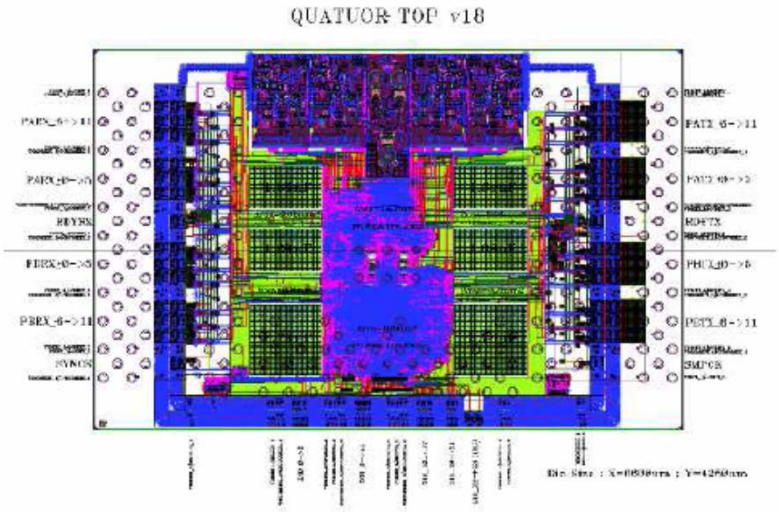
TC4 (C65 commercial library subset):

- Corelib 1000 general purpose cells

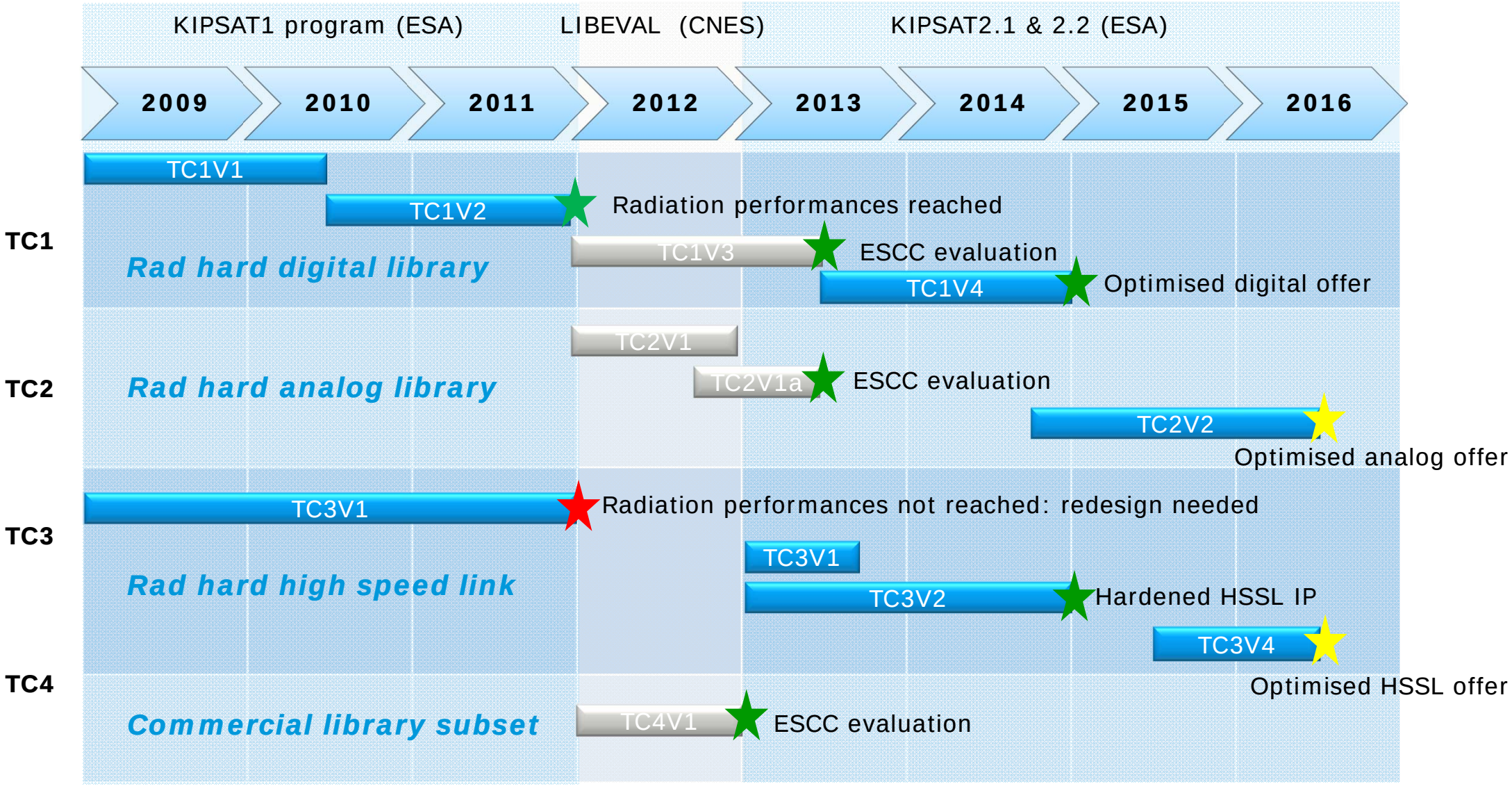


TC3 (rad hard high speed serial link):

- Quatuor / S7RADVAL quad high speed link 4 x 6.25 Gbps

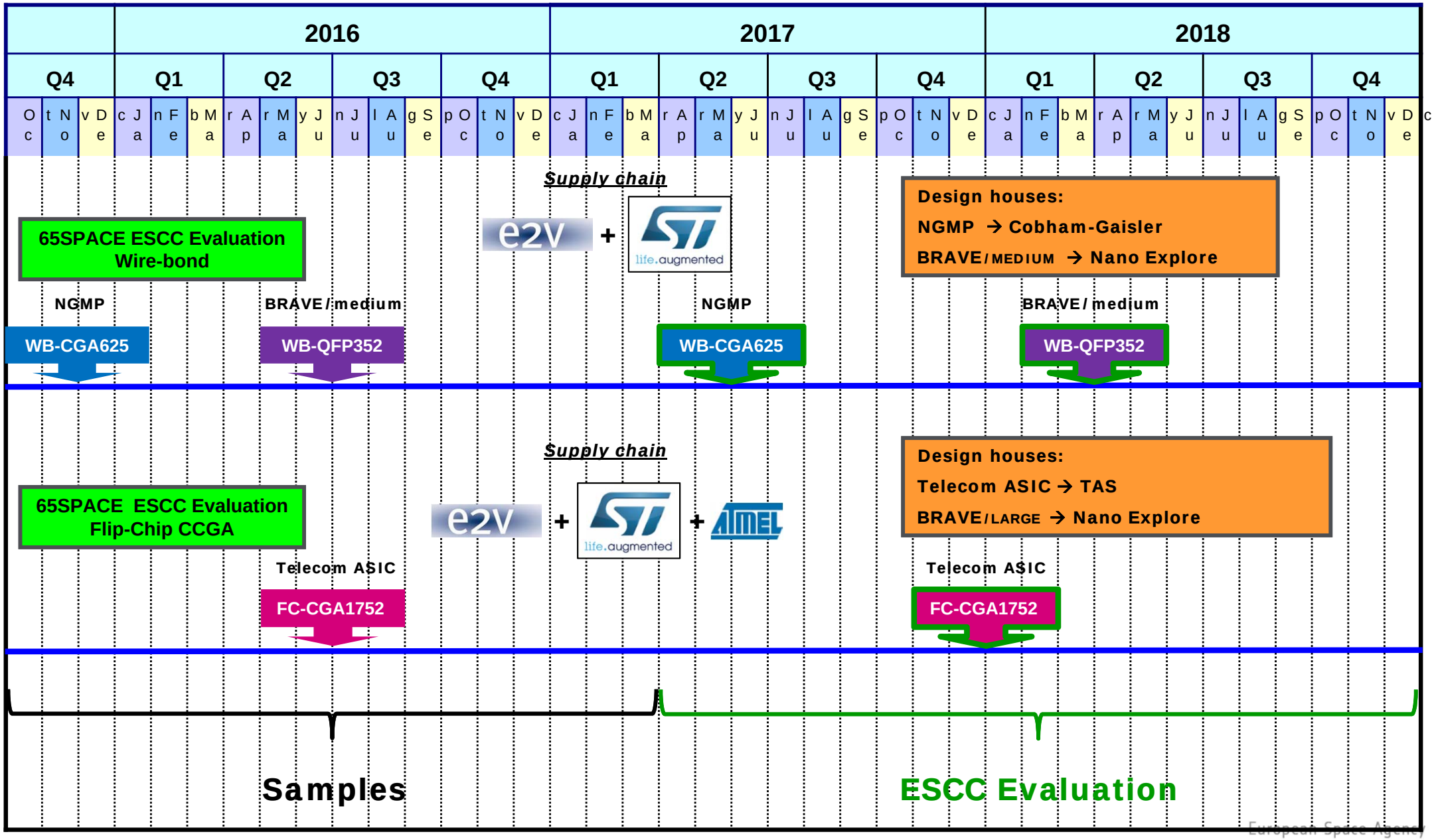


C65SPACE test vehicles development plan

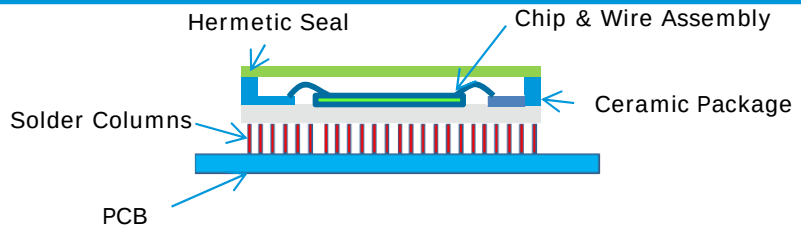


12 test vehicles developed

C65SPACE ESCC Evaluation Plan

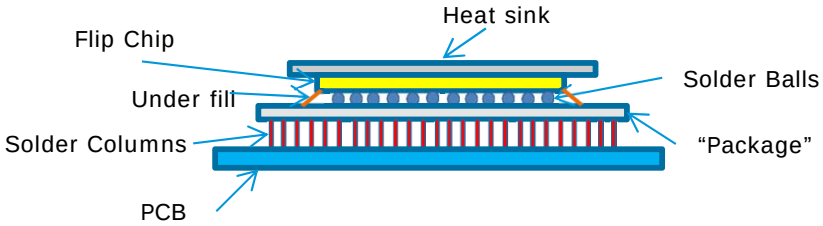


Flip Chip package technology (E2V)



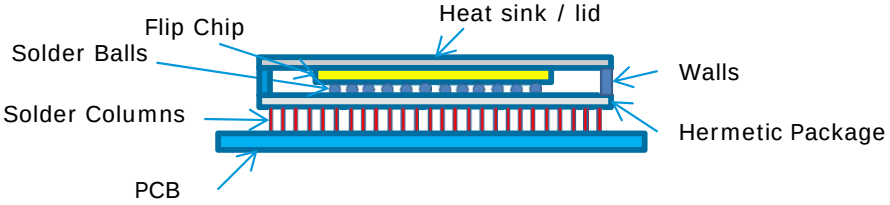
Today's wire bond package solution

Hermetic Package – Ceramic
Wire bonded – single or staggered rows
Soldered / Column mounted

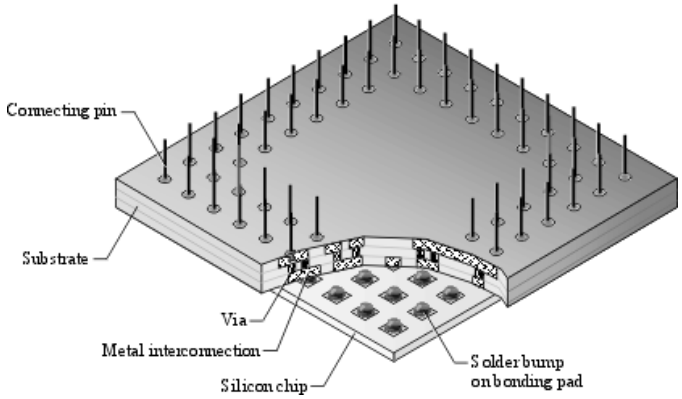


Emerging solutions

Non hermetic



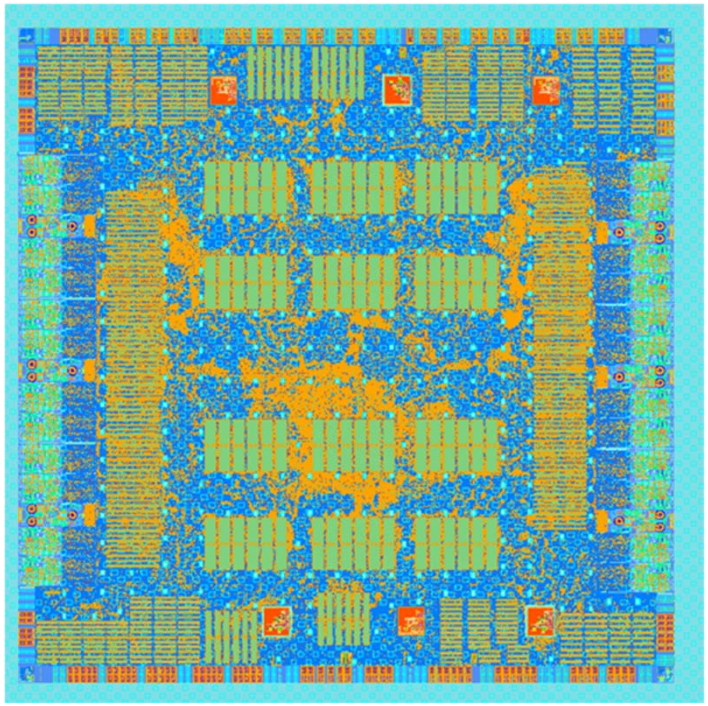
Hermetic



Flip Chip for Space applications

- ✓ High pin count package 1752 pins
- ✓ Pin pitch 1mm
- ✓ Column attach (6 Sigma)
- ✓ Signal integrity for high speed signals (HSSL 6.25 Gbps)
- ✓ Power integrity, better power grid distribution (lower voltage drop)
- ✓ Higher power dissipation 15…20W (dissipation from the backside of the die)
- ✓ Heat spreader attached on the backside of the active die
- ✓ Hermiticity capability

Application chips manufactured upon C65SPACE in 2015

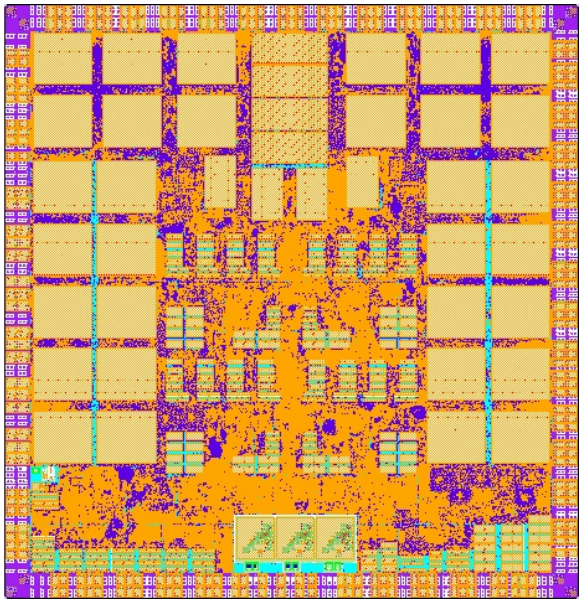


VT65 Telecom ASIC → CNES funding

200mm2

1752 Flip Chip -CGA Package

(courtesy: TAS / ST / ATMEL / CNES)



Next

Flight models in 2016

Next Generation Microprocessor NGMP → ESA funding

Quad Leon4 architecture clocked @ 250MHz

70mm2

Wire bond package CGA625

(courtesy: Cobham-Gaisler / ST)

Agenda

- Motivation for DSM program
- ST C65SPACE radiation hardened ASIC technology
- ST C65SPACE qualification status / roadmap
- **Conclusion**

Conclusions

- ✓ ST 65nm hardening activities are close to completion
- ✓ 3000 pages data book compiling datasheets + radiation reports (HI + Protons + Gamma)
- ✓ ST C65SPACE flow has been deployed to Alpha users in 2015
- ✓ Two applications test vehicles have been produced and functionally validated in 2015
  - ✓ NGMP next generation microprocessor developed by Cobham/Gaisler (ESA funding)
  - ✓ VT65 telecom processor developed by TAS-F (TAS / CNES / ST/ ATMEL funding)
- ✓ A flight version of the telecom ASIC is currently under development (TAS / CNES / ST/ ATMEL funding) and will be manufactured in 2016. The circuit will exhibits a complexity of ~ half Billion transistors ☺
- ✓ Radiation validation of HSSL IP version4 planned for Q2-2016. Circuit has been taped out in December 2015

Conclusions

Perspectives beyond 65nm

- ✓ Future developments will benefit from the lessons learned on ST C65SPACE program. C65SPACE has paved the way for future developments with ST.
- ✓ ST Fully Depleted SOI technologies 28nm / 14nm are promising nodes with respect to radiation hardening
  - ✓ Better starting point with respect to latchup hardening
  - ✓ Self heating might be an issue to tackle with care
- ✓ Cost might be a limiting element for the development and qualification of a general purpose ASIC technology beyond 65nm node. Economic considerations will instead push for the design and qualification of standard products (micro processor or FPGA).
- ✓ Still need to work very closely with technology supplier (ST) to get access to full reliability data based on mass volume production.
- ✓ Necessity to tackle reliability not only at technology level but also at architecture level with concepts such as FPGA, Network on Chip or GPU (many cores).

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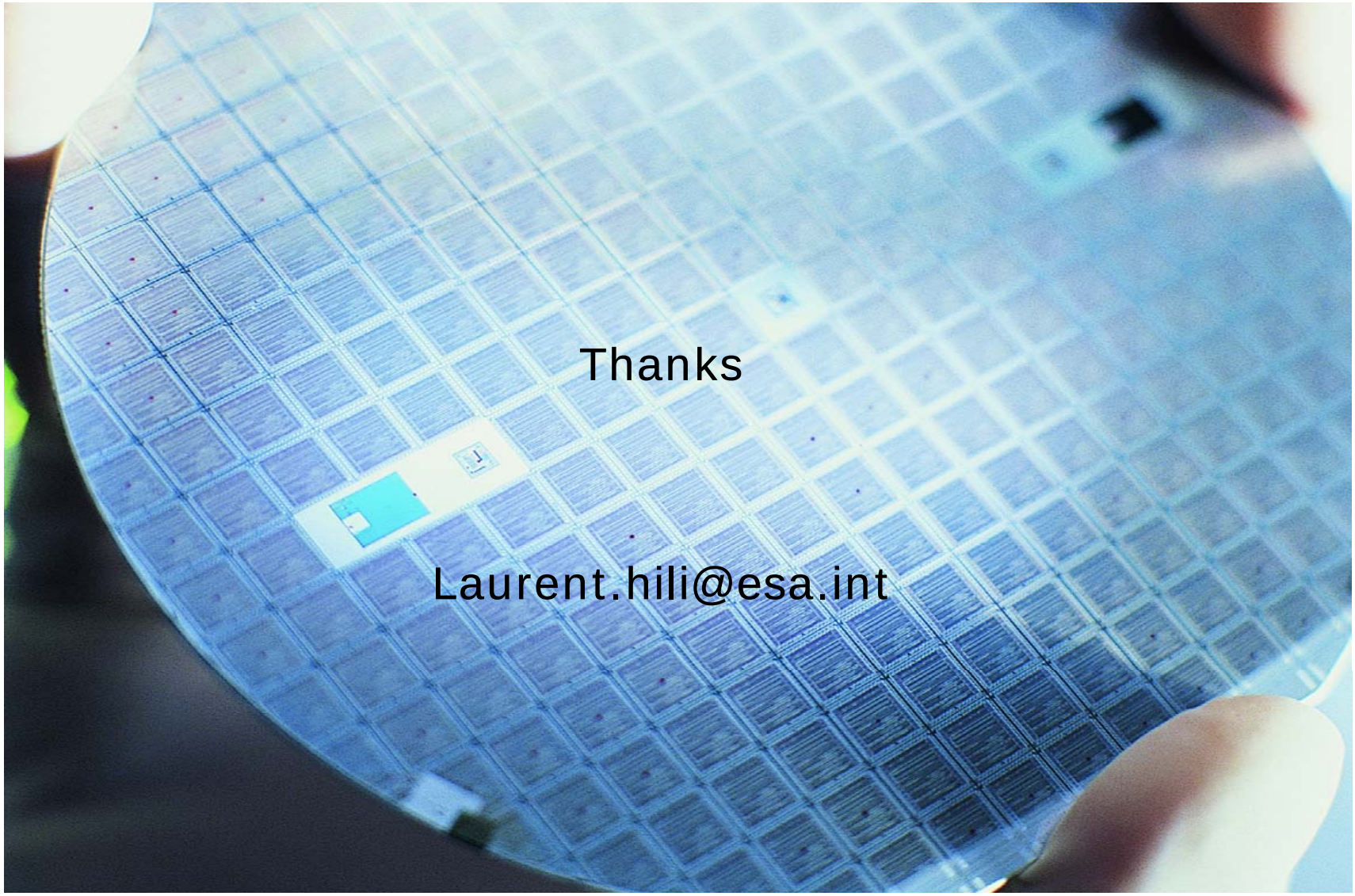
Thanks
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