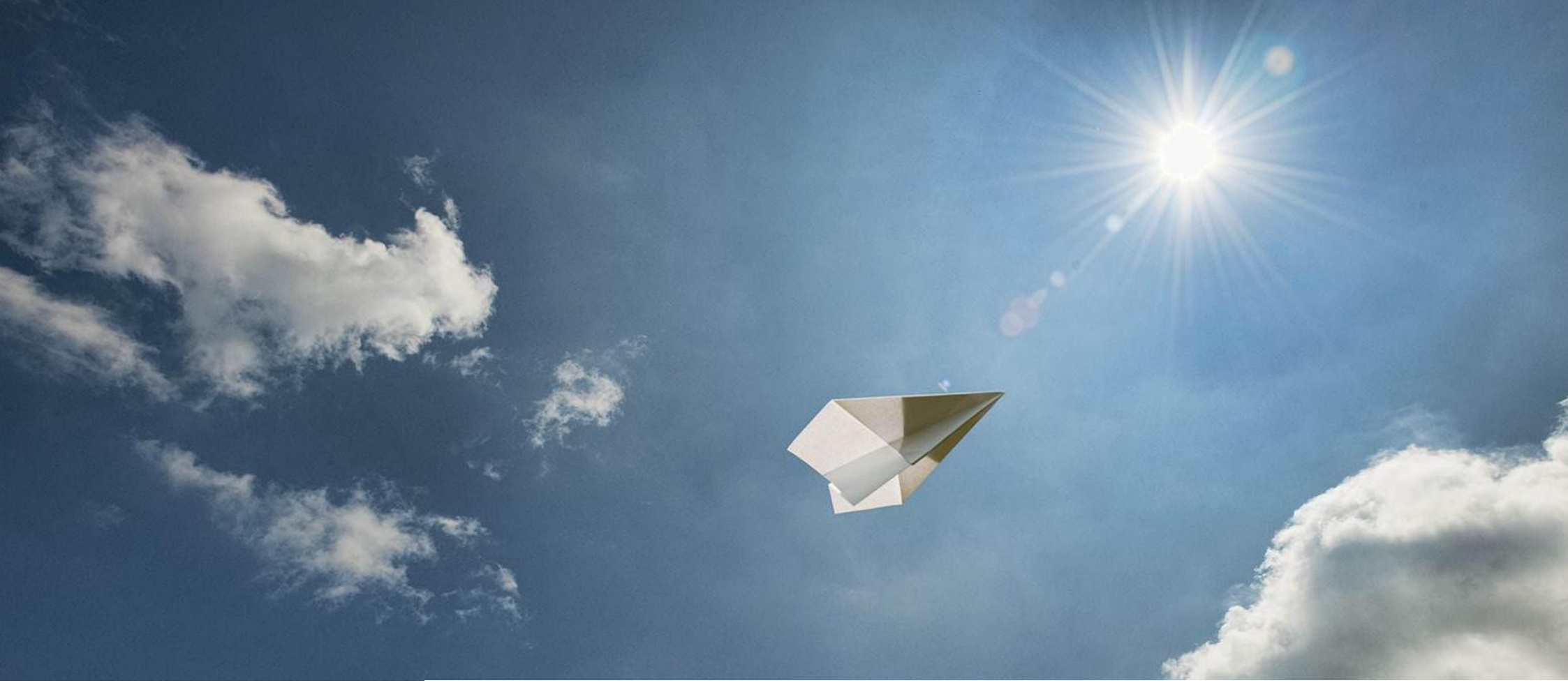

ESCCON 2016
Lifetime predictions of Deep Sub-Micron commercial EEE parts for space applications

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Lifetime predictions of Deep Sub-Micron commercial EEE parts for a specific application
Lifetime assessment by the OEM

Summary

1) Introduction

A. Context

Assets for Airbus Group to use COTS semiconductor technologies into design aeronautic/space designs:

- To implement performing functions in electronic equipment
- To remain competitive vs competitors with the integration of low cost components
- To have access to mature process due to the high volume in production

Issues with existing and future COTS semiconductor technologies:

- Driven by mass market needs (cost, performance, density, power consumption)
- Airbus Group does/will not have the definition of COTS semiconductors (long term reliability, various and harsh environments, obsolescence)

How to face with :

- Aerospace OEMs have to adapt its constraints & requirements
- OEMs have to redefine criteria of selection for COTS semiconductor components

1) Introduction

A. Context

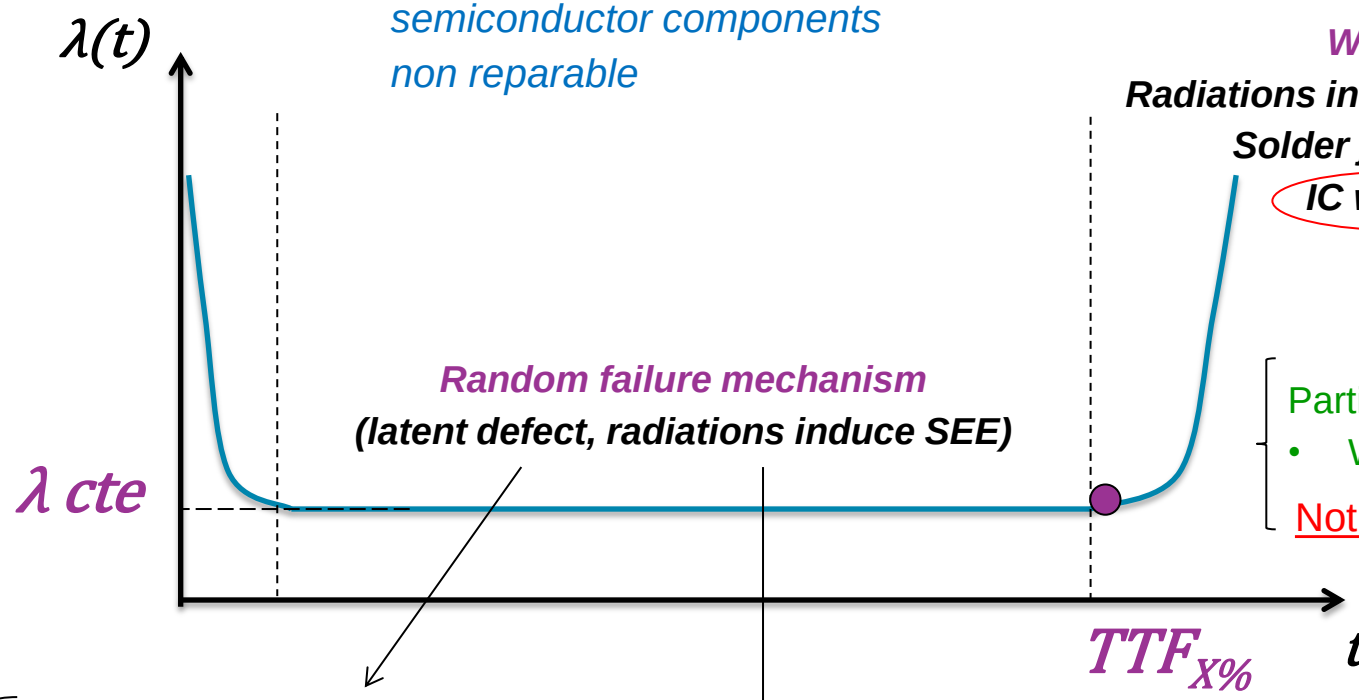
Criteria of selection for COTS semiconductor components:

- **Performance**
  - Frequency, number of macrocells (FPGA)
  - Density (Memories)
- **Board requirements:**
  - Bias voltage
  - Number of I/O
- **Power Management:**
  - Power consumption/dissipation (W)
- **Device packaging:**
  - Dimensions/type
  - Number of pins/balls/pads
  - Flip-chip die?
  - Others…
- **RoHS compliance**
- **Thermal Grade** (commercial, industrial, automotive, military, space etc…)
- **Availability**
  - Obsolescence, production life cycle
  - Sourcing, delay….
- **Radiation sensitivity**
  - Latchup
  - SEU/MBU/SEFI…
  - TID
- **Reliability**
  - Failure rate in operation
  - Lifetime in mission (wearout)

1) Introduction

A. Context

Lot made of " N" COTS semiconductor components non reparable



Wearout
Radiations induce Dose effects
Solder joint fatigue
IC wearout

Partially Covered by OCM/foundry:
- WLR qualification

Not covered by OEM!!

Random failure mechanism
(latent defect, radiations induce SEE)

Partially Covered by OCM:
- Product qualification

Partially covered by OEM:
- MIL-HDBK-217
- FIDES
- Equipement qualification

Hardly ever covered by OCM itseff:

Covered by OEM:
- Safety/Risk analysis and mitigations
- Predictions or test campain with particles accelerator if needed (heavy ions, protons…)

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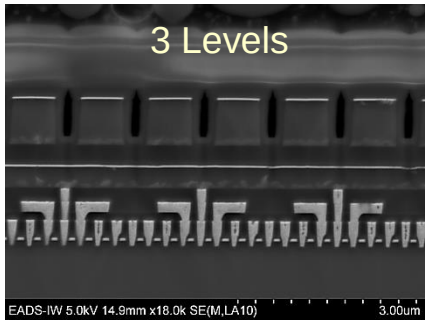
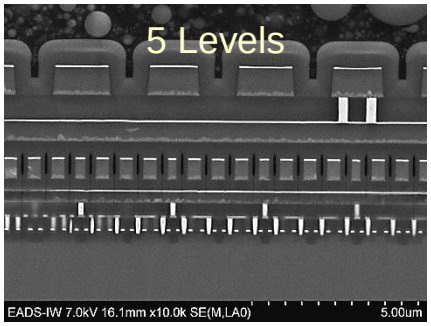
1) Introduction

B. Problematic with COTS semiconductors components

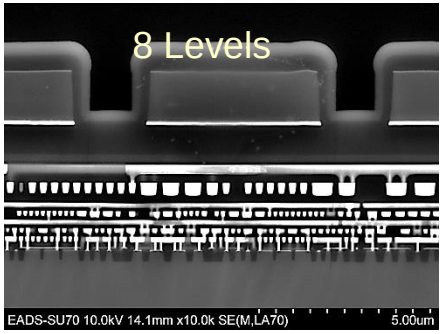
Increase of fonction density:



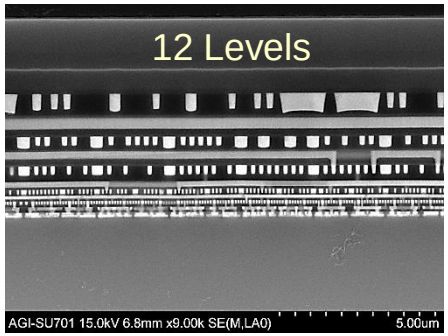
Metallizations 90 nm



Metallizations 65 nm



Metallizations 45 nm

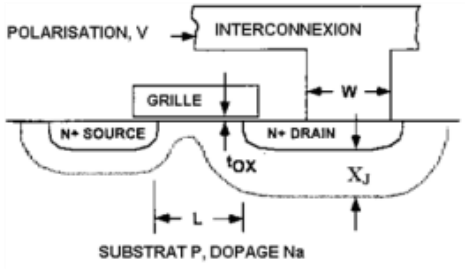


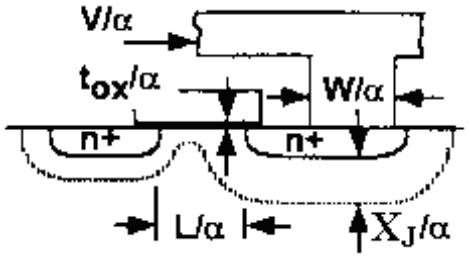
Metallizations 22 nm

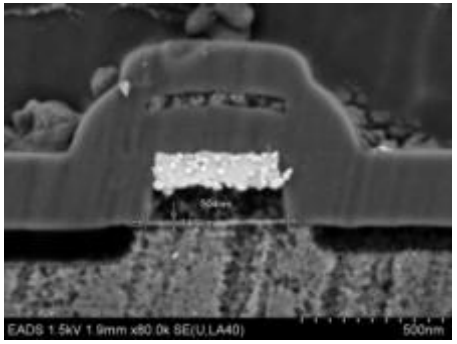
Non Homothetic FEOL shrink:

Deep Sub Micron

Year	**1990**	**1992**	**1995**	**1997**	**1999**	**2001**	**2004**	**2007**	**2009**	**2011**	**2012**	**2014**	**2016**
Technologie (nm)	1000	500	350	250	180	130	**90**	**65**	**45**	**32**	**28**	**20**	**16/14**







Increase of electrical field and current leakage vs integration

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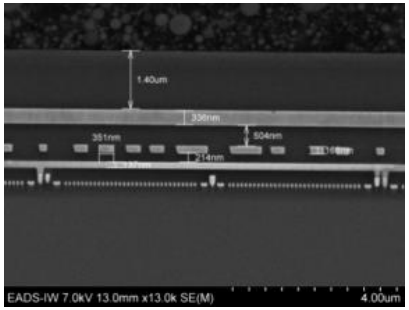
1) Introduction

B. Problematic with COTS semiconductors components

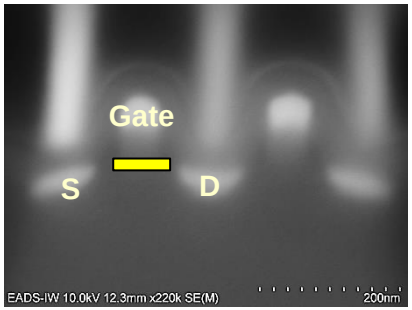
Introduction of new material/architecture for Performance/consumption purposes:

Operating frequency improvement (reduction of RC delay)



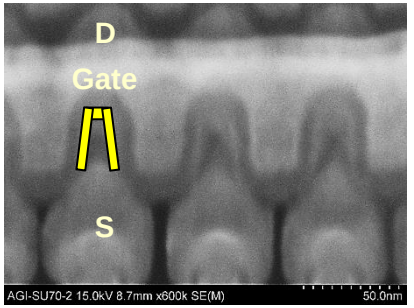
BEOL Copper wires + Low K oxides

Idsat increase (gate capacitance improvement)



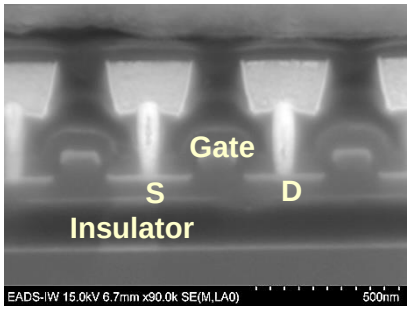
45 nm CMOS SiON transistors

Current consumption improvement (gate leakage), Idsat increase (gate capacitance improvement)



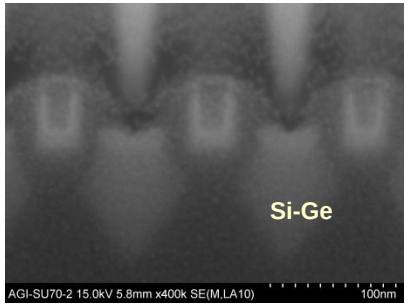
22 nm FinFETs HKMG transistors

Frequency switch improvement Drain current leakage reduction



Silicon On Insulator (SOI)

Frequency switch improvement (carrier mobility improvement)



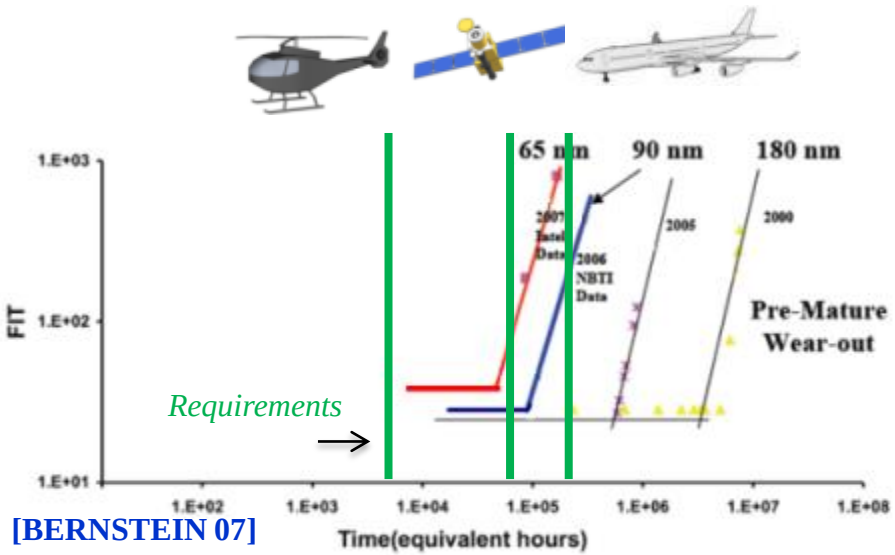
28nm CMOS Si-Ge transistor

What reliability Impact on HiRel applications ??

1) Introduction

B. Problematic with COTS semiconductors components

Technical issue: early wearout effects of IC



[BERNSTEIN 07]

With COTS semiconductor technologies < 180 nm:

- Increase of failure rate
- Decrease of intrinsic lifetime

Inputs necessary for relevant lifetime assessment:

- Impact of mission profile (aircraft, equipment)
- Impact of technology (BEOL, FEOL)
- Definition of failure mechanisms (PoF)

Industrial issues:

Not easy collaboration with OCM for COTS (proprietary WLR data, fabless strategy, low purchase volume)

Wearout effects on COTS semiconductors are not concerned by classical methodologies (MiL HDBK, FIDES…)

➡ Aerospace OEMs must define specific guidance devoted to COTS semiconductors

➡ Airbus Group Methodology
AVSI AFE83

AIRBUS GROUP

2) Airbus Group Methodology

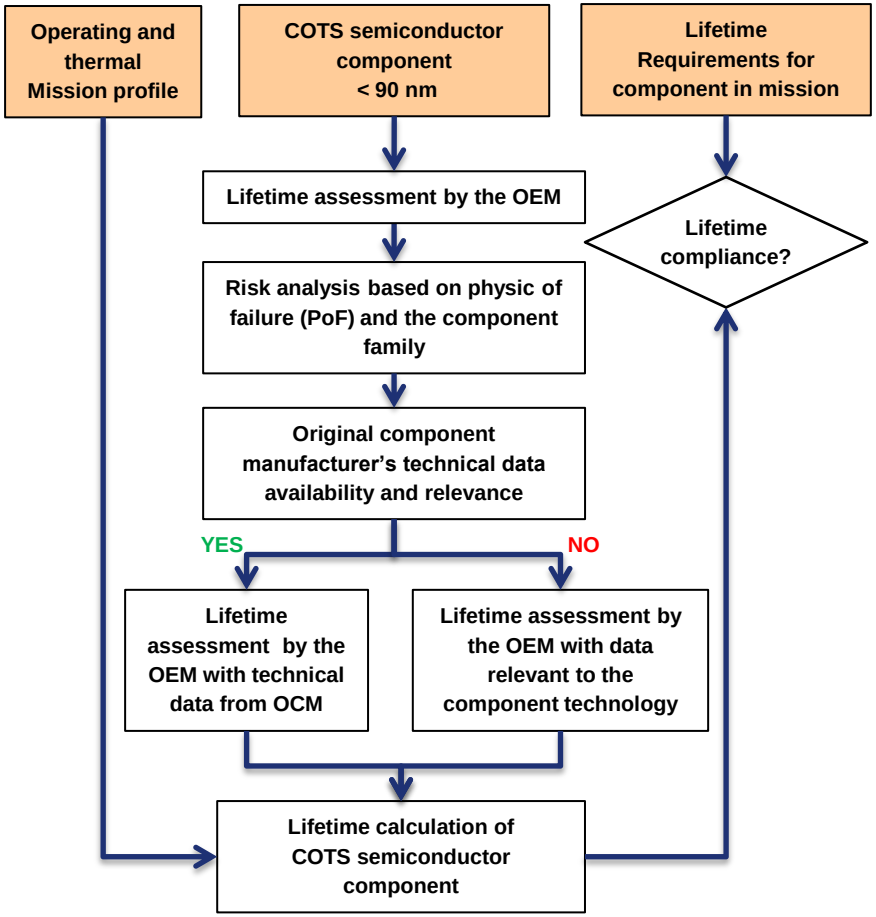
A. Scope of the methodology

Lifetime predictions of Deep Sub-Micron commercial EEE parts for a specific application
Lifetime assessment by the OEM

Criteria		Items concerned
Technology	Type of component	**COTS components** (ASICs are excluded)
	Component family	Focus on CMOS digital devices such as µProcessor, FPGA & SRAM and NVM memories, DRAM, Flash)
	Node	Focus on CMOS Deep Sub Micron **< 130 nm**
Degradation	Localization	Integrated circuit (areas BEOL et FEOL)
	Nature of failure	Integrated circuit Wearout failures (Radiation & overstress aspects are excluded)
	Failure mechanisms	Failure mechanisms: • **Time Dependent Dielectric Breakdown (FEOL)** • **Time Dependent Dielectric Breakdown (BEOL)** • **Bias Temperature Instabilities** • **Hot Carrier Injection** • **Electromigration**

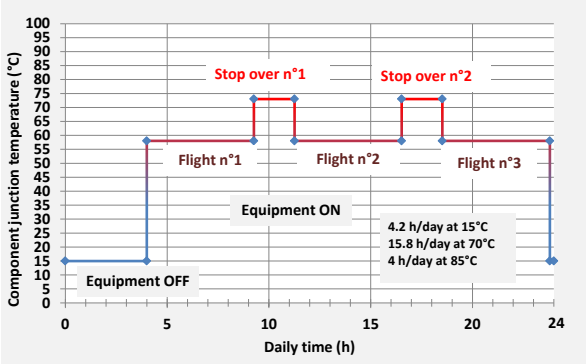
2) Airbus Group Methodology

B. Methodology process flow



Operating and thermal Mission profile

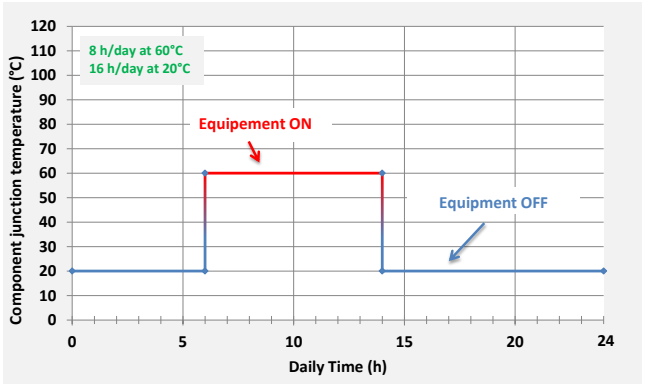
- Operating (Equipment/component ON state)
- Thermal junction temperature (Tj)



Ex: FPGA assembled in Flight computer (avionic bay)

- 166 000 h @Tj=73°C, V_{DD} nominal, f nominal
- 42 000 h @Tj=58°C, V_{DD} nominal, f nominal

→ 210 000h ~ 24 years



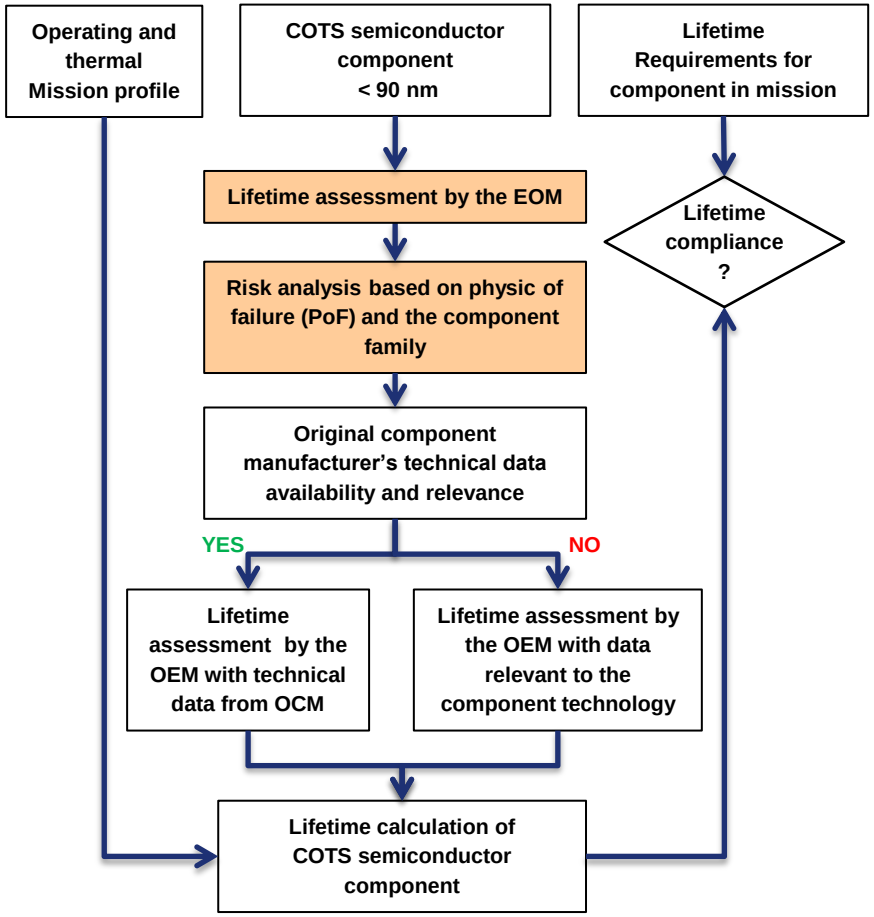
Ex: memory assembled on board equipment

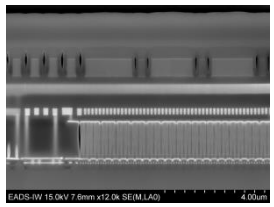
- 87 600h @Tj=20°C, OFF, f nominal
- 43 800 h @Tj=60°C, V_{DD} nominal, f nominal

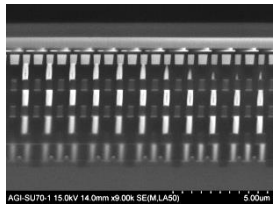
→ ~ 5 years

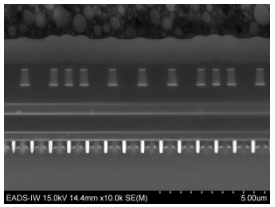
2) Airbus Group Methodology

B. Methodology process flow




DRAM


MRAM


Flash NOR

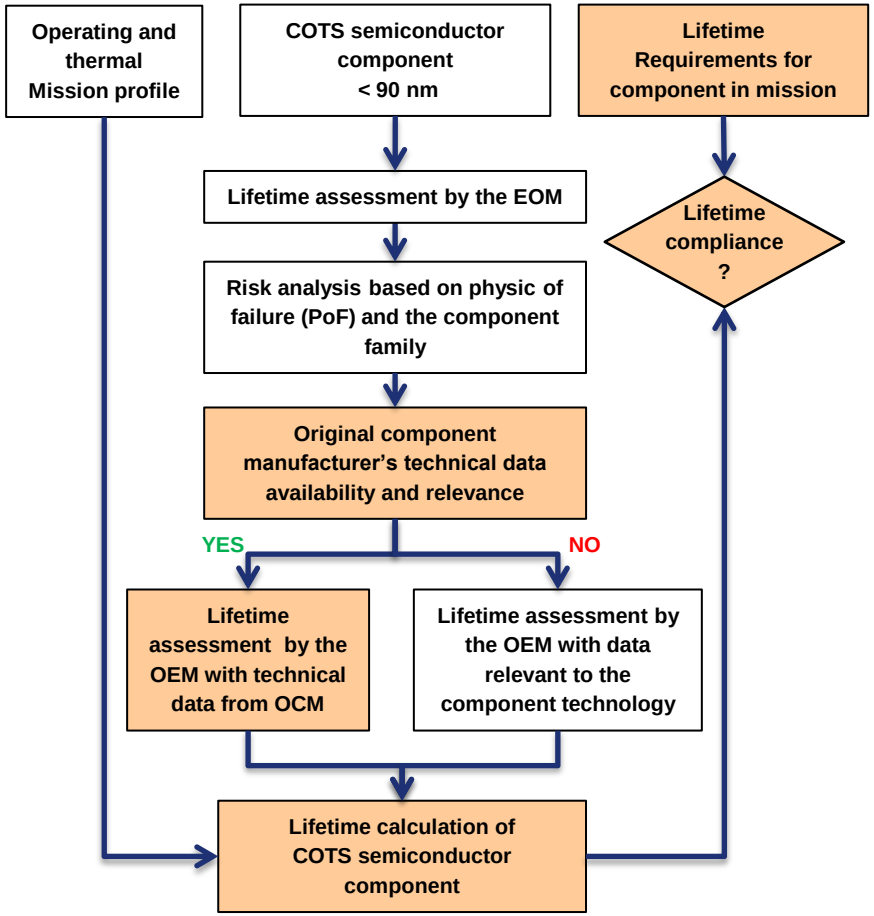
Matrix of Failure mechanism to investigate by the OEM vs product family

Failure mechanism	Component structure		Electronic component (<90 nm process)				
			FPGA	µP	DRAM	Flash	SRAM
EM	Levels	Global	√	√	√	√	√
		Intermediate	√	√	NA	NA	NA
		Local	√	√	√	√	√
TDDB BEOL	Levels	Global	√	√	√	√	√
		Intermediate	√	√	NA	NA	NA
		Local	√	√	√	√ (if LK oxides)	NA
TDDB FEOL	I/O	NMOS	√	√	√	√	√
		PMOS	√	√	√	√	√
	Core	NMOS	√	√	NA	NA	√
		PMOS	√	√	NA	NA	√
	Capacitor	Oxide	NA	NA	√	NA	NA
HCI	I/O	NMOS	√	√	√	√	√
		PMOS	√	√	√	√	√
	Core	NMOS	√	√	√	√ (if NOR)	√
		PMOS	√	√	NA	NA	√
BTI	I/O	NMOS	√	√	√	√	√
		PMOS	√	√	√	√	√
	Core	NMOS	√ (if HK oxides)	√ (if HK oxides)	NA	NA	√ (if HK oxides)
		PMOS	√	√	NA	NA	√

Selection of relevant failure mechanisms for a given product

2) Airbus Group Methodology

B. Methodology process flow



Data to collect by the OEM from the OCM:

Wafer fab qualification report

- Electromigration
- TDDB BEOL
- TDDB FEOL
- HCI
- BTI

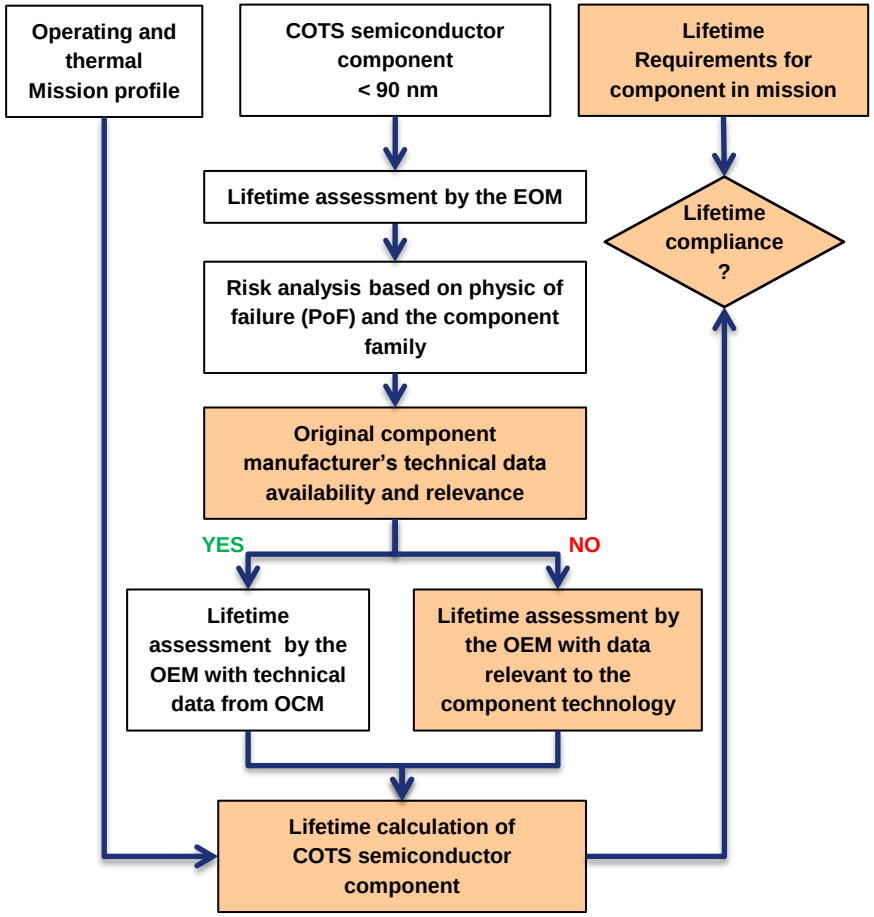
Non truncated test

For the failure mechanisms previously identified by the reisk analysis:

- Raw reliability test results
  - Failure distribution F(t)
  - Distribution parameters
- Compact models + parameters
  - Thermal acceleration
  - Bias acceletration

2) Airbus Group Methodology

B. Methodology process flow



Data to collect by the OEM form the scientific literature

For the failure mechanisms previously identified by the risk analysis:

- Raw reliability test results
- Acceleration models

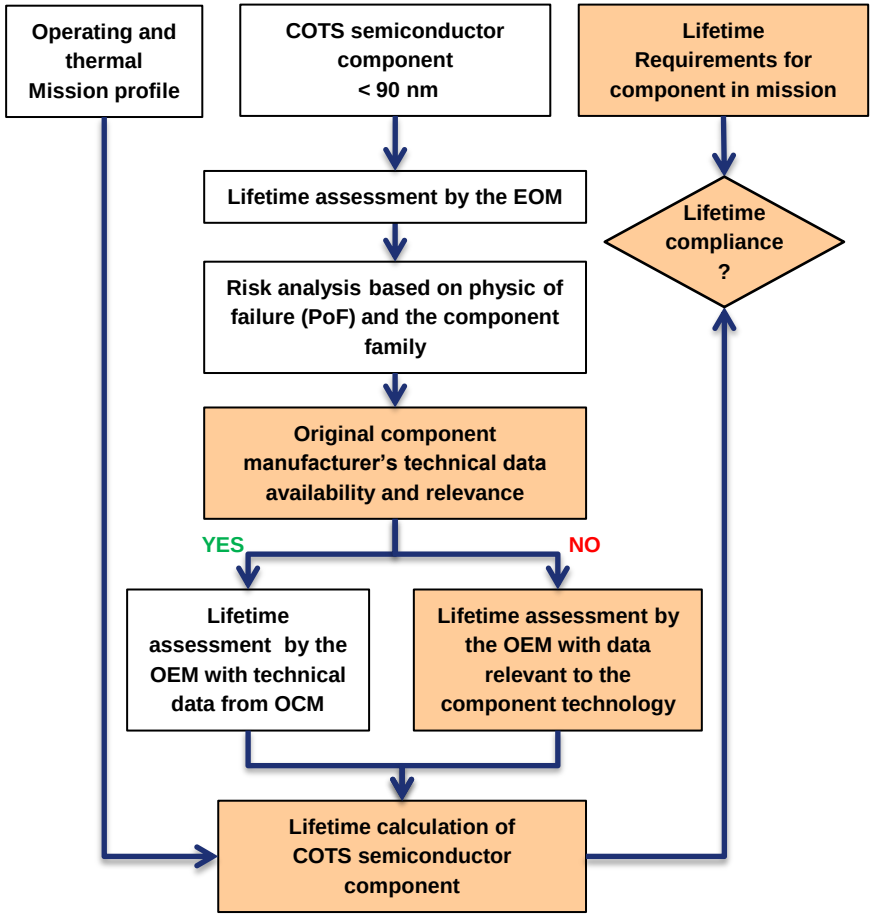
Example of models :

Failure mechanism	level	Acceleration model
EM	Global Intermediate Local	$AF_{EM} = \left(\frac{f_{TEST}}{f_{MISSION}}\right)^{n} \cdot \left(\frac{V_{TEST}}{V_{MISSION}}\right)^{-n} \cdot e^{\frac{E_a}{k}\left(\frac{1}{T_{MISSION}} - \frac{1}{T_{TEST}}\right)}$
TDDB BEOL	Global Intermediate Local	$AF_{TDDB\_BEOL} = \left(\frac{S_{TEST}}{S_{MISSION}}\right)^{n} \cdot e^{G\cdot\left(\sqrt{E_{MISSION}} - \sqrt{E_{TEST}}\right)} \cdot e^{\frac{E_a}{k}\left(\frac{1}{T_{MISSION}} - \frac{1}{T_{TEST}}\right)}$
TDDB FEOL	I/O	$AF_{TDDB\_FEOL\_I/O} = \left(\frac{S_{TEST}}{S_{MISSION}}\right)^{n} \cdot e^{\gamma\cdot\left(E_{MISSION} - E_{TEST}\right)} \cdot e^{\frac{E_a}{k}\left(\frac{1}{T_{MISSION}} - \frac{1}{T_{TEST}}\right)}$
	Core	$AF_{TDDB\_FEOL\_CORE} = \left(\frac{S_{TEST}}{S_{MISSION}}\right)^{n} \cdot \left(\frac{V_{TEST}}{V_{MISSION}}\right)^{\gamma} \cdot e^{\frac{E_a}{k}\left(\frac{1}{T_{MISSION}} - \frac{1}{T_{TEST}}\right)}$
HCI	I/O	$AF_{HCI\_I/O} = \left(\frac{f_{TEST}}{f_{MISSION}}\right)^{n} \cdot e^{\gamma\left(\frac{1}{V_{MISSION}} - \frac{1}{V_{TEST}}\right)} \cdot e^{\frac{-E_a}{k}\left(\frac{1}{T_{MISSION}} - \frac{1}{T_{TEST}}\right)}$
	Core	$AF_{HCI\_CORE} = e^{\gamma\left(\frac{1}{V_{MISSION}} - \frac{1}{V_{TEST}}\right)} \cdot e^{\frac{E_a}{k}\left(\frac{1}{T_{MISSION}} - \frac{1}{T_{TEST}}\right)}$
BTI	I/O	$AF_{BTI\_I/O} = e^{\gamma\cdot\left(V_{MISSION} - V_{TEST}\right)} \cdot e^{\frac{E_a}{k}\left(\frac{1}{T_{MISSION}} - \frac{1}{T_{TEST}}\right)}$
	Core	$AF_{BTI\_CORE} = e^{\gamma\cdot\left(V_{MISSION} - V_{TEST}\right)} \cdot e^{\frac{E_a}{k}\left(\frac{1}{T_{MISSION}} - \frac{1}{T_{TEST}}\right)}$

Models from literature are technology dependant !!

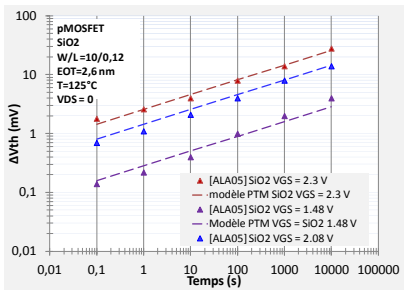
2) Airbus Group Methodology

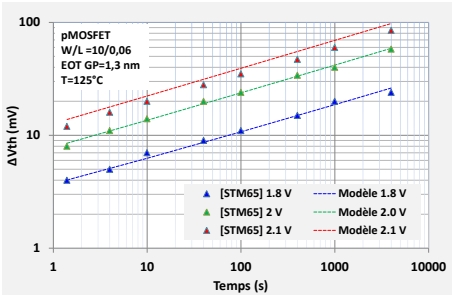
B. Methodology process flow



Action for OEM

- Adjust parameters/models on experimental results from literature (with technological relevancy)





$$\Delta V_{th} = K_v \cdot \beta^{0.25} \cdot T^{0.25} \cdot \left[\frac{1-\left(1-\sqrt{\eta(1-\beta)/n}\right)^{2n}}{1-\left(1-\sqrt{\eta(1-\beta)/n}\right)^{2}} \right]^{0.5} + \delta_v$$

$$K_v = A \cdot T_{ox} \cdot \sqrt{C_{ox}\left(V_{gs}-V_{th}\right)} \cdot \exp\left(\frac{E_{ox}}{E_0}\right) \cdot \left[1-\frac{V_{ds}}{\alpha\left(V_{gs}-V_{th}\right)}\right] \cdot \exp\left(-\frac{E_a}{kT}\right)$$

α,Ea….

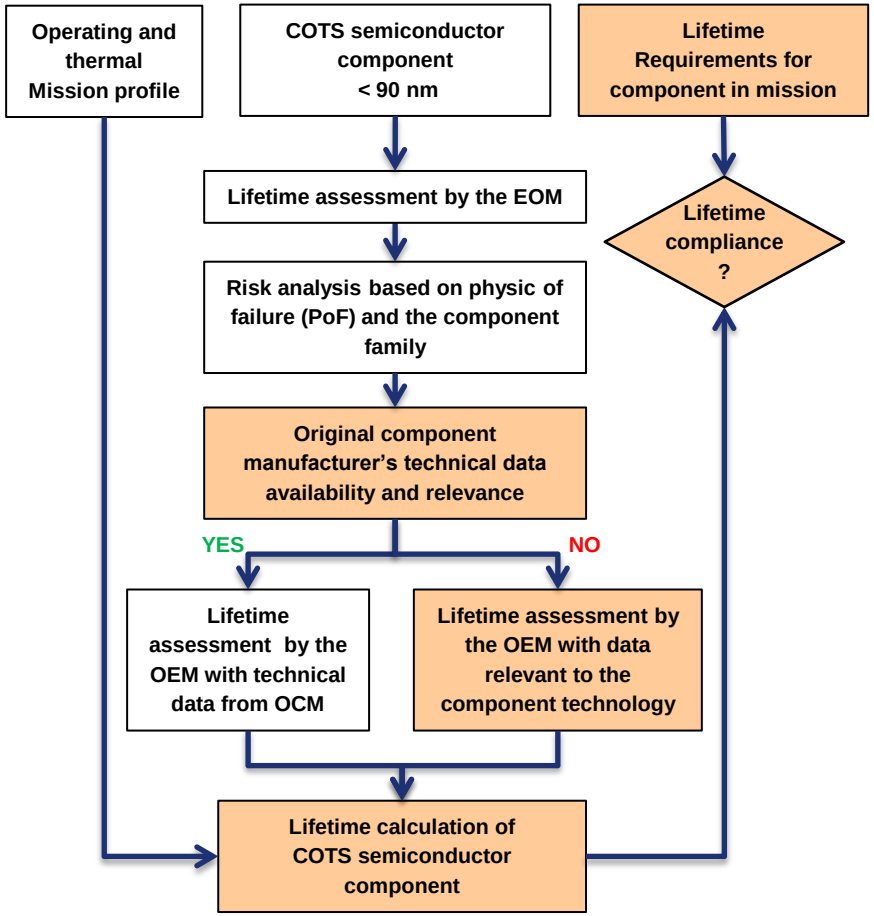
[BTI PTM model, ASU university]

- (or) use existing database

Database of AF degradation models relevant with all technologies of COTS semiconductor availlable on market

2) Airbus Group Methodology

B. Methodology process flow

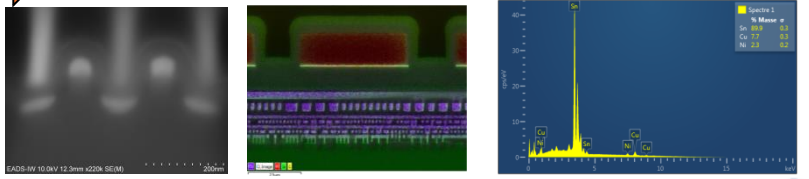


Data to collect by the OEM

- Description of component technology

Table D.1 - BEOL and FEOL technological parameters		Parameter	Notation	Unit
BEOL	**Global wires**	Nature of metallization	NA	NA
		Nature of insulation oxides	NA	NA
		Width of metal wires	W_{GLOBAL}	nm
		Thickness of metal wires	T_{GLOBAL}	nm
		Wire to wire pitch	P_{GLOBAL}	nm
	Intermediate wires	Nature of metallization	NA	NA
		Nature of insulation oxides	NA	NA
		Width of metal wires	$W_{INTERMEDIATE}$	nm
		Thickness of metal wires	$T_{INTERMEDIATE}$	nm
		Wire to wire pitch	$P_{INTERMEDIATE}$	nm
	Local wires	Nature of metallization	NA	NA
		Width of metal wires	NA	NA
		Thickness of metal wires	W_{LOCAL}	nm
		Dimension of metal wires	T_{LOCAL}	nm
		Wire to wire pitch	P_{LOCAL}	nm
FEOL	**I/0 Transistors**	Nature of Gate oxide	NA	NA
		Equivalent Oxide Thickness	$EOT_{I/O}$	nm
		Gate oxide surface	$S_{G\ I/0}$	nm
		Nature of gate	NA	NA
		Gate lengh	$L_{G\ I/0}$	nm
		Gate width	$W_{G\ I/0}$	nm
	Core Transistors	Nature of Gate oxide	NA	NA
		Equivalent Oxide Thickness	EOT_{CORE}	nm
		Gate oxide surface	$S_{G\ CORE}$	nm
		Nature of gate	NA	NA
		Gate lengh	$L_{G\ CORE}$	nm
		Gate width	$W_{G\ CORE}$	nm
	Substrate	Nature of substrate	NA	NA

From De Processing Analysis (DPA)



2) Airbus Group Methodology

Database of degradation models

Multitude of technology coexist on market

Technology CMOS Overview High performance family (nm)		USA										Taiwan										Europe			
		Intel					GlobalFoundry					UMC				TSMC						ST Micro			
		90 nm	65 nm	45 nm	32 nm	22 nm	90 nm	65 nm	40 nm	28 nm HPP	22 nm UHP	90 nm G	65 nm SP	40 nm G	28 nm HPM	90 nm G	65 nm G	40 nm GP	28 nm G	20 nm HP	16 nm HP	90 nm	65 nm	40 nm	28 nm FDSOI
FEOL	Metal gate	N	N	Y	Y	Y	N	N	N	Y	Y	N	N	N	Y	N	N	N	Y	Y	Y	N	N	N	N
	High-k Dielectrics	N	N	Y	Y	Y	N	N	N	Y	Y	N	N	N	Y	N	N	N	Y	Y	Y	N	N	N	N
	Strain silicion	Y	Y	Y	Y	Y	Y	Y	Y	?	Y	N	Y	Y	Y	N	?	Y	Y	Y	Y	N	N	Y	Y
BEOL	Copper metalizations	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
	Low-k Dielectrics	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
Substrate	Silicon on Insulator (SOI)	N	N	N	N	N	Y	Y	Y	Y	Y	N	Y	?	N	Y	Y	Y	Y	Y	N	N	Y*	N	Y
Architecture	FinFETs	N	N	N	N	Y	N	N	N	N	Y	N	N	N	N	N	N	N	N	N	Y	N	N	N	N

*On demand

At fixe node/OCM: different transistor optimization vs application

		TSMC 28 nm				
		28 nm High Performance (HP)	28 nm High Performance Mobile (HPM)	28 nm High Performance Compact Mobile computing (HPC)	28 nm High Performance Low power (HPL)	28 nm Low power (LP)
FEOL	Metal gate	Y	Y	Y	Y	N (PolySi)
	High-k Dielectrics	Y	Y	Y	Y	N (Nitride Oxide)
	Lengh gate (nm)	31 nm	35 nm	30 - 40 nm	35 nm	38 nm
	Vcore	0.85 V	0.90 V	0.90 V	1,00 V	1,05 V

[1]
[2]

1 technological node ~ 30 differents technologies ~ 30 degradation models

Airbus Group Data base ~ 110 models (2012)

2) Airbus Group Methodology

Assessment

Lifetime predictions of Deep Sub-Micron commercial EEE parts for a specific application
Lifetime assessment by the OEM

Advantage of the method:

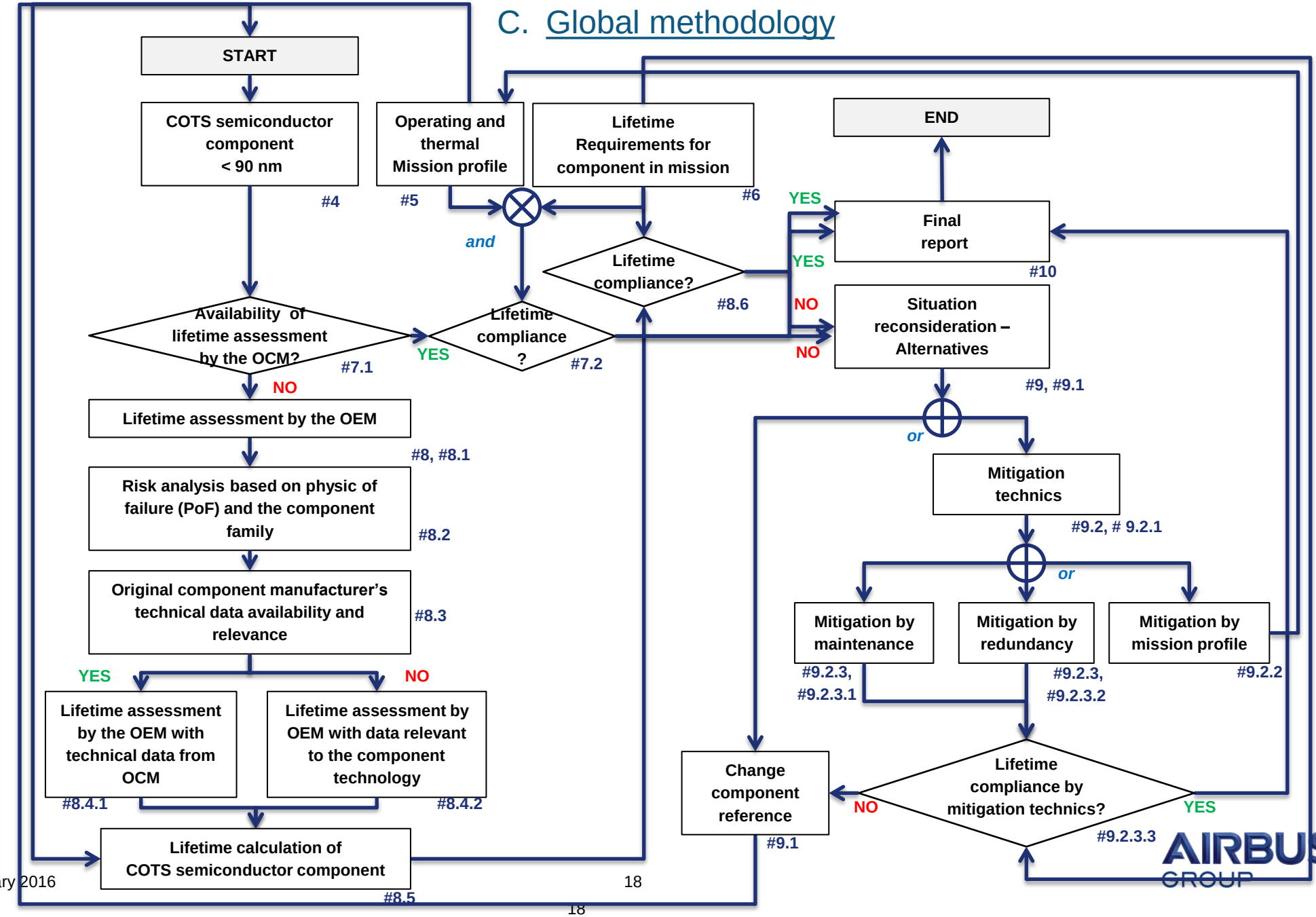
- Based on Physics of failure (PoF), environement and part technology
- Combine two approach:
  - Lifetime Assessement with technical data from OCM (by default if possible)
  - Lifetime Assessement with technical data relevant to the component technology (in absence of collaboration with OCM)
- Simply enough to be implemented in a tool (Airbus Tool for internal use so far)
- Methodology applied on Airbus Group parts (memories, FPGA, µProcerssors) for aeronautic, aerospace and military applications for 8 years!

Weakness/limitations of the method:

- May require to have access to the component technology (De Processing Analysis)
- Do not consider the impact of the design and the manufacturing process
- Method supposed that:
  - All failure mechanisms are independant between themselves
  - AF degradation models can be extrapolated over a long period of use

2) Airbus Group Methodology

C. Global methodology



3) Conclusion and perspectives

With COTS semiconductor technologies < 180 nm (and mainly <90 nm):

- Increase of failure rate
- Decrease of intrinsic lifetime

How to face with :

- Wearout is a deterministic phenomenon that has to be evaluated/predicted in design phase by OEM
- Some working group develop methodologies → France (Airbus, GIFAS)
  US (AFE83)

Discussion and proposition

Topic "*Assessment of COTS semiconductor component in Hi-Rel and long term application*"

- Has to be addressed at electronic component management level through Technical Standard document proposing an "industrial"

→ Can be based on Airbus 2015-IW-SI-000036-1 document

Or/and GIFAS document (reference GIFAS/2015/5022), public access [1]

→ IEC has included concepts from the Airbus Group methodology into their Wearout Life Calculation standard IEC TS 62239-1 (in revision to IEC TS 62239-2)

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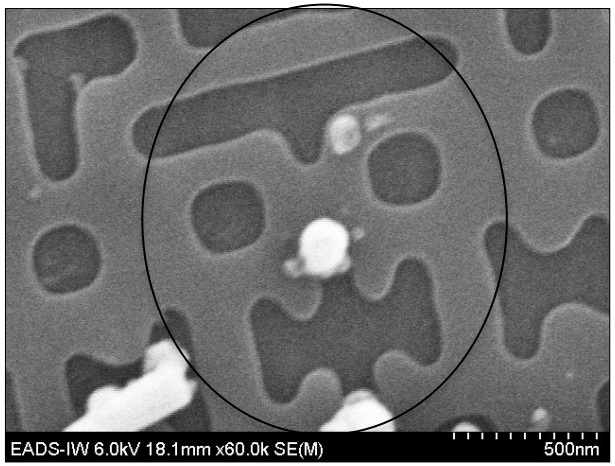
3) Conclusion and perspectives

Acknowledgement

- **Airbus Group Innovations Teams**
- **Divisions of Airbus Group**

Thanks for your attention



SRAM 90 nm, SEM, x 60k

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4) Sources

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[2]	Synopsys website, consulted the 03/01/2016 https://www.synopsys.com/Company/Publications/DWTB/Pages/dwtb-logic-libraries-tsmc28-hpc-2015q3.aspx
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