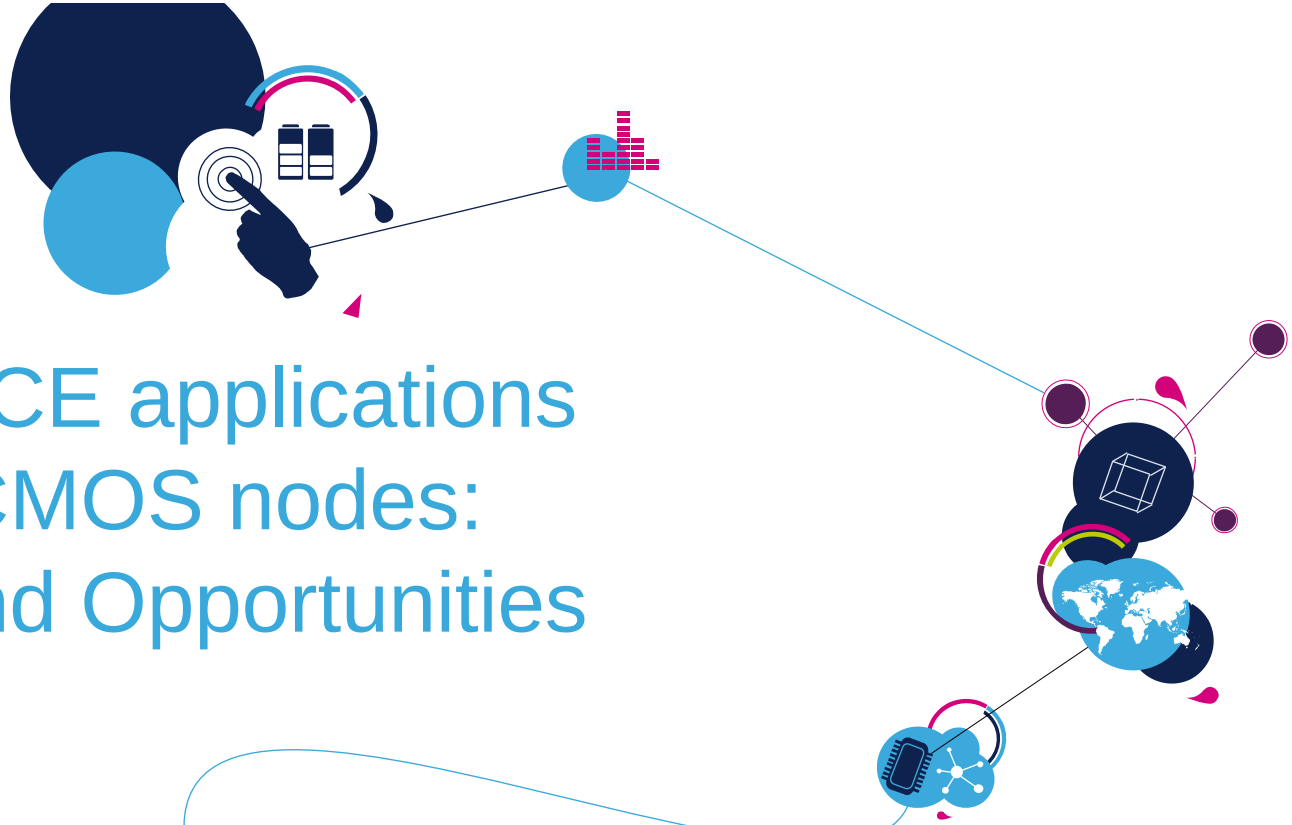


Enabling SPACE applications in advanced CMOS nodes: Challenges and Opportunities

STMicroelectronics, Crolles

V.Huard, *Member of Technical Staff*

March 1st-3rd, 2016

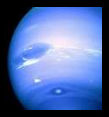
life.augmented

Space exploration and CMOS scaling
50+ years of common history











Vostok 1 1st spaceflight
Voskhod 2 1st spacewalk
Appolo 11 1st moonwalk
Pioneer 11 Saturn's flyby
MIR 1st space station
Hubble
Voyager 2 Neptun's flyby
Sojourner 1st Mars rover
ISS Largest space station
Hayabusa 1st asteroid sampling
Rosetta 1st comet landing

1960 1970 1980 1990 2000 2010 2016

IBM 1620
1

Intel 4004
2.300
Music Hall capacity

Intel 286
134.000
Large stadium capacity

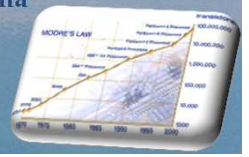
Power Mac G4
32 Million
Population of Tokyo

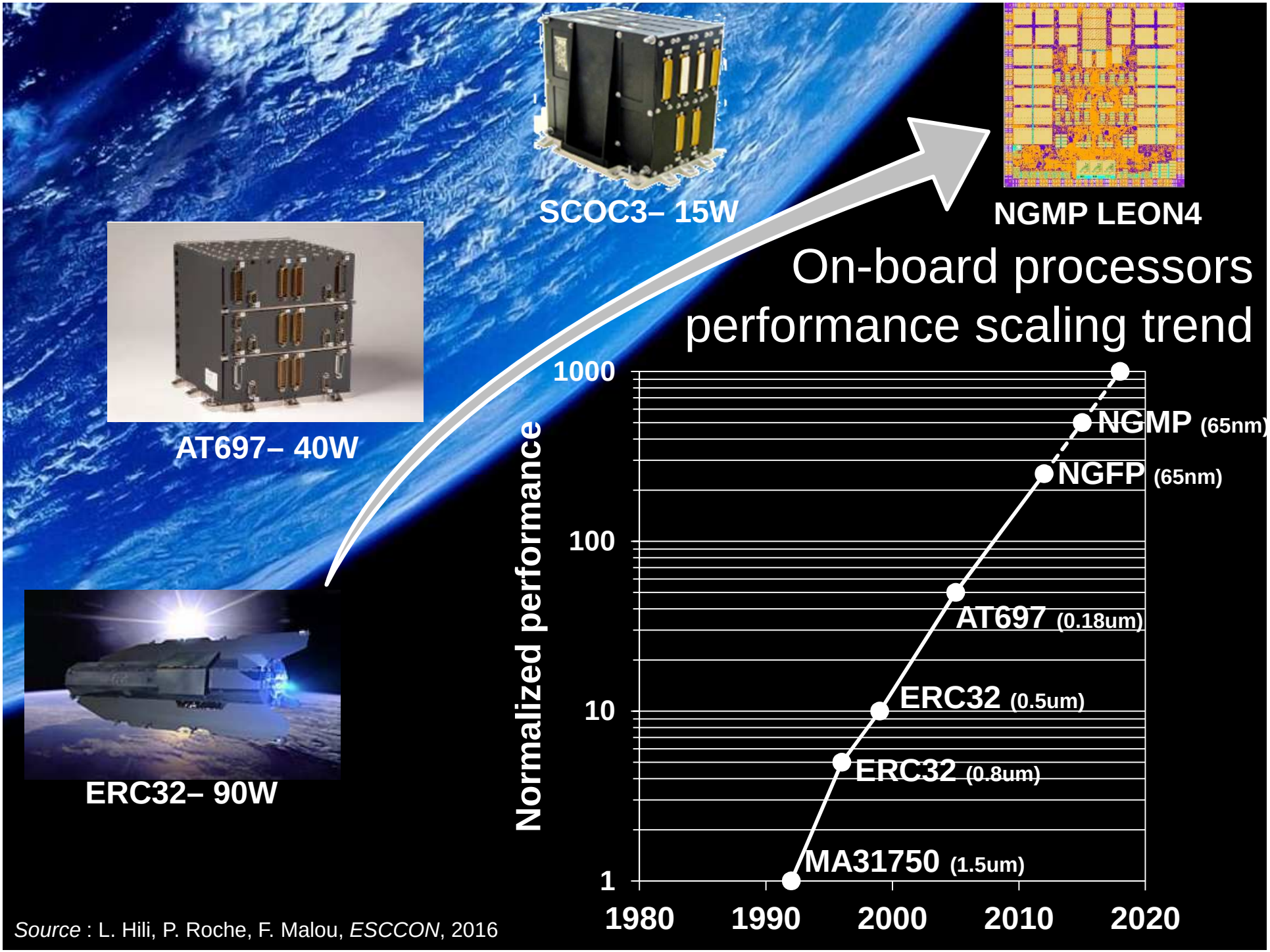
Core i7 Extreme Edition
1.3 Billion
Population of China

transistors



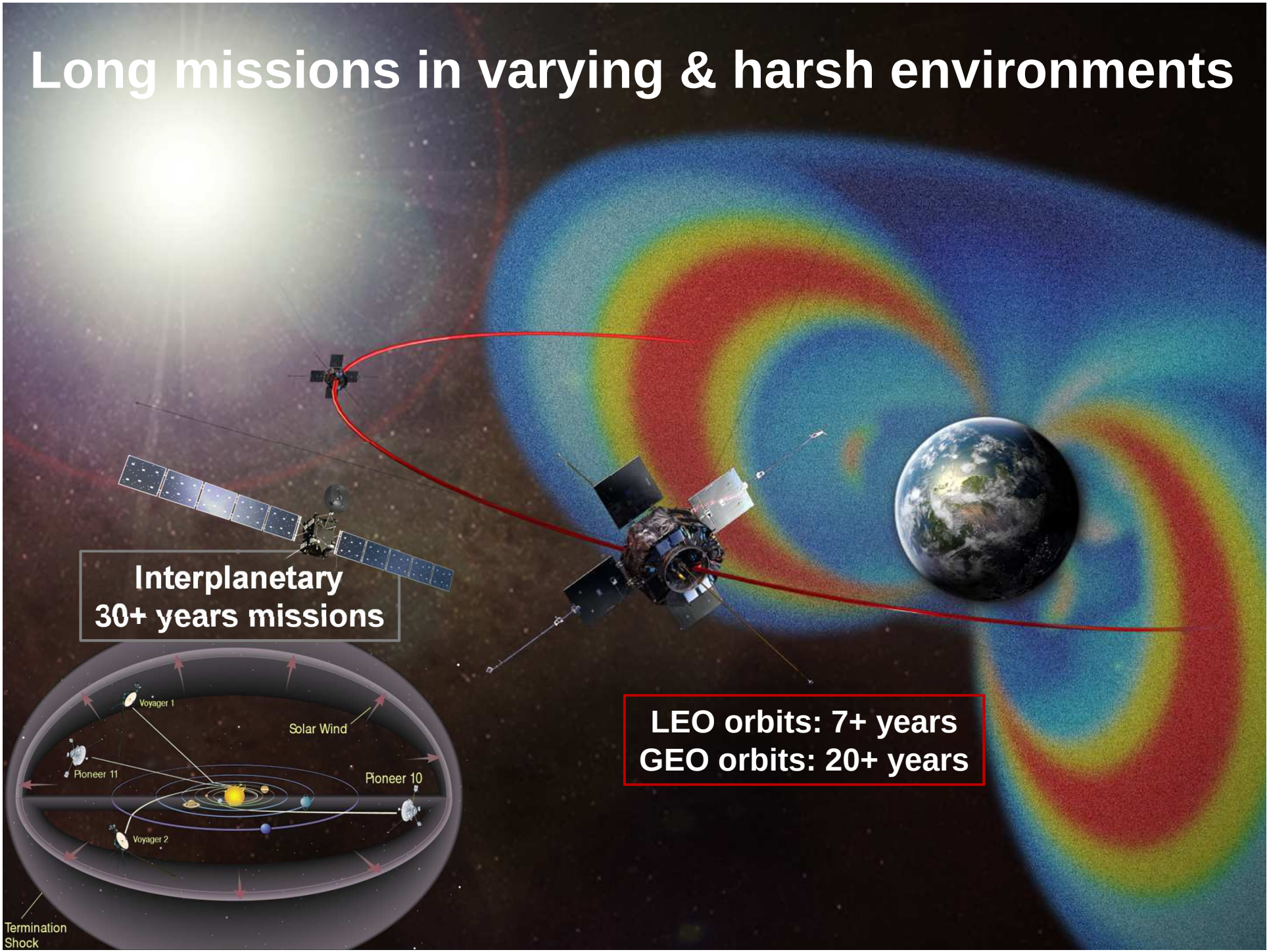




Source : L. Hili, P. Roche, F. Malou, *ESCCON*, 2016

Long missions in varying & harsh environments



Outline

- Scaling and Reliability Challenges
  - Electromigration
  - BTI degradation
  - HCI degradation
  - TID degradation
- Device Reliability Modelling
  - Physic-of-Failure (PoF) approach supported by ST-specific C code
  - Industrial, automated extraction flow
  - Generic simulations outputs
- Digital Hardening Flow
  - Design For Reliability flow for digital IPs
  - Predictive EMG checker
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  - Reliability-enabled design framework
  - Automated flow for hardening
- Conclusions and Perspectives

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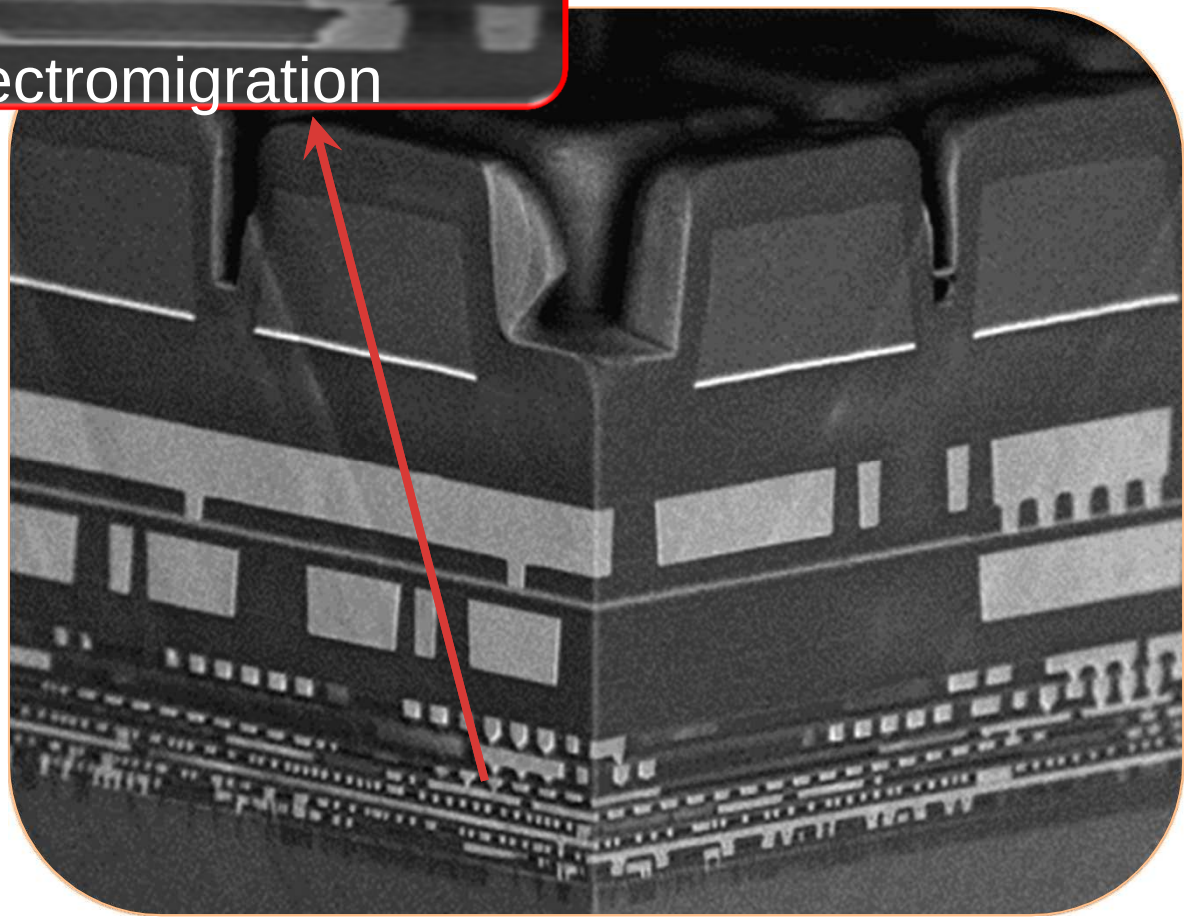
Degradation Mechanisms

$$\vec{J}_{flow} = c\frac{eD}{kT}Z^{*}\rho\,\vec{j}$$

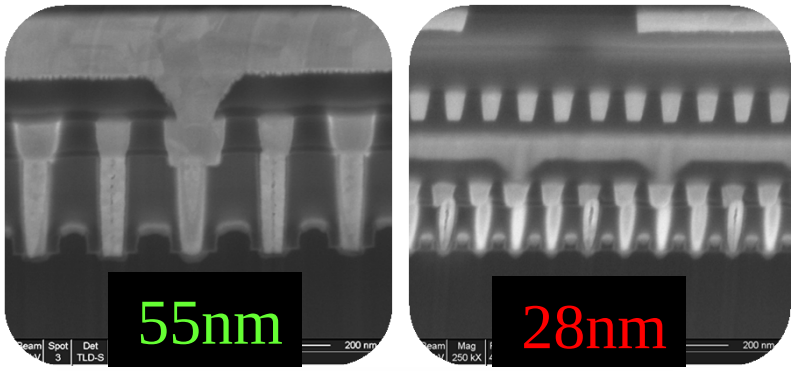
e-

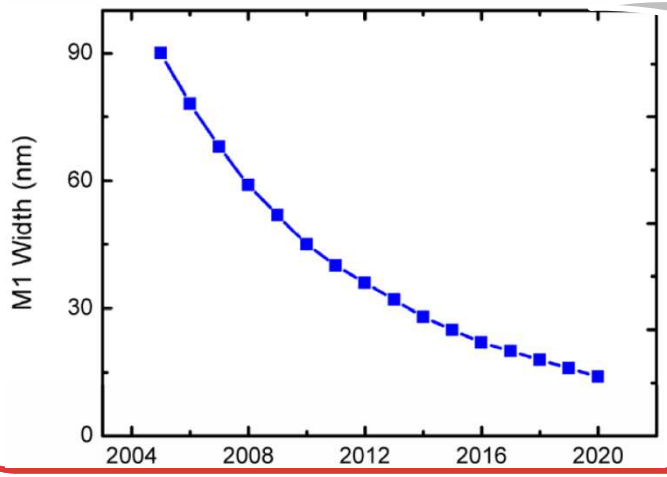
Electromigration



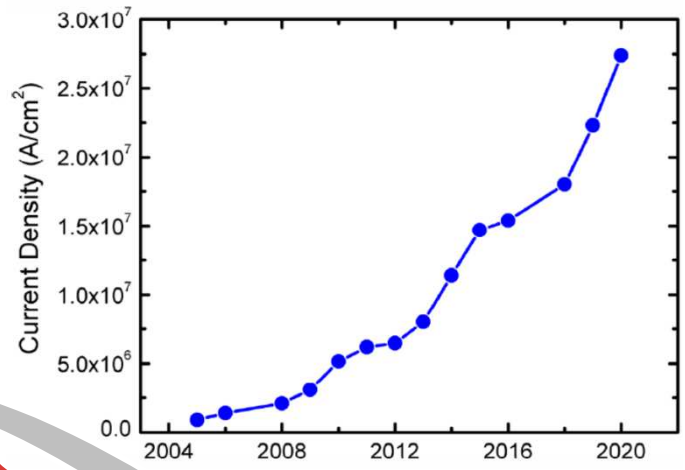
EMG and Interconnect scaling

Interconnect scaling

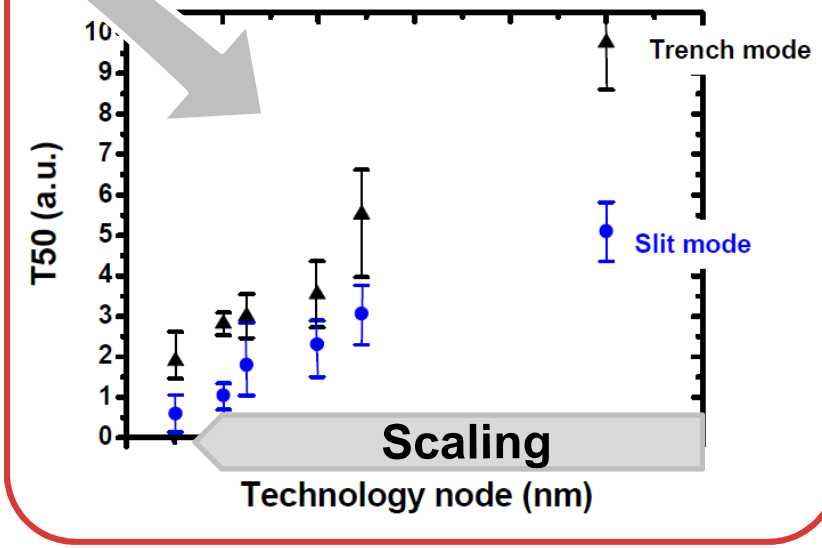




Increased current density



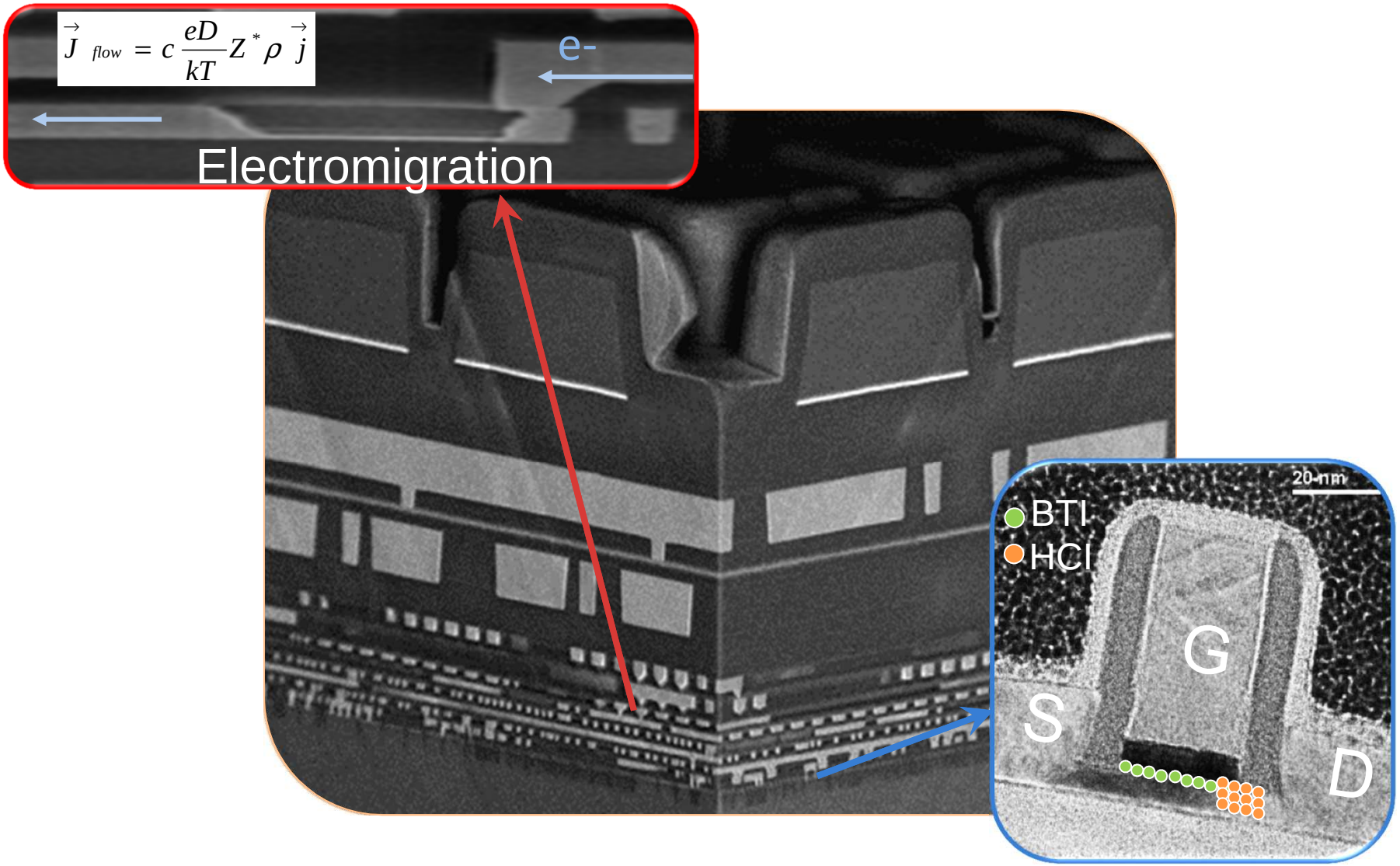
Decreased EMG lifetime



Source : ITRS, 2001/2013.

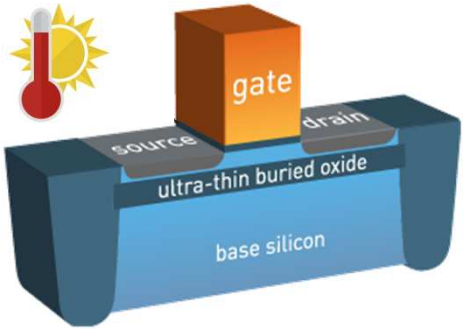
Source : T. Oates et al., *IRPS* , 2012

Degradation Mechanisms

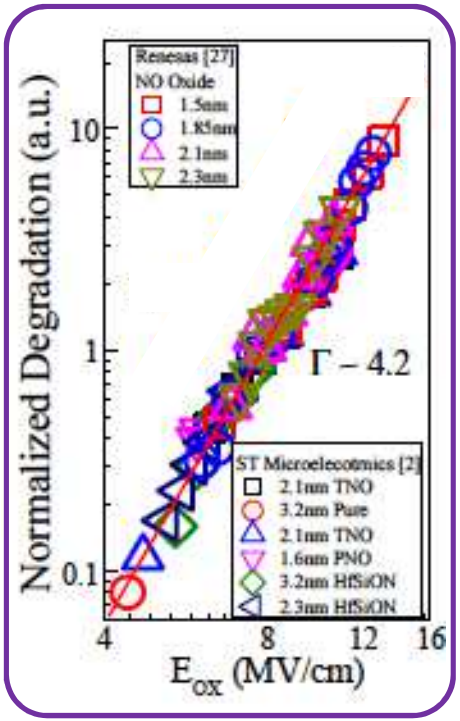


BTI Degradation

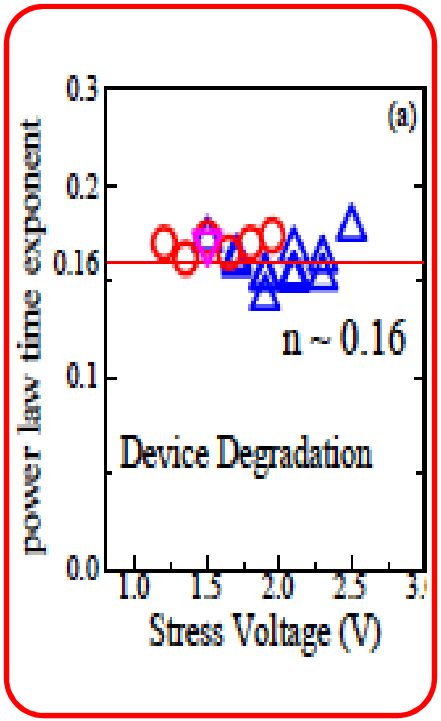
- BTI mean degradation
  - Universal behavior
- Scaling model for mean degradation



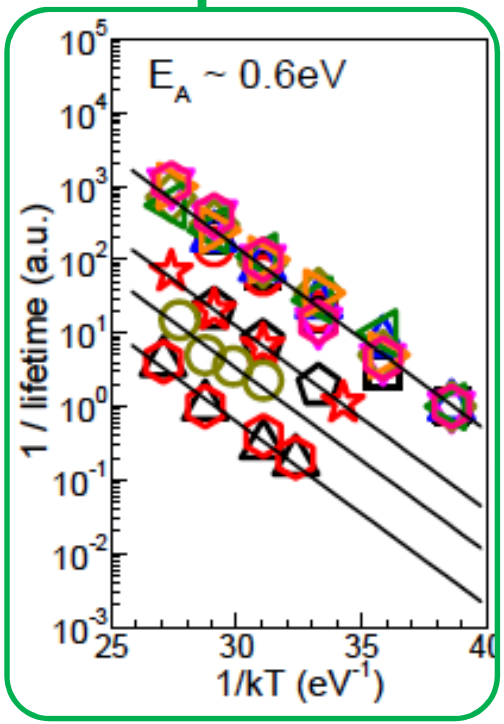
Oxide Field



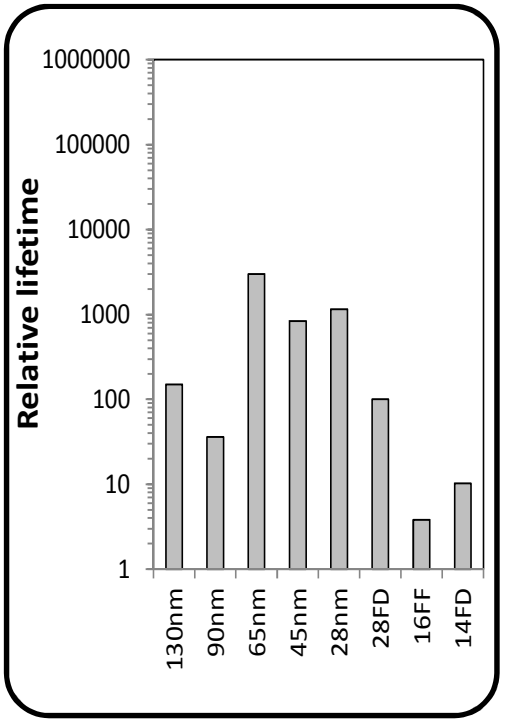
Time



Temperature



Lifetime



Source : Mahapatra et al., *IRPS*, 2014

Source : Ramey et al., *IRPS*, 2015

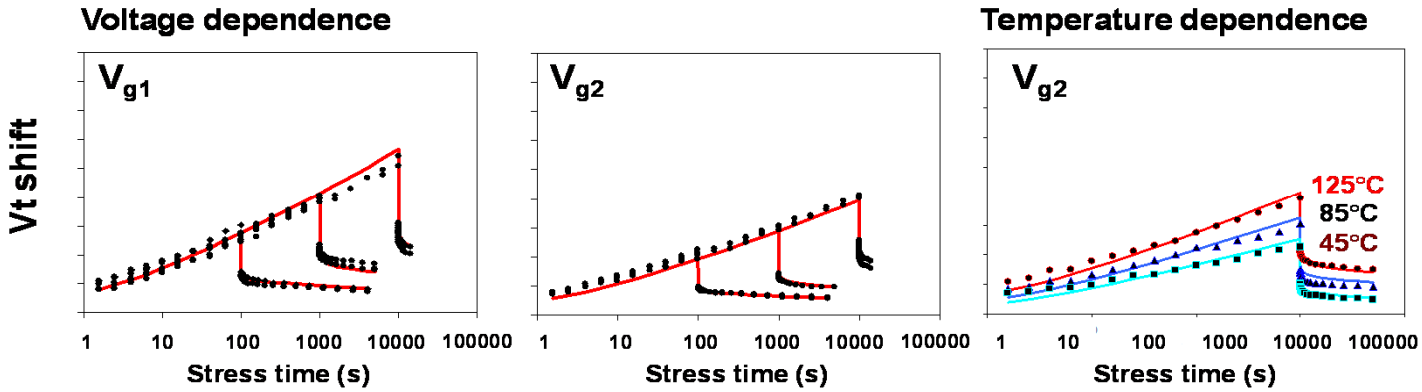
BTI Recovery

- BTI recovery modelling is a must-have feature

pMOS NBTI

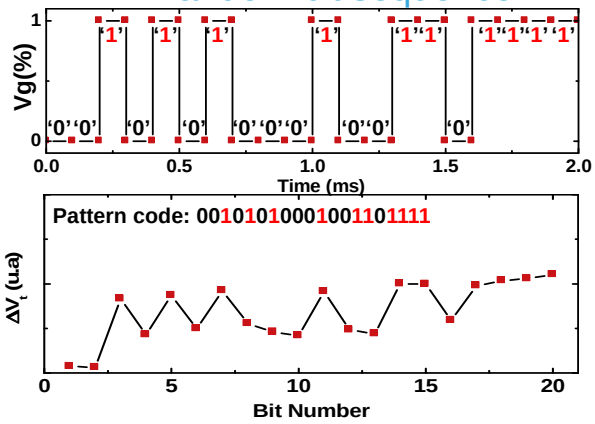
HK/MG techno

Stress/Recovery modeling

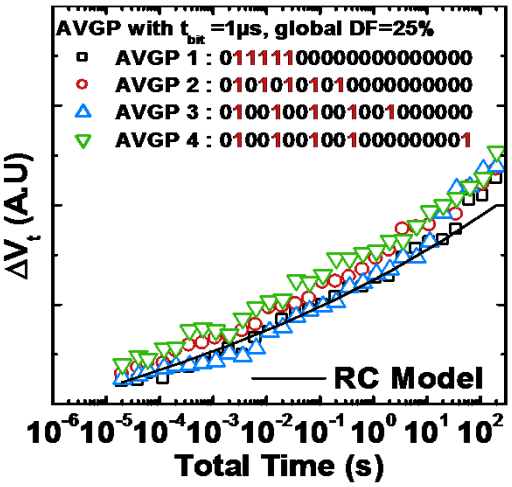


- BTI degradation is modulated by activity duty cycle

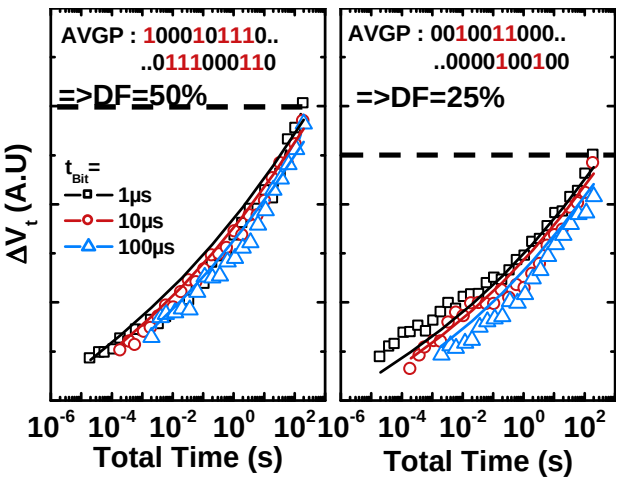
- PRBS technique:
  - Fast measurement (1us)
  - Random bit sequence



Bit sequence independence



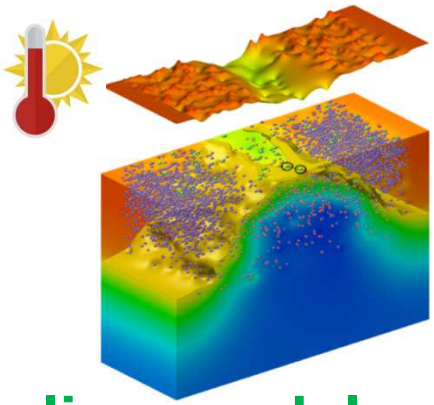
Duty cycle dependence



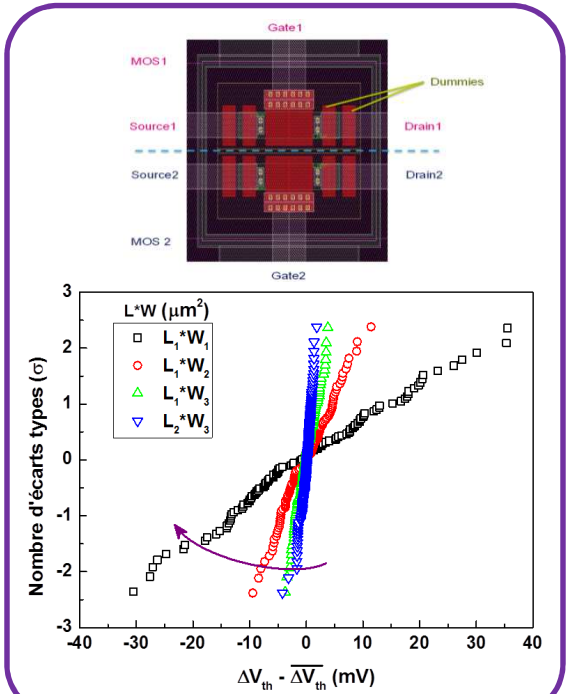
Source : Subirats et al., *IRPS* ,2014

BTI-induced mismatch

- BTI induces additional variability
- Scaling model for BTI-induced mismatch



BTI-induced mismatch

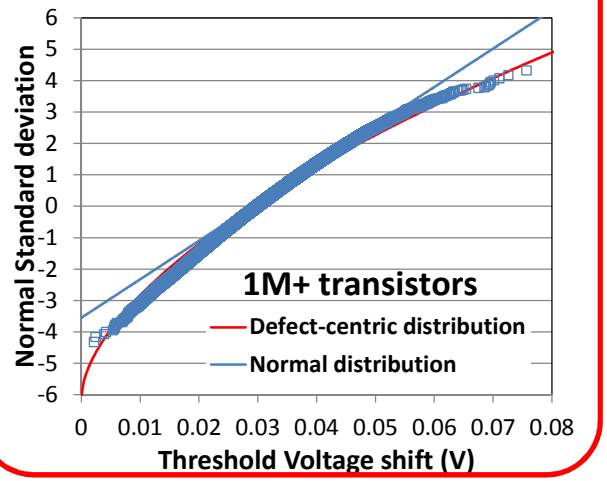


Defect Centric model

Poisson distribution of the average number N_t of defects

Exponential distribution of ΔV_{th} steps due to a single defect

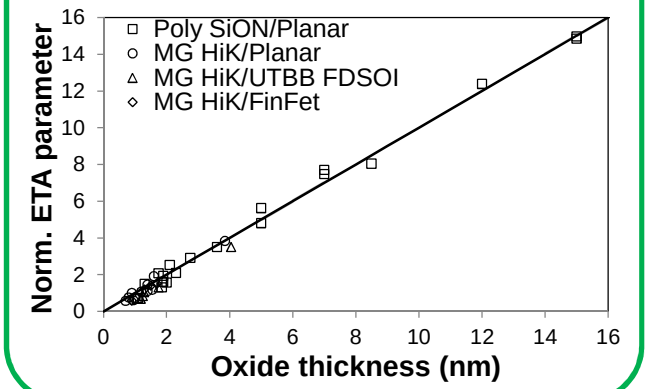
$$CDF(\Delta V_{th}) = \sum_{m=1}^{\infty} \frac{e^{-N_t}.N_t}{m!} \left(1 - \frac{\Gamma(m, \Delta V_{th}/\eta)}{(m-1)!}\right)$$



Scaling model

Average impact/defect

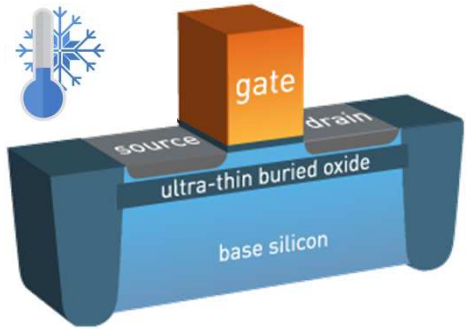
$$ETA = \frac{\sigma^2_{\Delta VT}}{2\overline{\Delta VT}} = \frac{q}{2.\epsilon.\epsilon_0}.\frac{EOT}{WL}$$



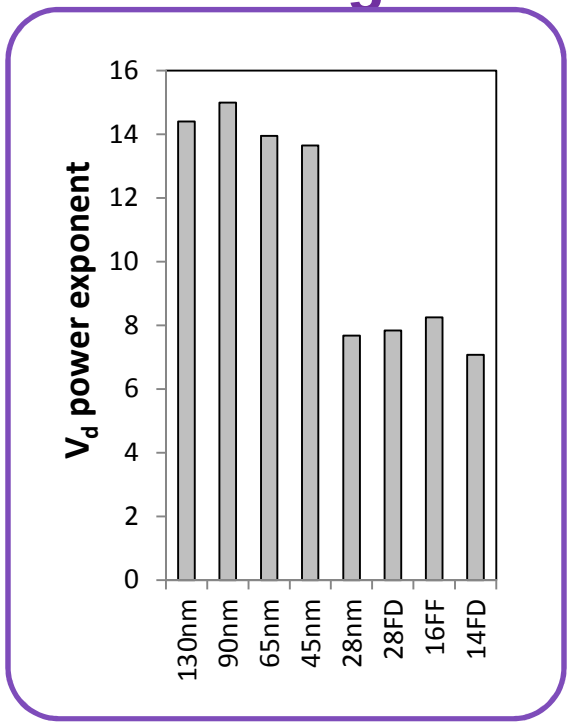
Source : Angot et al., *IEDM* ,2013
Source : Huard et al., *IRPS* ,2015

HCI Degradation

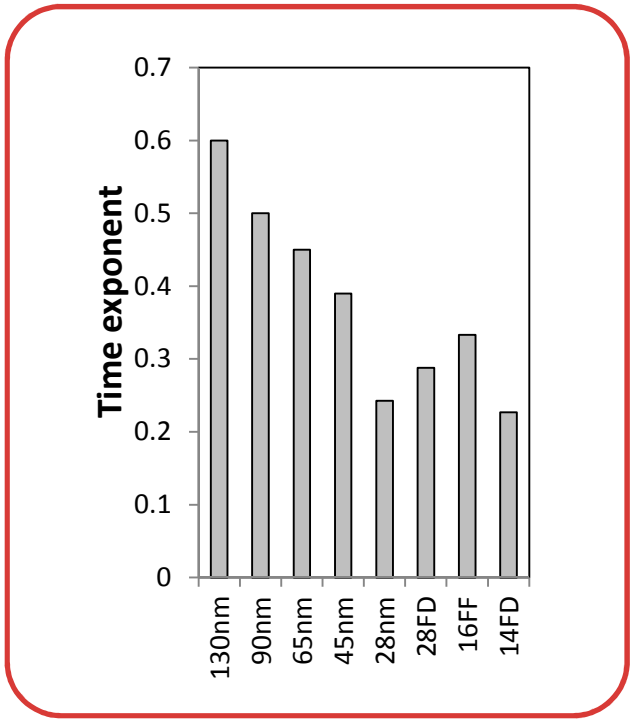
- HCI mean degradation
  - Predictable behavior
- Scaling model for mean degradation



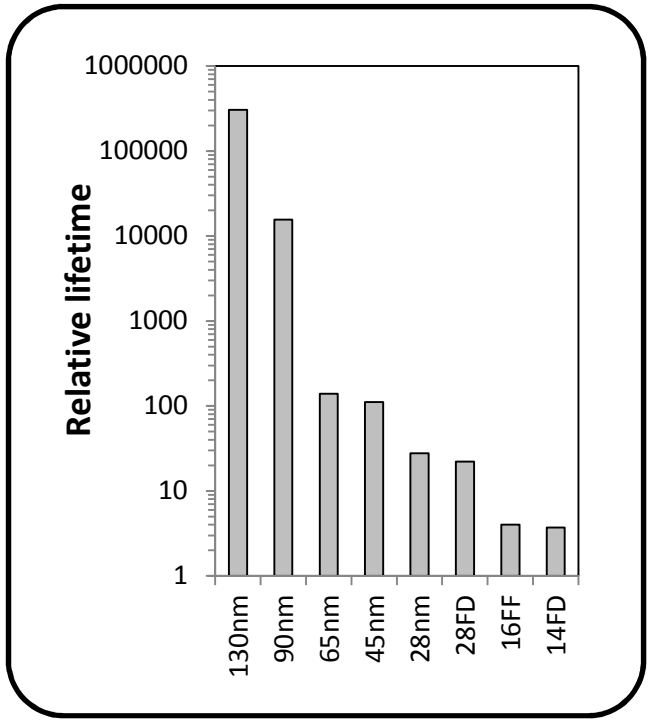
Voltage



Time



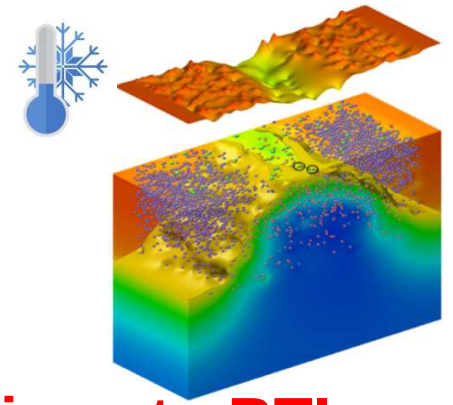
Lifetime



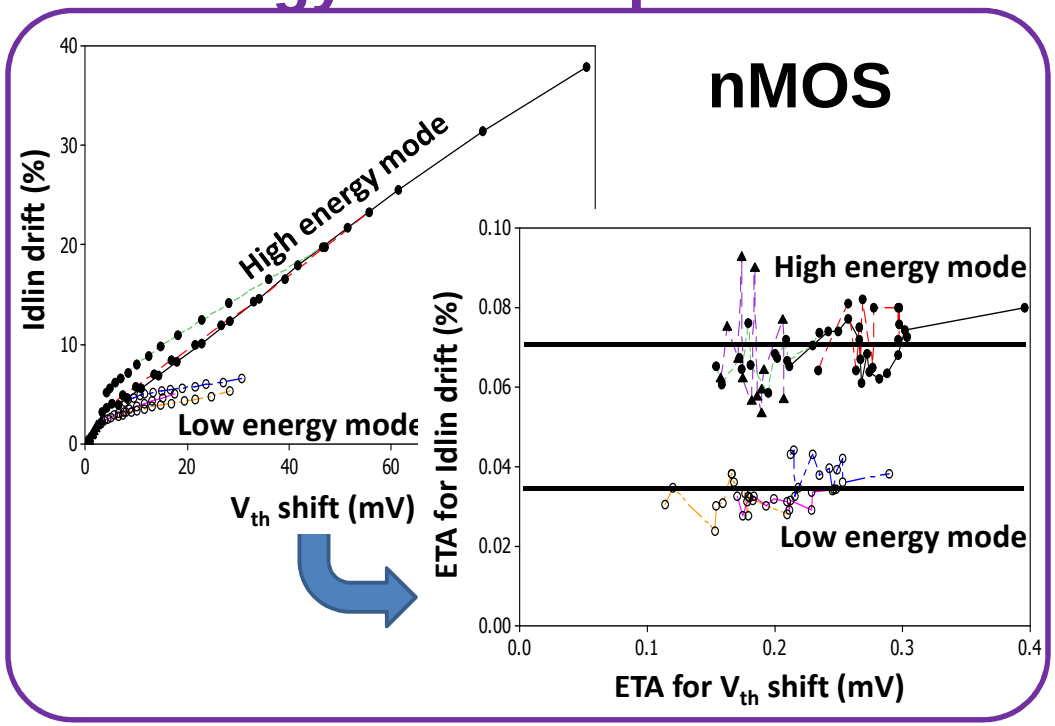
Source : Cacho et al., *IIRW*, 2014 and references therein

HCI-induced mismatch

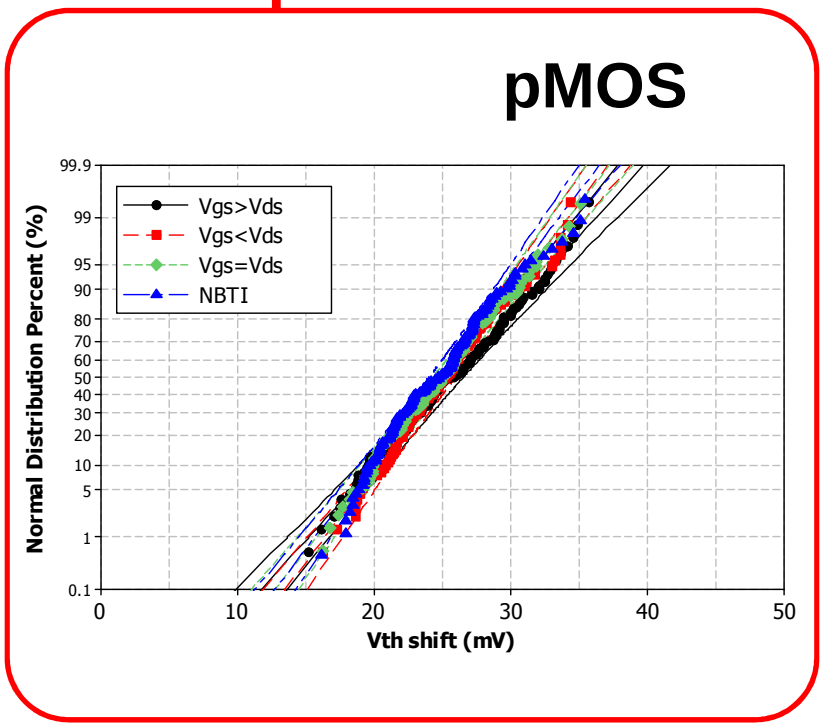
- HCI induces additional variability
- Scaling model similar to BTI degradation
  - Amplitude depends on energy mode



Energy mode dependence



Comparison to BTI

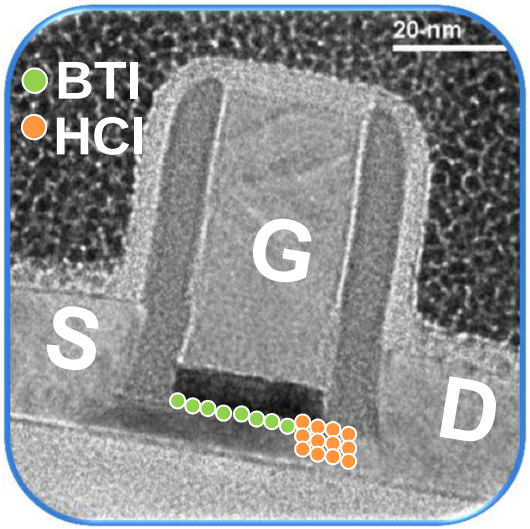


Source : Huard et al., *IEDM*, 2015

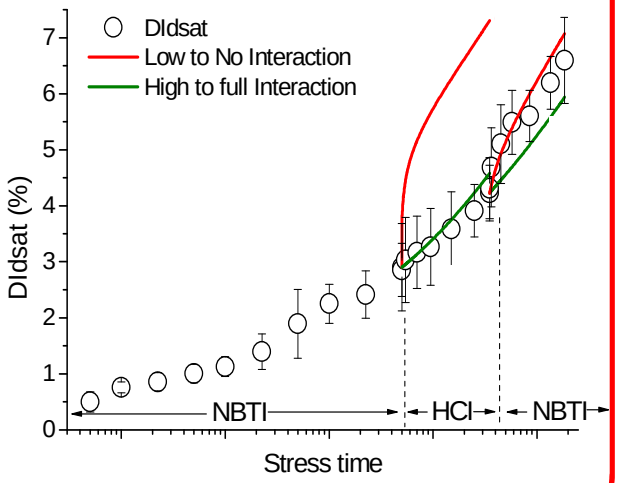
BTI/HCI degradation coupling

- Foundry qualification: BTI and HCI independent mechanisms
- BTI/HCI competition for the same defect creation sites
- Additive degradation exhibits pessimistic results

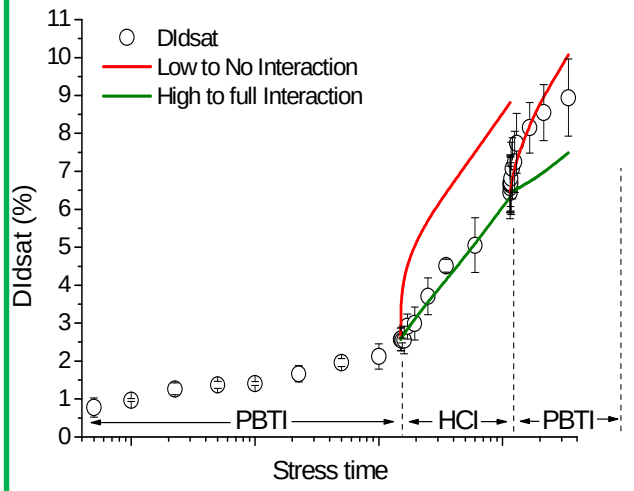
Defect sites competition



PMOS



NMOS



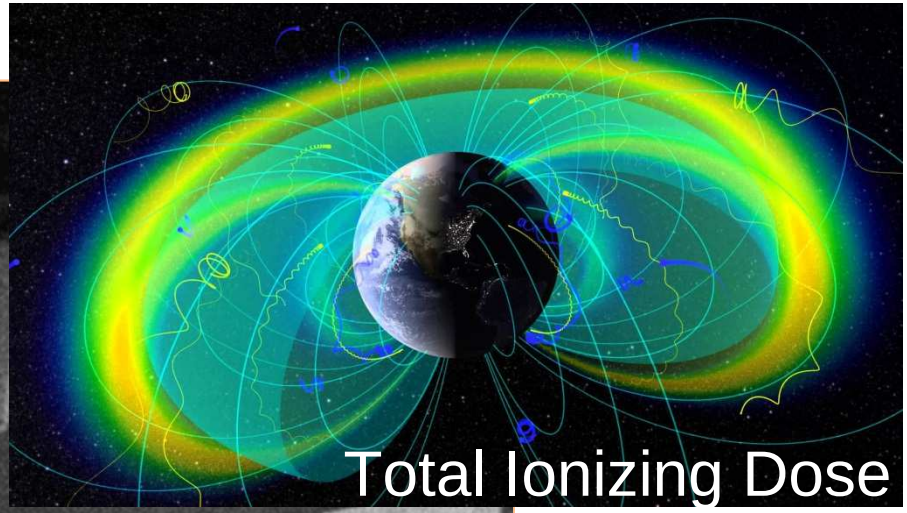
Source : Cacho et al., *IRPS* , 2014

Degradation Mechanisms

$$\vec{J}_{flow} = c\frac{eD}{kT}Z^{*}\rho\,\vec{j}$$

e-

Electromigration

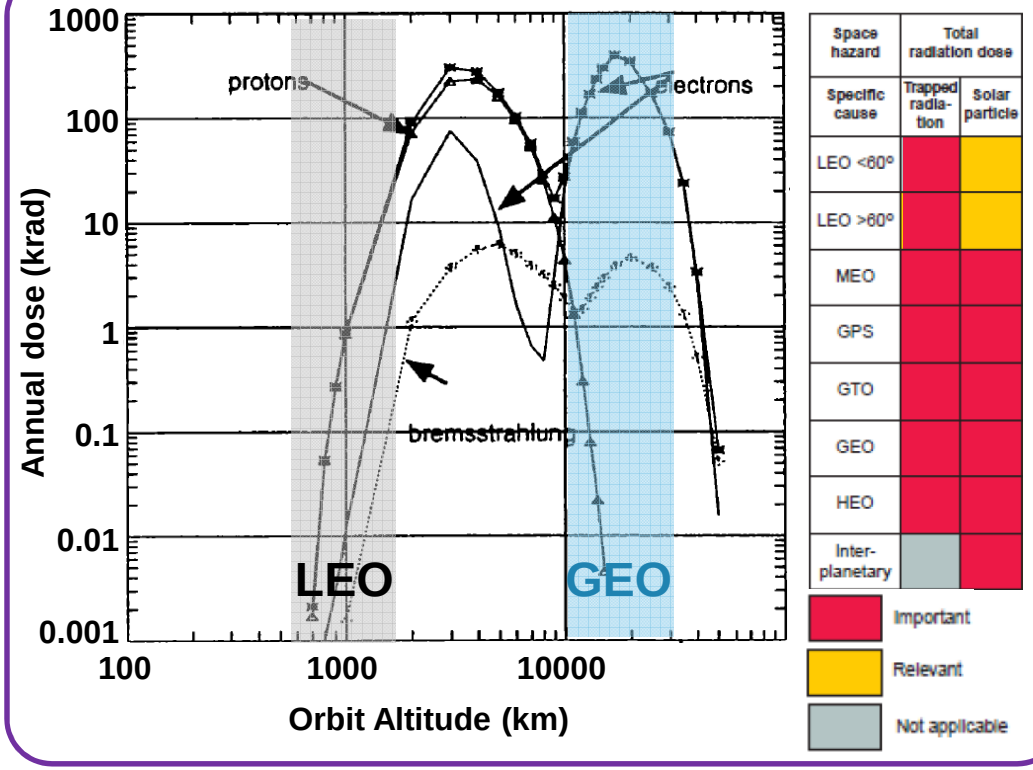


Total Ionizing Dose

TID degradation

- FDSOI transistors more sensitive to TID than bulk one due to buried oxide layer
- Positive charge build-up in buried oxide layer may lead to:
  - Threshold voltage shift due to electrical coupling with front gate → **observed**
  - Formation of back-channel leakage path → **not observed** due to high quality interface

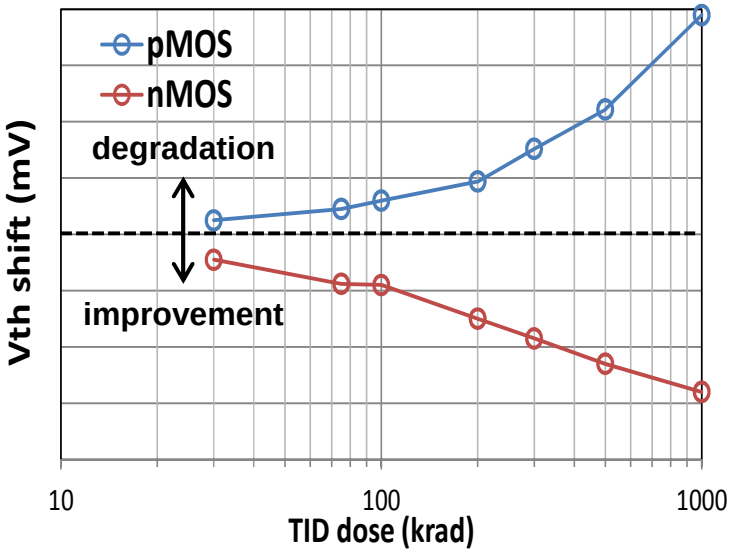
TID and space environment



Threshold Voltage shifts

Both nMOS and pMOS V_{th} shifts in same direction
- pMOS degradation
- nMOS improvement

Amplitude vary between nMOS and pMOS



Source: Space Environment Analysis, Experience and Trends

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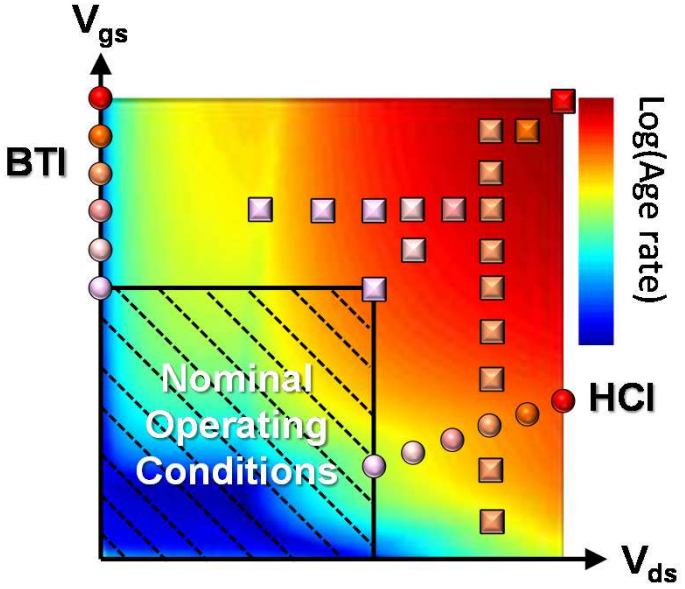
Device Reliability modelling

- Defect Generation Rate:
  - Physics-Of-Failure (PoF) approach
  - Model all reliability modes all over the $V_{gs}/V_{ds}/V_{bs}$ space
  - Stress renormalization using AGE rate function

$$\frac{\Delta P}{P} = K(AGE_i)^n \; where \; for \; mode \; i, AGE_i = f(V_{gs}, V_{ds}, V_{bs}, T)g(L, W)$$

  - ST-specific compiled C code:
    - compatible with major CAD vendors for Spice and FastSpice simulations through API usage
    - ST-specific equations for improved accuracy

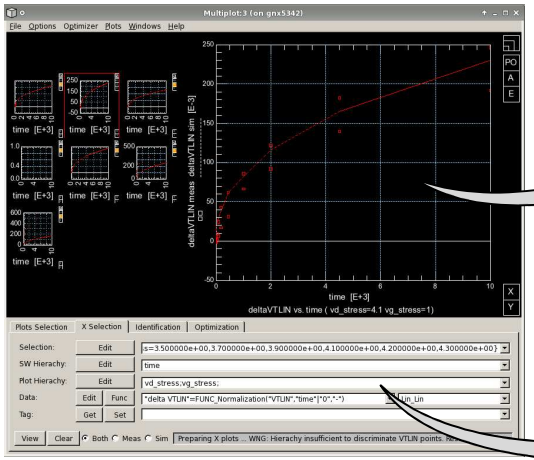


Source : Reliability subgroup in Compact Modeling Council

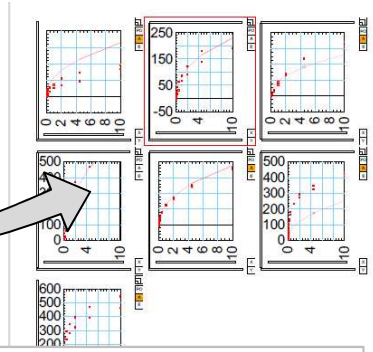
Framework strategy / Capability	Application Programming Interface (UDRM, MOSRA, RelXpert)	Wrapper style flow (TSMC Modeling Interface) (TMI2)	External wrapper program (VerilogA module)	Built-in simulator (equation written in simulator language)	End-Of-Life Models (aged SPICE corner)
Separation ageing flow from SPICE flow	Yes	No	Yes	No	No
Integration effort	No external .lib for ageing parameter and C code	Additional integration TMI2 dedicated options are written in .model	Additional scripting for files postprocessing	Additional integration steps	No
Ease at use	Yes	Yes	No additional postprocessing	Yes	Yes
Deployment in industrial flow	Yes	Yes	Limited due to additional postprocessing scripting	Yes	Yes
Equation implementation capability	Complex function capability to implement recovery contribution	Complex function capability to implement recovery contribution	Complex function capability to implement recovery contribution	Limited by CAD-vendor functions	No
Run time	Fast compiled c-code	Fast compiled c-code	Medium compiled c-code + Perl script	Slow interpreted function	Fast
Simulation capability	Very High 1M+ Xtor (SPICE-FastSPICE)	High Up to 100K Xtor (SPICE)	Low (memory limitations due to postprocessing)	High Up to 100K Xtor (SPICE)	Very High 1M+ Xtor (SPICE-FastSPICE)
Confidentiality of ageing equation	Yes compiled c-code	Yes compiled c-code	Yes compiled c-code	No Equations in netlist	No Equations in models

Reliability models Flow

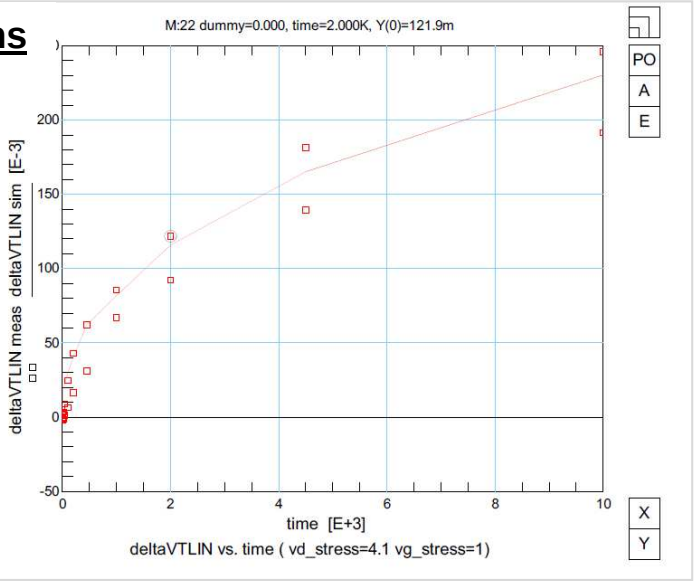
- Robust optimization
- Automated reporting



Various stress conditions

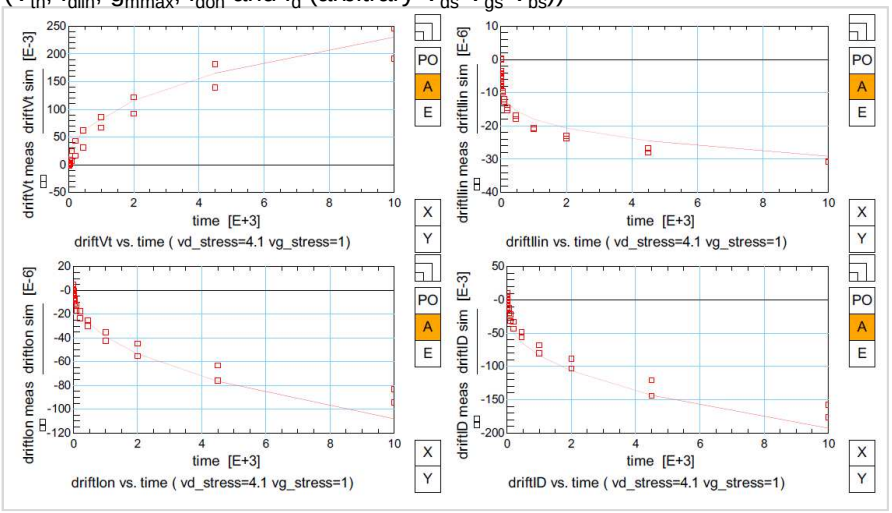


- Selection data
- Filtering
- Plot and sweep hierarchy
- Data to plot
- Selection graph for fit

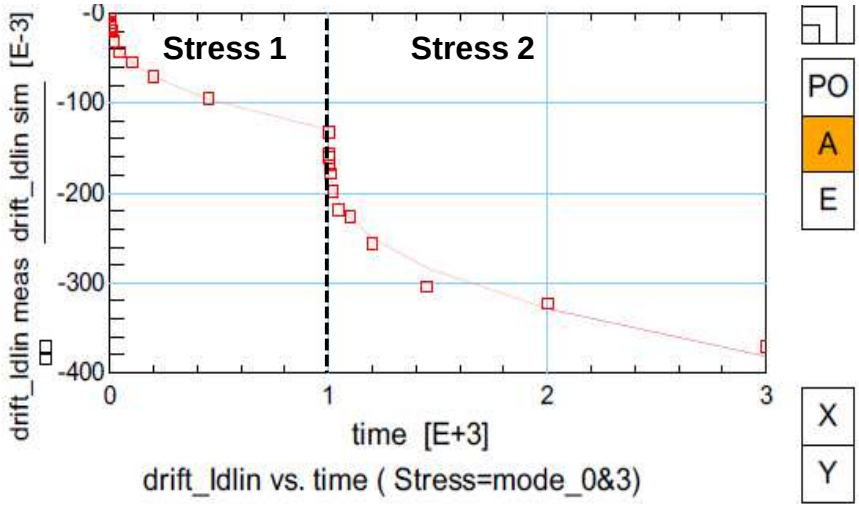


Various device parameters

(V_{th}, I_{dlin}, g_{mmax}, I_{don} and I_d (arbitrary V_{ds} V_{gs} V_{bs}))

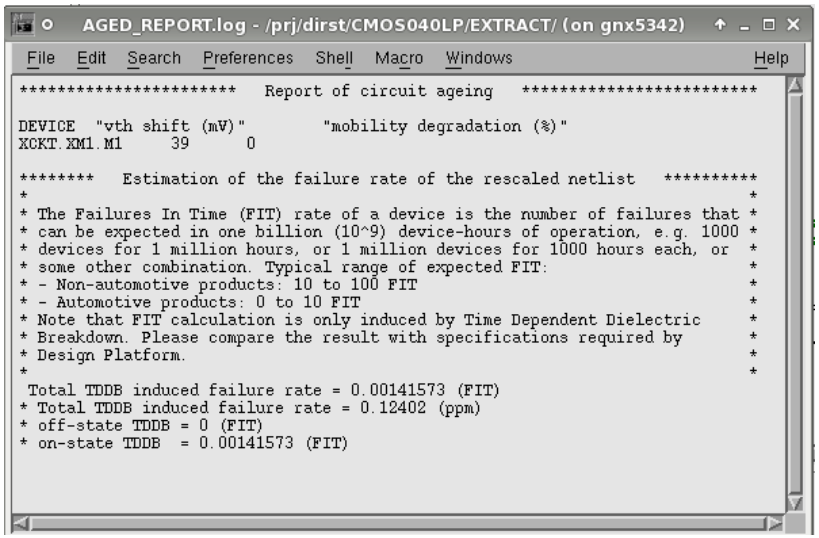


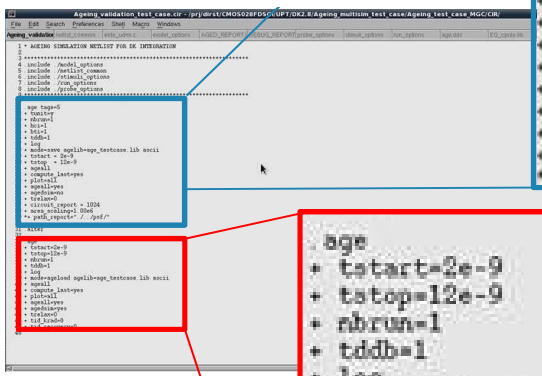
Interaction between modes

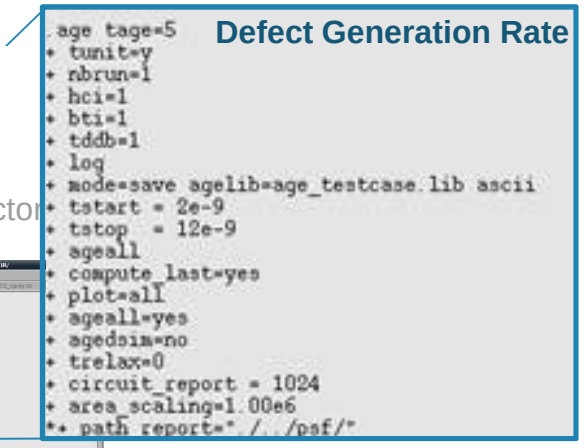


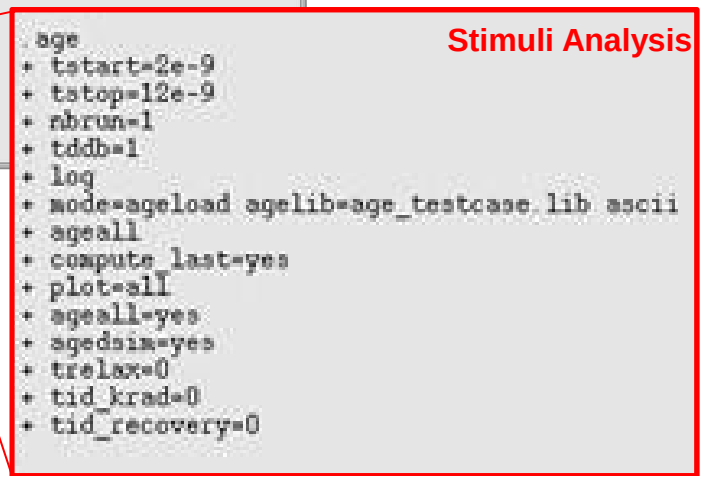
Reliability simulations inputs and outputs

- Inputs:
  - Dedicated switches for degradation mechanisms' selection (BTI/HCI/TDDB) for stimuli analysis
  - Fully scalable model in time with widened validity range (>WLR)
  - Dedicated TID switch with scalable dose model including recovery feature
- Outputs:
  - All informations stored in AGED_REPORT.log file:
    - Drift informations for all devices
    - TDDB failure rate informations (also available in the terminal in prompt)
  - TDDB model implemented in addition with BTI/HCI to address:
    - Transient and static violation of V_{gs}/V_{ds}, time to breakdown determination
    - Failure rate of the circuit (FIT and ppm calculation) assuming a scaling factor









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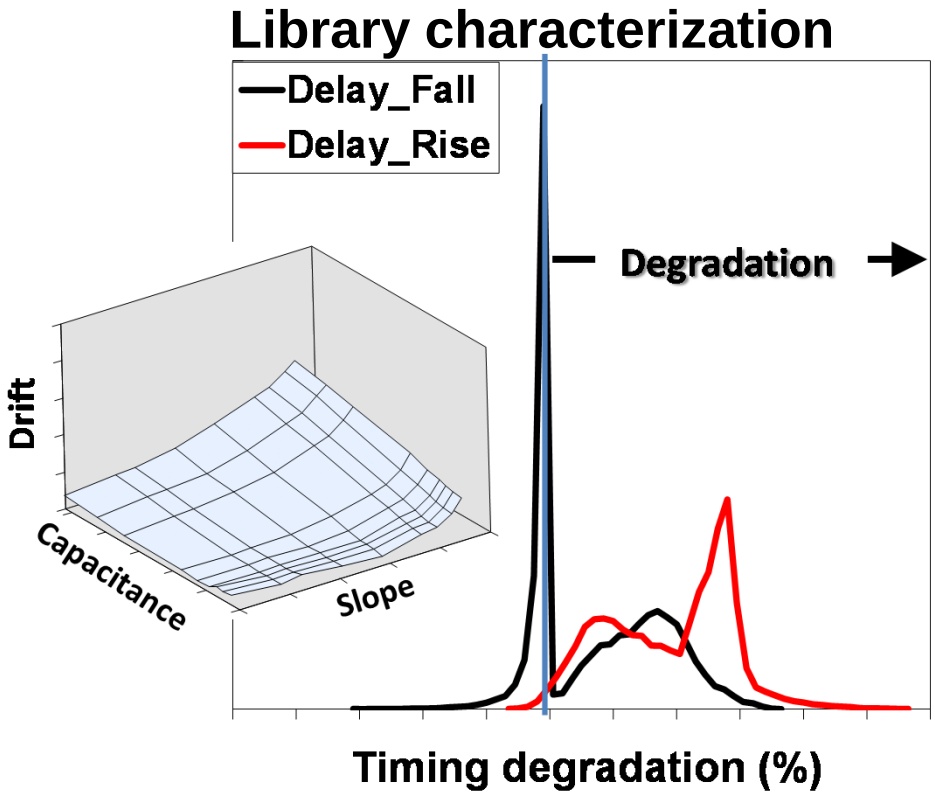
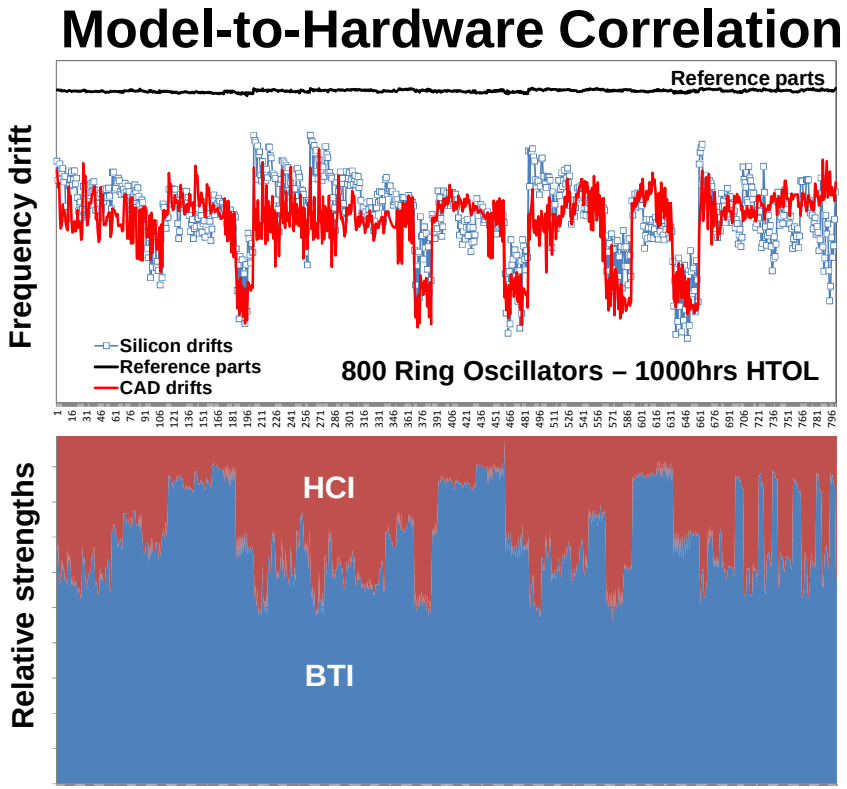
Library characterization

- Aged corners in library:
  - Another process corner characterized using reliability models
  - Copes with intercell degradation sensitivity and duty cycle dependence
- Good Model-to-Hardware correlation

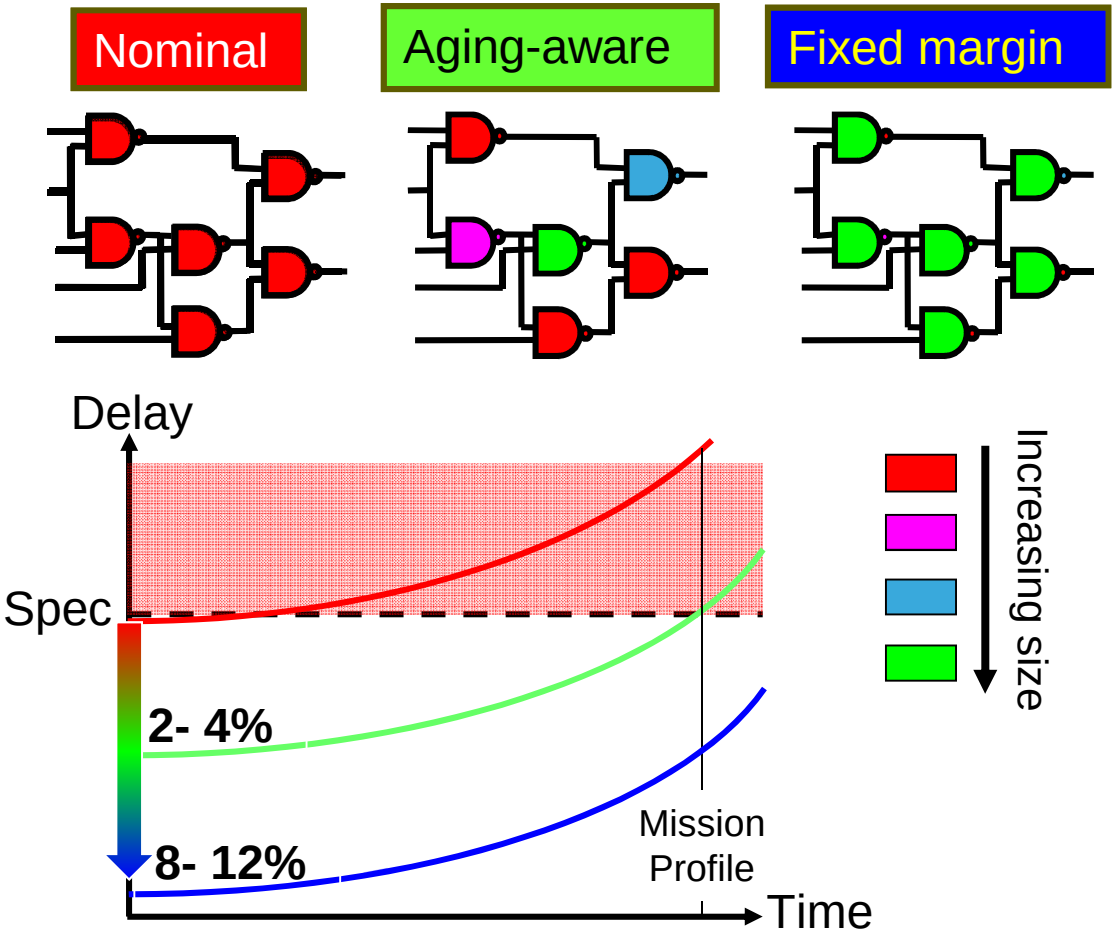


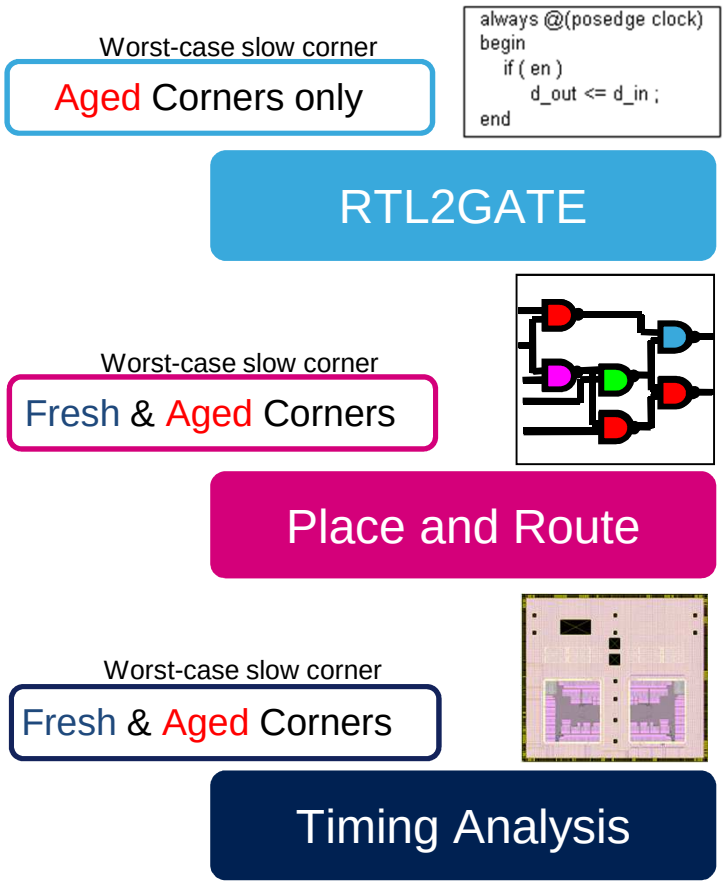


Source : Huard et al., *IEDM*, 2015

Digital Design for Reliability Flow

- Digital design hardening flow:
  - Aging-aware selective gate replacement
  - DFR approach to optimize reliability/area/power trade-offs

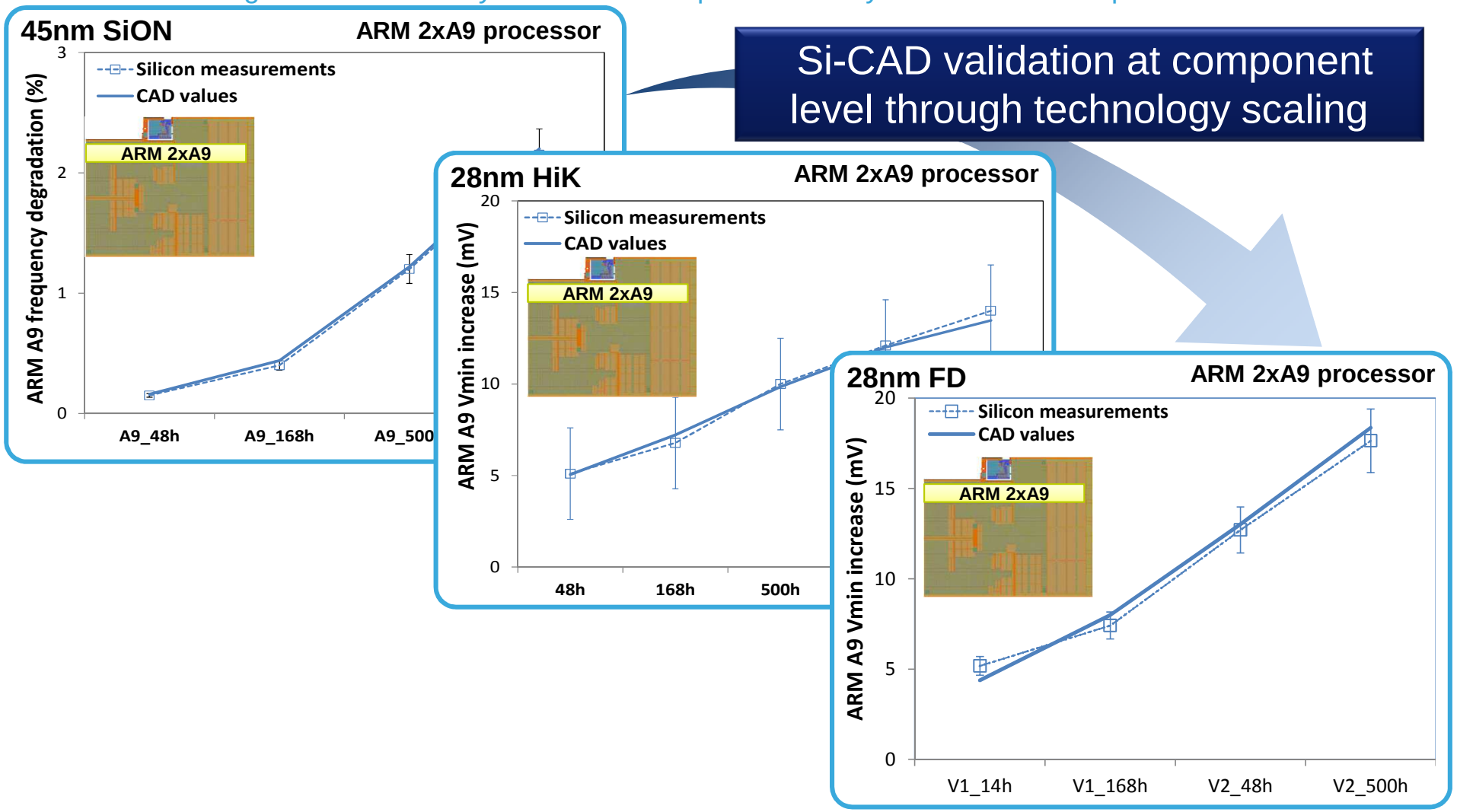




Source : Huard et al., *IEDM*, 2015

Predictive DFR flow

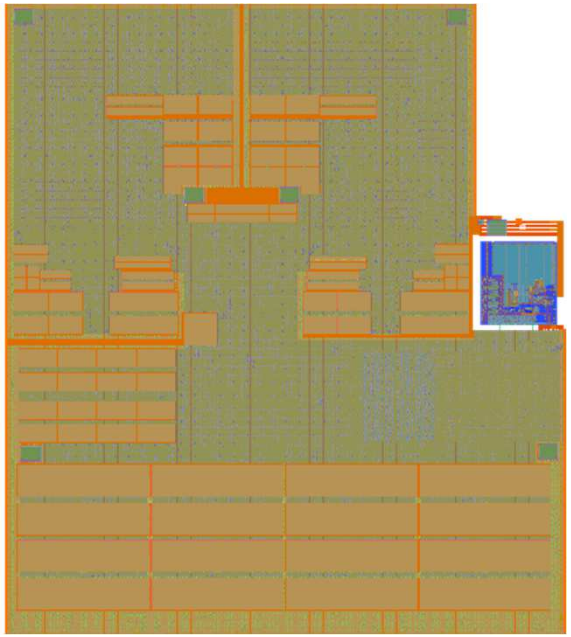
- DFR flow enables:
  - Predictive degradation at System-level for concurrent engineering
  - Getting rid of full reliability trials on all components for System Failure Rate predictions



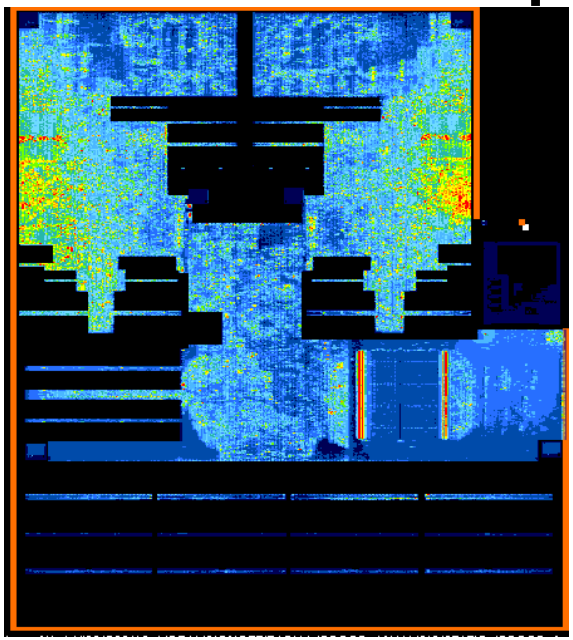
Predictive EMG checker flow

- EMG checker flow:
  - SOC-level CAD solutions with wide ecosystem
  - Accurate design rules to allow MHC on complex blocks

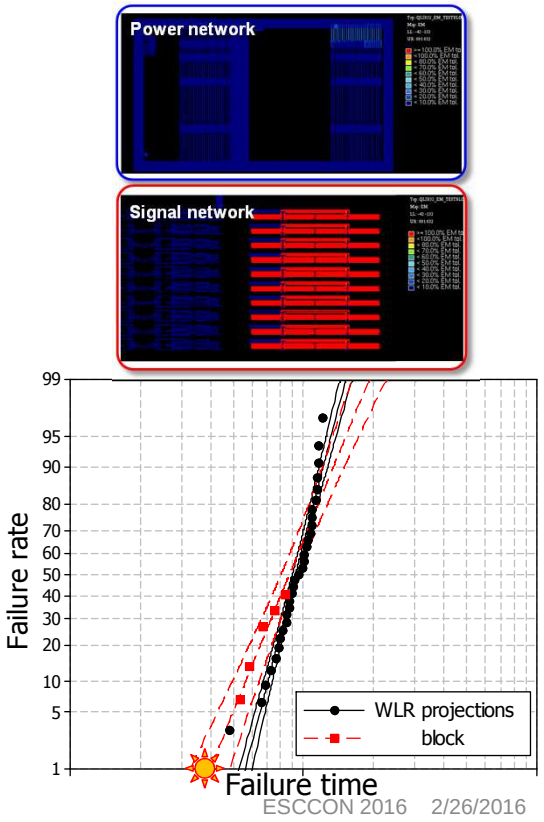
Layout view



EM violations map

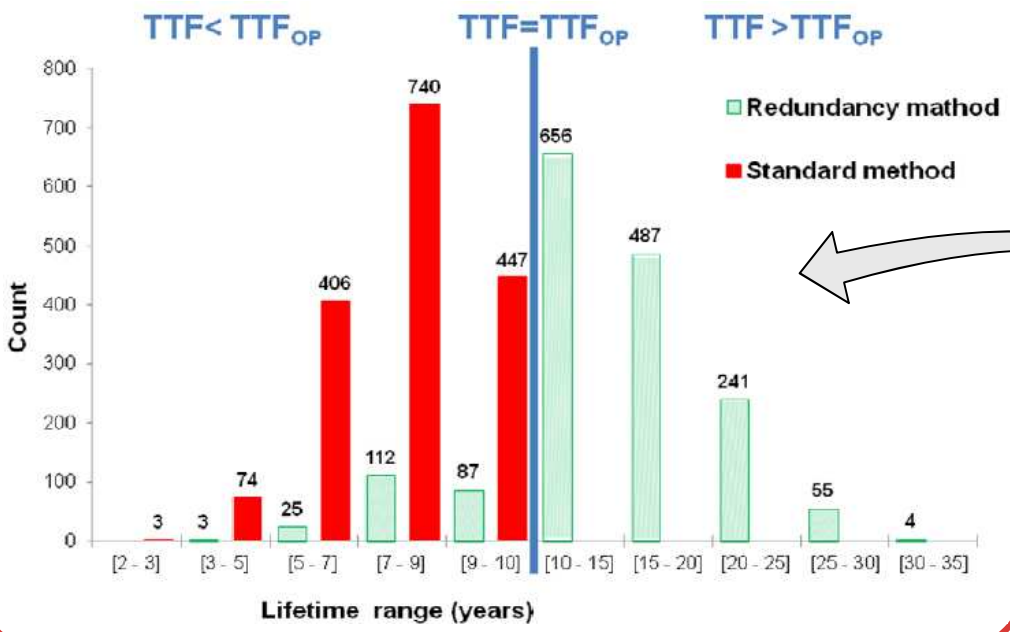


Accurate MHC



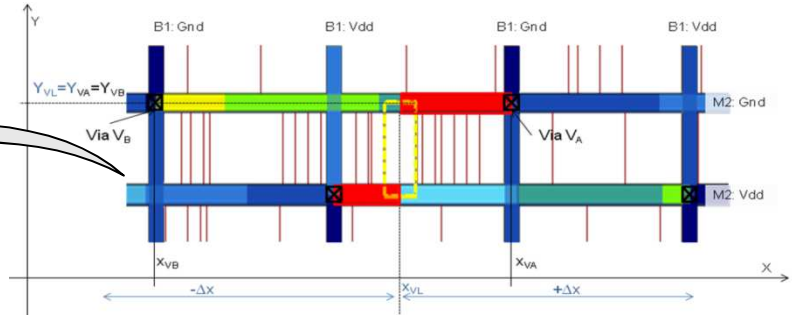
EMG redundancy/robustness methods

EMG violations and redundancy effects

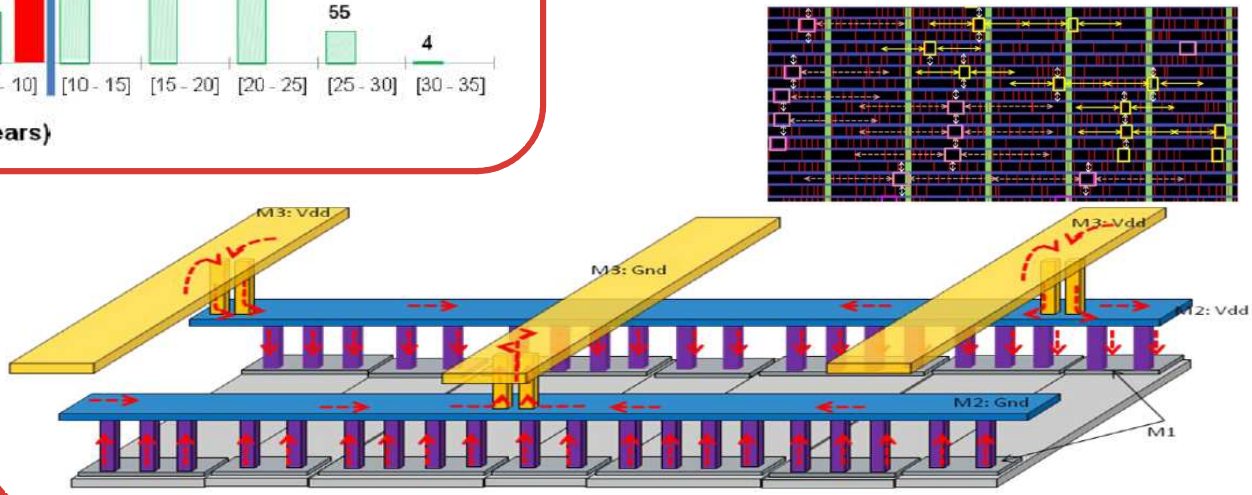


Redundancy/Robustness methods

- **Redundancy current paths**
  - **Mitigate EMG and increase TTF**



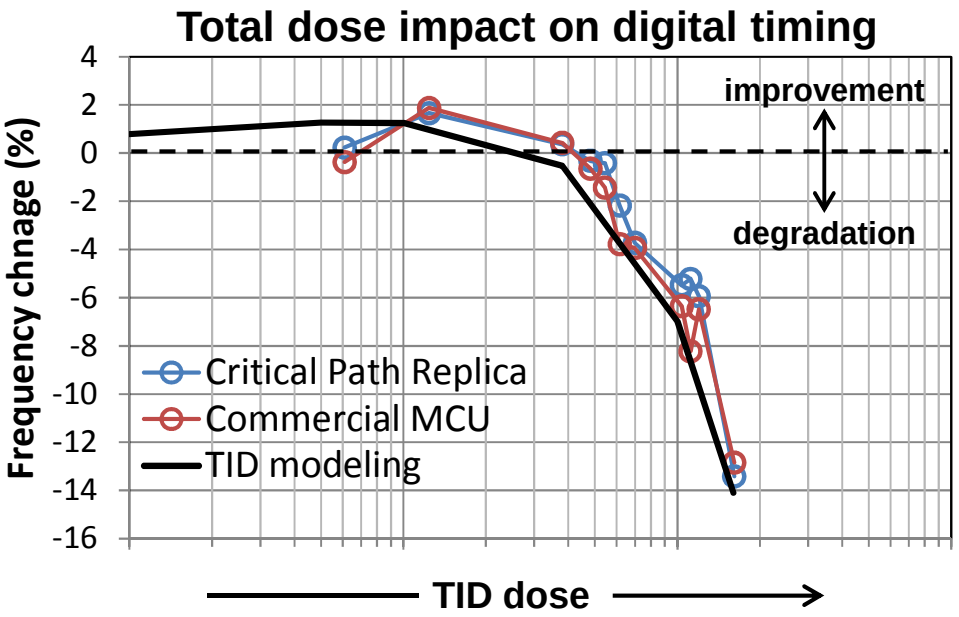
- **Dynamic Halo on CT cells**

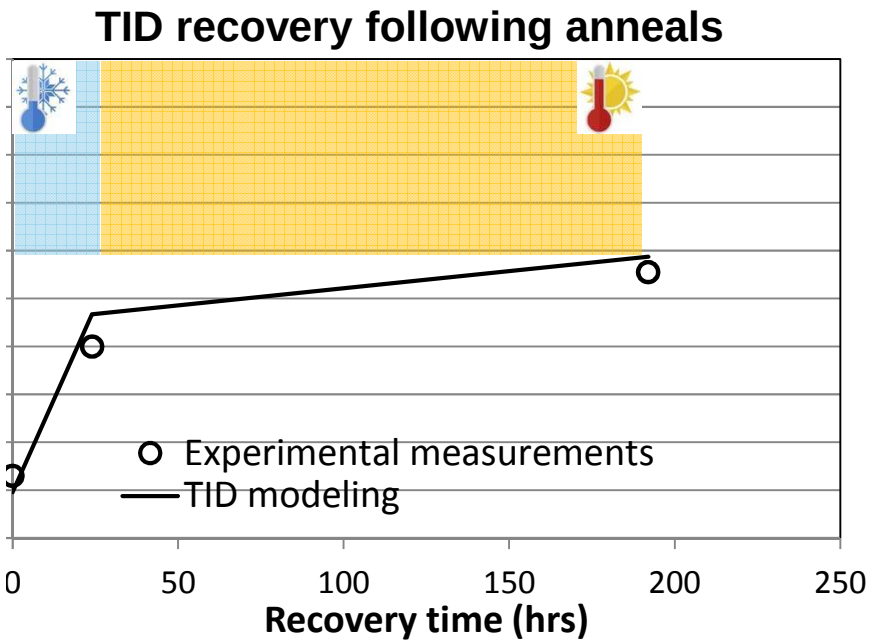


Source : B. Ouattara, *ITC*, 2013
Source : B. Ouattara, *Microelectronics Reliability*, 2014

Predictive TID modeling impact

- DFR flow enables:
  - Predictive degradation at both circuit (Path Replica) and System-level for concurrent engineering
  - Getting rid of full reliability trials on all components for System Failure Rate predictions





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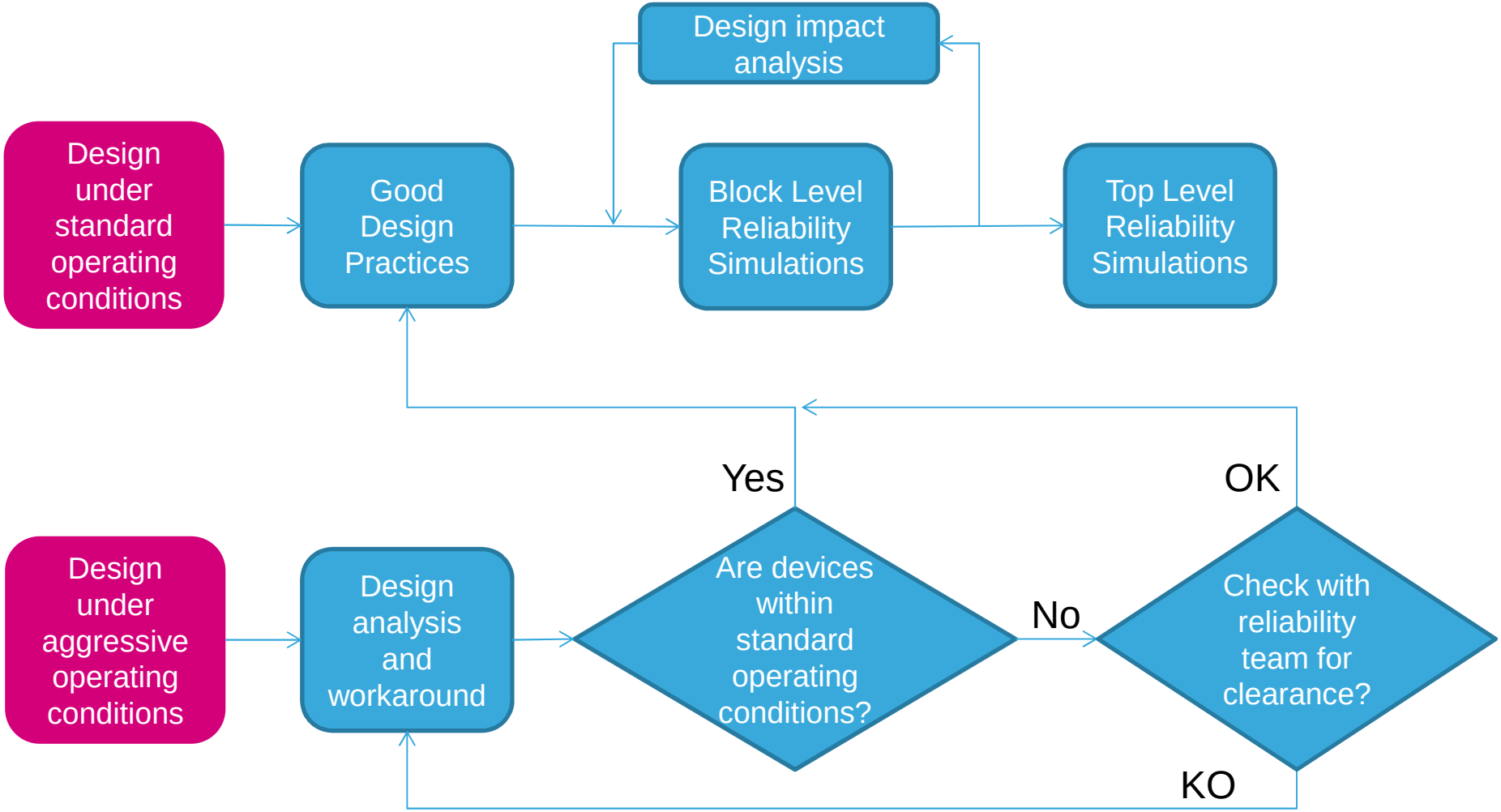
Industrial good design practices

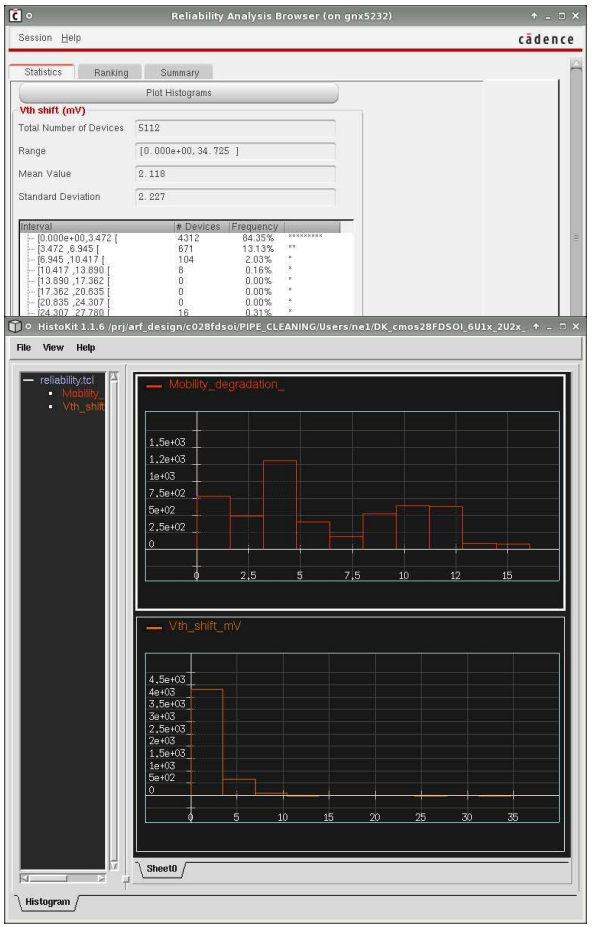
- Reliability insurance:
  - Analog IPs reliability guaranteed on worst-case mission profile by good design practices



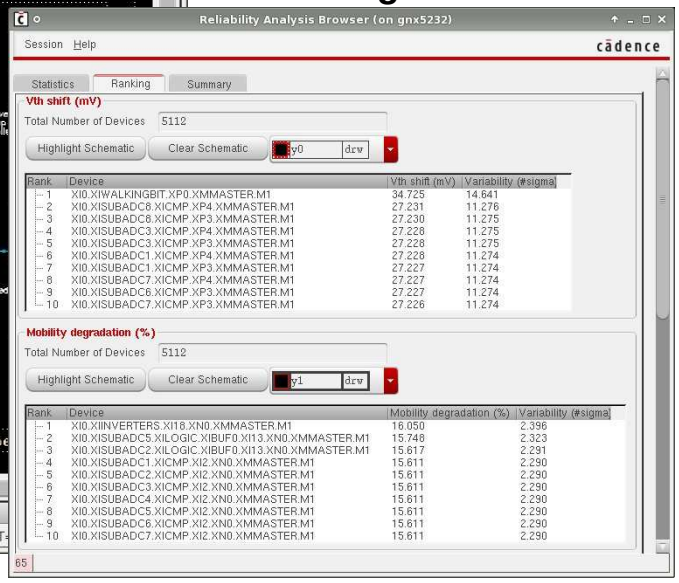
Industrial design for reliability framework

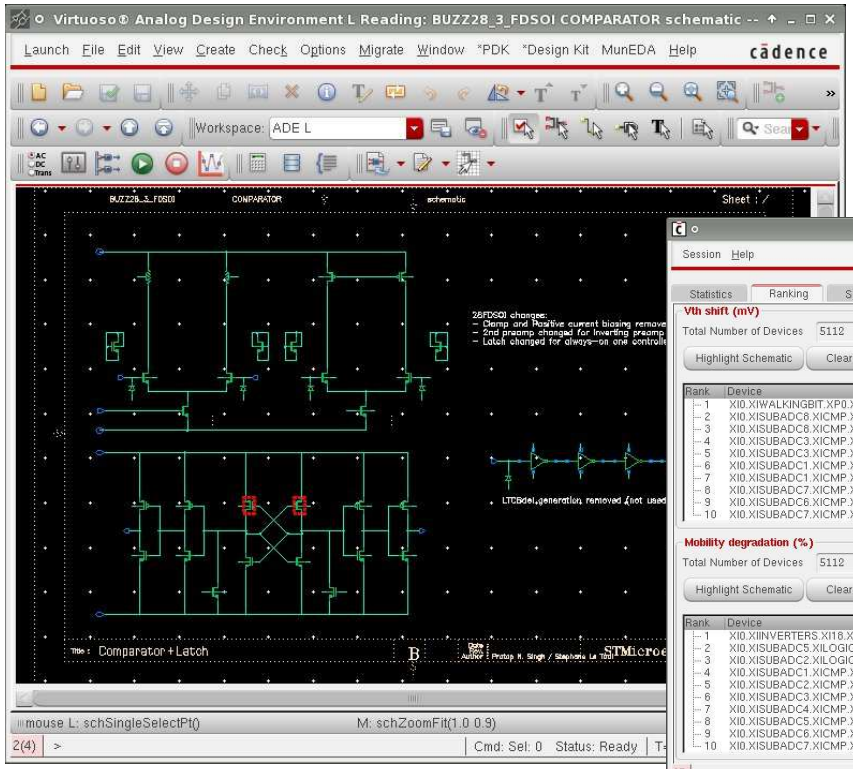
- Enhanced design environment to support design good practices:
  - Reference design environment with reliability-enhanced features enabled by reliability models
    - Degraded MOS highlight
    - Device Degradation Pareto
    - Device Degradation Histogram

Device Degradation Histo



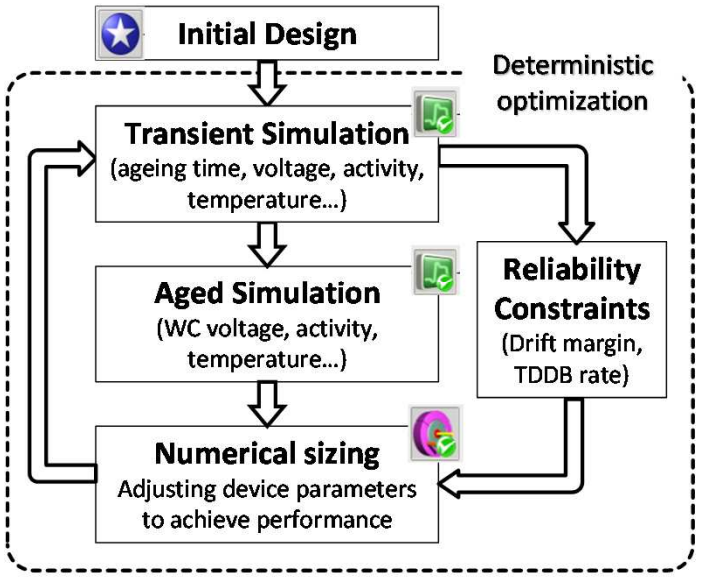
Device Degradation Pareto

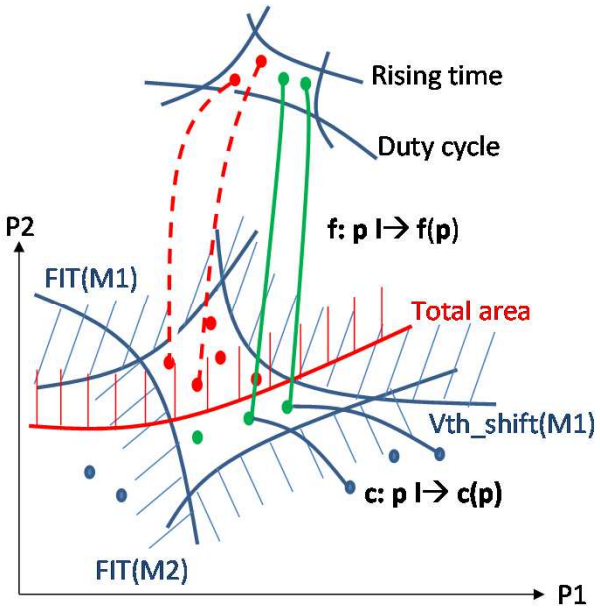


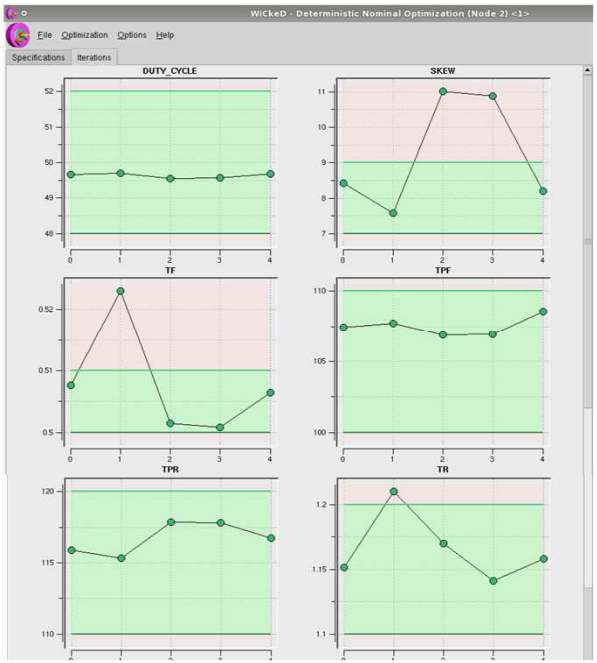


Automated sizing for reliability hardening

- Enhanced design tool for automated transistors' sizing for reliability:
  - Few optimization loops needed for optimal design
  - Average 10x gain in design time



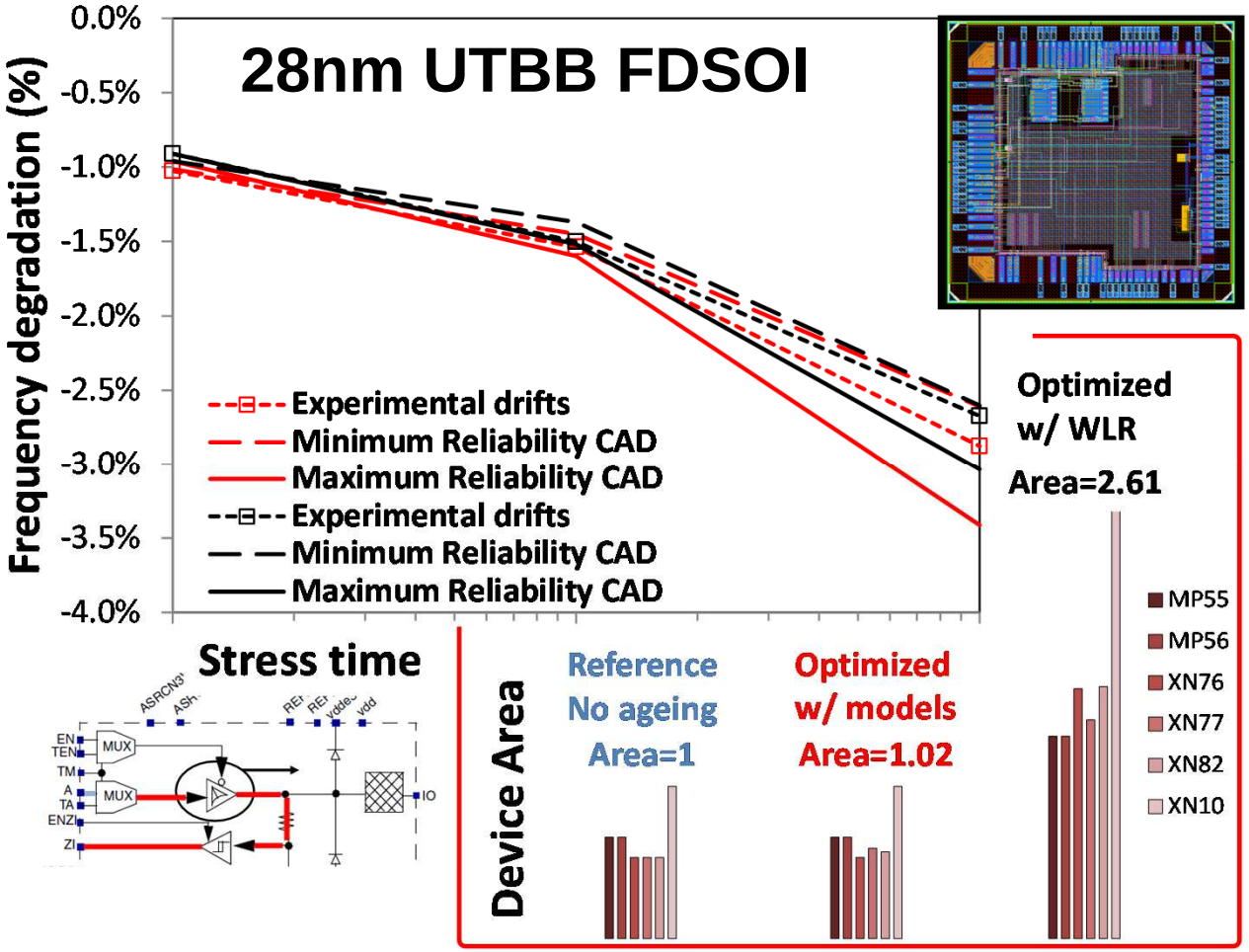




Source : Huard et al., *IRPS* ,2015

Automated sizing for reliability hardening

- Silicon-proven efficiency in advanced CMOS nodes to achieve:
  - More than 2x area savings compared to WLR rules
  - Similar reliability observed



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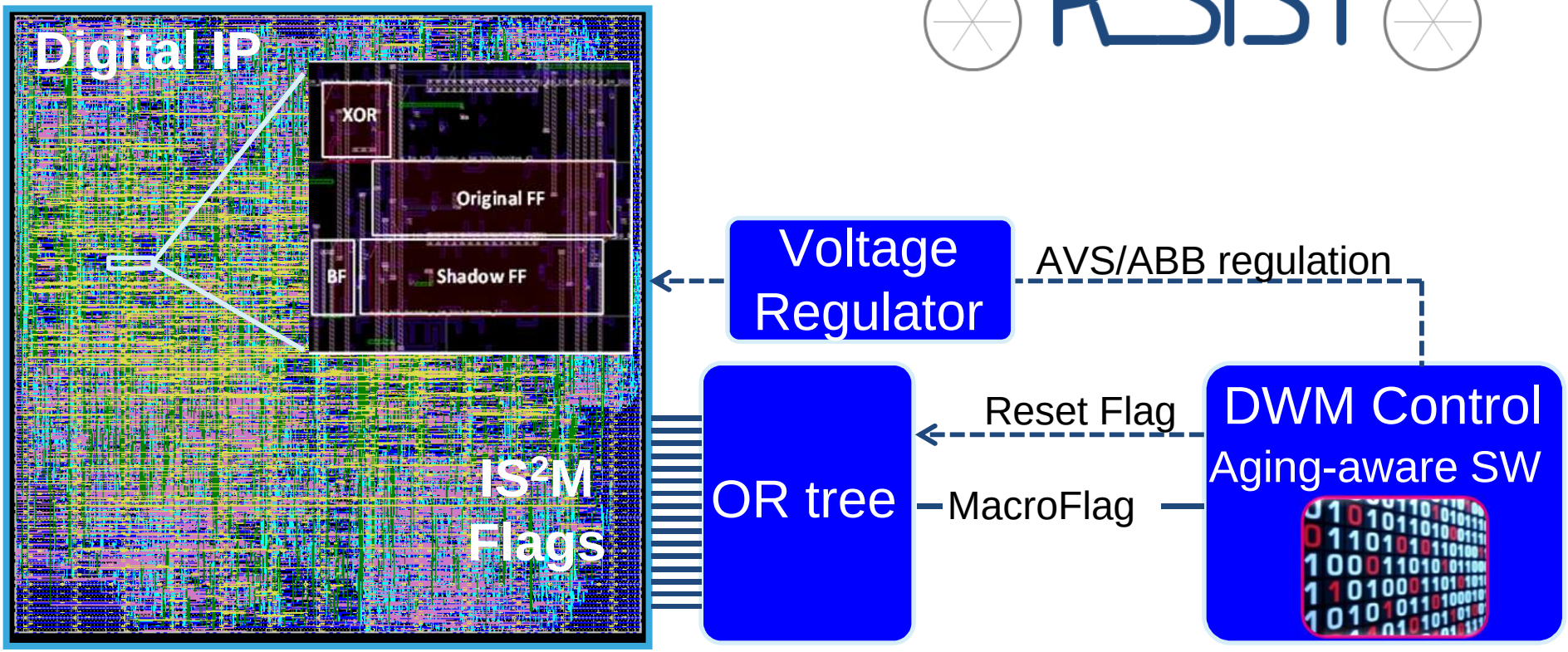
SPACE products in advanced CMOS nodes

- 50 years of scaling rise reliability challenges
  - New device architectures
  - Large range of interacting physical mechanisms
- Opportunities: Reliability-aware design flow
  - Known scaling rules for degradation modes
  - Production CAD ecosystem to push knowledge upwards into design flow
  - Entering Golden Age of design hardening flow
- Perspectives:
  - Lots of R&D efforts towards Resilient digital designs
  - Key enabler to cope with High-Reliability markets

Resilient digital designs

- European initiative towards resilient digital designs
- Dynamic Wearout Management inc. in-situ monitors and regulation



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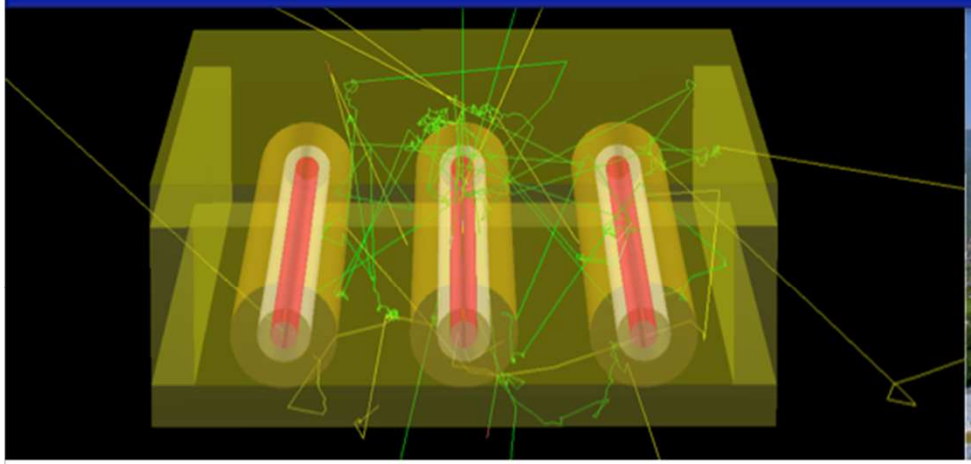
"High Reliability is our concern. We apply science to detect, mitigate and anticipate reliability issues"

Radiation Effects and Electrical Reliability Joint Laboratory



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