INSERTION OF FLIP CHIP IN SPACE SYSTEMS

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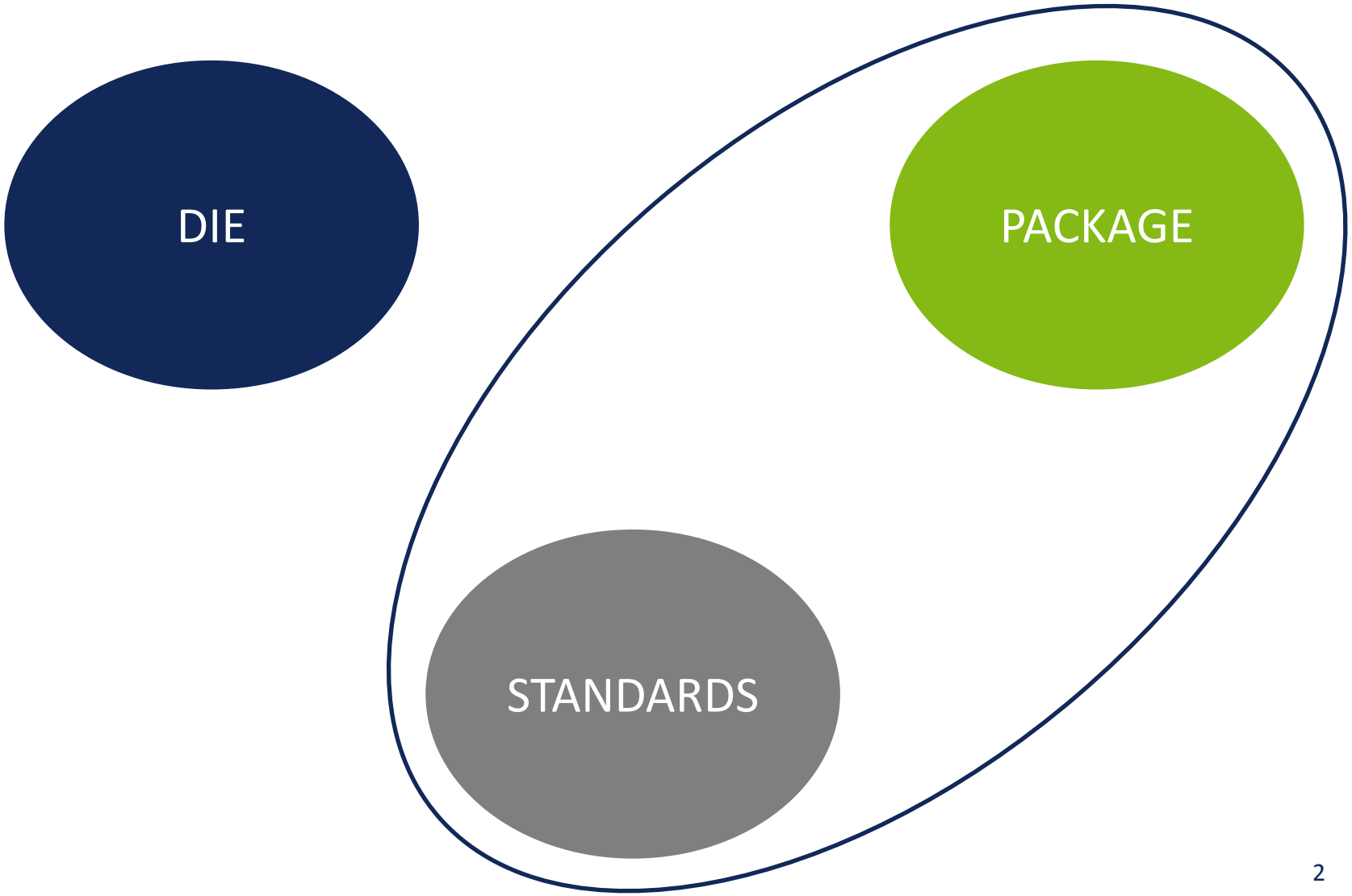
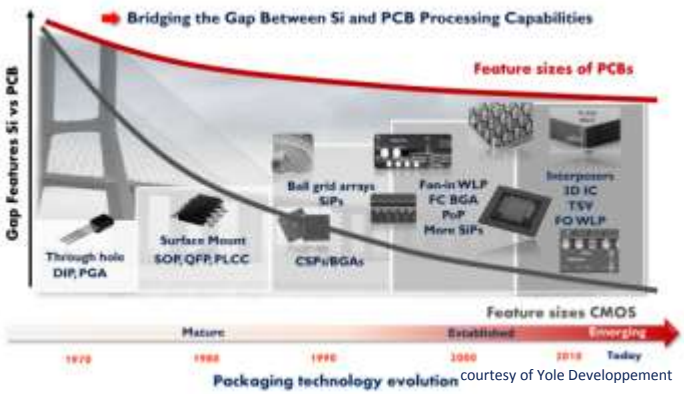
The 3 axis of Flip Chip for Space



Packaging Requirements



courtesy of Yole Developpement

Main Requirements

sub 90 nm technology nodes

die size > 300 mm²

package > 1700 balls

die > 5000 bumps

good thermal dissipation

numerous passive components

mission critical reliability

thermal shocks

vibrations

high temperature ageing

vacuum

…

Which flip chip ? For which application ?

Hermetic or Not ?

HERMETIC

no potential failure modes linked to moisture / chemicals ingress

NON HERMETIC

fewer constraints brought by package / process

no perfect, unique choice

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HERMETIC SOLUTION

Hermetic Flip Chip for Space

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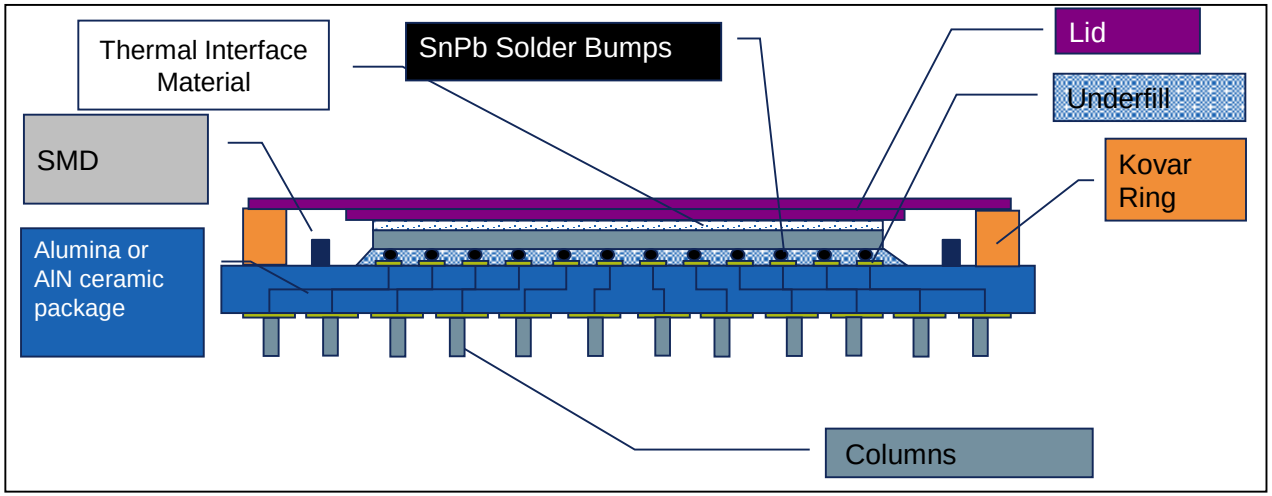
Project Scope

Funded by ESA & French government

Partnership with

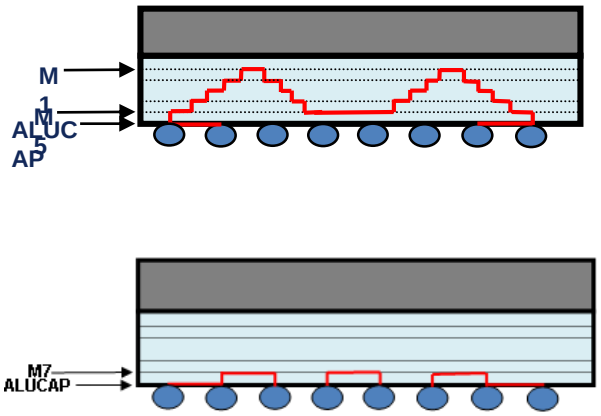
Project start : 2013

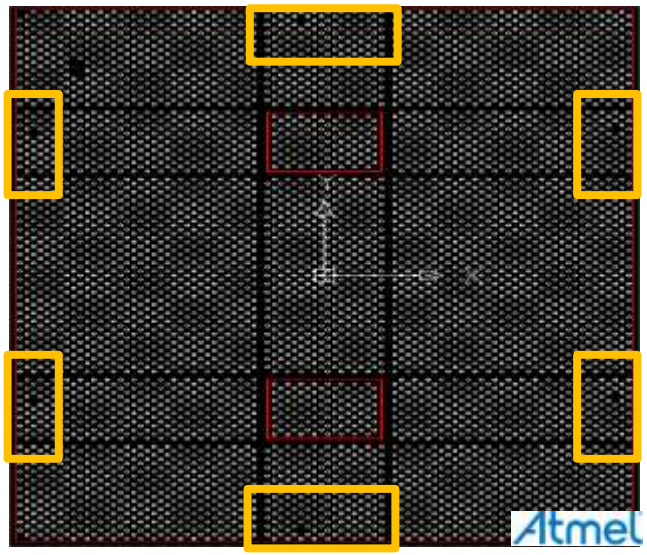


Hermetic Flip Chip for Space

Test Vehicle: Die

Full Features Test Vehicle





65 nm

300 mm², 5461 bumps, 225 µm pitch

Daisy Chains

Heating resistors

Thermal sensors

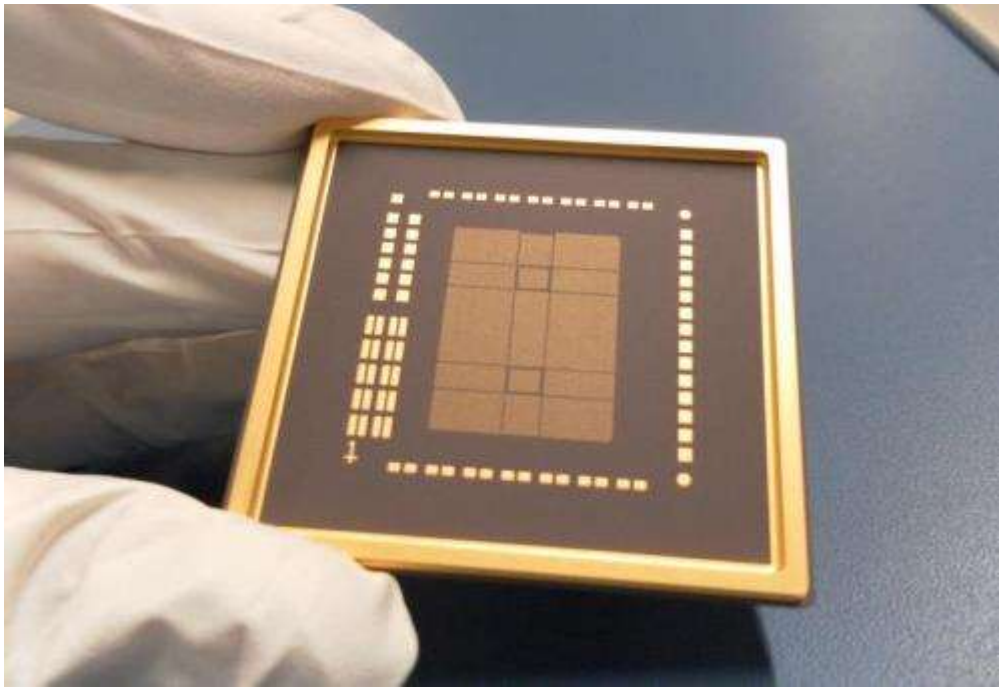
High speed structures

Electromigration structures

Hermetic Flip Chip for Space

Test Vehicle: Package

Specific Test Vehicle Package



Alumina

45 x 45 mm

1752 lands for balls/columns

Kovar ring

37 passives in package cavity (capas & resistors)

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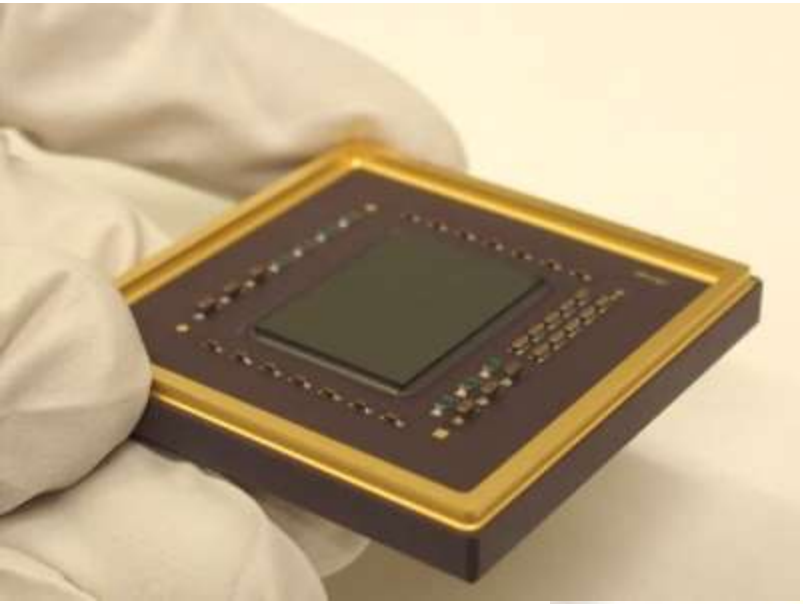
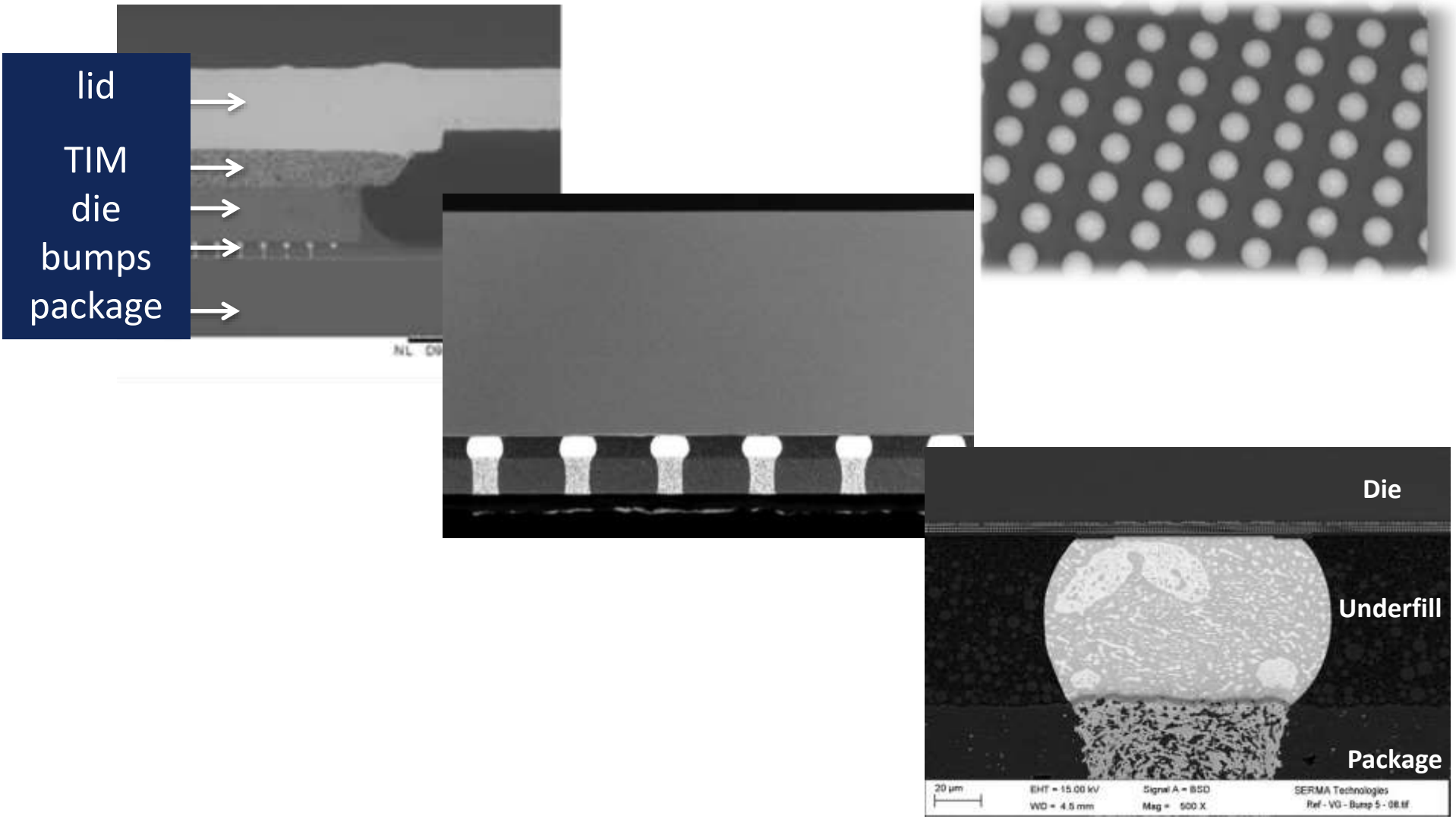


Hermetic Flip Chip for Space

Closer Look



Hermetic Flip Chip for Space

Reliability Status

Thermal Cycling: 1200 cycles @ -65°C/+150°C

- ✓ SAM: no delamination (Underfill &TIM inspection)
- ✓ SMD: no issue (for all types/sizes of SMD)
- ✓ Electrical test ok

Multiple reflows

- ✓ 20 reflows (Eutectic temperature profile)

Hermetic Flip Chip for Space

Schedule

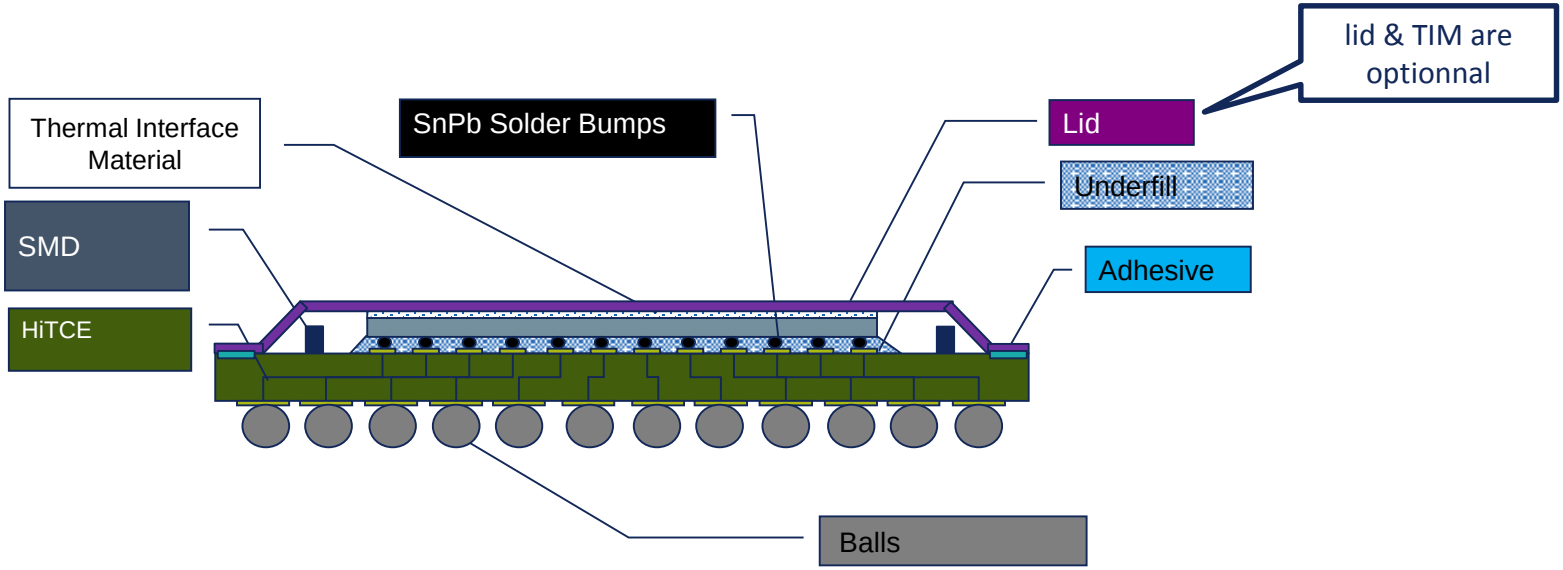
Test Vehicle Design & Manufacturing Manufacturing Equipments: new/upgrade	2013 - 2014	
Process Development & Reliability Validation PID availability	October 2015	
ETP Evaluation Test Program (Level 1 & 2) on ESCC screened Test Vehicles	Dec. 2016	

First Customer product assembly performed, Nov. 2015
(representative process & materials, not qualified)

NON HERMETIC SOLUTION

Non Hermetic Flip Chip for Space

Overview

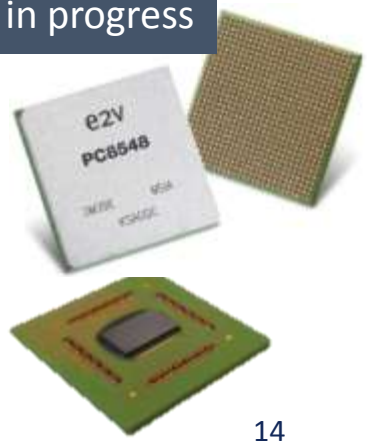


w/o lid: qualified

25 x 25 mm HiTCE package
360 balls, 1.27 mm pitch
1100 bumps
24 passives

w lid: reliability testing in progress

29 x 29 mm HiTCE package
783 balls, 1 mm pitch
1300 bumps
24 passives
with TIM & lid



Non Hermetic Flip Chip for Space

Non Hermetic Flip Chip BGA with lid: Reliability Status

lidded flip chip, current status: end of development / reliability testing

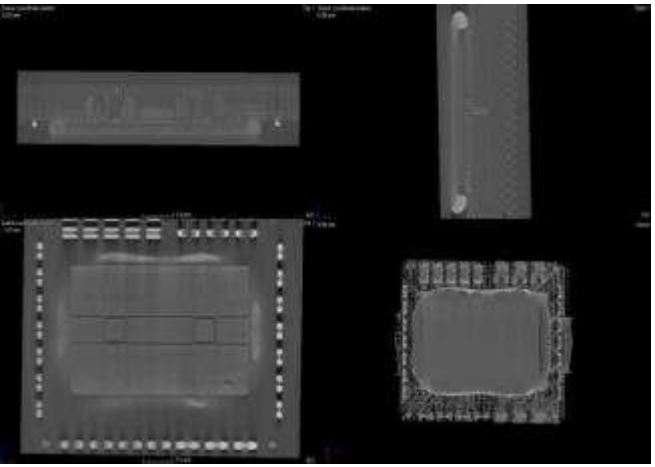
- MSL
- humidity testing
- thermal cycling
- shocks / vibrations
- …

Non Hermetic Flip Chip for Space

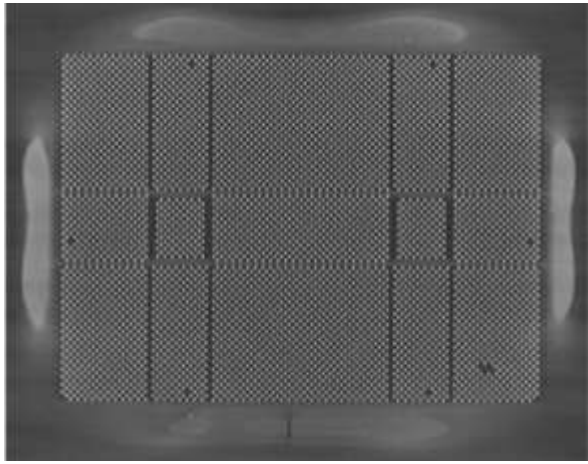
Non Hermetic Flip Chip BGA with lid: Schedule

End of Development validation (reliability testing)	**Q2 2016**	...
Product Qualification (incl. 4000 h life test)	**Q1 2017**	

Computed Tomography



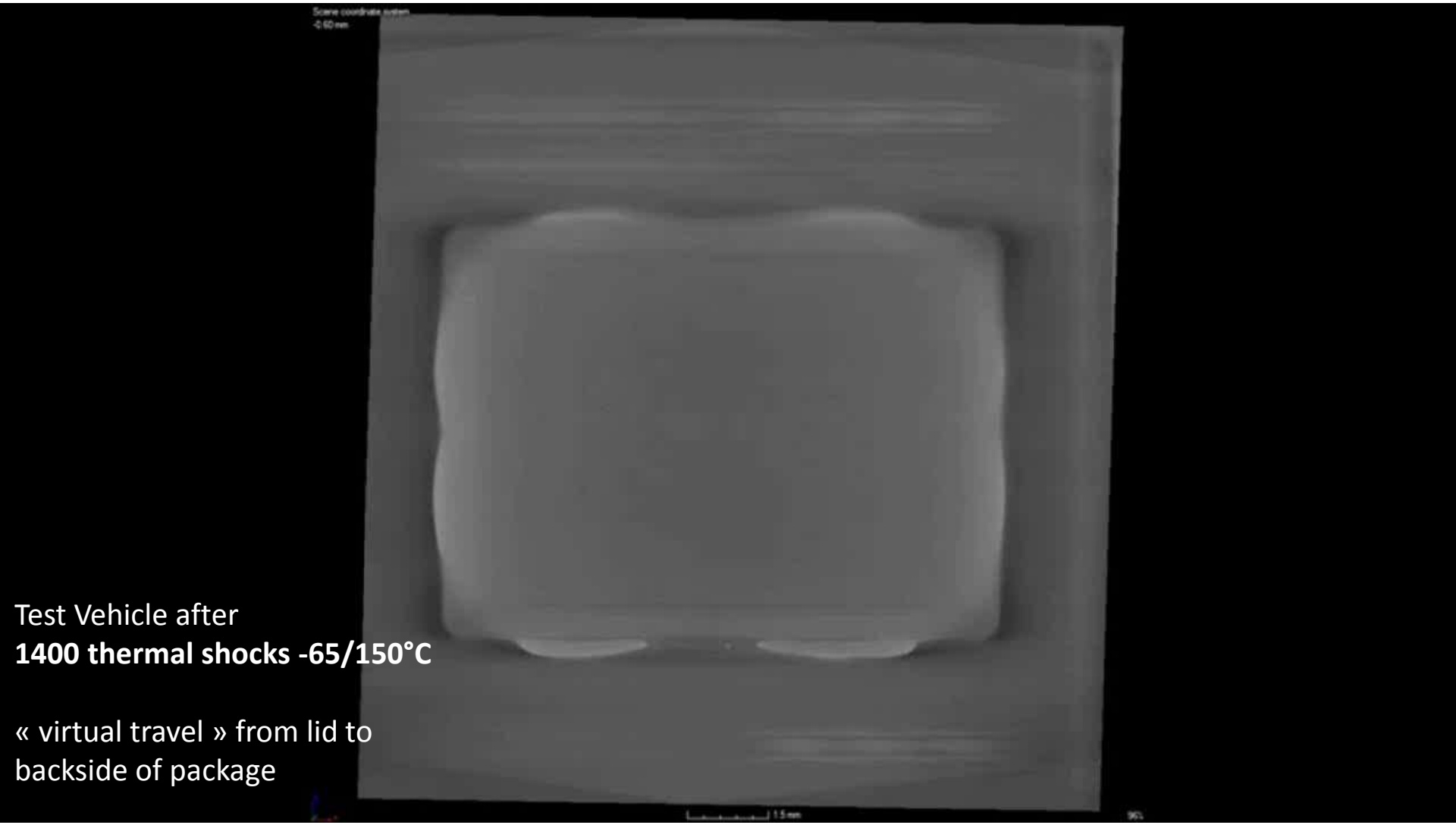
3D X Ray



Resolution of CT cannot compete with 2D Xray, and it is very slow.

Nethertheless CT brings tremendous informations to Development, Process & Reliability engineers

Computed Tomography



Test Vehicle after
1400 thermal shocks -65/150°C

« virtual travel » from lid to backside of package

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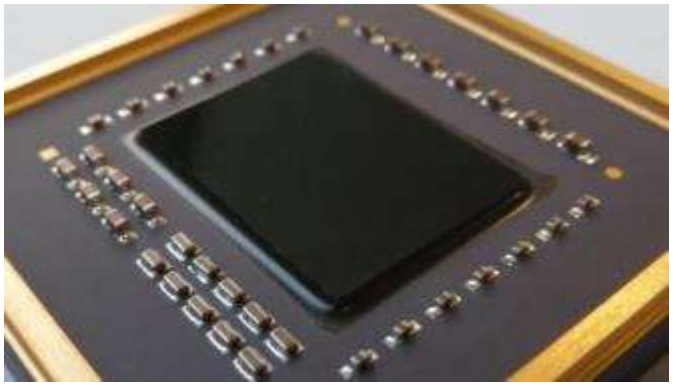
STANDARDS

Standards for Flip Chip

The Flip Chip Issue

2

CONCERNS



no flip chip in space standards for many years

solved with last revisions of Mil Prf 38535 / Mil Std 883

…even if some items still need some improvements

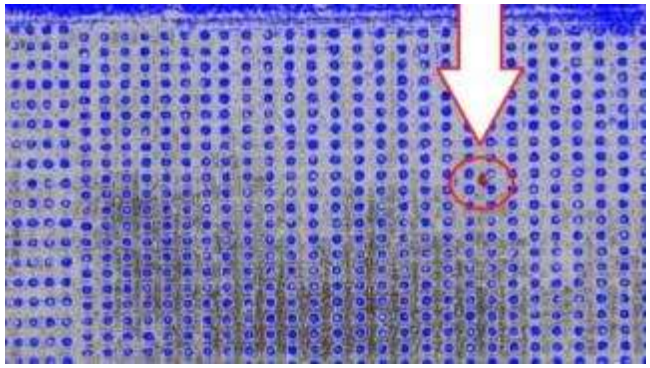
potential defects are not visible through sacrosanct optical inspection

change of paradigm:
from « visual flight rules » to « instrument flight rules »

means:

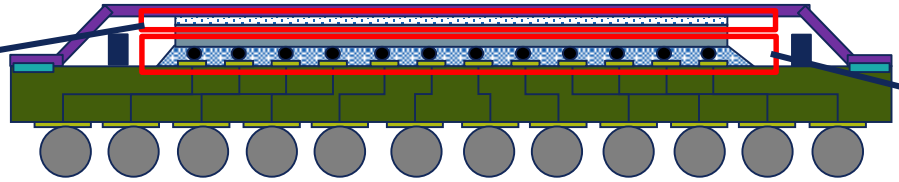
- **more QA**
- **new test / inspection methods**

Scanning Acoustic Microscopy



Check for Delaminations

control of delaminations at TIM level is mandatory for good thermal behaviour



control of delaminations at underfill level is mandatory for good thermomechanical reliability

Flip Chip for space requires comprehensive use of Scanning Acoustic Microscopy at all steps:

- development
- industrialisation
- screening
- reliability testing

Conclusion

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what a great progress since 2011 & 2013 ESCCONs !

then,

space level flip chip devices were expected

standards for those were expected

today, there is still some way to go…

But we have moved from expectation to reality !

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Thank you for your attention