

ESCCON 2016 @ ESA/ESTEC

New EEE components R&D activity in JAXA for realization of novel space missions

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Today's talk

Introduction.

Updated status of JAXA's EEE components development.

New component technology research activities to realize novel space missions.

Summary.

Introduction.

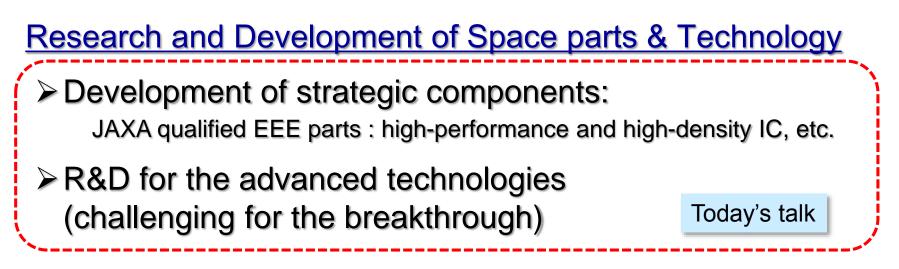
Updated status of JAXA's EEE components development.

New component technology research activities to realize novel space missions.

Summary.

Strategy of JAXA parts program





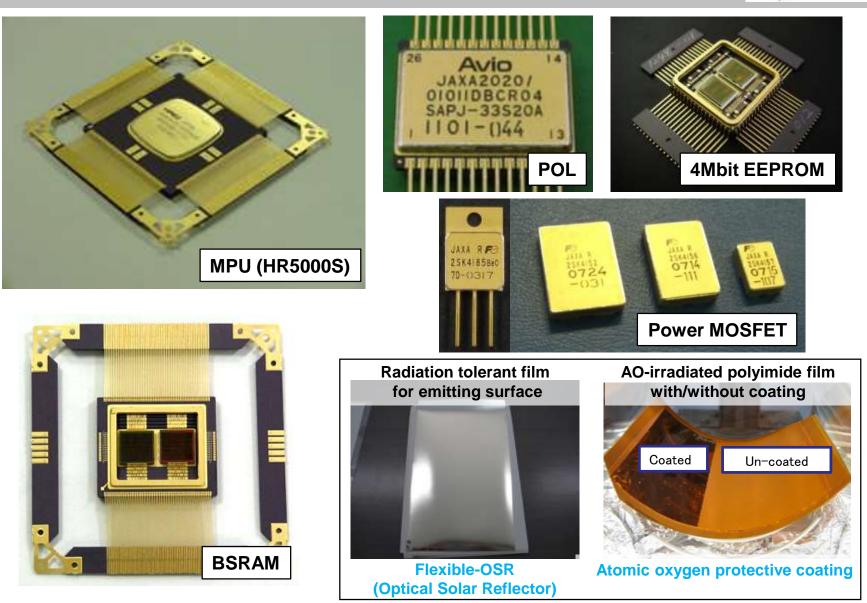
Qualification and Engineering Support regarding EEE parts

Cooperation with foreign entities: Improving independence from ITAR by cooperating with European countries

- Ensuring quality of imported components: Ensuring the quality of the imported components
- Promoting utilization of JAXA qualified components:

JAXA qualified parts and materials





Introduction.

Updated status of JAXA's EEE components development.

C-BGA package.
SJ Power MOSFETs.

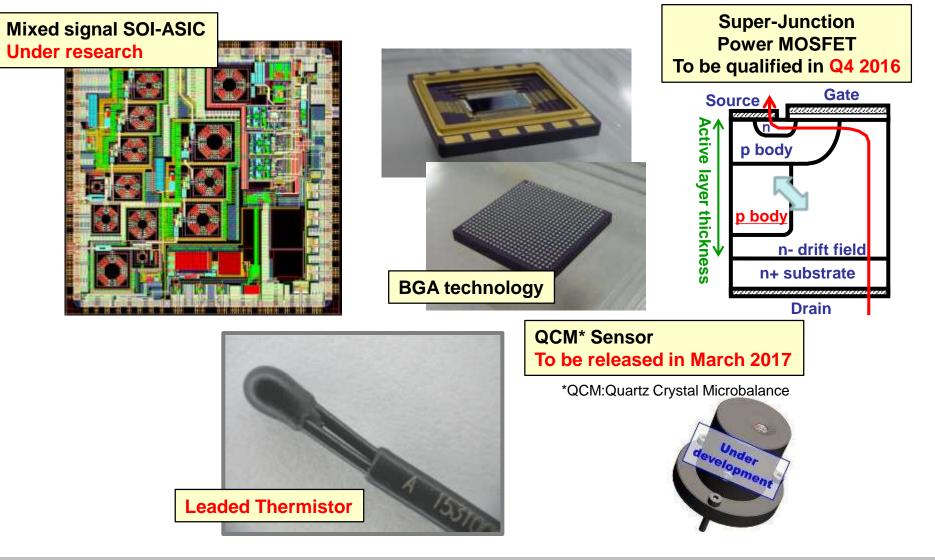
New component technology research activities to realize novel space missions.

Summary.

JAXA EEE parts development (on-going)



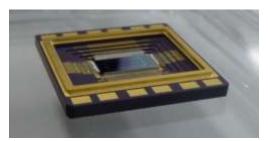
Developing high-performance and downsizing technologies



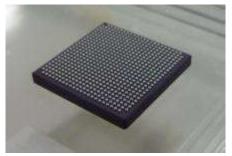
C-BGA package



✓ Now in evaluation phase. QT will be completed 1^{st} quarter 2017.



C-BGA package without seal-cap (top-side)



C-BGA package (bottom-side)

Target feature of C-BGA package

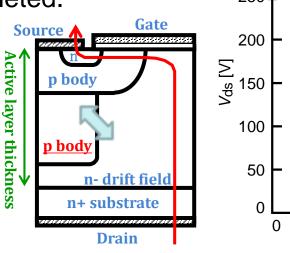
	Target feature	Remark
TYPE	C-BGA	Al ₂ O ₃
Pin count	572 / 357 / 165	24x24 / 19x19 / 13x13 (no corner-pins)
Pin pitch	1.0 mm	
Pin material	Solder	63Sn/37Pb and 10Sn/90Pb Attached with a vacuum reflow
Internal Wiring	AI wire-bonding	Conventional process
Mount tech.	BGA	With/without underfill

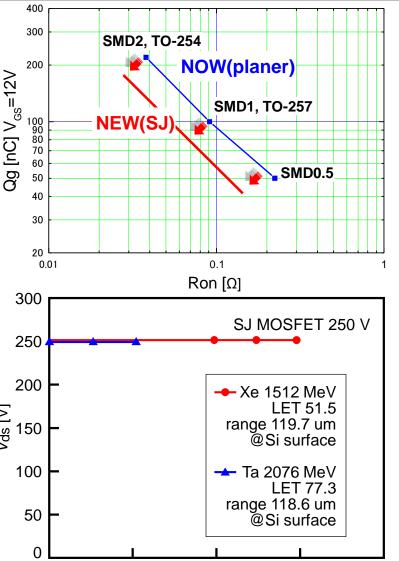
SJ Power MOSFET



- Low R_{ON} x Qg (compare to planer type)
 - 45% reduction (250V type)
 - 75% reduction (600V type)
- High SEGR/SEB tolerance
 - SEGR/SEB FREE up to LET of 75 MeV/(mg/cm²)
 - NOW: Manufacturing QT parts.
 - By 4th quarter, 2016:
 QT will be completed.







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Introduction.

Updated status of JAXA's EEE components development.

New component technology research activities to realize novel space missions.

RHBD methodology for nano-scale CMOS process.

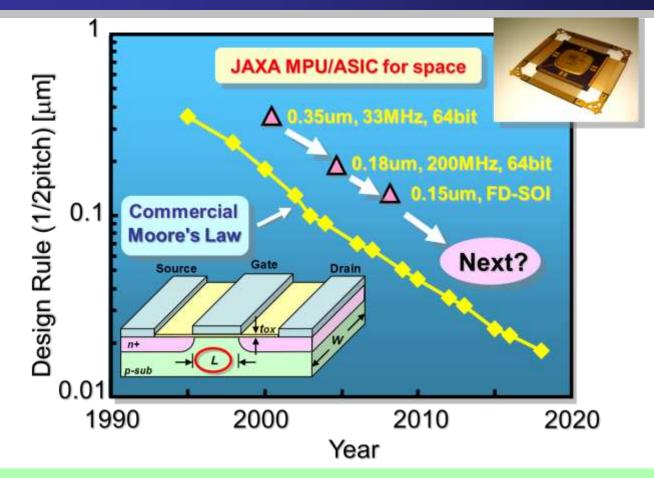
Ultra-low power consumption technology.

High-density surface mount technology.

Summary.

CMOS scaling trend comparison



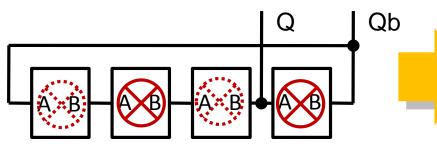


Recently, due to the requirements for higher density integration and device scaling, the logical circuits have been designed with <100 nm design rule. Single-Event Effects become serious problems for those integrated circuits.

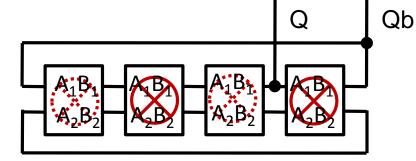
RHBD for nano-scale (Hyper- DICE)



- ✓ It was indicated from our previous research that SEUs caused by charge sharing can not be ignored for nano-scale devices.
- JAXA proposed a new RHBD circuit which is applicable for nano-scale technology called "Hyper-DICE". Four critical transistors have to be affected simultaneously for memory state upset in Hyper-DICE.
- ✓ JAXA designed and fabricated memory circuit based on Hyper-DICE on 65nm bulk CMOS process. Irradiation tests are in progress.



Stable Isolate Stable Isolate (a) Normal DICE circuit concept



Stable Isolate Stable Isolate

(b) Hyper DICE circuit concept

Fig. Hyper DICE and Normal DICE circuit concept

 RHBD : Radiation Hardness By Design
 DICE : Dual Interlocked Storage Cell

Necessity of ultra-low power technology



- Recently, it is concerned that power consumption of IT devices in terrestrial, as well as in space, is increasing explosively!
- To reduce the energy consumption, "Normally-off computing" which is shut power down whenever not being used, and/or ultra-low power operation are strongly desired.



JAXA has started the investigation of state-of-the-art non-volatile memory technologies for new memory of high performance, ultra-low power consumption and high radiation immunity in space.

Keyword: MRAMs, Atom switch, etc.

Feasibility study of "Atom switch"



Atom switch : A nano-scale switch which controls connection/disconnection of Cu⁺ ion bridge electrochemically.

Atom switch has features of low power, small area and non-volatility for the memory applications. In addition, it is also expected to replace a conventional SRAM/Pass-Tr. switch for a reconfigurable LSI.

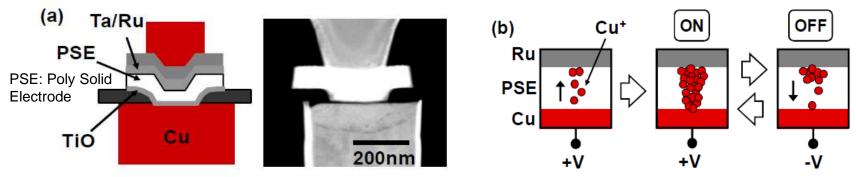


Fig. (a) Cross sectional illustration (left) and TEM image (right) of atom switch cell,

(b) Schematic diagrams of switching mechanism.

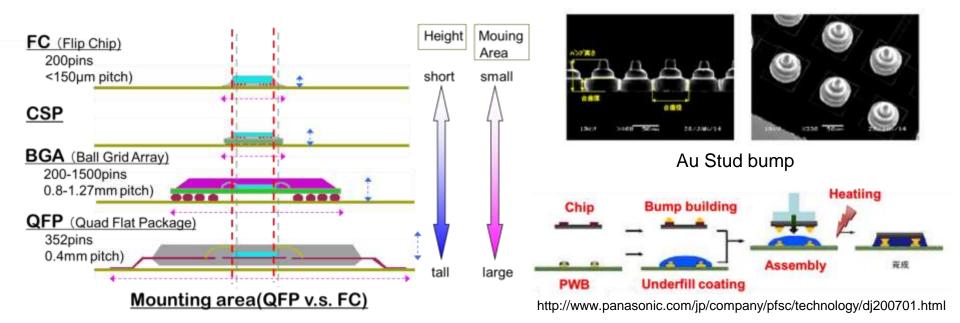
Ref: K. Okamoto et al., "Conducting mechanism of atom switch with polymer solid-electrolyte," Tech. Dig. Int. Electron Devices Meet. IEDM, vol. 1, pp. 279–282, 2011.

✓ JAXA started the evaluation of radiation tolerance of this switch as the first step of feasibility last year. (Results indicated excellent tolerance.)

High-density surface mount technology



- ✓ JAXA is studying and developing System In a Package (SIP) technology for space devices with high-density Surface Mount Technology (SMT).
- ✓ Flip Chip(FC) would reduce CPU mounting area by 83.70%, which is expected to give a drastic miniaturization of space devices.
- Now element technology evaluations are on-going.
 Stud bump, Build-up PWB for FC, Epoxy-encapsulated solder connection.



Summary

 Updated status of JAXA's EEE components R&D activities has been reported.

 New research activities for extending the possibility of space activities have also been introduced.

 Although the state-of-the-art component technology is very attractive, sufficient characterization is required to identify potential failure mechanisms.