

The ECSS -Q-ST-60-13C

Approach to Commercial EEE Components

The concept and key requirements

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Objective of the presentation : to explain the ECSS requirements on PEMS

- 1. ORIGIN**
- 2. BASICS**
- 3. COTS SPECIFICITIES**
- 4. CONCEPT**
- 5. CONTENT (SOME HIGHLIGHTS)**
- 6. IMPLEMENTATION DIFFICULTIES**
- 7. CONCLUSION**

See also the associated presentation : First experiences with ECSS-Q-ST-60-13C use in CNES projects

2. SPECIFICITIES



Integrated circuits	Space	MIL	Commercial
Technology	Dedicated or not		commercial
Manufacturing	Dedicated	dedicated, off shore	
Qualification Specification	Agency	Agency/manufacturer	manufacturer
Tests	screening, lot tests		manufacturer
Temperature range	-55/125°C		-55/125 ; -40/85 ; 0/70
Package, terminations	Hermetic, majority Sn/Pb		Hermetic, Plastic, Pb free
Life cycle	Many years		Several year(s)

- Purchasing cost << cost of ownership which includes engineering tasks, additional tests, etc.
- The question is not "COTS authorised or not" but authorisation with which conditions (i.e. with which additional tests).

3. BASICS (1/3)



- Perimeter limited to active parts (VLSI, discrets)
- Pretailoring included as per 3 risk classes (same as ECSS-Q-ST-60)
- Written by delta with the existing ECSS on 3^E parts requirement (ECSS-Q-ST-60C) : to highlight specificities
- Requirements categories :
 - Management (DCL, Parts Control Board)
 - **Selection**
 - Procurement
 - Inspection
 - Quality
- For performance access, cost motivation at a lesser extent
- Preference to space qualified components



- **Consider specificities :**

- Pure tin terminations
- Temperature range
- Non hermetic packages : storage, humidity test & moisture sensitivity
- Traceability at trace-code level
- Need for Manufacturer data collect

Trace code : Unique Manufacturer identifier to label and trace a quantity of components with a common manufacturing history and thereby common characteristics.
Several trace codes can be part of a same delivery from the manufacturer or the distributor.
It is possible to have several diffusion lots in the same trace code.

- **No specificity for :**

- Declared components list
- Parts Control Board
- Radiation Hardness Assurance



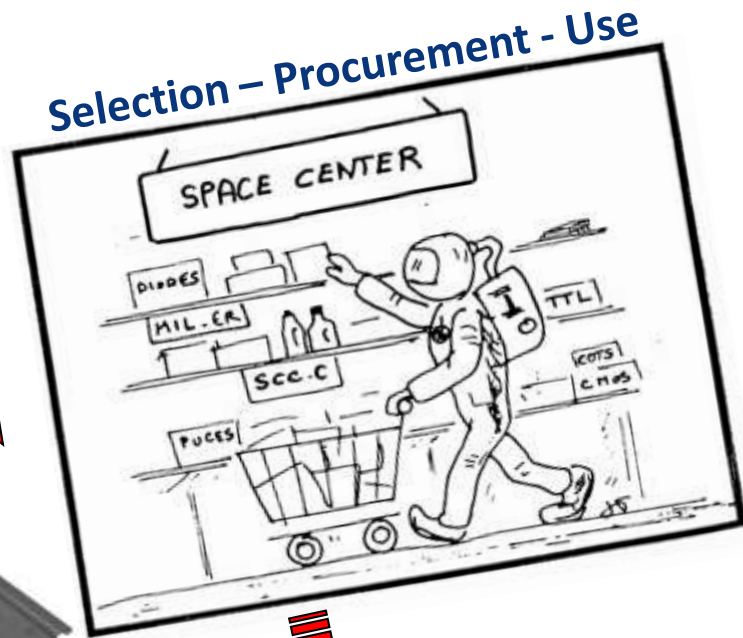
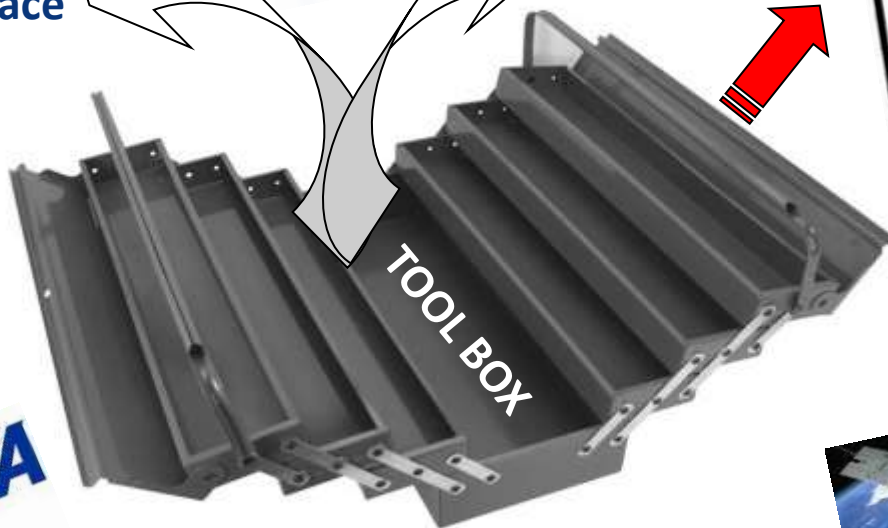
3. BASICS (3/3)



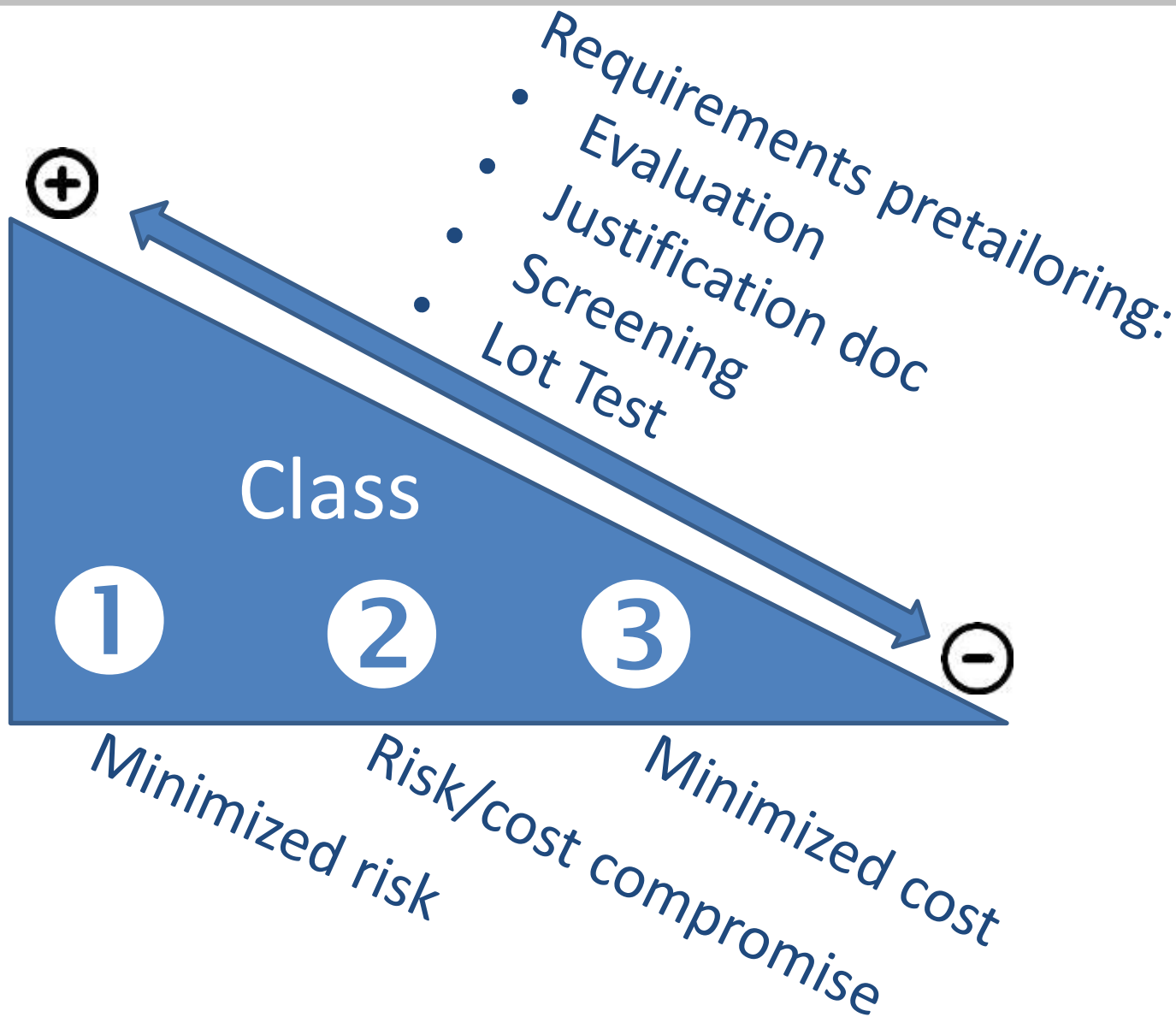
European Space parts



COTS



4. CONCEPT (1/2)



4. CONCEPT (2/2)



	Class 1	Class 2	Class 3
Eval.	<p>CA Elect. charact. HAST 96h or THB 1000h LT 2000h @ 125°C+DPA 500 T/C -55/+125°C</p>	<p>CA Elect. charact. HAST 96h or THB 1000h LT 2000h @ 125°C+DPA 500 T/C -55/+125°C</p>	<p>CA</p>
Doc.	<p>JD</p>	<p>JD</p>	<p>JD</p>
Screening	<p>10T/C -55/+125°C Burn in 240h @ 125°C</p>	<p>10T/C -55/+125°C Burn in 160h @ 125°C</p>	
LAT on screened parts (TC, LT, rad)	<p>CA HAST 96h or THB 1000h LT 2000h @ 125°C 100T/C -55/+125°C</p>	<p>CA HAST 96h or THB 1000h LT 1000h @ 125°C 100T/C -55/+125°C</p>	<p>CA HAST 96h or THB 1000h LT 1000h @125°C 100T/C -55/+125°C</p>

**Only PEDs considered
Radiation not included**



**Required
Case by case**

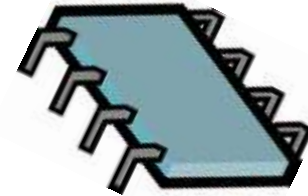
Temperature :

- Commercial EEE part to be selected in its highest temperature range.
- No usage outside temperature range (!)
- Minimum 10°C margin between maximum manufacturer temperature range and the application (including worst case).
- If margin below 10°C, electrical characterization up to using temperature + 10°C.



Pure tin :

- Class 1 : Sn/Pb solder dip with a qualified process, before screening & Lot test
- Class 2 & 3 : Sn/Pb solder dip or risk analysis & mitigation based on collected data + application



Storage for Plastic encapsulated devices :

- Dry Nitrogen
- Dry and ionised air with RH in a range of 15% to 20%
- Dry pack as specified in J-STD-033 for dry pack inspection and control



Justification Document = data collection including :

- Justification need /trade-off wrt space qualified solution
 - Manufacturer max rating
 - Data sheet
 - Process/techno Changes Notification services
 - Life cycle, maturity : (emerging/maturity/decline)
 - Lead finish
 - Manufacturer qualification, reliability, lot & screening tests, Early Failure Rate
 - Manufacturer part traceability: *tracecode, datecode assembly plant, wafer fab, diffusion lot*
- + Eval, additional test (screening, Lot test) at user level

For approval

6. IMPLEMENTATION DIFFICULTIES



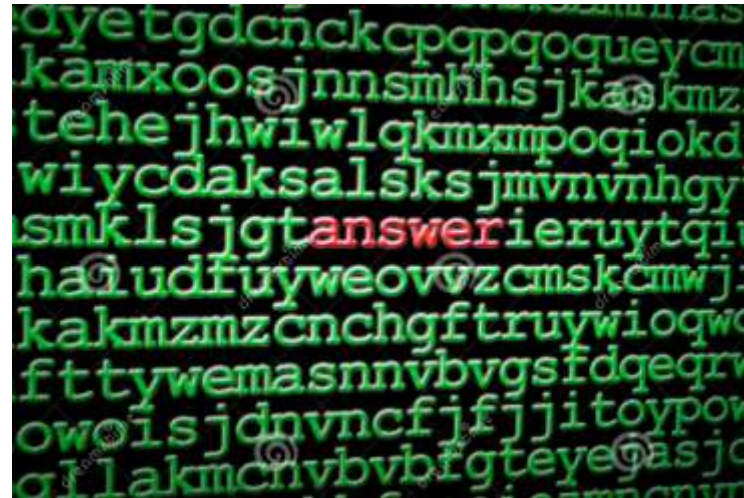
- Tradeoff with High Rel parts vs preference to High Rel parts
- Engineering resources, focus on the selection step
- Engineering arbitration : to decide when no test is acceptable
- Similarity approach
- A standard not optimized vs case by case approach
- Real cost of ownership/true prices & costs. Debate about the cost reduction drivers :
 - Electrical architecture (design to cost & COTS vs pin to pin replacement)
 - Industrial organisation complexity & interfaces
- Perimeter limited to PEMS




7. CONCLUSION



- COTS Standard, necessary, useful, progressively implemented & experienced



- ... And very positive lessons learned  see next presentation “First experiences with ECSS-Q-ST-60-13C use in CNES projects” ...