European Space Components Conference **ESCCON 2016** ESA/ESTEC

The ESCC Policy and Standards Working Group (PSWG)

01-03 March 2016

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ESCC

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1. PSWG MISSION & ORGANISATION

Space Components Steering Board

- **P**olicy & **S**tandard **W**orking **G**roup
- Component Technology Board
- Executive

PSWG Membership :

- Eurospace (Airbus D&S, Alter, TAS, TESAT)
- Agencies (ESA, DLR, CNES, ASI, UKSA)
- Manufacturers (Atmel, ST, Vishay)

2. RECENT ACHIEVEMENTS

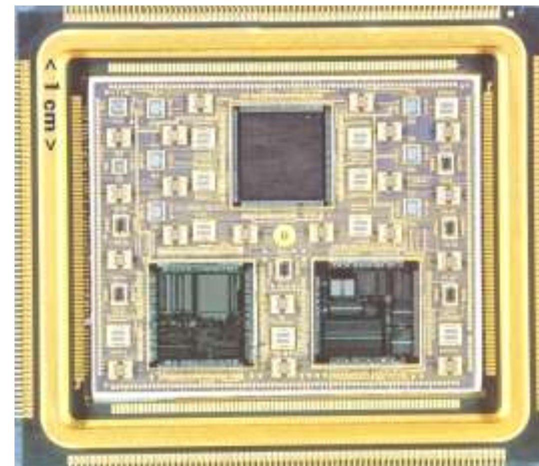
- **Pure tin inspection**
- ECSS-Q-ST-60-13 (see dedicated presentation)
- **Process Capability Approval**
- **Hybrid Capability Approval +PID + line survey check list**
- **MultiChip Microcircuits**
- **DPA**
- Precap (Internal Visual inspection)
- **Oscillators ETP, Generic**
- **Laser diodes ETP, Generic**
- Ceramic Capacitors
- EPPL management

2.1 PURE TIN DETECTION

- Methodology for the detection of pure tin in the external surface finish of case & leads of EEE components : ESCC 25500 April 2013
- Lead finish check during incoming inspection
- Pure tin if >= 97%
- X-Ray Fluorescence Test Method to detect more than 93% of Sn
- Then complementary Test Method to confirm Pure tin : Scanning Electron Microscopy Energy Dispersive Spectroscopy
- Microsection

2.2 MULTICHIP MICROCIRCUIT

- Definition of a Multichip Microcircuit : A microcircuit consisting of two or more semiconductor dice coming from the same manufacturer, from one or more foundries, individually attached to a single package cavity.
- Incorporated in the generic Spec for Monolithic Integrated circuits (ESCC 9000)
- Screening, Lot test at product level, some exceptions at each die level : TID, die shear



2.3 PROCESS CAPABILITY APPROVAL

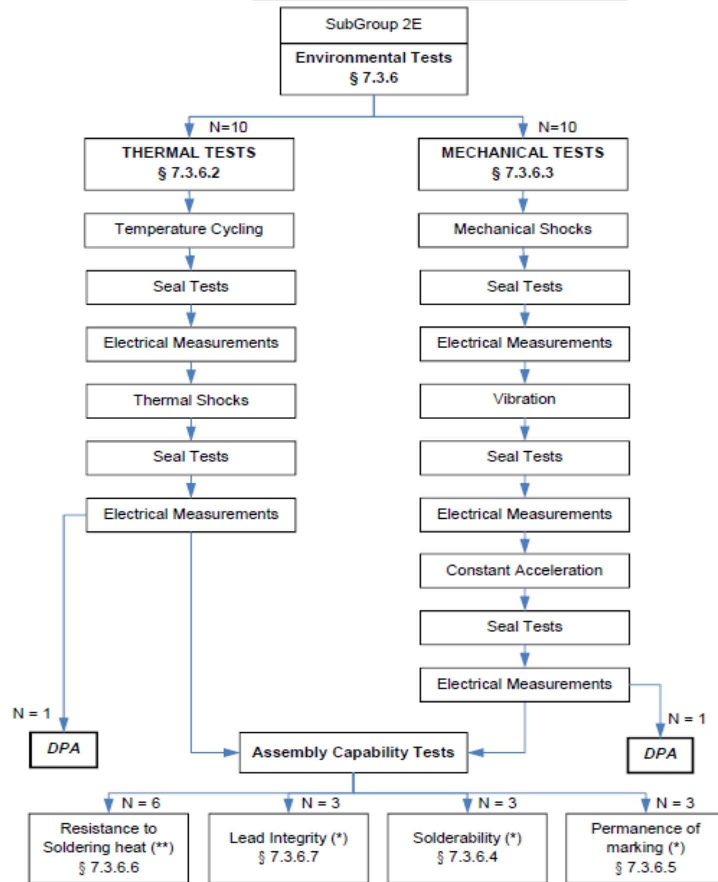
- ESCC 25600 June 2014
- For suppliers in manufacturing, assembly & test operations
- Not a Product qualification
- Do not confuse with :
  - ESCC24300 : Capability Approval of Electronic Component Technologies
  - ESCC20100 : Qualification of Standard Electronic Components
  - ESCC 25400 : Technology Flow Qualification of Electronic Components
- Details in ancillary specification for the particular component technology.
- Process capability domain and boundaries.
- Manufacturing, inspection and test facilities.
- Supplier's organisation.
- PID including all flow charts.
- Existing data
- Constructional analysis.
- Quality assurance system.

➢ Application to Hybrids Capability Approval

2.4 OSCILLATORS (1/3)

Evaluation Test Plan :

- Hybrid techno
- ESCC 2263503 November 2015



9 **CHARTS**

CHART I: EVALUATION TEST PROGRAMME

INSPECTION § 5

§ 5.2	Dimensions	100%
§ 5.3	Weight	100%
§ 5.4	Electrical measurements	100%
§ 5.5	External Visual Inspection	100%
§ 5.6	PIND	100%
§ 5.7	Radiographic Inspection	100%
§ 5.8	Hermeticity (Fine & Gross Leak)	100%
§ 5.9	Marking and Serialization	100%
§ 5.10	Materials & Finishes	100%

N = 92

INITIAL MEASUREMENTS § 6

100% Read & Record @ Room Temperature in accordance with the Detail Specification

N = 92

N = 5	N = 52	N = 30	N = 5
Group 1	Group 2	Group 3	Group 4
Control Group § 7.2	Destructive Tests § 7.3	Accelerated Life Tests § 7.4	ESD Testing § 7.5

Group 3:

N = 10	N = 10	N = 10
T_1 °C 1000hrs	T_2 °C 700hrs	T_3 °C 400hrs

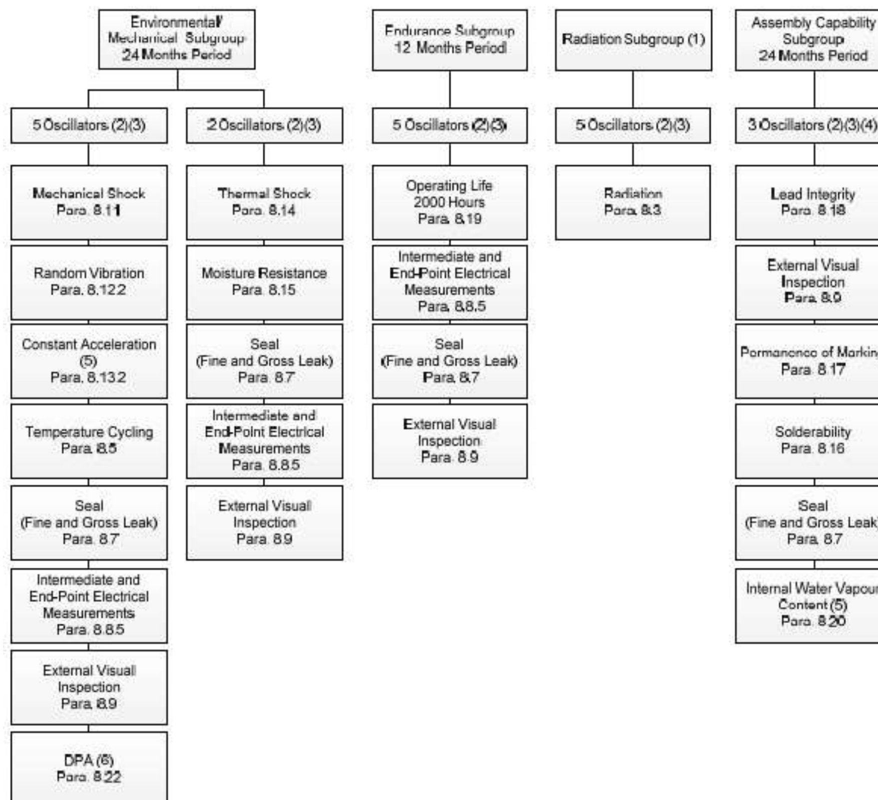
Group 2:

N = 8	N = 8	N = 11	N = 5	N = 20
Subgroup 2A	Subgroup 2B	Subgroup 2C	Subgroup 2D	Subgroup 2E
Temperature Step-Stress Tests § 7.3.2	Voltage Step-Stress Tests § 7.3.3	Radiation Test § 7.3.4	Construction Analysis § 7.3.5	Environmental Tests § 7.3.6 / Chart III

2.4 OSCILLATORS (2/3)

Generic spec :

- Discrets/PCB, hybrids, XO, VC/TCXO
- ESCC 3503 November 2015
- Add-on parts (encapsulated passives, passive & active dies)



12.3 CHART F3 - SCREENING TESTS

OSCILLATORS FROM PRODUCTION CONTROL (1)

Para.	Test	Note
Para. 8.4	High Temperature Stabilisation Bake	(2)
Para. 8.5	Temperature Cycling	
Para. 8.12.1 or Para. 8.13.1	Random Vibration (3) or Constant Acceleration (4)	
Para. 8.6	Particle Impact Noise Detection (PIND)	(4)
Para. 8.10	Radiographic Inspection	
Para. 8.8.2	Parameter Drift Values (Initial Measurements)	
Para. 8.23	Burn-in	
Para. 8.8.2	Parameter Drift Values (Final Measurements)	(5)
Para. 8.21	Frequency Ageing	(5)
Para. 8.8.3	High and Low Temperatures Electrical Measurements	(5)
Para. 8.8.4	Room Temperature Electrical Measurements	(5)
Para. 6.4.1	Check for Lot Failure	(6)
Para. 8.7	Seal (Fine and Gross Leak)	
Para. 8.9	External Visual Inspection	
Para. 8.16	Solderability	(5) (7)

TO CHART F4 WHEN APPLICABLE

2.4 OSCILLATORS (3/3)

Passive Encapsulated Chips

- Bondability = Bake, 100 TC, Bond Pull and Shear

Bare Passive Chips

- bondability = Ageing+300°C/ 1h, Bond & shear

Naked Semiconductor Dice

- Elec 3T
- Bondability = Ageing+300°C/ 1h, Bond & shear
- Lot Validation Test on assembled dies
  - Encapsulation and serialization
  - Storage +125°C/72 hours
  - 10 TC
  - Acceleration
  - Burn-In: 240 h/125°C
    Read and record , drift calculation
  - LT 1000/125°C, bond, shear, TID

12.5 CHART F5 - NAKED SEMICONDUCTOR DICE ADD-ON COMPONENT TESTING

WAFER LOT MANUFACTURING

Wafer Lot Acceptance
(ref. ESCC 5000/9000)
Para. 5.2.2.4.1(a)

Wafer Screening
Para. 5.2.2.4.1(b)
Chart F6

Packaged Test Sublot Testing
Para. 5.2.2.4.1(d)

'Screening'
Para. 5.2.2.4.1(d).i

Endurance Testing ('LVT')
Para. 5.2.2.4.1(d).ii

Radiation Testing ('LVT')
Para. 5.2.2.4.1(d).ii

Check for Wafer Lot Failure
Para. 5.2.2.4.1(d).iii

Bondability
Para. 5.2.2.4.1(c)

Deliverable Naked Dice

Release

TO OSCILLATOR PRODUCTION

2.5 LASER DIODE MODULE

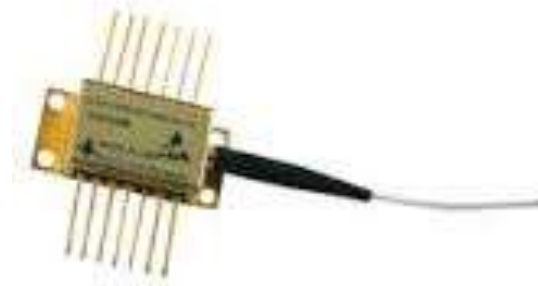
- Module = optical fibers, connector, IC, thermocooler, photodiode, etc.
- Hermetic & non hermetic

- Guidelines for the evaluation : ESCC 23201, January 2014

Includes : Displacement Damage, Vibrations/shocks, TC, depressurisation, Th Vacuum, Moisture, Catastrophic Optical Damage (COD) Threshold

- Guidelines for validation and lot acceptance testing : ESCC23202, October 2014

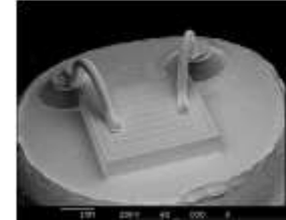
Includes Electro-optic parameters, RGA, Fibre pull, Catastrophic optical mirror damage

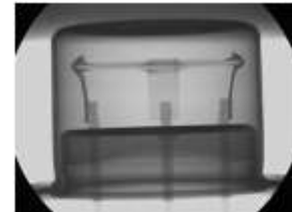
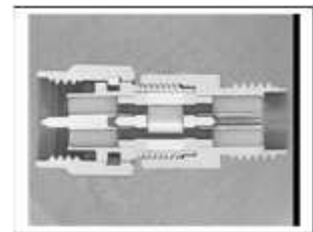


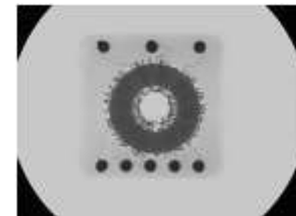
2.6 DPA

- Capacitors (ceramic, tantalum, variable, filter, plastic film)
- Connectors
- Crystals
- Diodes
- Fuses
- Heaters
- Hybrids
- Inductors
- ICs hermetic, plastic, MMICs, MEMs, CCDs, SAWs
- Optocouplers, LEDs, Optical sensors
- Relays
- Passive microwave
- Resistors, Thermistors
- Switches, thermal
- Transistors (hermetic, plastic)
- Wires, cables

ESCC21001 December 2015





3. IN PROGRESS/TO BE DONE

- Flip Chip (hermetic & non-hermetic)
- Cable Assemblies (Connector+cable)
- Dies
- TRL (3E scale in ECSS handbook)
- Relifing (ECSS update)
- Hermeticity Test Method
- Mounting capabilities assessment
- Non-Hermetic Resin Encapsulated Hybrids
- TID (including ELDRS)
- Incoming, Buy off
- Construction Analysis
- QA for ASICs & FPGA (ECSS update)
- Non hermeticity (PEMs)
- Opto (e.g. optical fibers connectors)
- Review of the ESCC Test Methods (replacement by US TM)
- EPPL reshaping

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4. CHALLENGES

- New technologies insertions
  - New packages (e.g. 3D, Non hermetic)
  - Multi technologies (e.g. PCB, add-on parts, integrated functions)
  - New materials (e.g. SiC, GaN, copper bonding)
- Non "conventional", non integrated manufacturers (outsourcing, subcontracting, Assembly & Test houses)
- Test Methods & Standards
- ESCC improvement
  - Competitiveness / efficiency/ time to market
  - Support Portfolios development
  - Internal working procedures
  - Promotion