



Advanced Concepts and Components for adaptive Avionics

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ESTEC

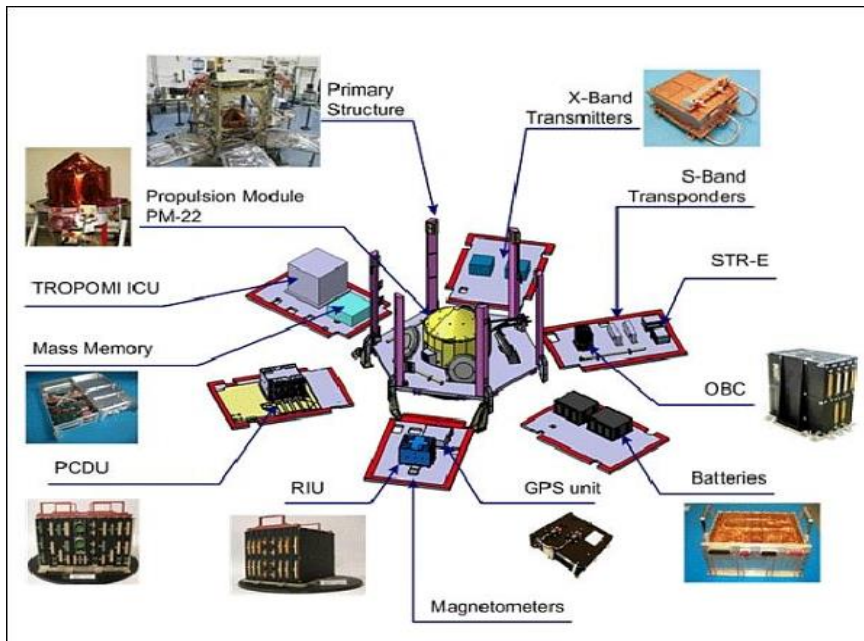
03/03/2016

AVIONICS : Cost reduction as a challenge

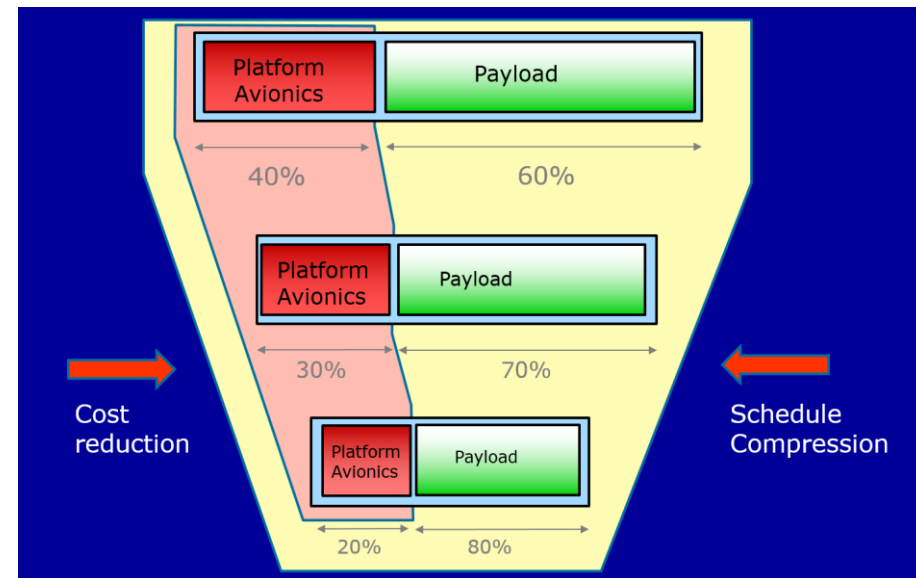


AVIONICS include:

- Data Handling – TM/TC
- Attitude and Orbit Control - FDIR
- Central Software – embedded SW



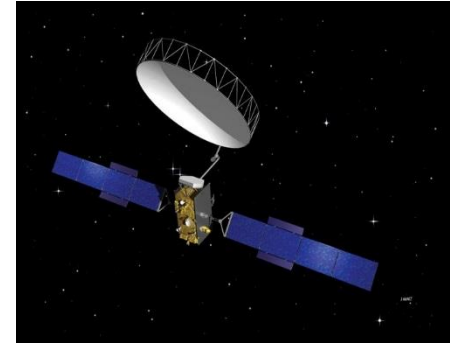
Additional constraint :
more € for the Payload ...
Less for Avionics !



Avionics : How to reduce the cost ?



- ✓ Through generic platforms ?
 - Astrobus, Spacebus, small GEO, Alphabus, Neosat



- ✓ Thanks to a higher level of recurrence, by reusing existing designs, Building blocks and components

- ✓ Via "more standardized" Avionics

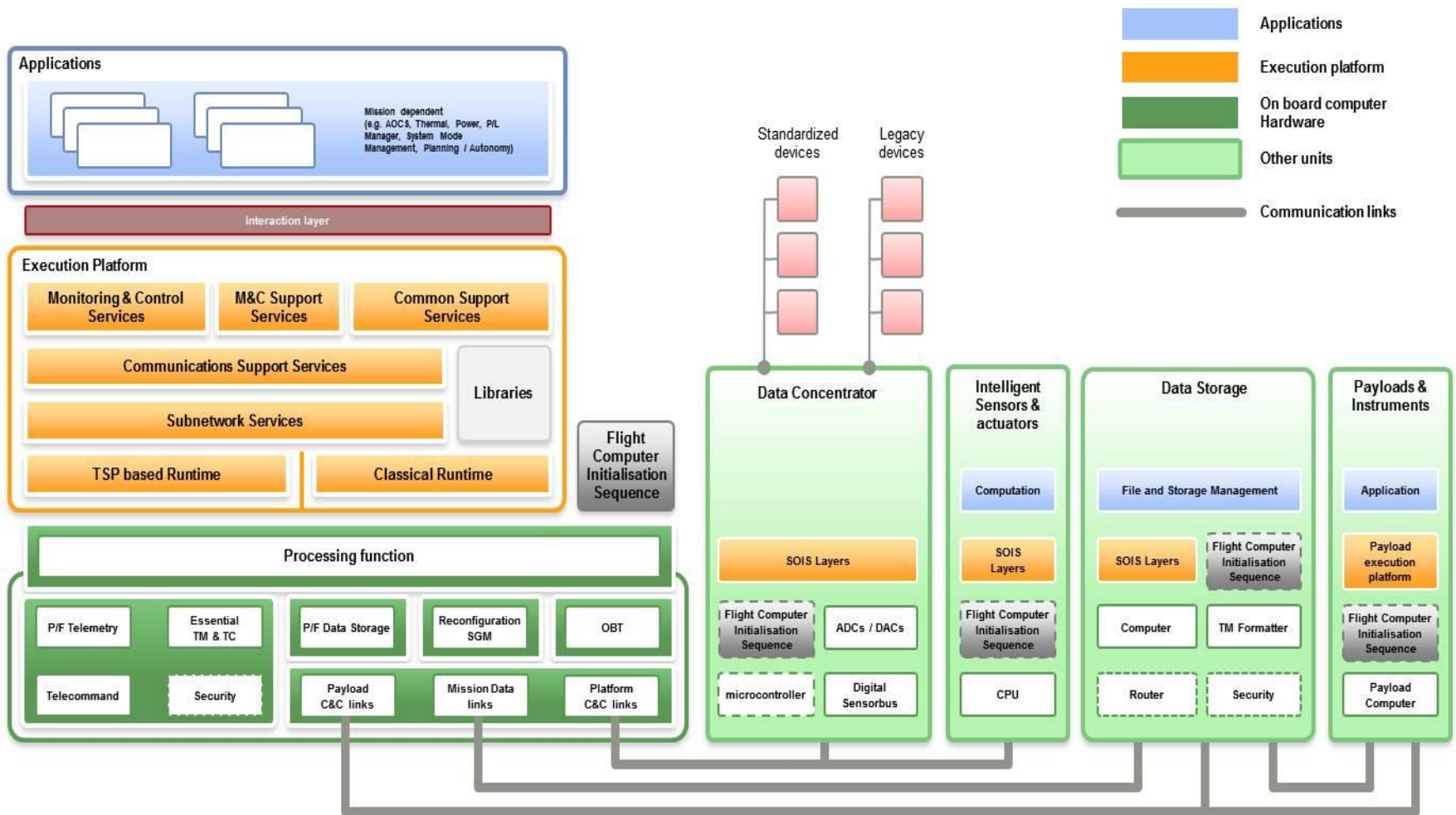
Space
AVionics
Open - Interfaces
ARchitecture



- ✓ By making tailoring of Data Systems easier:

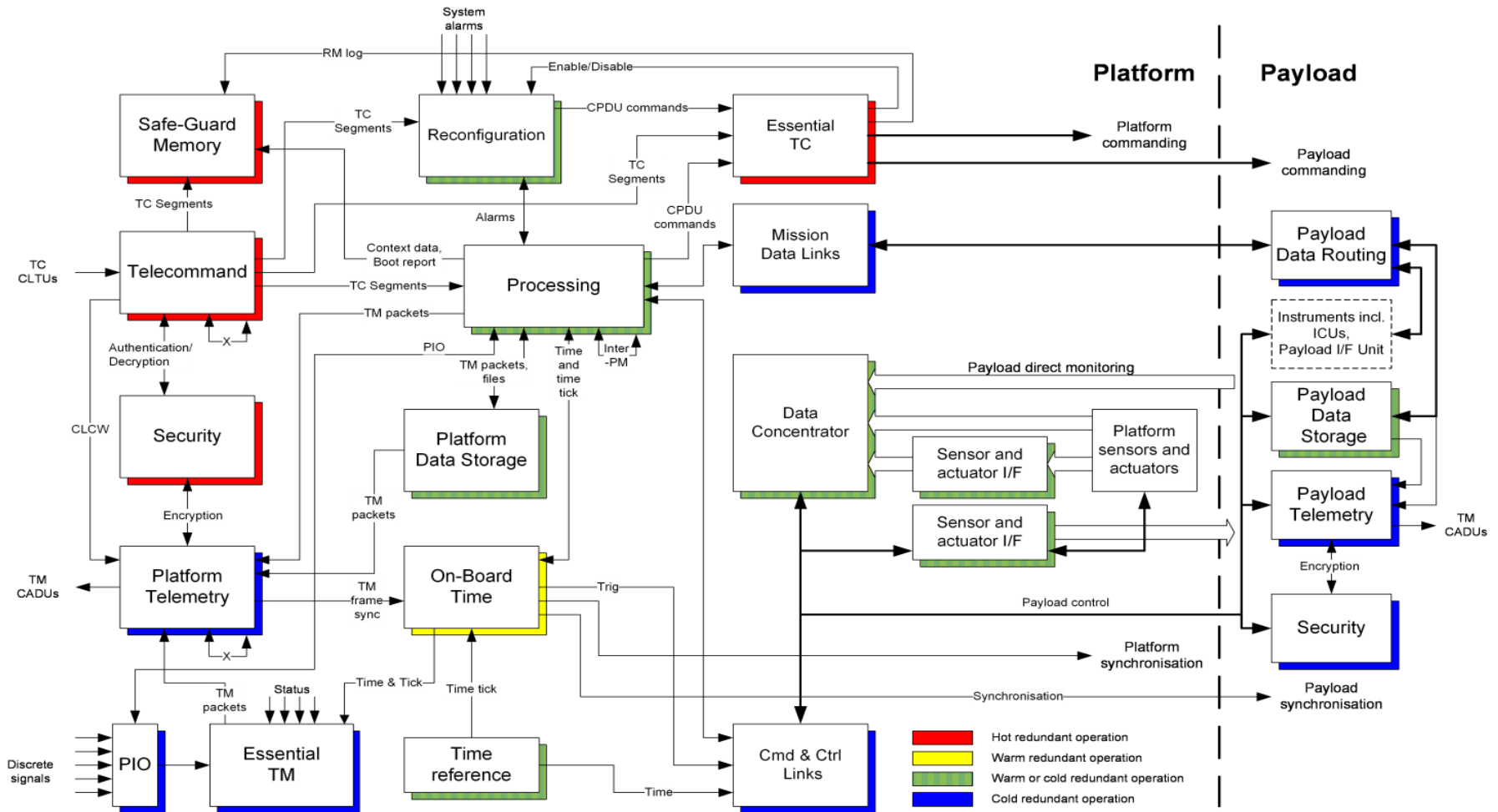
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SAVOIR : Reference Architecture

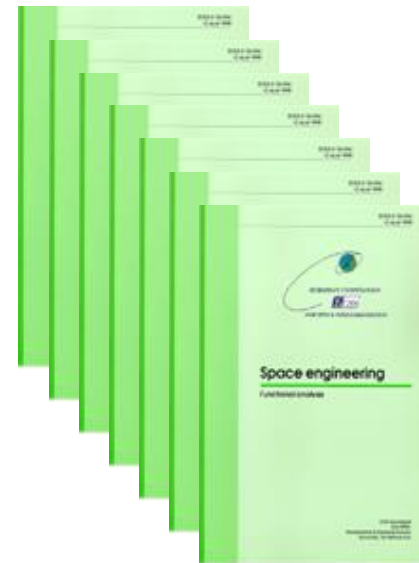


SAVOIR Functional Reference Architecture

Generic Specifications for OBCs, RTUs and Mass Memories



SAVOIR : Standardised Interfaces, Services and Protocols



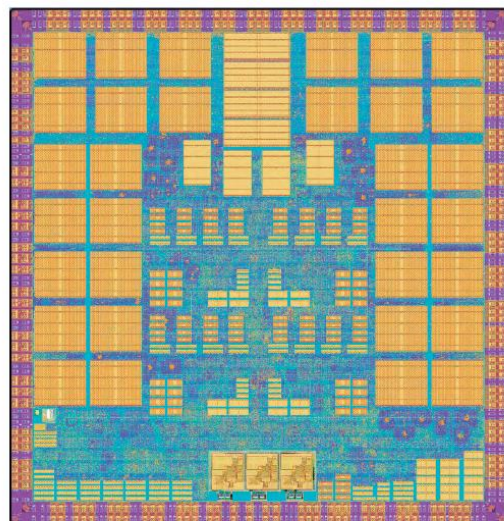
New interfaces:

- Sensor buses, I2C, SPI
- PowerLinks

Enhanced Networks:

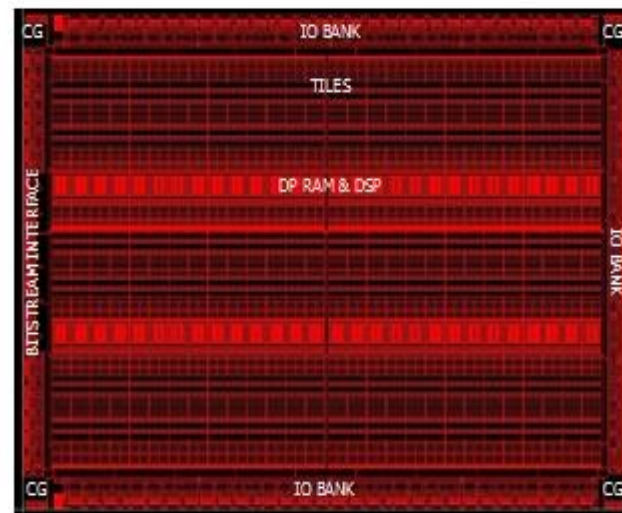
- Time Triggered Ethernet
- SpaceWire-D
- SpaceFibre

ESA's Next Generation Microprocessor



GR740 Quad-Core LEON4FT - Prototypes available in 2016
www.gaisler.com/GR740

ESA's Next Generation FPGA



Courtesy: NanoXplore

In cooperation with CNES

History of ESA Microprocessor Developments



MA 31750 (Dynex Semiconductor)

- MIL-STD-1750A architecture
- GEC-Plessey 1.5 μm

SPARC V7 ERC32 3-chipset

- IU, FPU, MEC: "TSC691 , 692, 693"
- Temic 0.8 μm

SPARC V7 ERC32 single chip

- Temic 0.5 μm – "TSC695"

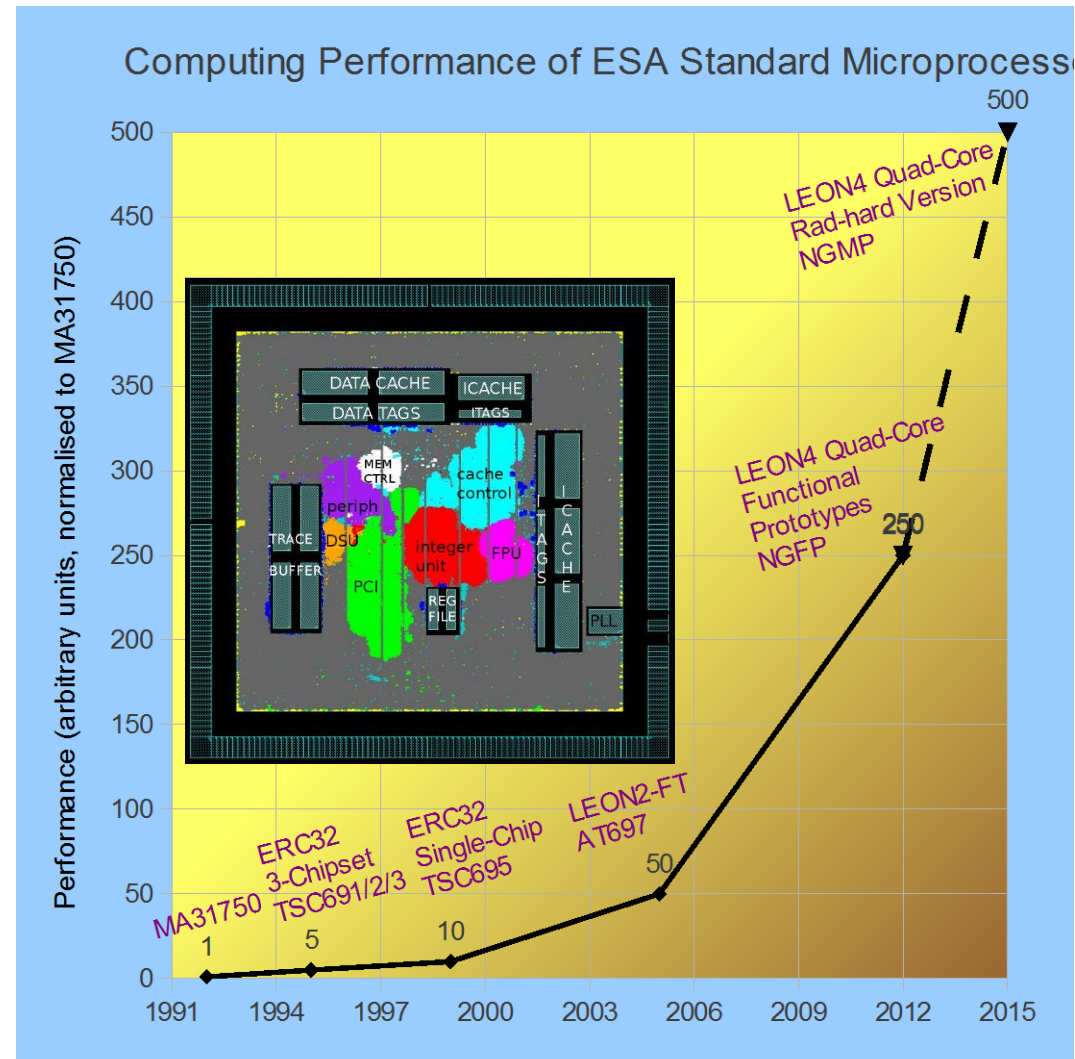
SPARC V8 LEON2 – "AT697"

- Atmel 0.18 μm

SPARC V8 LEON4/NGMP – "GR740"

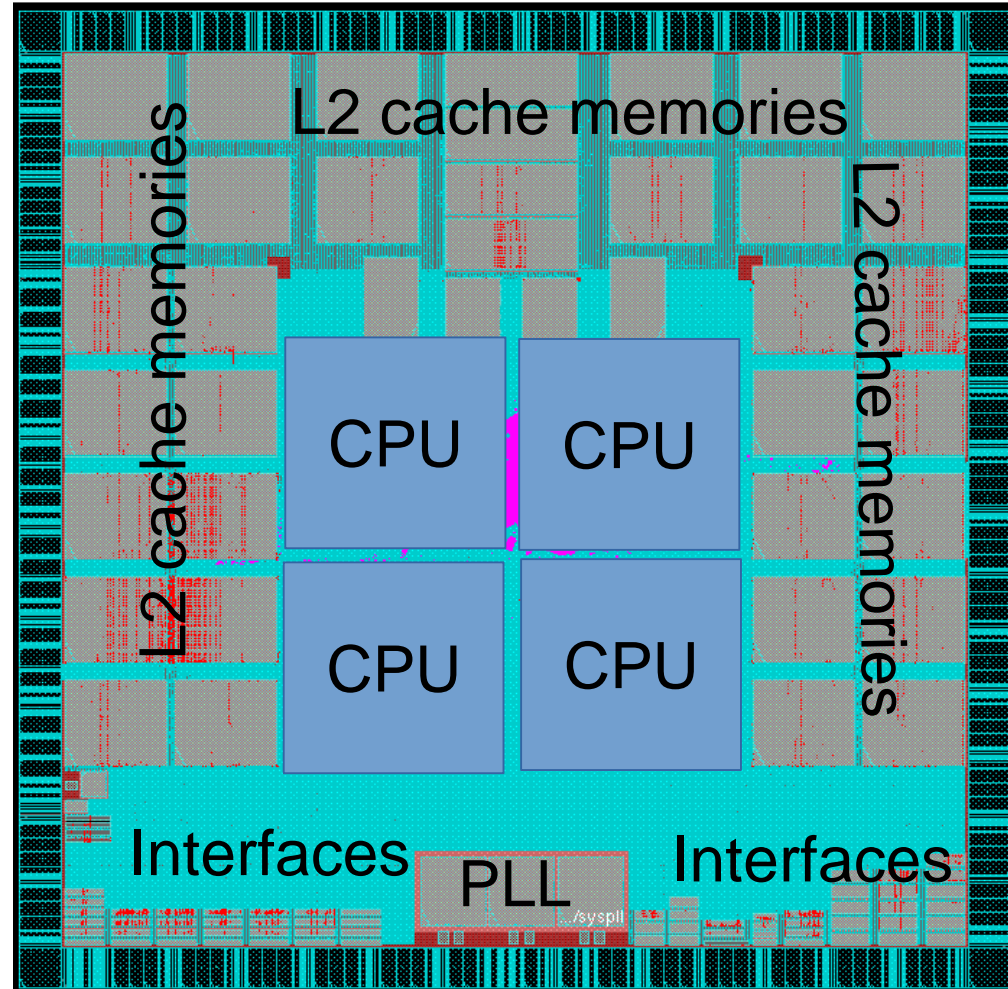
- ST Microelectronics 65 nm

Goal: 10x AT697 performance



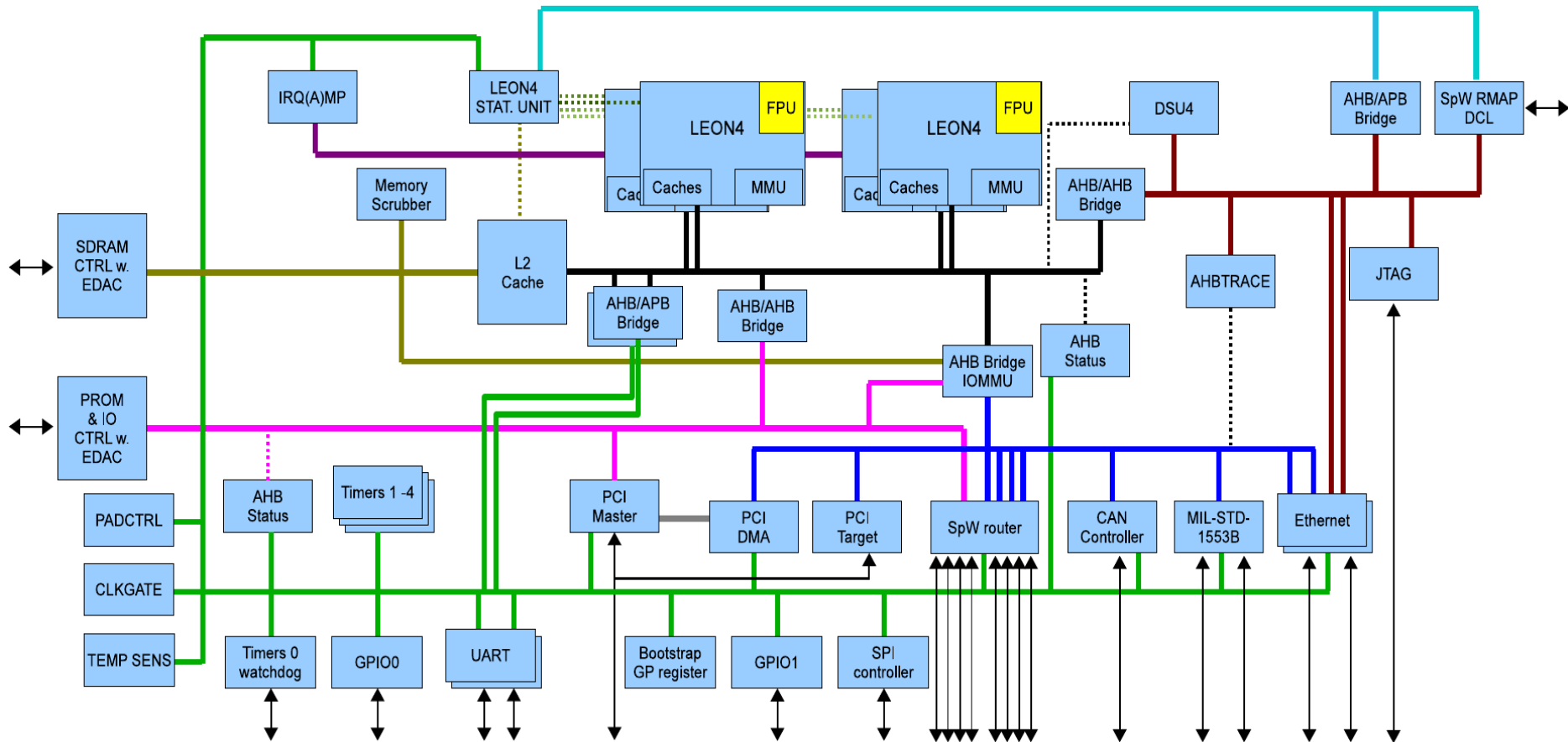
GR740 Trade-Offs

- Traded specification taking into account technology constraints and capabilities
- Increased L2 cache size 2 Mbyte
- Improved performance counters to ease execution time analysis
- L2 cache controller split support to reduce inter-core interference
- Sign-off frequency 250 MHz (WC)
- $4 \times 250 \text{ MHz} = 10 \times 100 \text{ MHz}$
 - We reach our goal (10xAT697)
- Pin multiplexing to reduce pin count
 - PROM with UART, CAN, 1553 and SPW debug ports
 - Half of SDRAM port multiplexed with PCI and one of 2 Ethernet ports



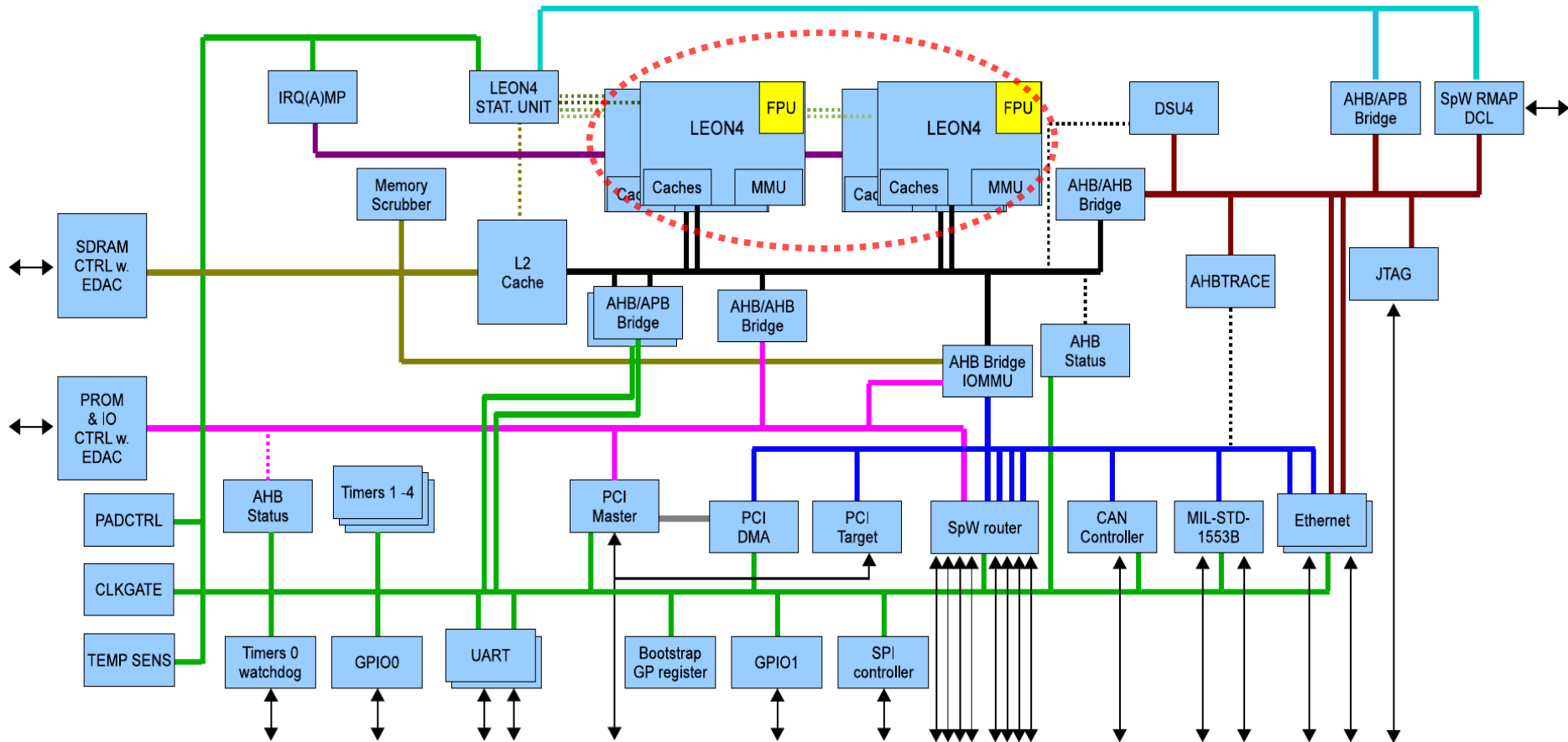
Chip area $\sim 8.4 \times 8.7 = 73 \text{ mm}^2$

GR740 Block Diagram



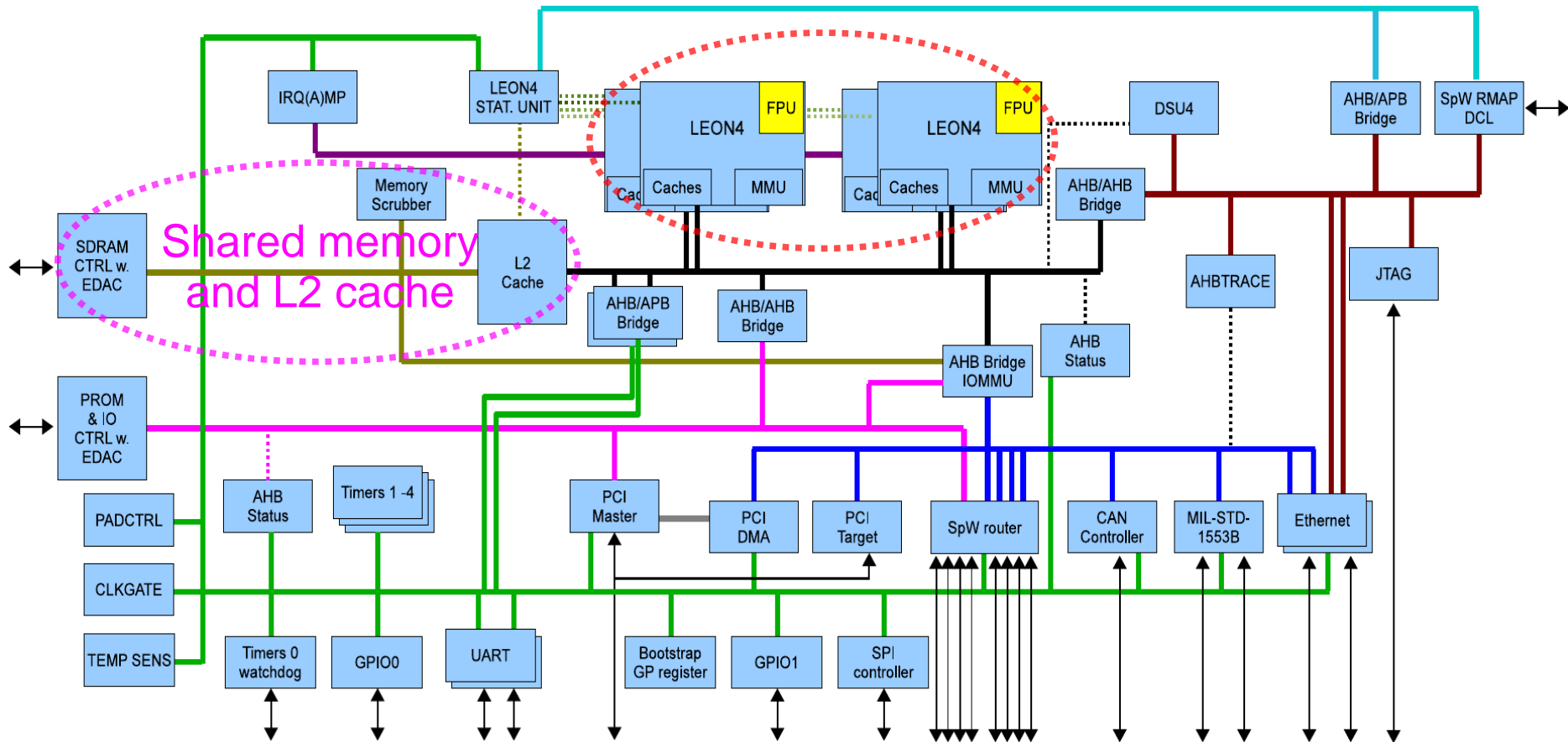
GR740 Block Diagram

4 CPU cores with FPU and L1 cache



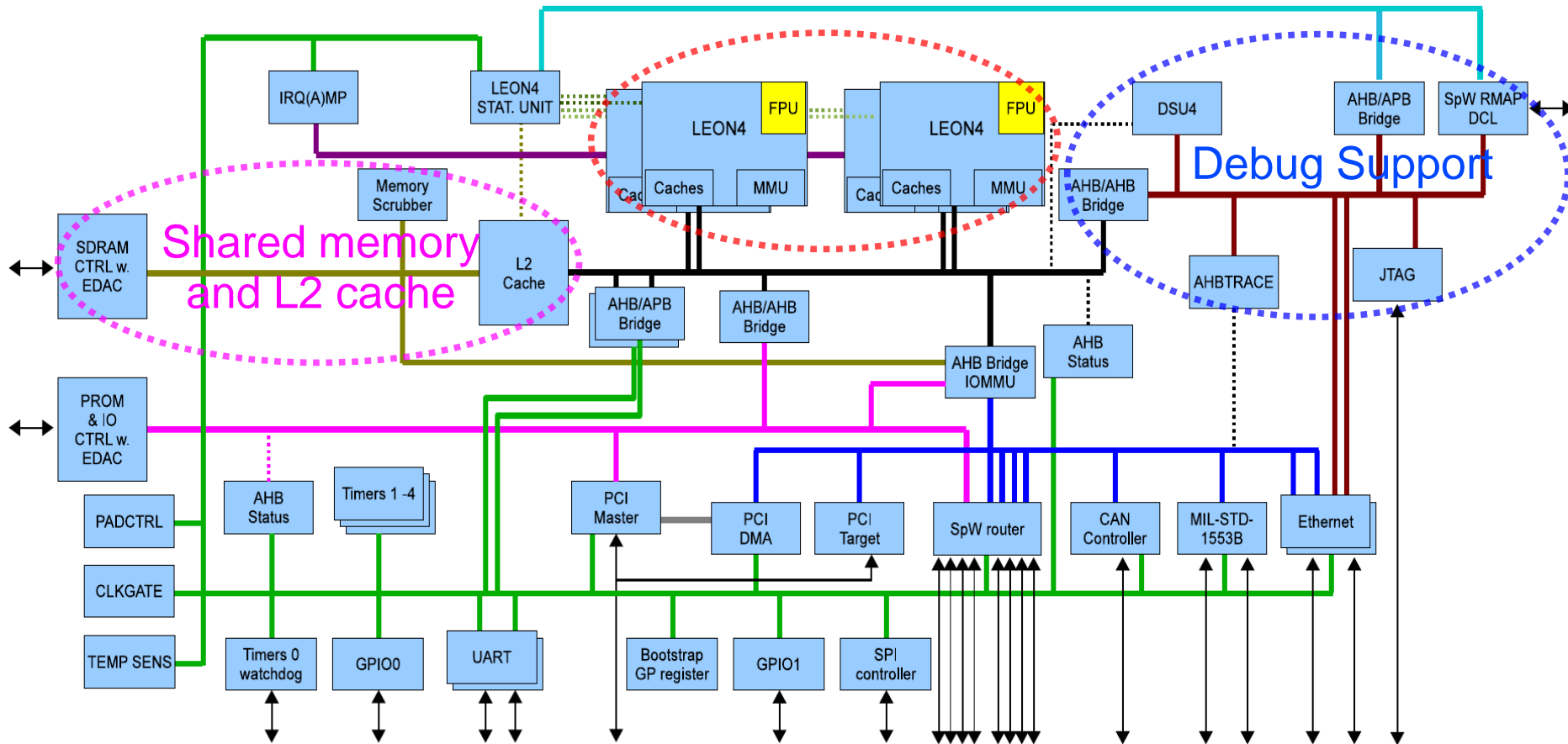
GR740 Block Diagram

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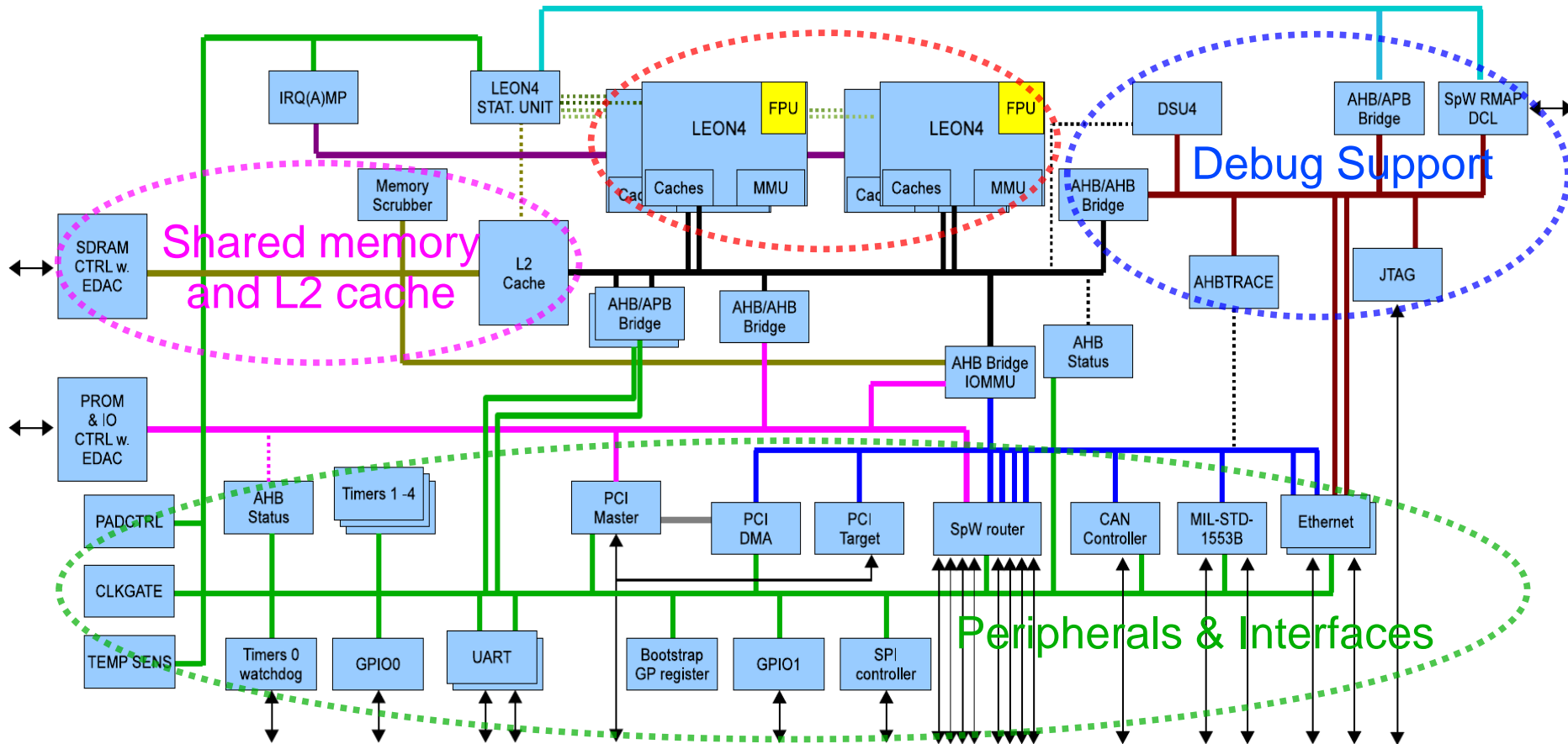
GR740 Block Diagram

4 CPU cores with FPU and L1 cache

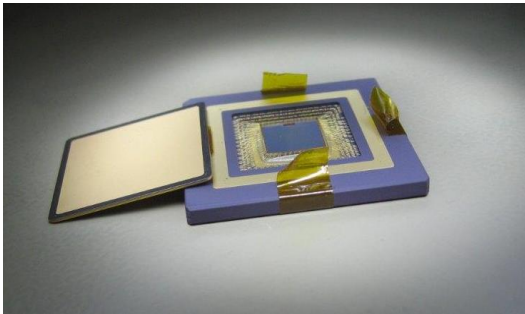


GR740 Block Diagram

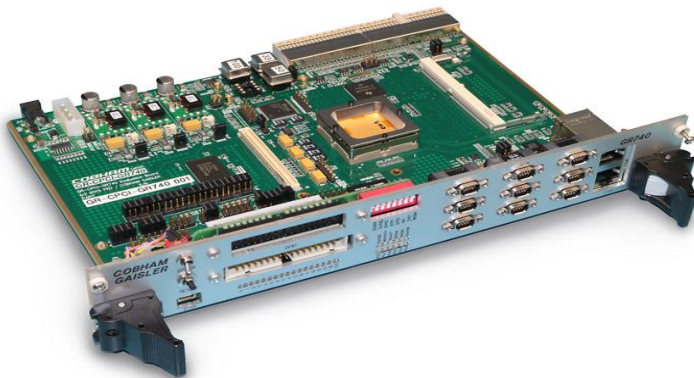
4 CPU cores with FPU and L1 cache



GR740 : more information



GR740 prototypes currently (Q1/2016) under test in evaluation board



COBHAM

Cobham Gaisler AB provides IP cores and supporting development tools for embedded processors based on the SPARC architecture. We specialize in digital hardware design for both commercial and aerospace applications

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COBHAM GAISLER AB

AMICSA & DSP Day
June 12-16, 2016, Gothenburg, Sweden
Hosted by Cobham Gaisler and supported by ESA

NEWS & EVENTS

Latest Releases

- GR712RC user's manual 2.7
- GR712RC data sheet 2.3
- GR712RC-BOARD document 0.7
- LEON3FT-RTAX document 1.9
- RT-SPW-ROUTER document 1.2
- GR740 user's manual 1.3
- GRLIB IP Library 1.5.0-b4164
- GRMON Debug Monitor 1.1.61
- Nucleus support for LEON
- GRMON2 Debug Monitor 2.0.71
- TSIM2 LEON/ERC32 Simulator 2.0.43
- GRSIM LEON MP Simulator 1.1.54
- BCC Bare-C Compiler 1.0.45
- RCC RTEMS Compiler 1.2.18
- VxWorks 6.9 support for LEON
- VxWorks 6.7 support for LEON
- GRTools installer 2015-01-21

Rad-Hard Quad-Core System-on-Chip

Quad-Core LEON4-FT

GR740 Quad-Core LEON4-FT Processor, 1000 MIPS, 1000 MFLOPS

GR740 SoC in LGA-625

GR740 Development Board

GR712RC CQFP-240

GR712RC Development Board

BRAVE: Big Re-programmable Array for Versatile Environments

- Main Goal:

Provide to the Space Industry a High-capacity, high-performance radiation hardened reprogrammable European FPGA

- Main motivation:

- ✓ Competitive FPGA **capacity**, **performance** and **radiation hardness** to be used in a wide range of space equipment across all ESA missions in Science, Exploration, Earth Observation, Telecom and Navigation. Also in Launchers and Human Spaceflight.
- ✓ FPGA unlimited **re-programmability** extra advantage: enable **re-configurable** and **adaptive** systems; and also **reduces impacts** in the (frequent) event of unexpected design changes or modification

BRAVE – Introduction and General objectives

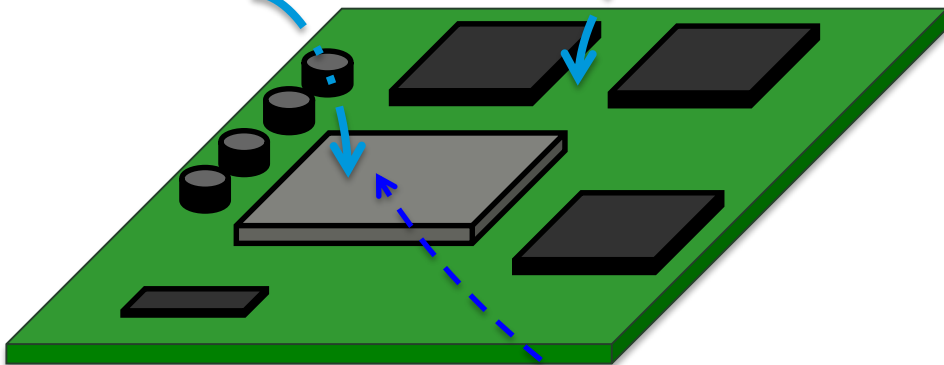


- Extra motivations/ considerations:
 - **FPGA cost advantages:**
 - FPGAs offer shorter development times, simpler, less expensive design and manufacturing phases than Application Specific Integrated Circuits (ASICs).
 - Equipment suppliers (including SMEs) have access to FPGAs and often cannot afford advanced ASIC technologies
 - **Reduce dependency** on USA EAR/ITAR FPGA key components
 - Extend and keep the **European Competence** to develop FPGAs and capability to specify and develop **future** FPGA products for space.

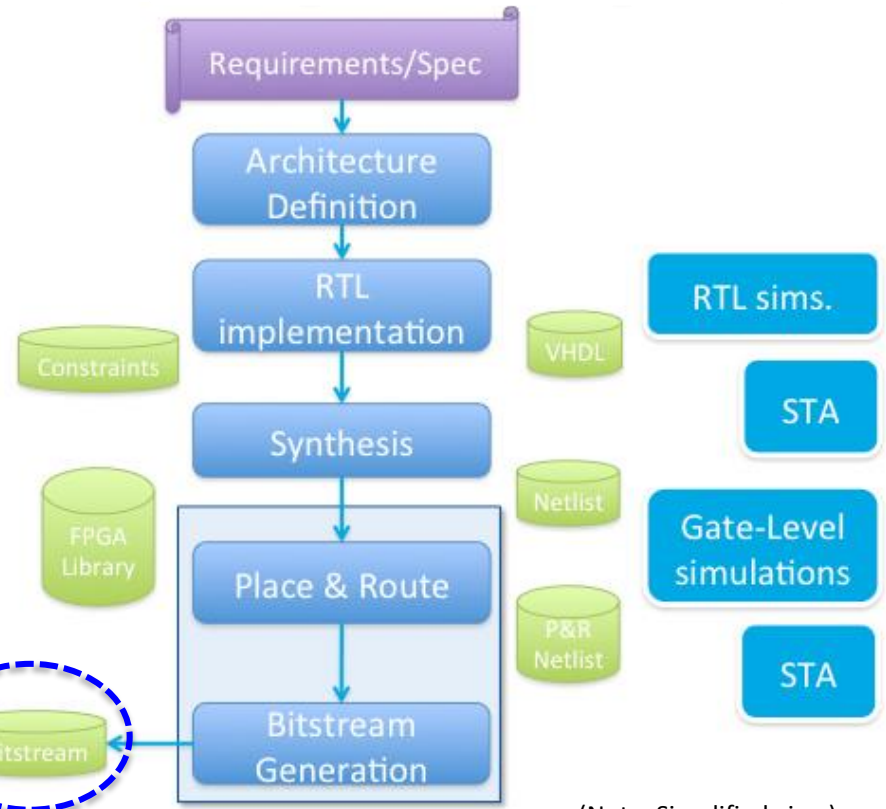
Evaluation Kit (EK)

FPGA Component

EK Board



FPGA Design Flow (FPGA Tools)



(NB: the figure does not represent the final board design)

ESA Presentation | Ph. Armbruster | ESTEC | 03/03/2016 | D/TEC | Slide

ESA UNCLASSIFIED - For Official Use

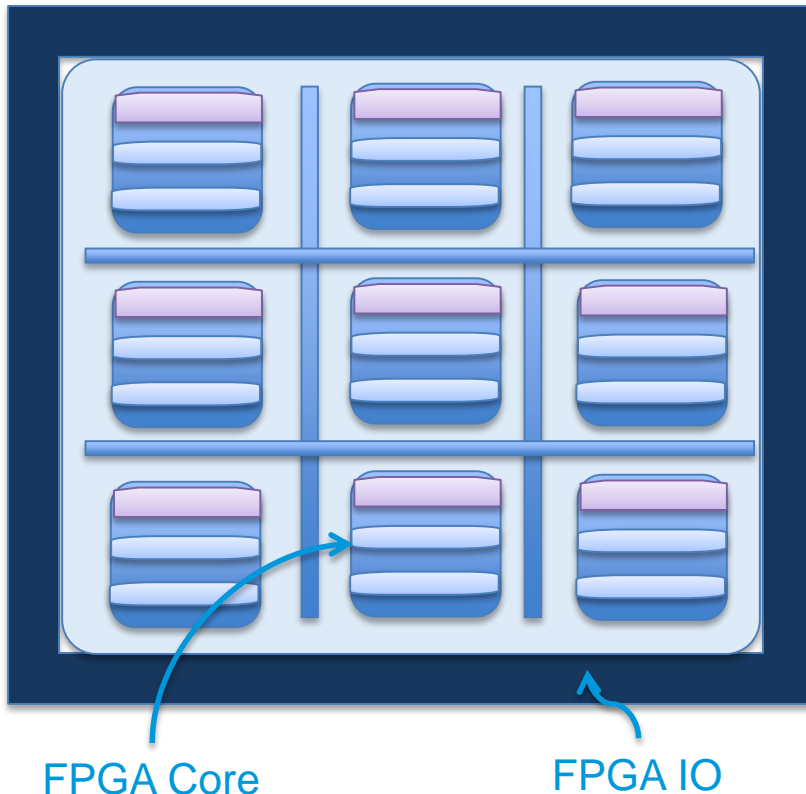
(Note: Simplified view)

➤ The FPGA architecture is based on **TILES** that have the following elements:

- Clusters of Look-Up Tables (**LUTs**): based on 4-inputs LUT + DFF
- **Memory block** blocks:
DP-RAM: based on 48Kb RAM blocks
Register Files: 64x16bits
- **DSP** blocks:
based on 18x18 bits multiplier
- **Interconnect**:
Innovative interconnect that allows high density.

➤ The FPGA includes also:

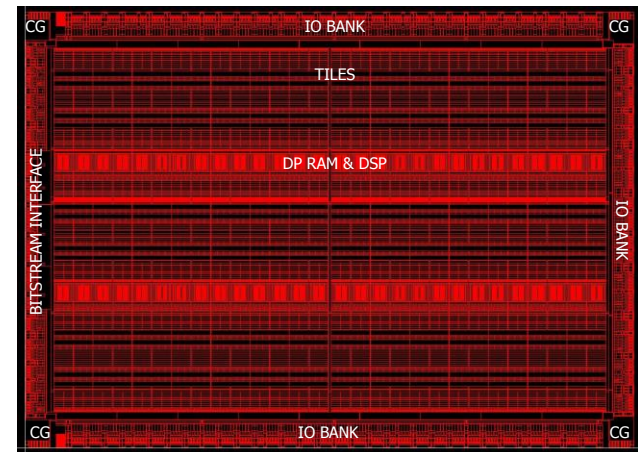
- Multi-standard configurable IOs
- **PLLs**
- Configuration logic with **internal self-check** (rad-hard)



NG-MEDIUM overview, first FPGA of BRAVE

- First BRAVE rad-hard FPGA developed in 65nm
- Unlimited re-configurability (SRAM-based FPGA)
- Key milestone:
 - First silicon and FPGA tools available for end-user: **Mid -2016**
- Configurable by SpaceWire (and other serial/ parallel options)
- Build-in(*) EDAC for Internal memory RAM blocks
- Build-in(*) CMIC ("Configuration Memory Integrity Check")
- Hardening performance (expected):
 - TID > 100Krad (300krad tested)
 - Single-Event Latch-Up Immunity (SEL) to $LET_{TH} > 60 \text{ MeV.cm}^2/\text{mg} @125^\circ\text{C}$
- (*)Build-in in Radiation Hardened Logic

Device	NG-MEDIUM
Capacity: ASIC Gates	550 000
Modules	
Register	32 256
LUT-4	34 272
Embedded RAM (Mb)	2,1
Embedded DSP	112
Clocks	24
Embedded Serial Link	
SpaceWire 400Mbps	1
User I/Os	
LGA-625	380
MQFP-352	160



Courtesy: NanoXplore

BRAVE, more public details soon



The first BRAVE FPGA will be officially pre-announced at the **SpacE FPGA Users Workshop (SEFUW)** at ESTEC on the 17th of March:

<https://indico.esa.int/indico/event/130/>

SEFUW: SpacE FPGA Users Workshop, 3rd Edition

15-17 March 2016
European Space Research and Technology Centre

(ESTEC)
Europe/Amsterdam timezone

SEFUW 2016

- Call for Abstracts
 - View my Abstracts
 - Submit Abstract
- Registration
 - Modify my Registration
- Accommodation
- Venue and Practical Information
- Past and Related Events

For information please write to
✉ sefuw@esa.int

All FPGAs share several design methodologies, yet each of them face specific challenges. The anti-fuse FPGAs are currently heavily used in most electronic equipment for space yet there are other emerging technologies too: Flash-based and SRAM-based. The use of COTS FPGA is also increasing; specially for space missions with shorter lifetime and less quality constraints.

The aim of the workshop is to share experiences and wishes among FPGA designers, FPGA vendors and research teams developing methodologies to address radiation mitigation techniques and reconfigurable systems.

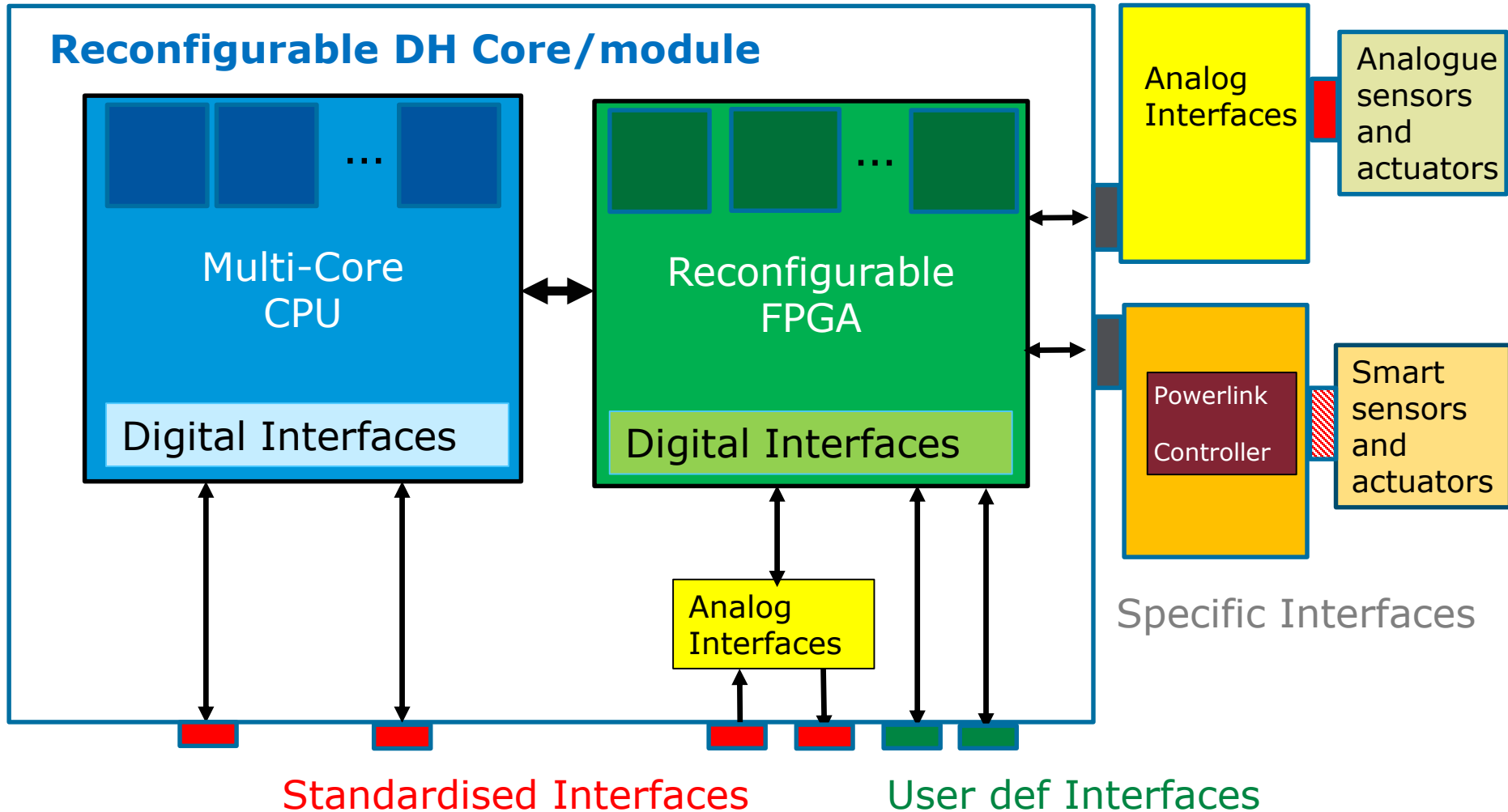
The topics related to FPGAs for space are covering (not limited too):

- general design, verification and test issues and good practices
- performance achievements and potential problems
- power consumption achievements and potential issues
- design tools performance, good practices and potential limitations
- radiation mitigation techniques, tools and potential limitations (avoiding repetitions of what has already been presented at RADECS, NSREC and SEE Symposium)
- trends of FPGA usage in space applications
- reconfigurable systems
- lessons learned: ensuring successful and safe use of FPGA in space applications
- choosing the best FPGA type for our space application
- export license limitations / changes / ITAR / EAR
- package and assembly challenges
- companion non-volatile memory (when required) experience

The FPGA vendors ALTERA, ATMEL, MICROSEMI and XILINX will present updates and will be available for questions.

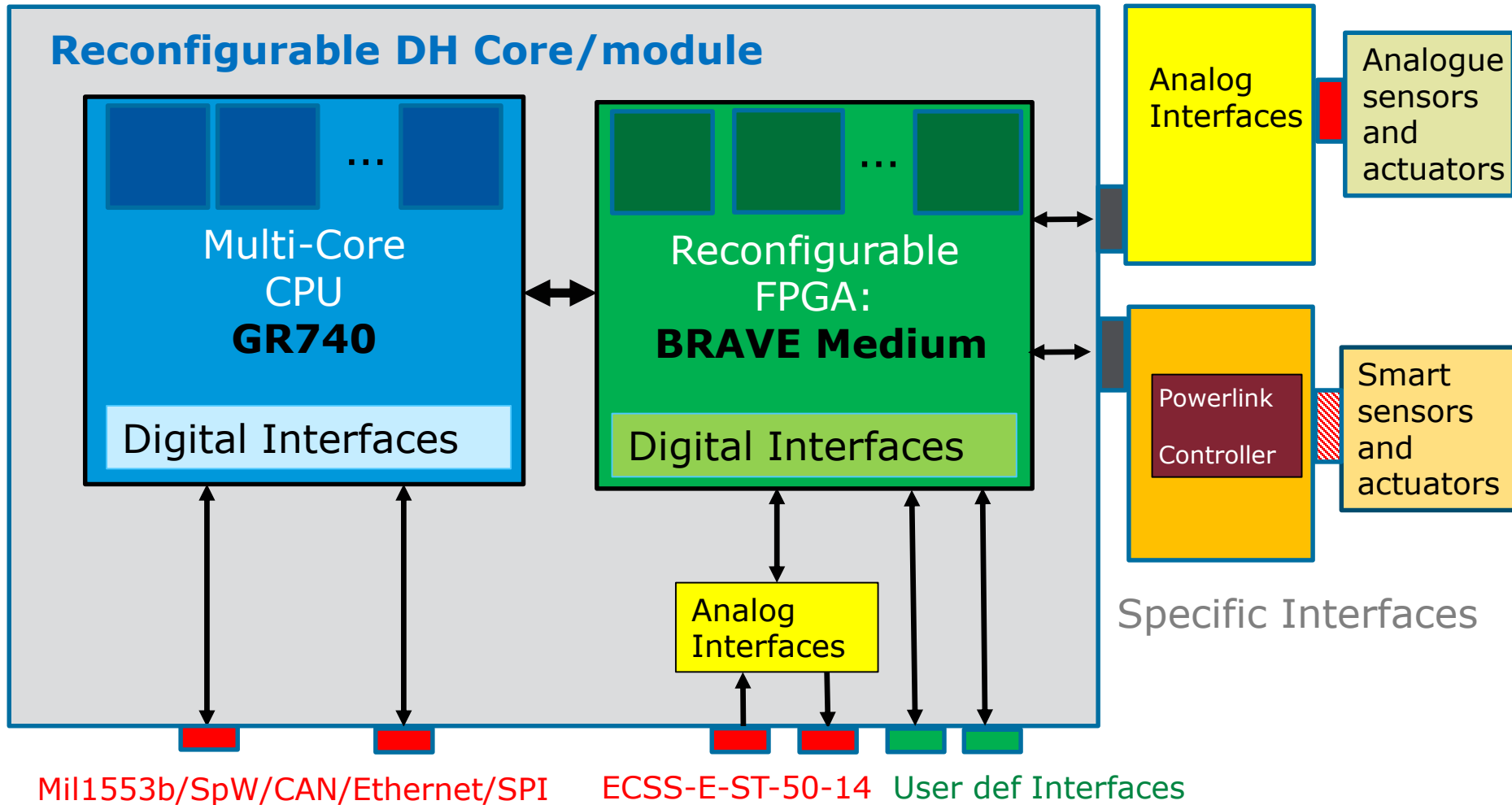
A major update on the European FPGA status will be presented. Presentations from at least the major design groups (Primes) are expected.

Compact Reconfigurable Avionics Concept : Reconfigurable Data Handling core

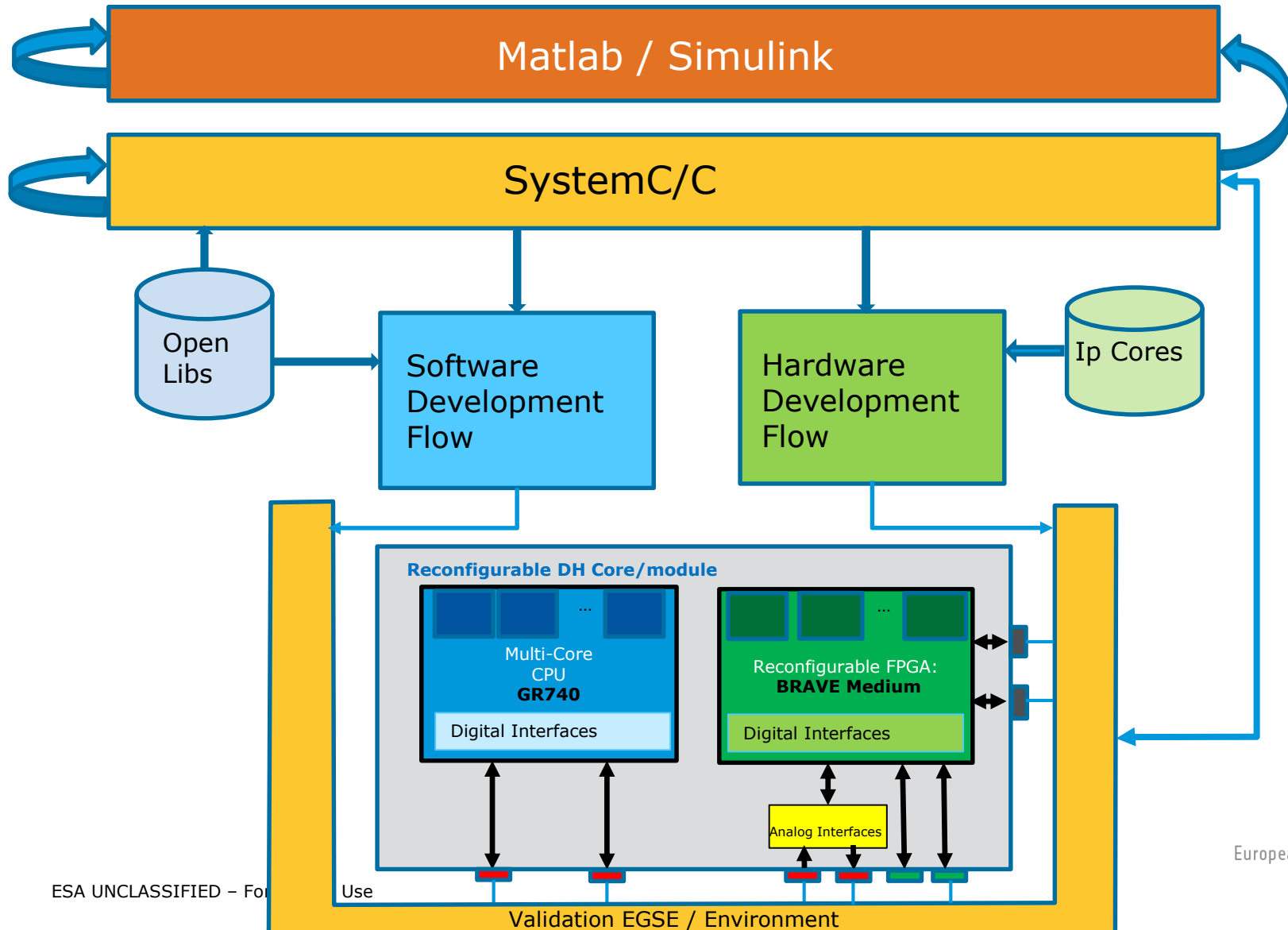


Compact Reconfigurable Avionics: Mk I

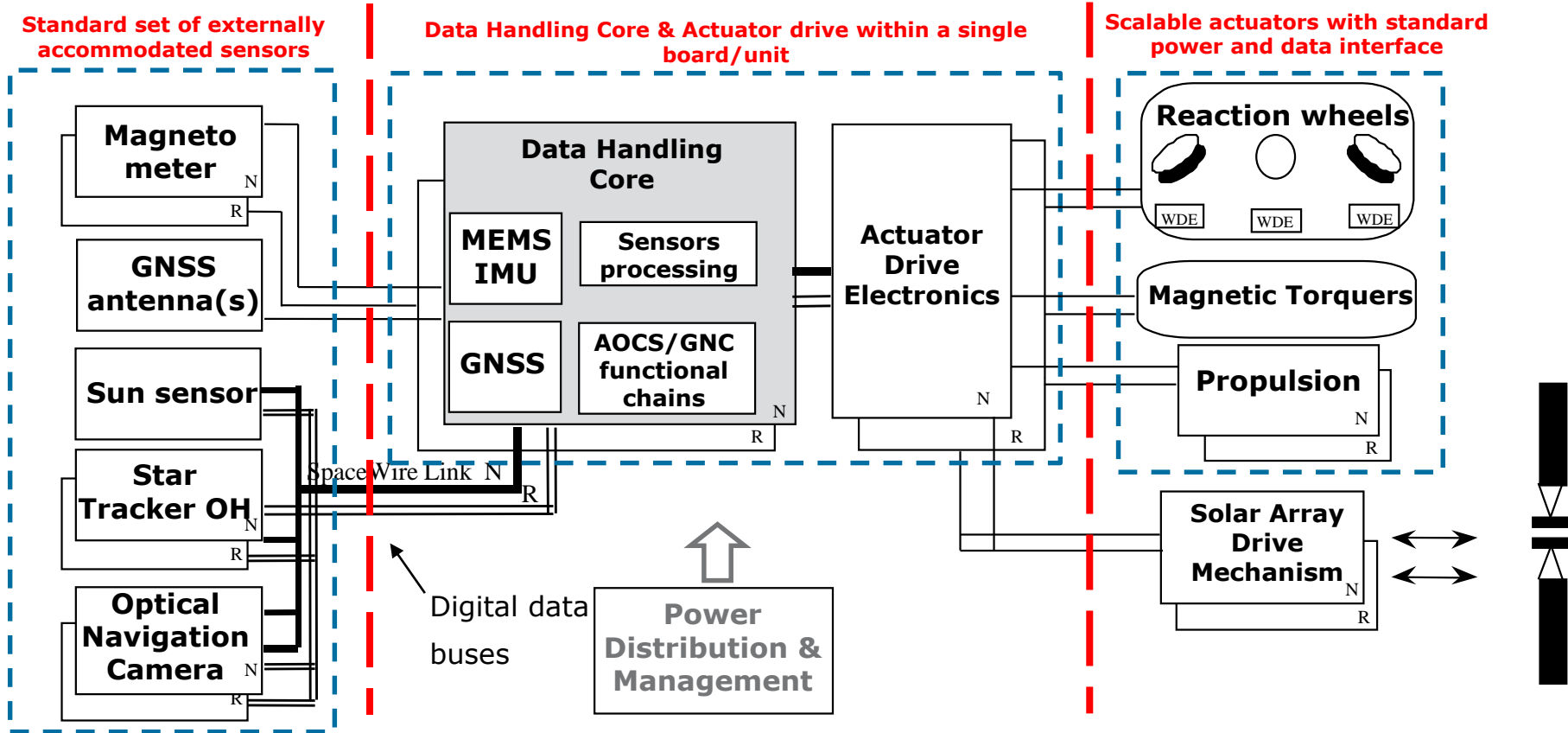
Reconfigurable Data Handling core



Compact Reconfigurable Avionics: Mk I Development flow



Compact Reconfigurable Avionics: Smart AOCS & GNC Elements



Candidate sensors:

FaintStar-based Star Tracker, MEMS-based IMU, Sun sensor on a chip, Navigation on a chip

Applications:

LEO Earth Observation, LEO Telecom, Exploration, In-orbit servicing

Concepts:

SAVOIR-SAFI, Spacewire AOCS prototyping, Time and Space partitioning

A good design of complex VLSI components starts by a proper and in depth analysis of its field of application

Microprocessors and re-programmable FPGAs are playing an increasingly important role for on-board Electronics

GR740 Leon-4 based processors and BRAVE FPGAs pave the ... European way ... to Adaptive Avionics

Acknowledgments to many ESTEC colleagues, R. Weigand and D. Merodio and also to Cobham Gaisler, NanoXplore teams and ST Microelectronics