Advanced Concepts and Components for adaptive Avionics

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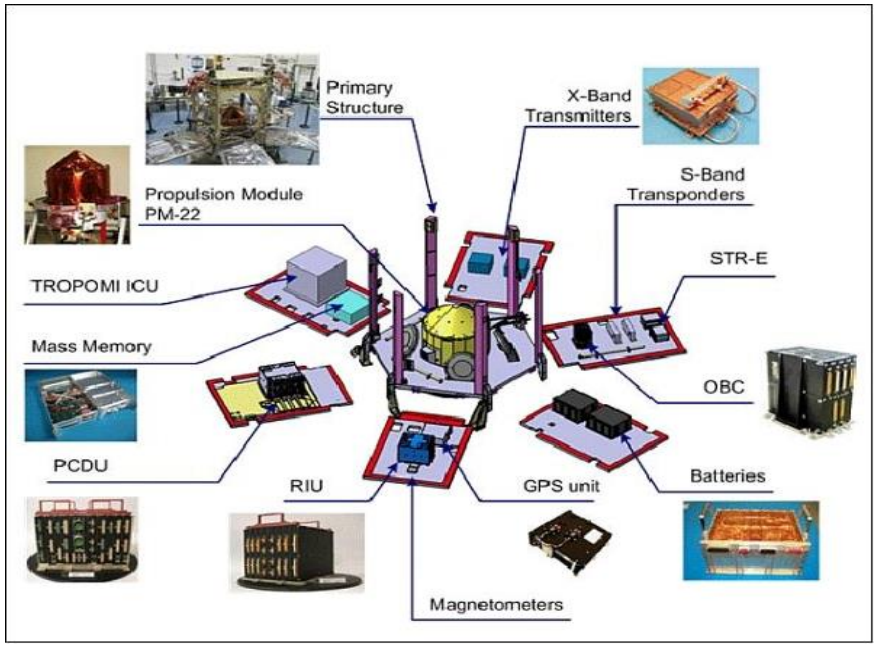
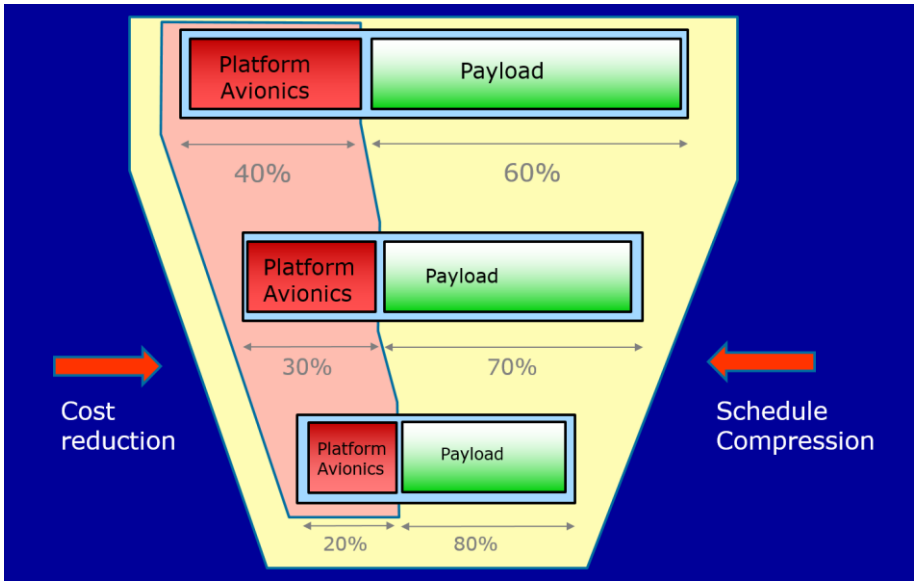
AVIONICS : Cost reduction as a challenge

AVIONICS include:

- **Data Handling – TM/TC**
- **Attitude and Orbit Control - FDIR**
- **Central Software – embedded SW**



Additional constraint :
more € for the Payload …
Less for Avionics !



Avionics : How to reduce the cost ?

- ✓ Through generic platforms ?
  - Astrobus, Spacebus, small GEO, Alphabus, Neosat

- ✓ Thanks to a higher level of recurrence, by reusing existing designs, Building blocks and components

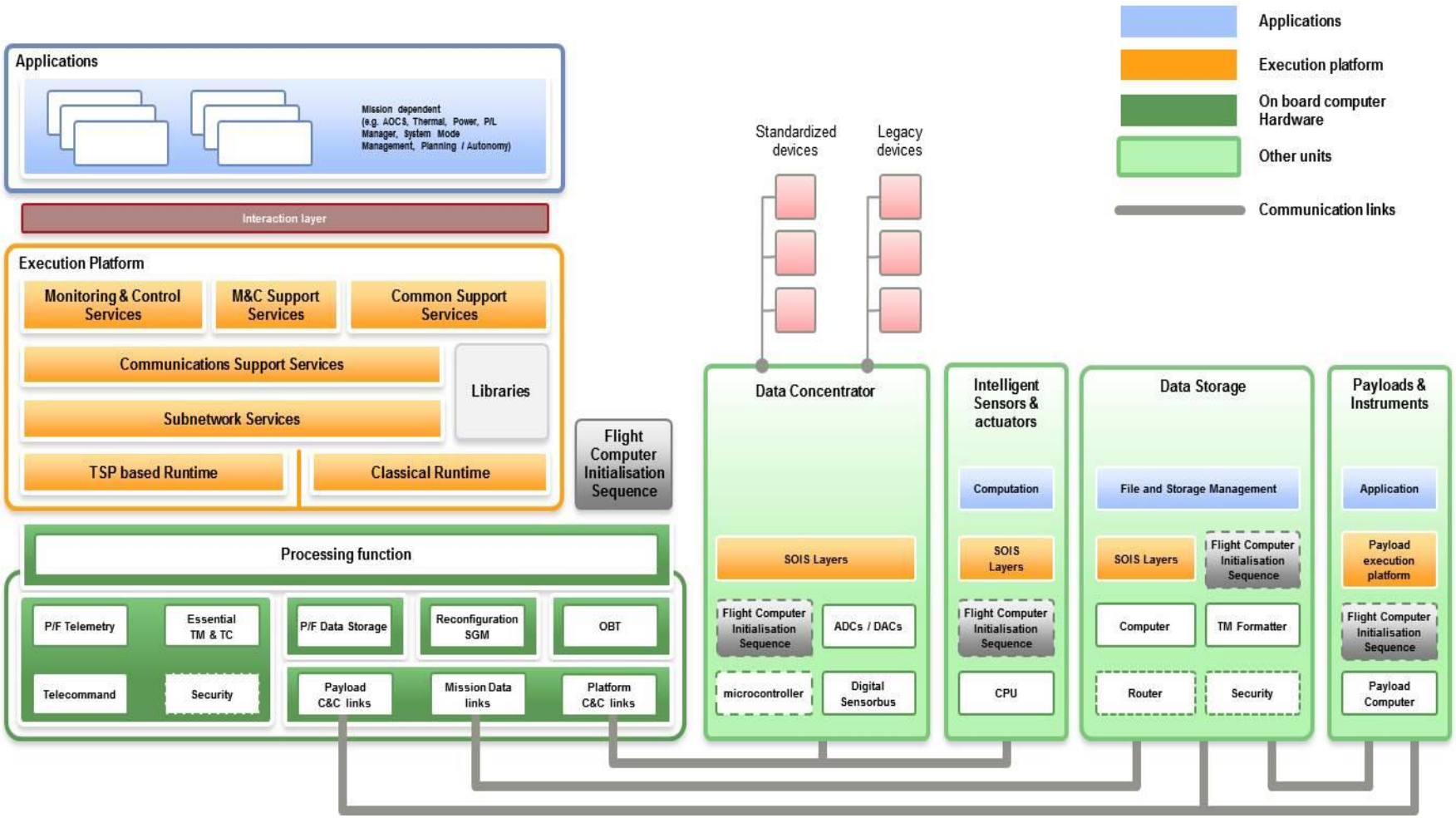
- ✓ Via "more standardized" Avionics
  Space
  AVionics
  Open **- I**nterfaces
  A**R**chitecture

SAVOIR
space avionics open interface architecture

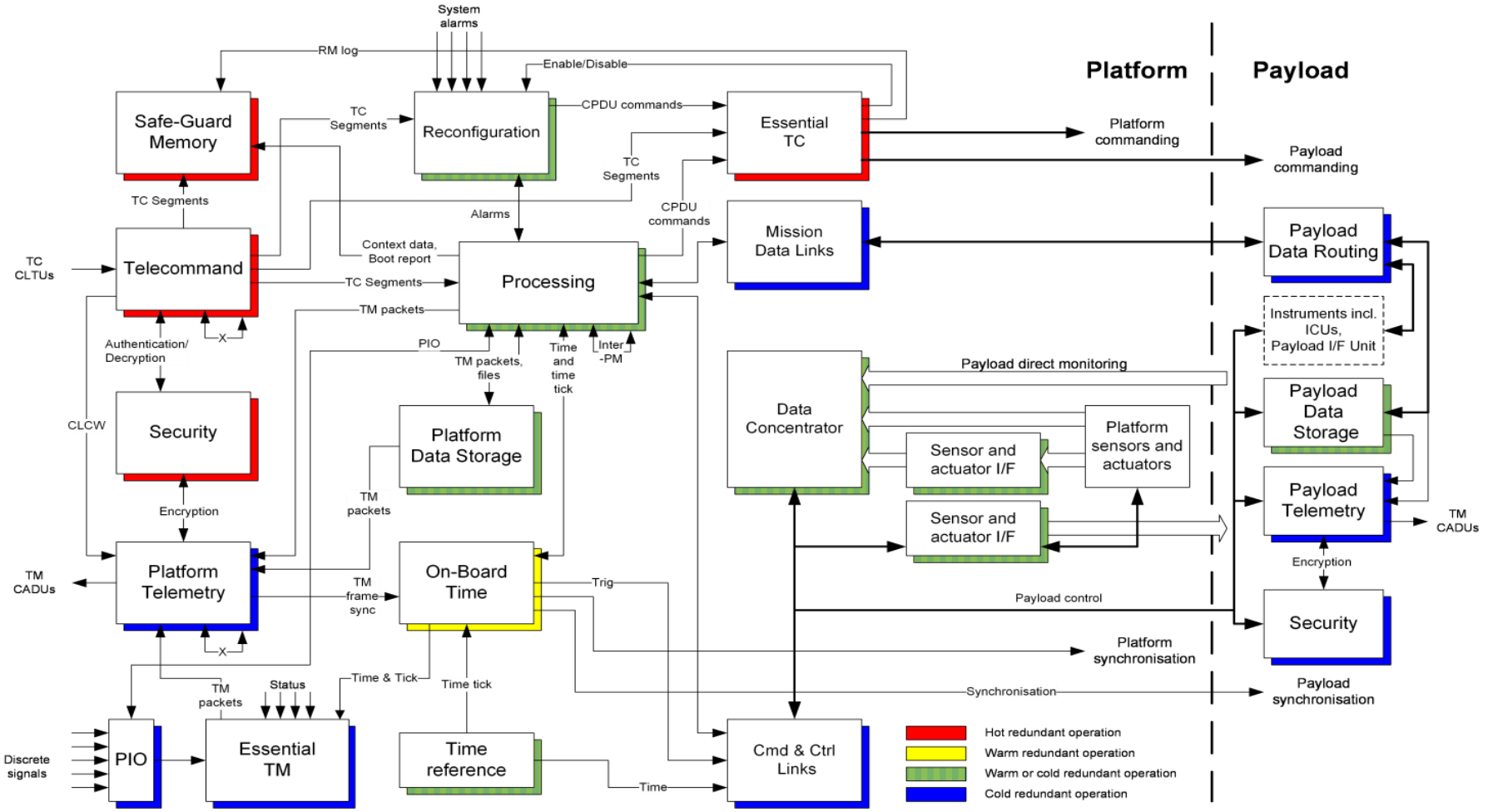
- ✓ By making tailoring of Data Systems easier:

Advanced Concepts and Components for Adaptive Avionics

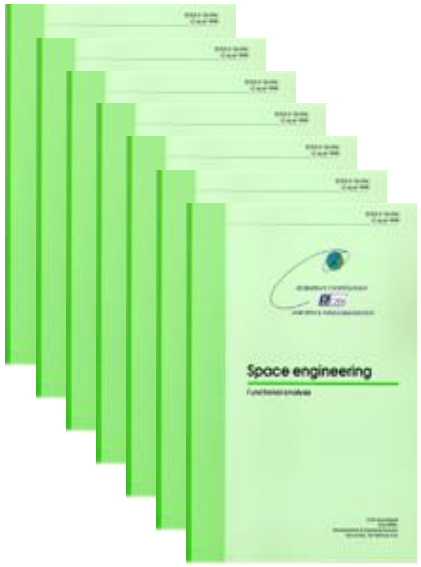
SAVOIR : Reference Architecture



SAVOIR Functional Reference Architecture
Generic Specifications for OBCs, RTUs and Mass Memories



SAVOIR : Standardised Interfaces, Services and Protocols



New interfaces:

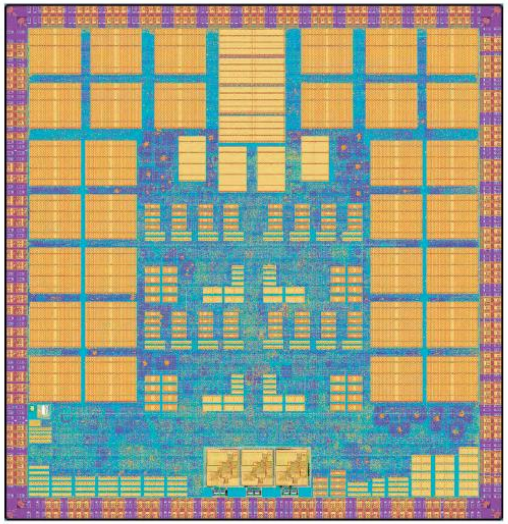
- Sensor buses, I2C, SPI
- PowerLinks

Enhanced Networks:

- Time Triggered Ethernet
- SpaceWire-D
- SpaceFibre

Building blocks

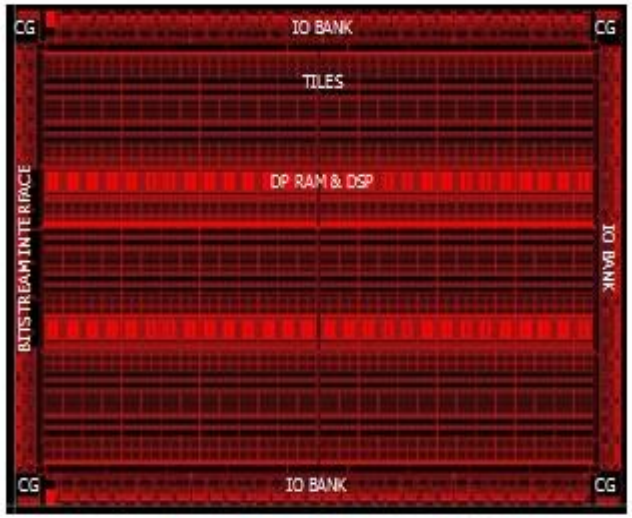
ESA's Next Generation Microprocessor



GR740 Quad-Core LEON4FT - www.gaisler.com/GR740

Prototypes available in 2016

ESA's Next Generation FPGA



Courtesy: NanoXplore

In cooperation with CNES

History of ESA Microprocessor Developments

MA 31750 (Dynex Semiconductor)
- MIL-STD-1750A architecture
- GEC-Plessey 1.5 µm

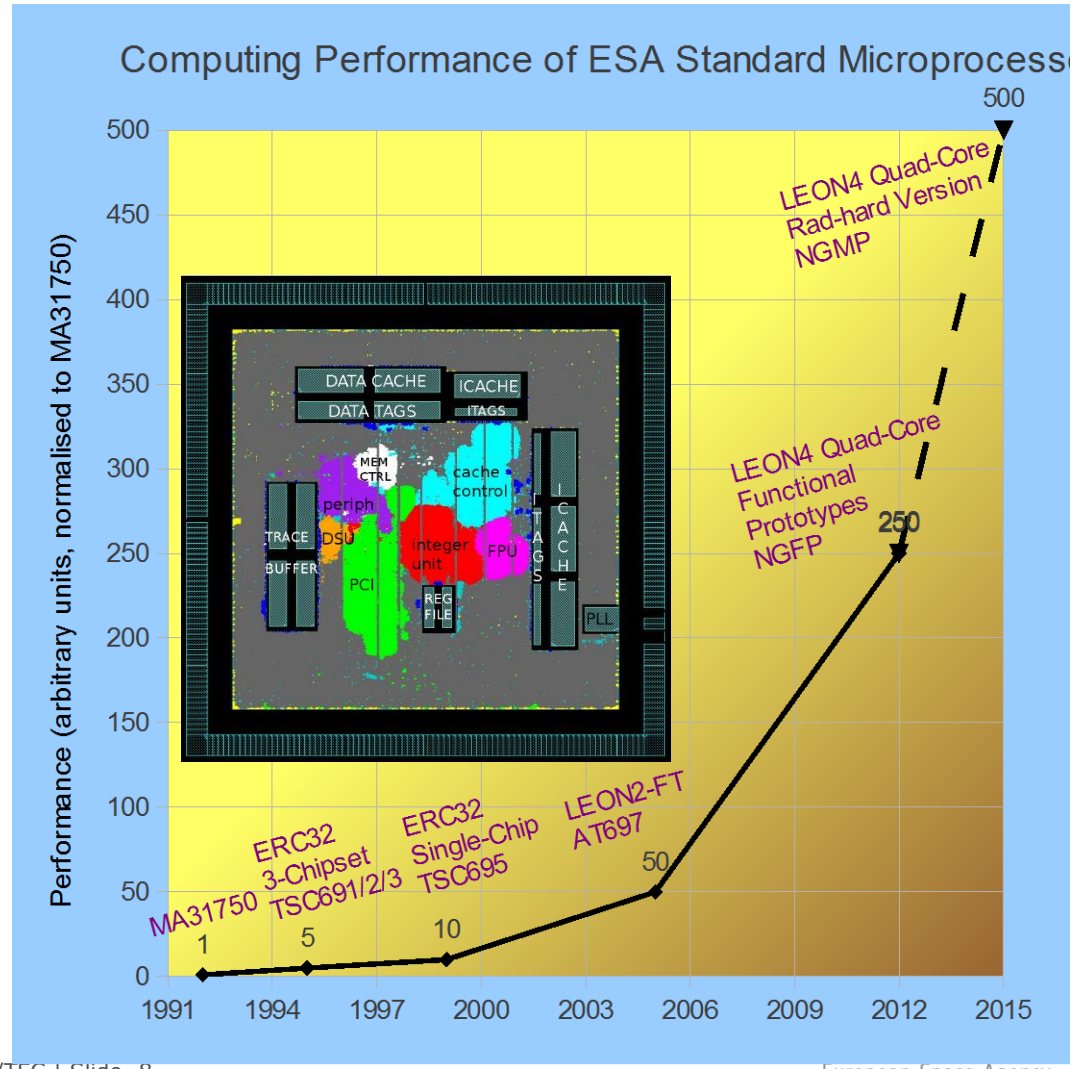
SPARC V7 ERC32 3-chipset
- IU, FPU, MEC: "TSC691 , 692, 693"
- Temic 0.8 µm

SPARC V7 ERC32 single chip
- Temic 0.5 µm – "TSC695"

SPARC V8 LEON2 – "AT697"
- Atmel 0.18 µm

SPARC V8 LEON4/NGMP – "GR740"
- ST Microelectronics 65 nm

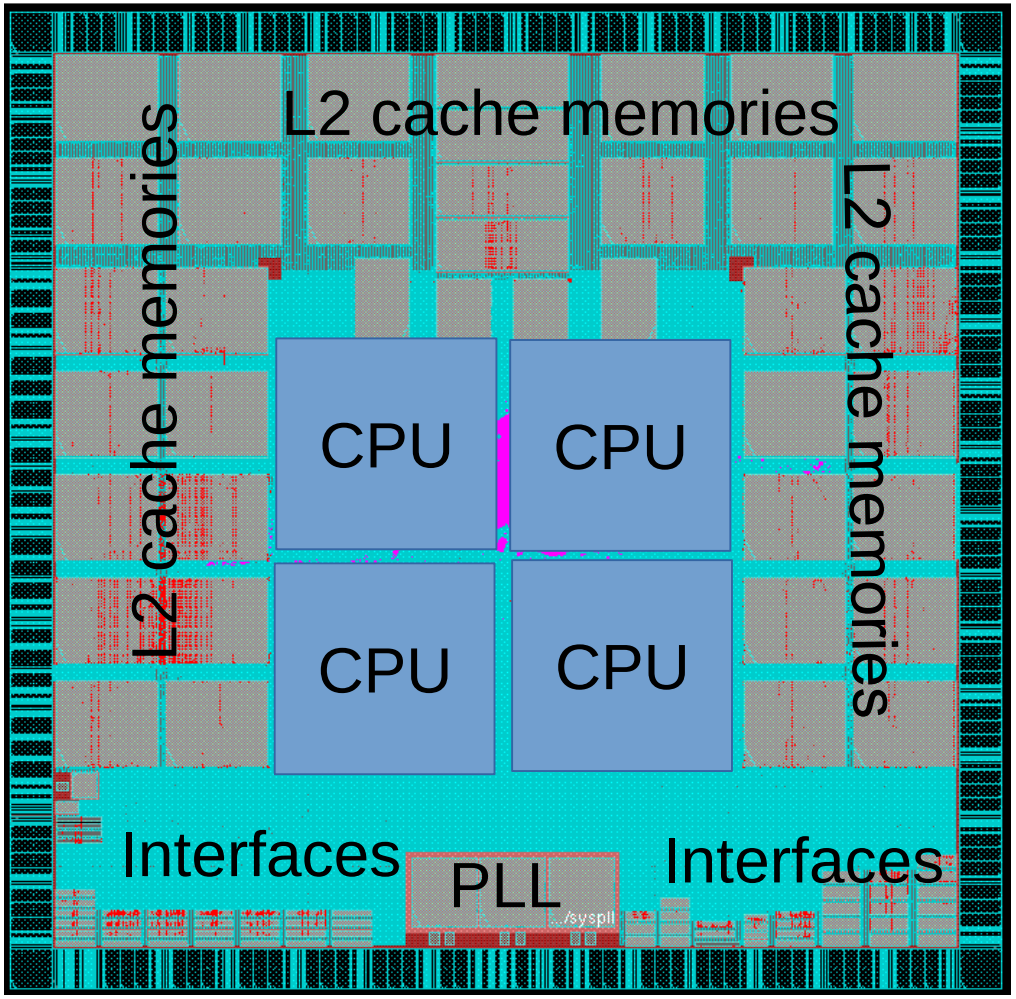
Goal: 10x AT697 performance



GR740 Trade-Offs

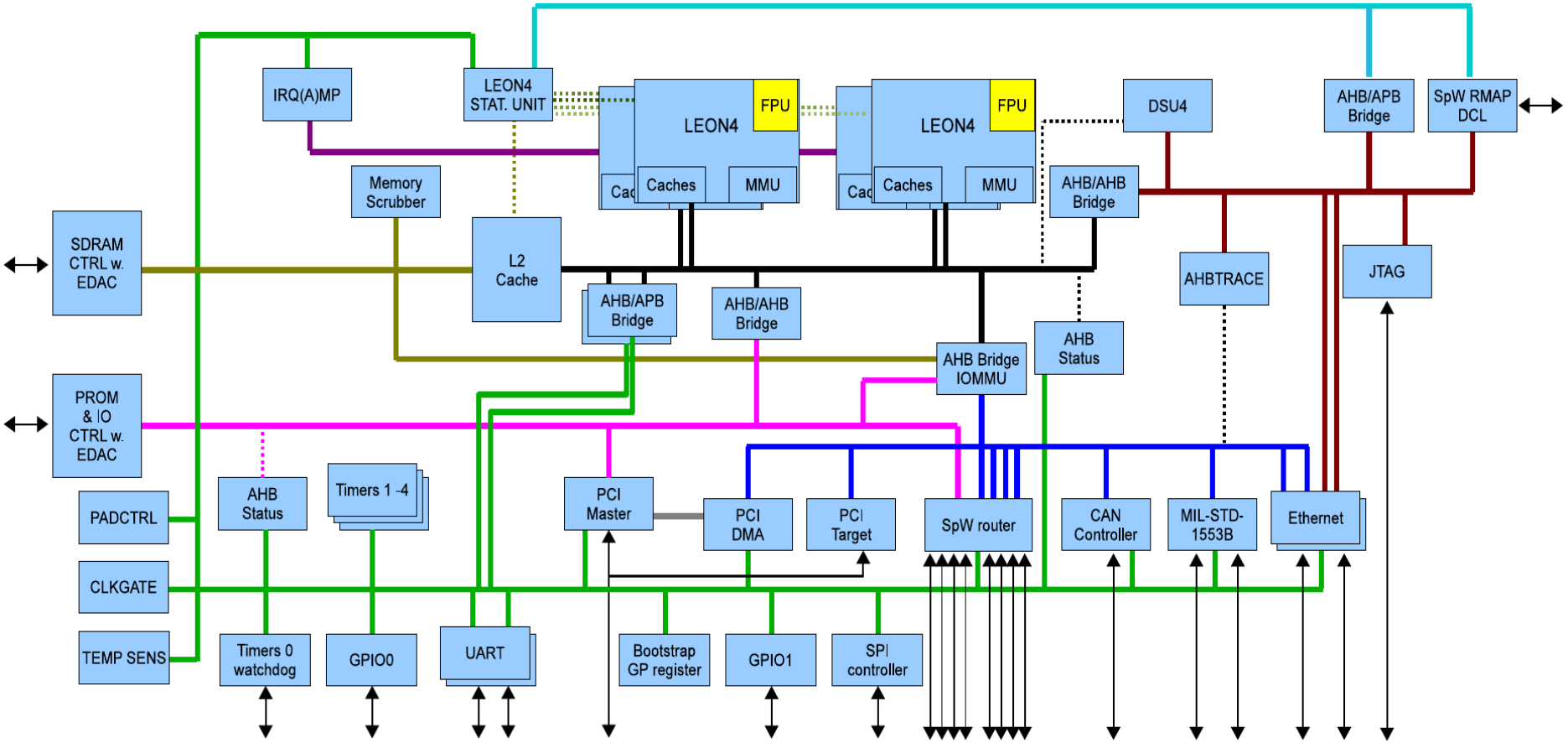
- Traded specification taking into account technology constraints and capabilities
- Increased L2 cache size 2 Mbyte
- Improved performance counters to ease execution time analysis
- L2 cache controller split support to reduce inter-core interference
- Sign-off frequency 250 MHz (WC)
- 4x250 MHz = 10x100 MHz

  → We reach our goal (10xAT697)
- Pin multiplexing to reduce pin count
  - PROM with UART, CAN, 1553 and SPW debug ports
  - Half of SDRAM port multiplexed with PCI and one of 2 Ethernet ports

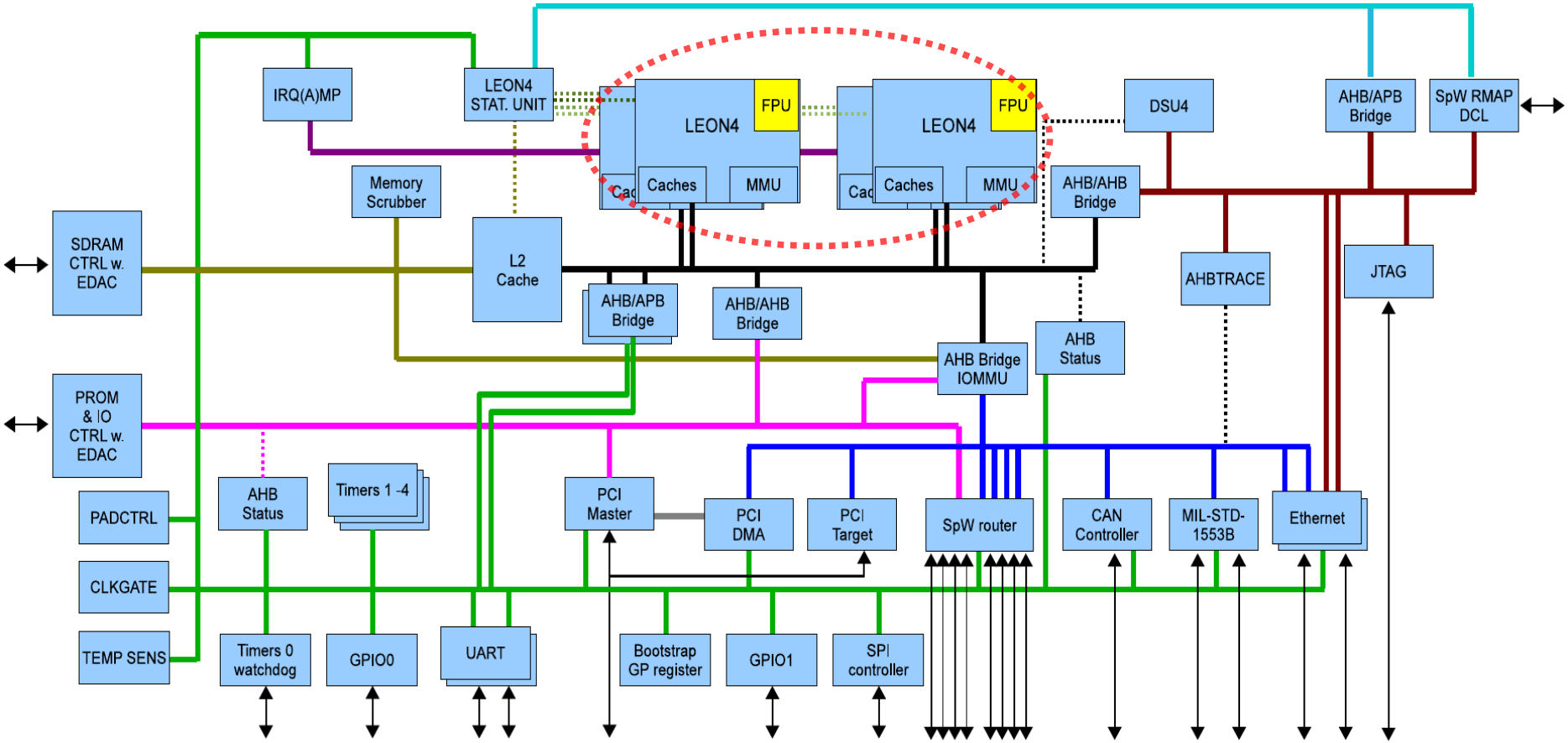


Chip area ~ 8.4 x 8.7 = 73 mm²

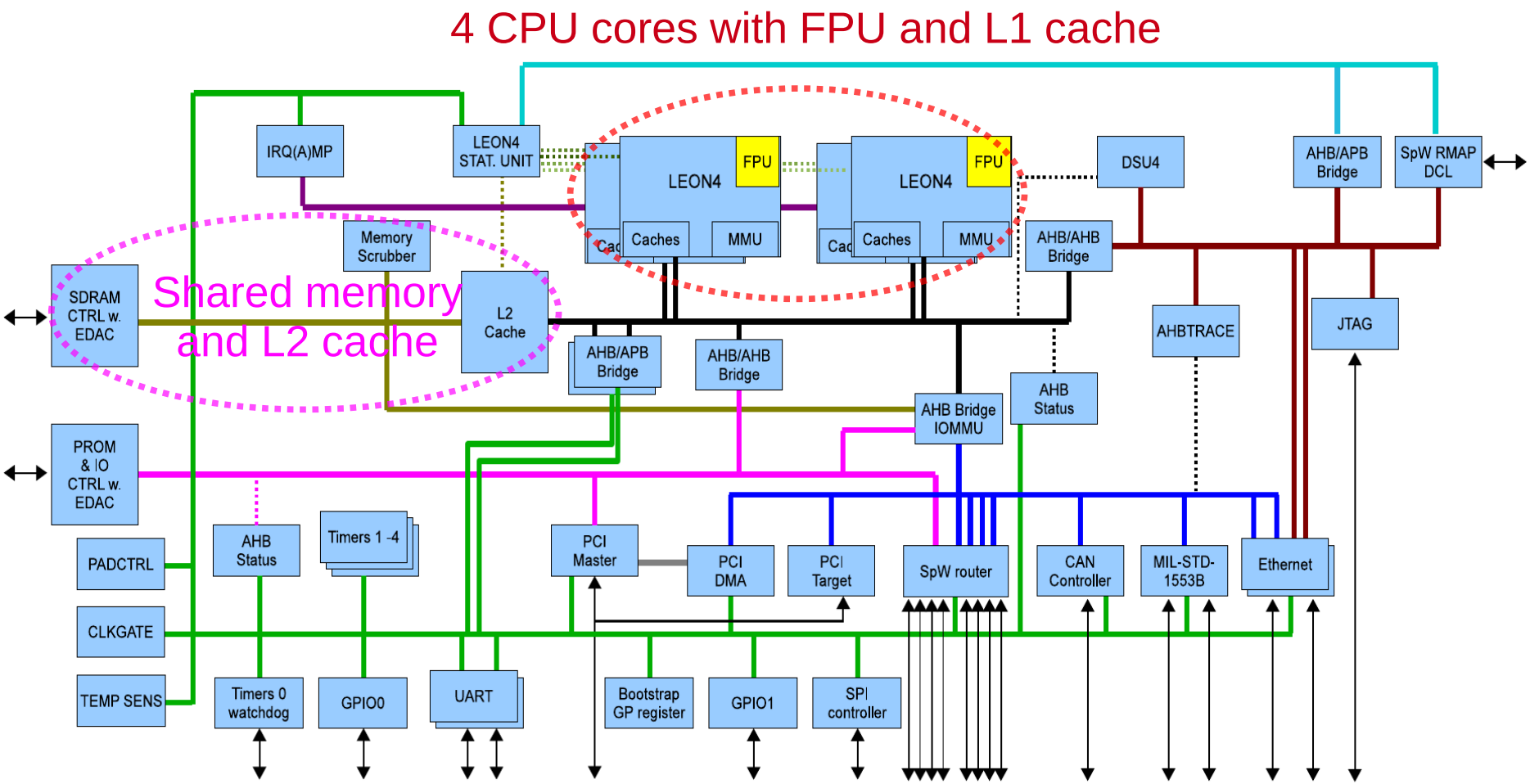
GR740 Block Diagram



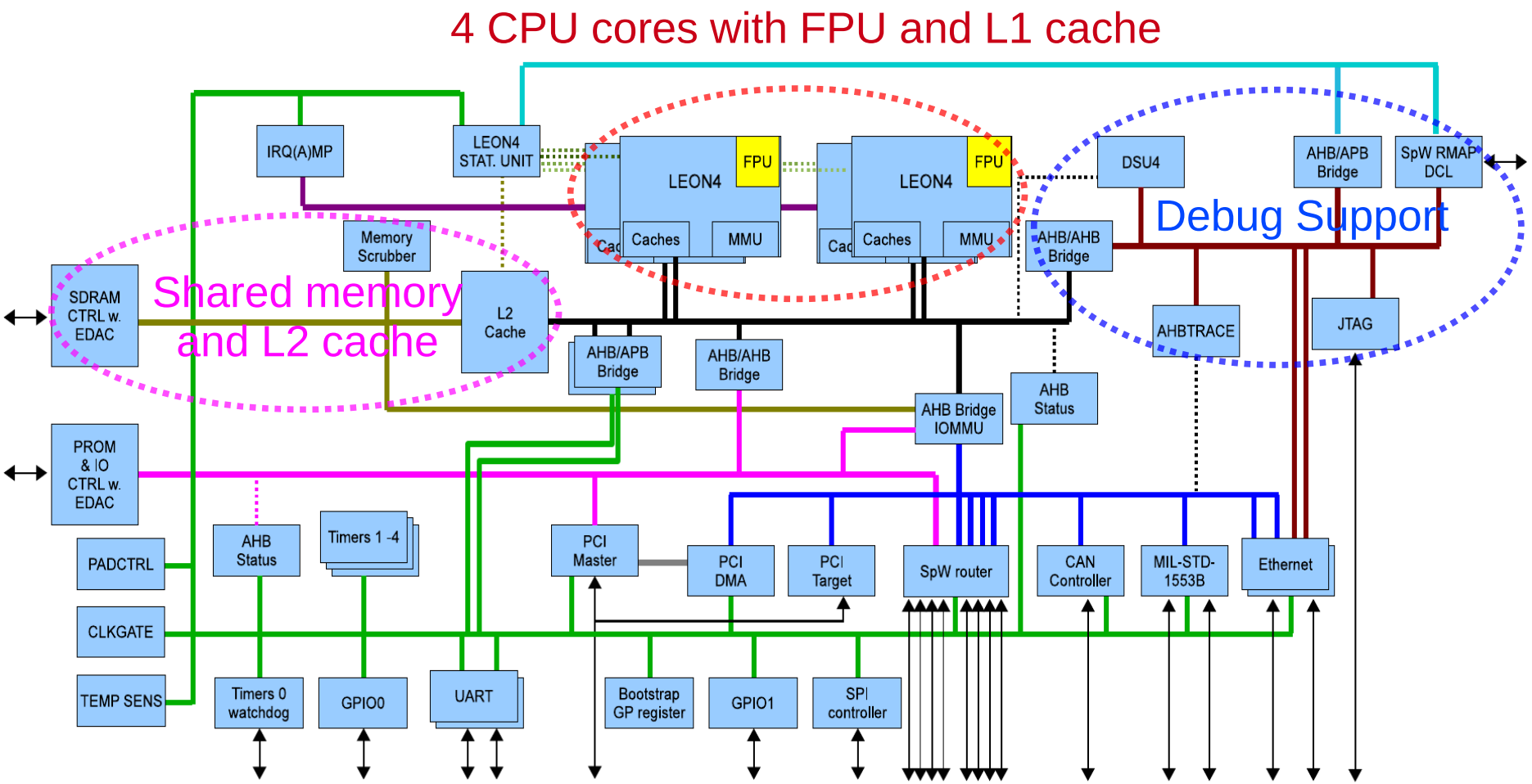
GR740 Block Diagram



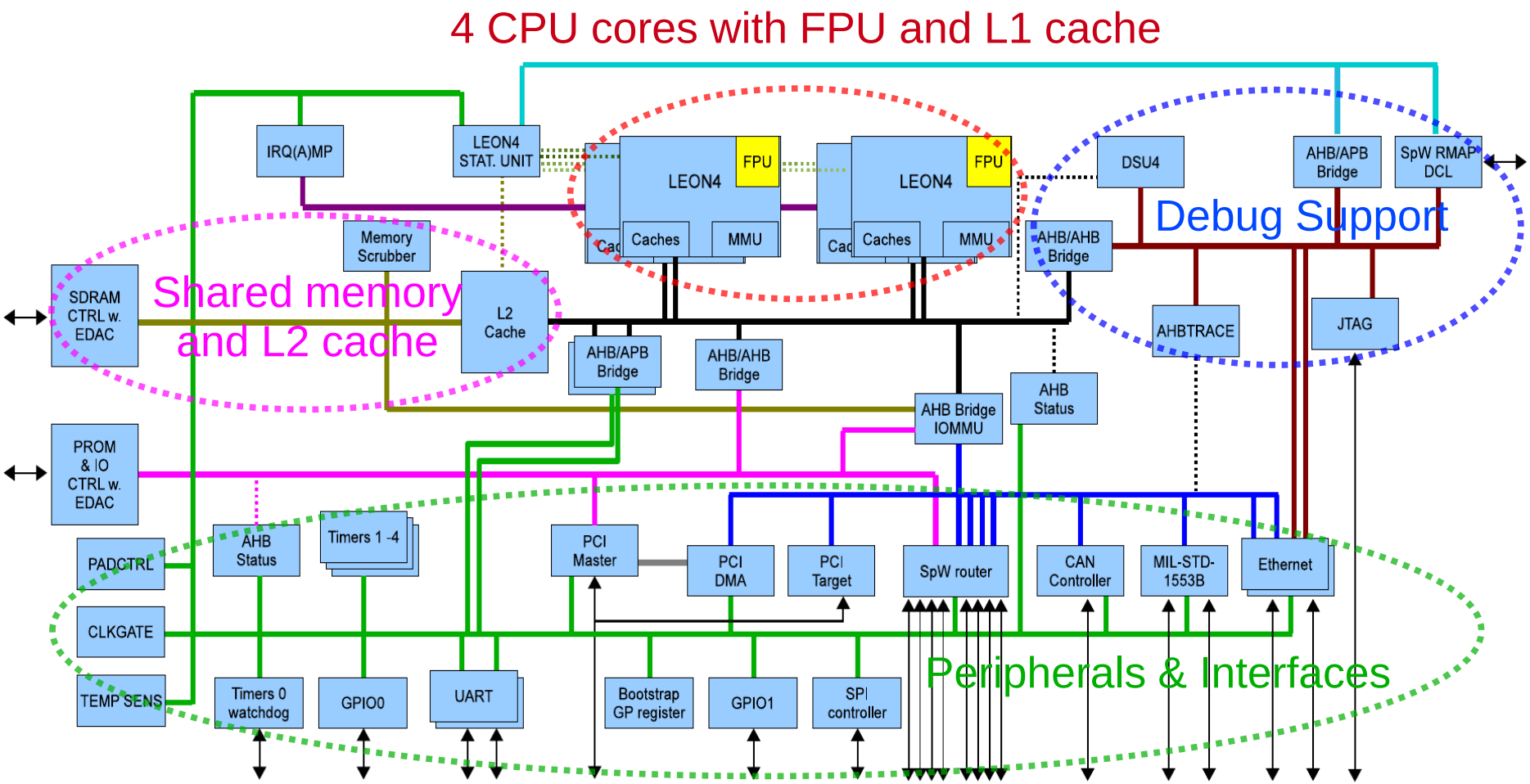
GR740 Block Diagram



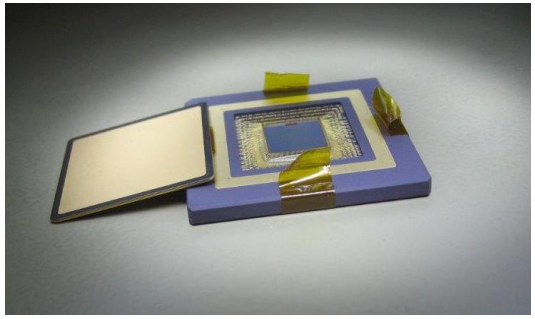
GR740 Block Diagram



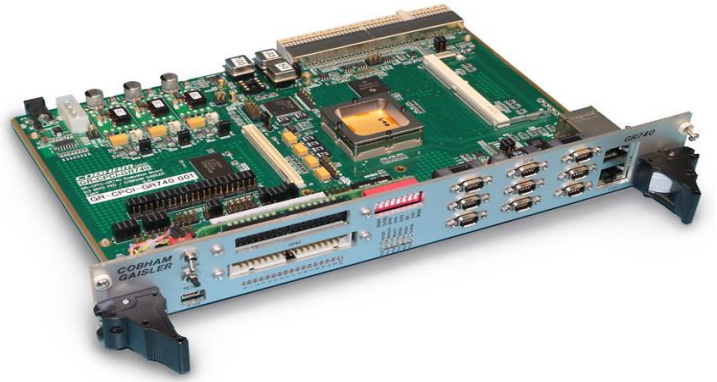
GR740 Block Diagram



GR740 : more information



GR740 prototypes currently (Q1/2016) under test in evaluation board



BRAVE – Introduction and General objectives

BRAVE: Big Re-programmable Array for Versatile Environments

- Main Goal:

  Provide to the Space Industry a High-capacity, high-performance radiation hardened reprogrammable European FPGA

- Main motivation:
  - ✓ Competitive FPGA capacity, performance and radiation hardness to be used in a wide range of space equipment across all ESA missions in Science, Exploration, Earth Observation, Telecom and Navigation. Also in Launchers and Human Spaceflight.
  - ✓ FPGA unlimited re-programmability extra advantage: enable re-configurable and adaptive systems; and also reduces impacts in the (frequent) event of unexpected design changes or modification

BRAVE – Introduction and General objectives

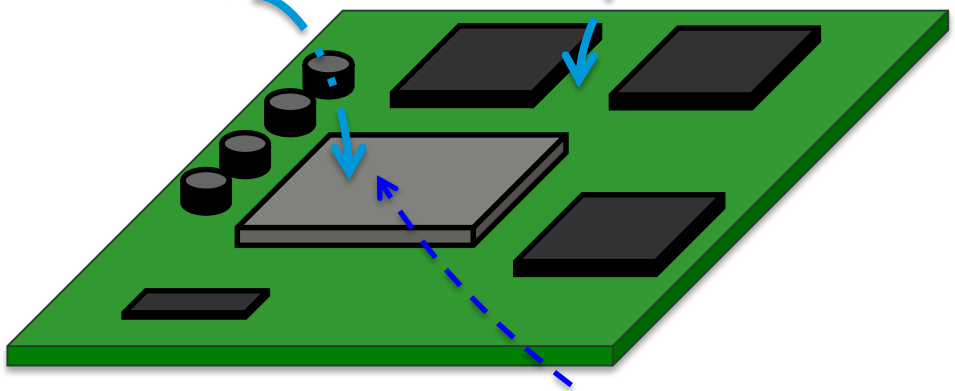
- Extra motivations/ considerations:
  - FPGA cost advantages:
    - FPGAs offer shorter development times, simpler, less expensive design and manufacturing phases than Application Specific Integrated Circuits (ASICs).
    - Equipment suppliers (including SMEs) have access to FPGAs and often cannot afford advanced ASIC technologies
    - Reduce dependency on USA EAR/ITAR FPGA key components
  - Extend and keep the European Competence to develop FPGAs and capability to specify and develop future FPGA products for space.

BRAVE Product elements overview

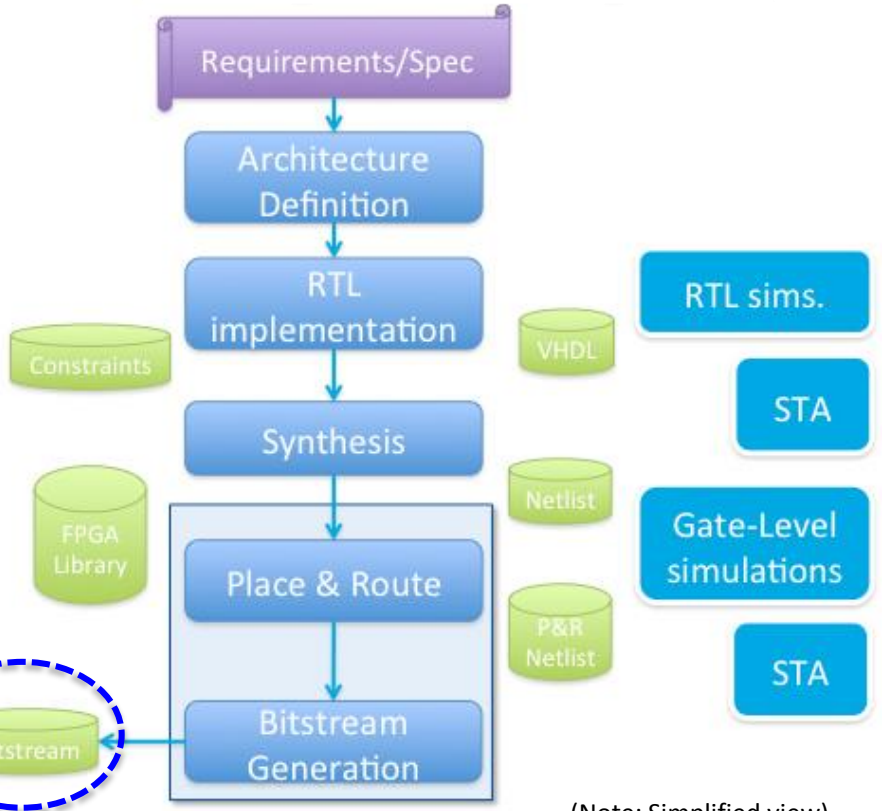
Evaluation Kit (EK)

FPGA Component

EK Board



FPGA Design Flow
(FPGA Tools)

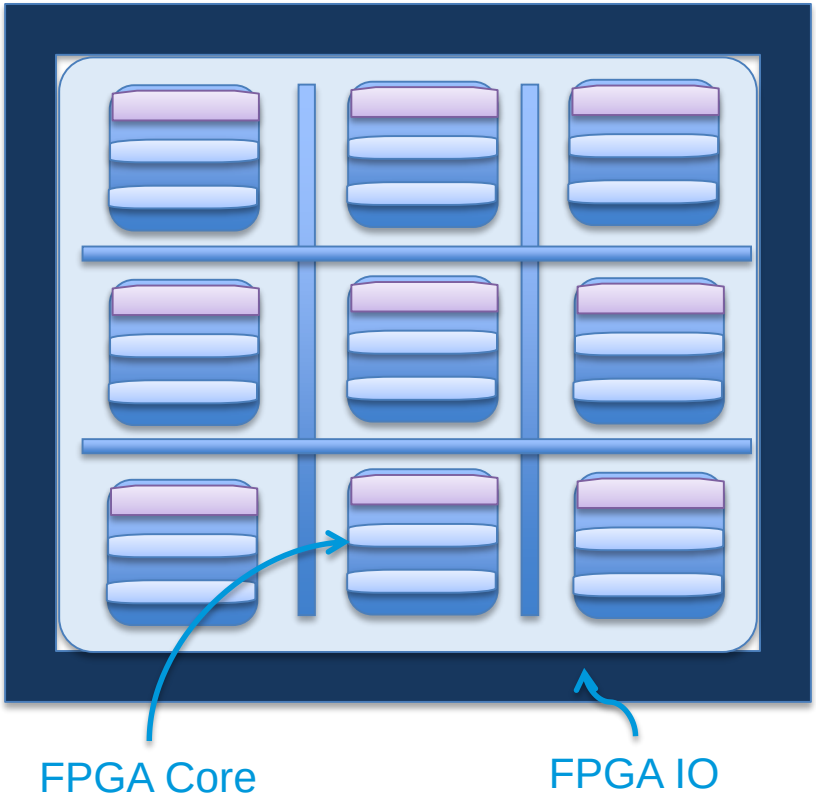


(NB: the figure does not represent the final board design)

(Note: Simplified view)

BRAVE: FPGA architecture overview

- The FPGA architecture is based on TILES that have the following elements:
  - Clusters of Look-Up Tables (LUTs):
    based on 4-inputs LUT + DFF
  - Memory block blocks:
    DP-RAM: based on 48Kb RAM blocks
    Register Files: 64x16bits
  - DSP blocks:
    based on 18x18 bits multiplier
  - Interconnect:
    Innovative interconnect that allows high density.
- The FPGA includes also:
  - Multi-standard configurable IOs
  - PLLs
  - Configuration logic with internal self-check (rad-hard)

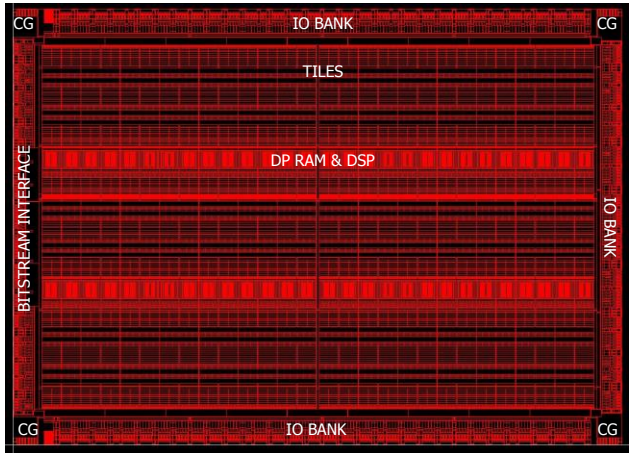


NG-MEDIUM overview, first FPGA of BRAVE

- First BRAVE rad-hard FPGA developed in 65nm
- Unlimited re-configurability (SRAM-based FPGA)
- Key milestone:
  - First silicon and FPGA tools available for end-user: Mid -2016
- Configurable by SpaceWire (and other serial/ parallel options)
- Build-in(*) EDAC for Internal memory RAM blocks
- Build-in(*) CMIC ("Configuration Memory Integrity Check")
- Hardening performance (expected):
  - TID > 100Krad (300krad tested)
  - Single-Event Latch-Up Immunity (SEL) to LET_{TH} > 60 MeV.cm2/mg @125°C

(*)Build-in in Radiation Hardened Logic

Device	NG-MEDIUM
Capacity: ASIC Gates	550 000
Modules	
Register	32 256
LUT-4	34 272
Embedded RAM (Mb)	2,1
Embedded DSP	112
Clocks	24
Embedded Serial Link	
SpaceWire 400Mbps	1
User I/Os	
LGA-625	380
MQFP-352	160

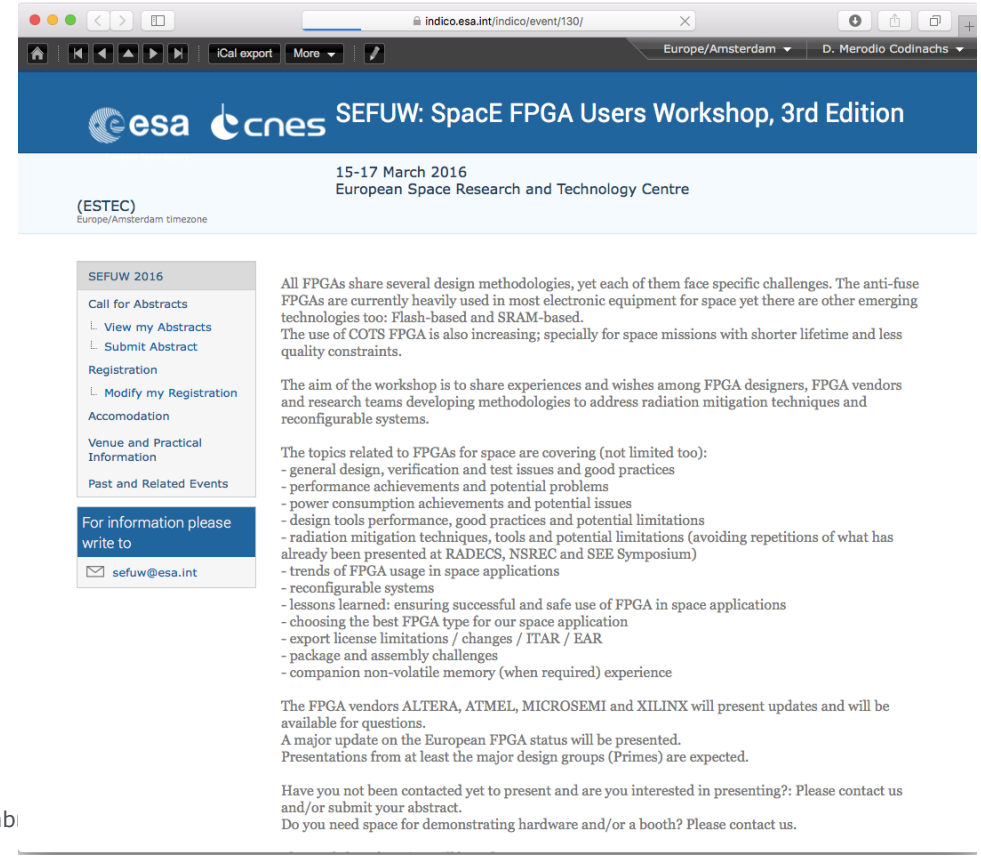


Courtesy: NanoXplore

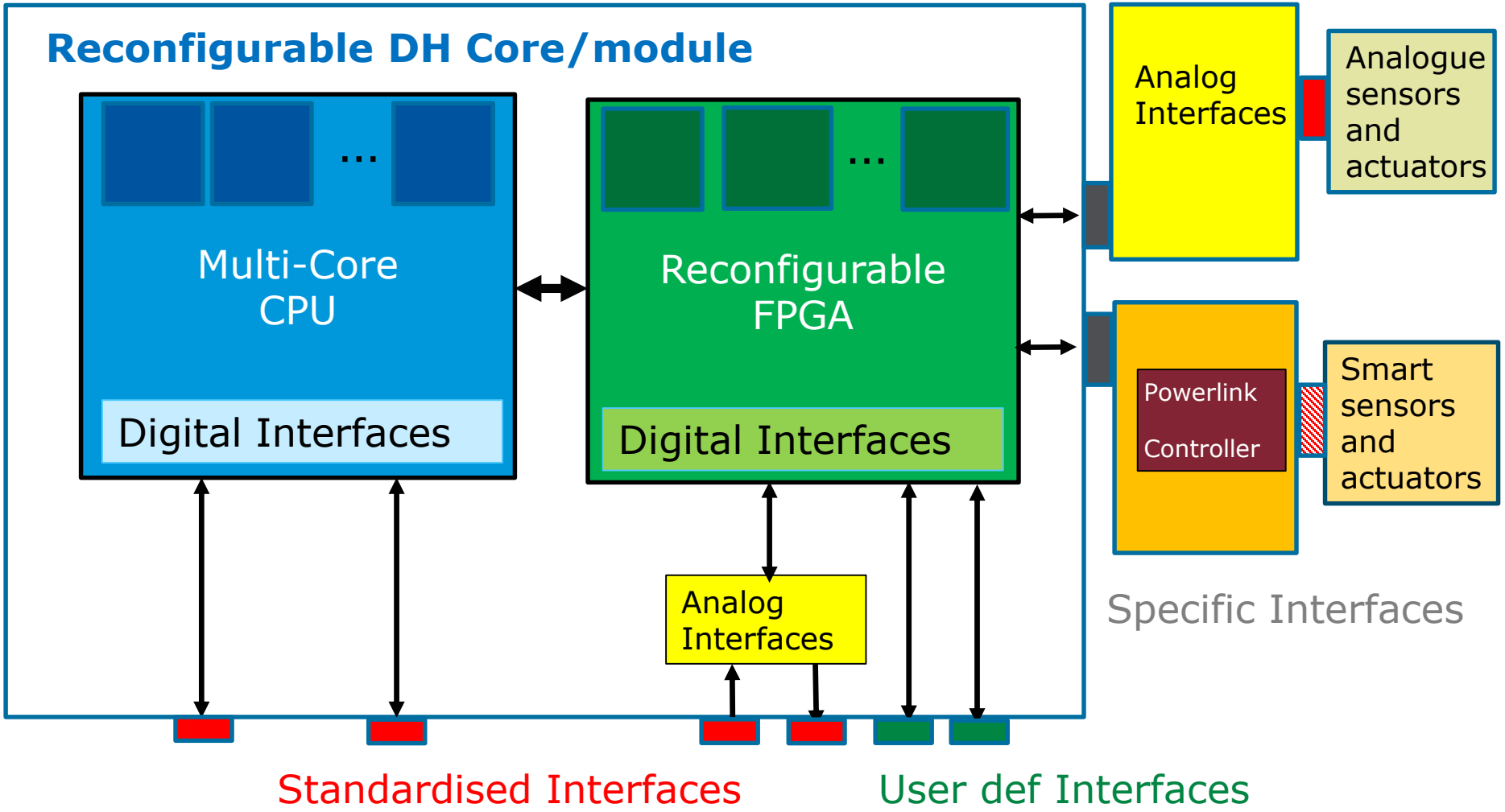
BRAVE, more public details soon

The first BRAVE FPGA will be officially pre-announced at the SpacE FPGA Users Workshop (SEFUW) at ESTEC on the 17th of March:

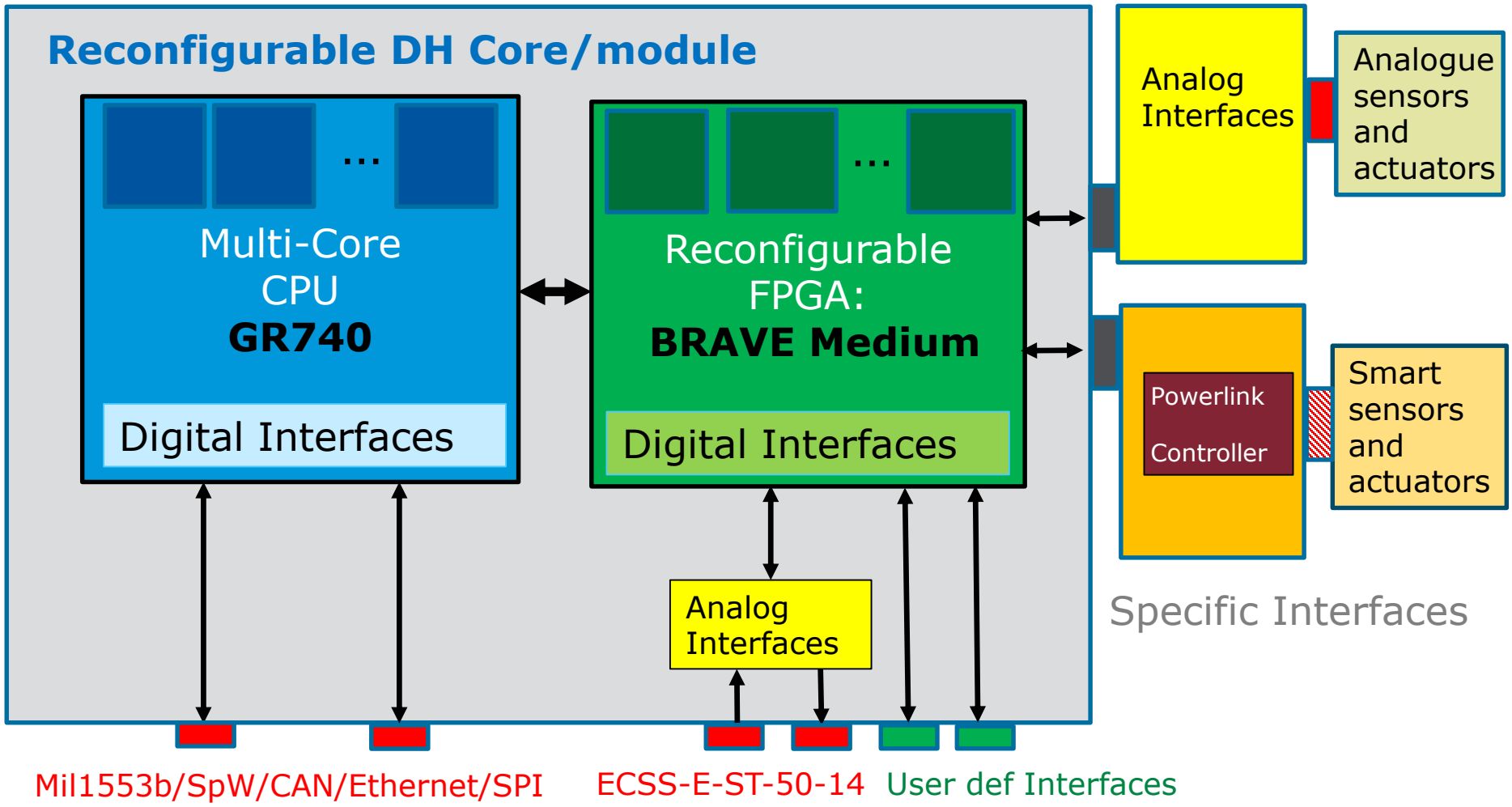
https://indico.esa.int/indico/event/130/



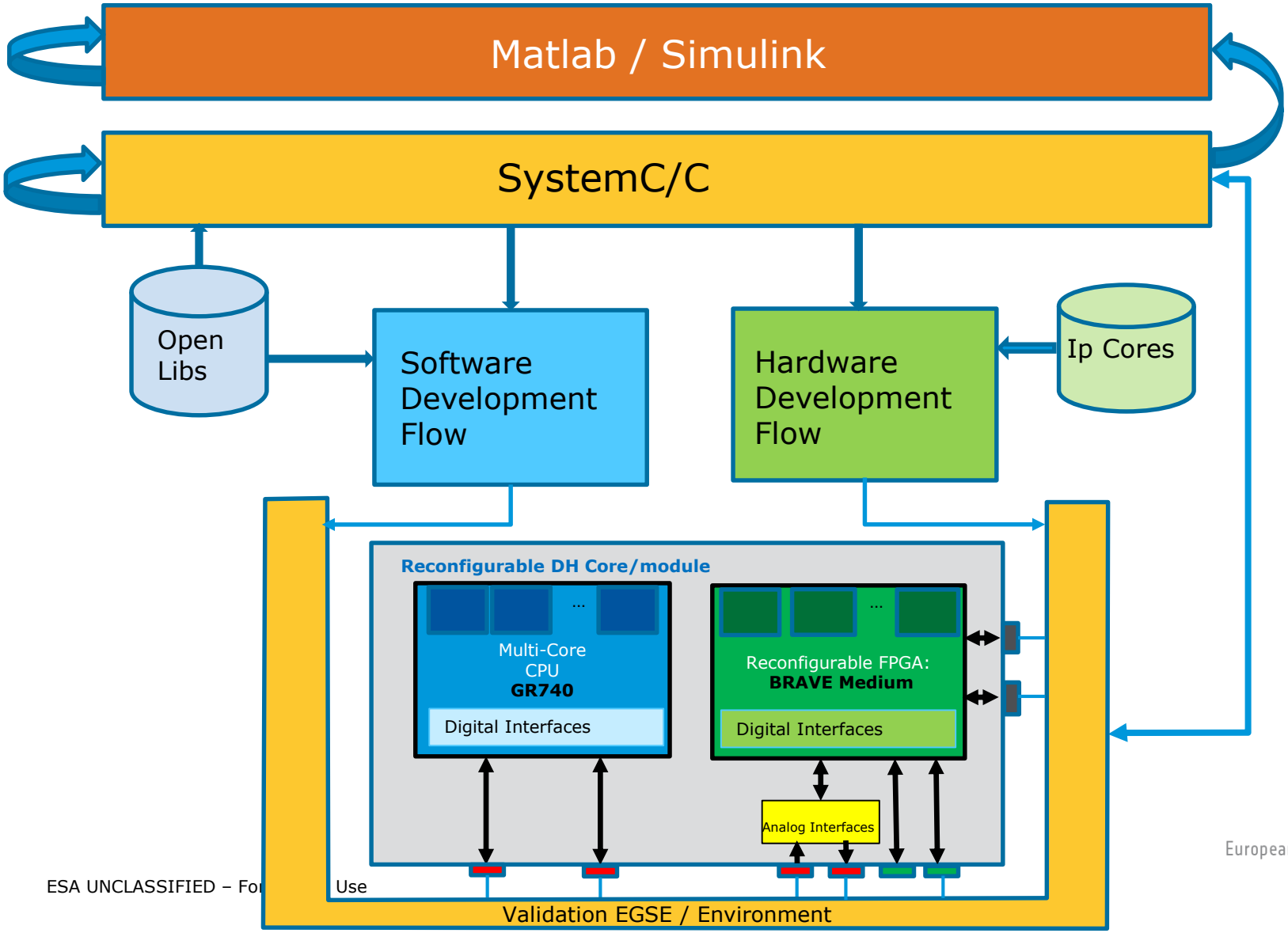
Compact Reconfigurable Avionics Concept : Reconfigurable Data Handling core



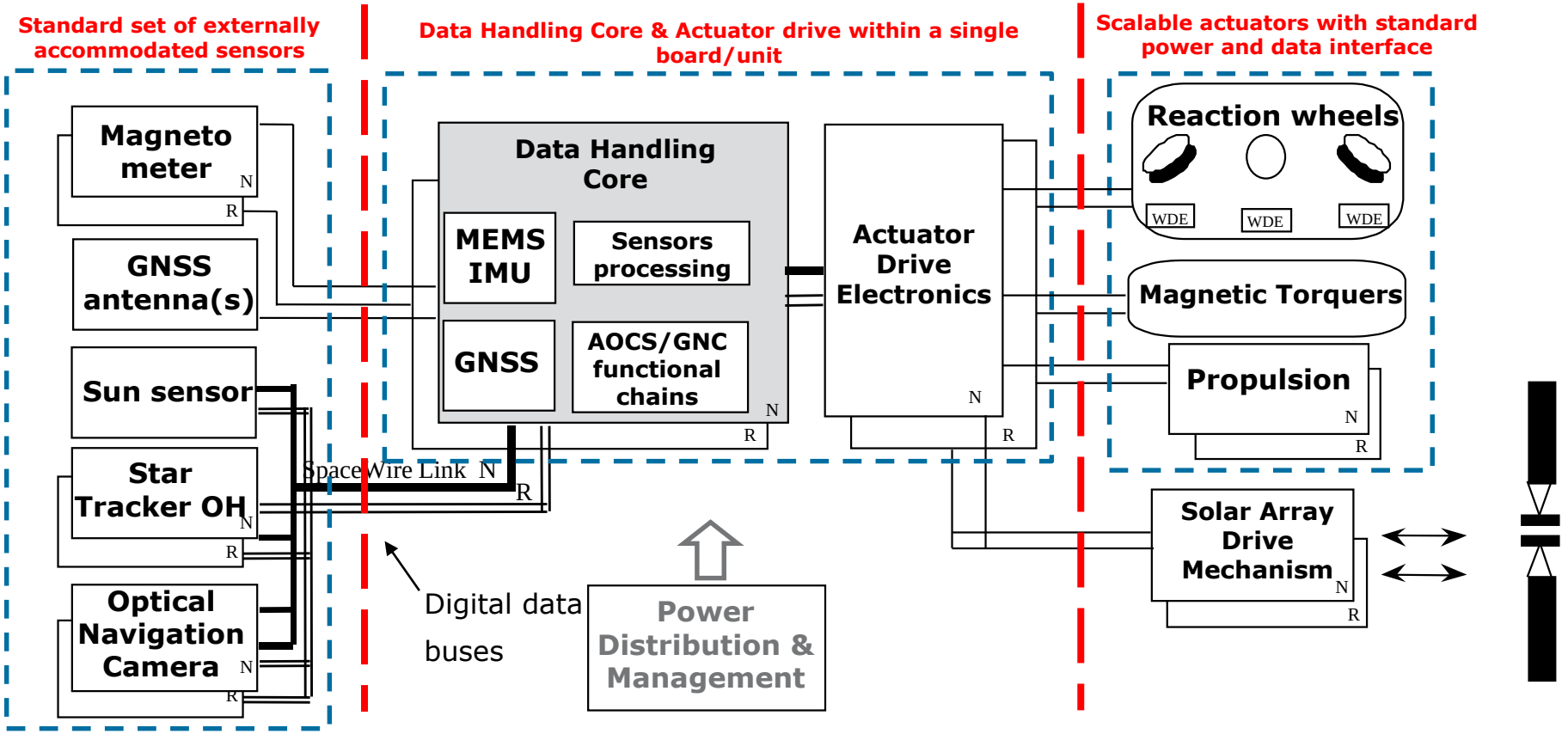
Compact Reconfigurable Avionics: Mk I
Reconfigurable Data Handling core



Compact Reconfigurable Avionics: Mk I
Development flow



Compact Reconfigurable Avionics: Smart AOCS & GNC Elements



Candidate sensors:

FaintStar-based Star Tracker, MEMS-based IMU, Sun sensor on a chip, Navigation on a chip

Applications:

LEO Earth Observation, LEO Telecom, Exploration, In-orbit servicing

Concepts:

SAVOIR-SAFI, Spacewire AOCS prototyping, Time and Space partitioning

Conclusions

A good design of complex VLSI components starts by a proper and in depth analysis of its field of application

Microprocessors and re-programmable FPGAs are playing an increasingly important role for on-board Electronics

GR740 Leon-4 based processors and BRAVE FPGAs pave the … European way … to Adaptive Avionics

Acknowledgments to many ESTEC colleagues, R. Weigand and D. Merodio and also to Cobham Gaisler, NanoXplore teams and ST Microelectronics