MEMO

Date	9th of May 2016	**Ref**	ESA-TECQTM-MO-1892
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To	ESA Approved Assembly	**Copy**	ESA PA Managers, G. Corocher, J. Hokka,

Subject: Use of Non ESA qualified PCB finish for assembly on ESA programmes

1. INTRODUCTION

Assembly verification of through holes technology or Surface Mounted Technology is performed in compliance with the ECSS-Q-ST-70-07C, ECSS-Q-ST-70-08C and ECSS-Q-ST-70-38C.
The assembly is therefore performed using tin lead solder on PCB substrates with fused tin lead finish and indium lead solder (limited to SMT) for PCB finish with thick gold.

In case the required PCB finish is not available from ESA qualified sources or not covered by the applicable ECSS standards, the use of a PCB finish that is not ESA qualified shall be handled through an RFA issued by the user and submitted to the project.

In this case, the requirements of this memo shall apply.

2. REQUEST FOR APPROVAL

For some applications and when justified that no other finish is suitable the use of non ESA Qualified PCB finish such as ENIG, ENIPIG, ENEPIG may be used provided that the following conditions are met:

1. The PCB technology, including the surface finish, shall be qualified by general qualification or by project qualification. For the latter, the memo QT/2014/148/SH (available on escies.org/pcb/) is applicable.

2. For what concerns the assembly verification of through holes and SMT a dedicated verification shall be performed ideally on boards from the same batch as the flight hardware (See Annex 1),

3. In addition to vibration, shocks, thermal cycles, incremental reworks and repair simulations, the long term storage (LTS) effect shall be evaluated during the

verification of the assembly in order to evaluate the reliability impact of intermetallic growth.

4. Two verification test flow shall be performed in parallel:

   a. A test flow with environmental tests, as per bullet 3 (see also Annex 1- Flow 1a), and assessment performed by microsectioning. The number of thermal cycles shall be 500 in compliance with the ECSS-Q-ST-70-38C or, in case of project limited verification, a margin of 3 will apply.
   b. Evaluation of the assembly, as per bullet 3 (See also Annex 1-Flow 1b), until failure in order to determine the failure mechanisms. Electrical monitoring could be a process to be used to identify when failure appears. The objective of this flow is to identify the failure mechanism.

5. In case the above verification programme (bullet 4) is not performed on boards from the same batch as the flight ones then an additional verification as per bullet 4.a, shall be performed on a PCB from the same batch as the flight boards and limited to the verification of the assembly of the sensitive devices (See escies list) and parts that may be sensitive on the used finish (See Annex 1-Flow 2a). The list of the parts to be tested on this board will be determined following the results from test results from bullet 4 a and 4b.

6. In case ECSS verification of the assembly has already been performed on the same finish from the same PCB manufacturer, without any processes changes and with the same PCB technology, then the results from the assembly verification shall be provided for review. In such case the verification test using a board from the same manufacturing batch of the flight boards may be limited to the verification of the assembly of sensitive devices and parts that may be sensitive to intermetallic growth based on the result of the ECSS verification. The verification performed on this board shall be performed in compliance with bullet 4.b (See Annex1 –Flow 2b)

7. The microsections at the completion of the test flow 4a and 5 (See Annex 1-Flow 1a and 2a) will be assessed in compliance with the ECSS-Q-ST-70-38.

8. The pass fail criteria of the failure mechanism samples of the test flow 4b and 6 (see Annex 1-Flow 1b and 2b) will be agreed in the frame of the RFA.

9. The following shall be provided in the RFA

a) The list of all packages assembled on the flight board with its associated assembly approval status on planned finish.
b) The location and number of the parts assembled on the flight hardware
c) A test plan that includes, in addition to the ECSS-Q-ST-70-38, the tests identified in bullet 4 and 5 when no previous verification on the PCB finish is available or in compliance with bullet 6 in case the assembly has already successfully passed the assembly verification in compliance with the ECSS-Q-ST-70-38C (See Annex 1 for required test flow).

d) When specific project limited verification is performed the description of the thermal stress seen by the flight hardware, on ground, during transfer and mission shall be identified to justify the limited number of thermal cycles. A margin of 3 shall be applied for the number of thermal cycles to be applied during the testing as per bullet 4.

e) Microsectioning shall be performed on all different packages and assembly technology. For sensitive devices (see ESA-TECQTM-MO-1143) the minimum number of parts to be microsectioned shall be five per assembly technology. Verification by similarity may be considered for all parts except for sensitive devices.

f) Justification of heritage shall be provided by the PCB manufacturer including the following information:
   a. Number of boards manufactured by the PCB manufacturer with same technology and finish manufactured for commercial, military and space application.
   b. Results of already passed qualification programmes.
   d. List of non conformances related to finish of the PCB (e.g. Poor wetting, black pads...) from PCB manufacturer and from returns from PCB users.

g) Justification of heritage shall be provided by the OEM manufacturer with the following information
   a. Number of assembled boards manufactured with same technology and finish for military or space applications.
   b. List of non conformances issued related to the finish of the PCB (poor wetting, black pad, ...)

h) The repeatability of the plating process between qualification batches and flight batch shall be verified . The verification of the repeatability could be done during a project audit.

Annex 1

1. No previous verification

The following shall apply ideally on flight PCB batch or on PCB batch with same process and same technology and materials.

a. Verification in compliance with the ECSS-Q-ST-70-38 and 08 and 07 with in addition incremental reworks and repairs and LTS. Microsections will be performed to determine the acceptability of the assembly in compliance with the ECSS-Q-ST-70-38. Repair and incremental reworks (up to three on the same solder pad) will be performed after assembly and prior to LTS. LTS shall be performed once conformal coating has been applied if applicable. The number of thermal cycles and its temperature range shall be in compliance with the ECSS-Q-ST-70-08C or higher if 500 thermal cycles are not sufficient to cover the application. See Flow 1a

Or

Verification as a) but with limited number of thermal cycles.
The test flow shall be the same but with limited number of thermal cycles determined applying the modified Norris Landzberg formula. A margin of 3 shall be used during testing. Microsections will be performed at the completion of the tests in compliance with the ECSS-Q-ST-70-38.

b. Verification until failure to determine the failure mechanism.
The tests will be in compliance with the ECSS-Q-ST-70-38 and 08 and 07 with in addition incremental reworks (up to five on the same soldering pad) and repairs, LTS and thermal cycles until failure. Electrical measurement may be performed during the thermal cycles in order to identify the failure. The purpose of this test is to determine the failure mode and its reproducibility. Microsection will be performed to determine failure mode. See flow 1b.

In case the verification and the determination of the failure mechanism has not been performed on the flight batch then a project limited verification shall be performed in addition on a PCB from the same batch than the flight batch.
The tests will be in compliance with the ECSS-Q-ST-70-38 and 08 and 07 with in addition incremental reworks (up to three on the same solder pad) and repairs and LTS and shock tests and microsections completed as per a). See flow 2a.

2. Previous verification performed

A verification until failure to determine the failure mechanism shall be performed on a PCB from flight batch.
The tests will be in compliance with the ECSS-Q-ST-70-38 and 08 and 07 with in addition incremental reworks (up to five on the same solder pad) and repairs, LTS and thermal cycles until failure as per b). Electrical measurement may be performed during the thermal cycles in order to identify when the failure occurs. See flow 2b.

No previous verification

Flow 1 a + Flow 1b

Flow 1 a	Flow 1b
- Assembly by machine reflow when applicable AND -Assembly method used for repair	- Assembly by machine reflow when applicable AND -Assembly method used for repair
- Incremental repairs	- Incremental repairs
- Conformal coating	- Conformal coating
- LTS	- LTS
- Vibration in compliance with ECSS-Q-ST-70-08C	- Vibration in compliance with ECSS-Q-ST-70-08C
- Shock tests in compliance with project requirements	- Shock tests in compliance with project requirements
- 500 thermal cycles in compliance with the ECSS-Q-ST-70-08C	- Thermal cycles in compliance with the ECSS-Q-ST-70-08C until failure to determine failure mechanism
- Microsections	- Microsections

Verification on flight board batch

Flow 1a and 1b
not performed on
flight batch

Previous verification
in compliance with
ECSS-Q-ST-70-38C and 08C
already performed

Flow 2a

-Assembly by machine reflow
when applicable
AND
-Assembly method used for repair

Incremental repairs

Conformal coating

LTS

Vibration in compliance
with ECSS-Q-ST-70-08C

Shock tests in
compliance with
project requirements

500 thermal cycles in compliance
with the ECSS-Q-ST-70-08C

Microsections