ESCC QUALIFIED MANUFACTURERS LIST

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DOCUMENTATION CHANGE NOTICE

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DCR No.	CHANGE DESCRIPTION
938	Document re-scoped to include Qualified Technology Flows (ESCC 25400) and Process Capability Approvals (ESCC 25600) Updated with extended validities of Qualification for Atmel and Vishay technology flows. Corrected editorial errors found across the document, mostly in bullet/ sub-paragraph numbers inside paragraphs

FOREWORD

This document contains a list of qualified manufacturers that have been certified by the European Space Agency for technology flows to the rules of the ESCC system with principle reference to ESCC Basic Specification no. 25400.

The qualified electronic components produced from the technology flows are intended for use in ESA and other spacecraft and associated equipment in accordance with the requirements of the ECSS standard ECSS-Q-ST-60.

Each technology flow qualification and its subsequent maintenance is monitored and overseen by the ESCC executive. ESA certifies the qualification upon receipt of a formal application from the executive stating that all applicable ESCC requirements have been met by the pertinent manufacturer. The qualified status of a technology flow is noted by an entry in this document, a corresponding entry in the European space components information exchange system, ESCIES, and the issue of a certificate to the qualified manufacturer.

Starting from its issue 13 of September 2015, this document also contains suppliers of EEE manufacturing, assembly or test services which have achieved ESCC Process Capability Approval (PCA) as described in ESCC Basic Specification 25600. It is recalled that this scheme of certification does not include nor enable the ESCC Qualification of products. Therefore, this listing of a PCA in the QML just confirms the validity of the ESCC certification of approval within the limits of the applicable domain as described in a Process Identification Document, but does not imply any declaration of individual product(s) qualification.

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1 PROMOTION

It is permitted to advertise the ESCC qualification status of a component provided such publicity or advertisement does not state or imply that the component is the only qualified one of that particular type, range or family.

2 PROCURER'S RESPONSIBILITY

When procuring ESCC qualified components, the procurer is responsible for ensuring that the qualification status is valid and that delivered components fulfil the specified requirements of the applicable ESCC specifications. The procurer is advised to utilise the ESCC non- conformance system, per ESCC Basic Specification No. 22800, in the event that a qualified manufacturer delivers non-conforming components.

3 QML ORGANISATION

3.1 TECHNOLOGY FLOWS AND PROCESS CAPABILITY APPROVALS (PCA)

The individual Technology Flows and PCA and are listed in this document by manufacturer in alphabetical order. They may also be found on the ESCIES web site, https://escies.org. A Technology Flow Abstract is provided to describe the main features of the qualified Technology Flow.

3.2 QUALIFIED COMPONENTS

Under each technology flow a list of the qualified components is provided.

3.3 TYPE DESIGNATION

Wherever possible the referenced type (style) designations are derived from industrial standards Where no standardised type designation is applicable the manufacturer's designation is referenced.

3.4 COMPONENT CHARACTERISTICS

The precise characteristics of the qualified component are defined in the referenced ESCC Detail specifications.

3.5 MANUFACTURER

Contact information and plant locations are indicated in the individual Technology Flow listings Contact information may also be found in the ESCC QML section of the ESCIES web site, https://escies.org.

4 QUALIFIED TECHNOLOGY FLOWS

The following Technology Flows are qualified:

4.1 ATMEL, FRANCE: MH1RT

NOTES:

1. An end of life notification affected the MH1RT process at the end of 2011, setting last delivery dates in June 2013.
2. LFoundry in Rousset ceased to supply MH1RT chips in December 2013 as well.
3. ATMEL MH1RT is therefore not available for any new designs. However, assembly and test operations (on legacy product designed and fabricated before January 2014) have remained possible beyond the scheduled last time delivery dates, within the ESCC qualified Technology Flow as described in the rest of this paragraph.

4.1.1 Contact Information

Address	ESCC Chief Inspector
Atmel Nantes SAS Route de Gachet 44300 Nantes France	Ms V. Lepaludier Tel. +33 2 40 18 1633 FAX +33 2 40 18 1946 Valerie.Lepaludier@atmel.com

4.1.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
278D	Dec. 2006	Integrated Circuits, Silicon Monolithic, CMOS Gate/ Embedded Array based on type MH1RT

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/076

Atmel Process Identification Document PID 0026

4.1.3 List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Atmel for use in conjunction with the ESCC Detail Specification No. 9202/076. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

ASIC Sheet	Component Type
FPK	Integrated Motor Controller for Mechanisms

4.1.4 Technology Flow Abstract

1. Technology Flow
See Paragraph 4.1 Notes 1 and 2

The MH1RT gate array family is designed with a 0.35µm radiation tolerant CMOS technology. The offering is based on a 4 metal layer 3.3volts AT56KRT process.

The family features arrays with up to 1.6 million routeable gates and 596 pads. The MH1RT is suitable for high speed, low power digital applications working in a radiation intensive environment.

The Technology Flow covers the foundry design, fabrication, assembly and testing of the

MH1RT Sea of Gates family.

	Scope	Site
Design Centre	Array Sizes: - 99K - 156K - 242K - 332K - 3V and 5V tolerant/compliant	Atmel Nantes BP 70602 44306 Nantes Cedex 3 France
Wafer Fabrication	Process Flow: AT56KLRT	LFoundry Rousset Zone Industrielle 131106 Rousset Cedex France
Assembly	Packages: - Multilayer Quad Flat Pack 196, 256, 352 pins	E2V Grenoble BP 123 38521 Saint-Egrève Cedex France

	Scope	Site
Test	Lot Formation Wafer Acceptance Inspection - SEM - Wafer Lot Acceptance In-process Inspection Test Testing Flow Sampling Plans Test Procedures - Test Vector Generation - Test Program Validation Customer Source Inspection Qualification Testing Lot Acceptance Support Qualification Test Plan/Report Technology Characterization Reliability Monitoring	Atmel Nantes BP 70602 44306 Nantes Cedex 3 France
	Incoming Inspection Final Test - Credence, Type Octet Screening External Visual Inspection	Atmel Nantes BP 70602 44306 Nantes Cedex 3 France

(a) Basic Information

- 0.35 µm CMOS technology AT56KRT Process.
- High Speed Performance
  - 170 ps typical gate delay (NAND, fanout 2) @ 3V
  - 800 MHz typical toggle frequency @ 3.3V
- Triple Supply Operation
- 3.3, 3 and 2.55 V operation
  - 5V compliant
- Low Supply Current
  - Operating Maximum Value
    0.32 W/gate/MHz @ 2.5V,
    0.54 W/gate/MHz @ 3V,
    0.69 W/gate/MHz @ 3.3V
  - Maximum Stand-by Value
    4nA/gate@ 2.5V
    5nA/gate@ 3 and 3.3V
- I/O Interface
  - CMOS, LVTTL, LVDDS, PCI, USB
  - Output Currents Programmable from 2 to 24 mA, by Steps of 2 mA
  - Cold Sparing Buffers (2 µA maximum leakage current at 3.6V and 125oC)
- Radiation
  - qualified to 1000 Gy(Si) letter R per ESCC Basic Specification No. 22900, tested successfully to 2000 Gy(Si)
  - No Single Event Latch-up below a LET Threshold of 70 MeV/mg/cm^2
  - SEU Hardened Flip-flops
- Four Arrays and Four Composite Arrays
  - Device Types
  - Refer to ESCC Detail Specification No. 9202/076

(b) Component Types
This table presents the available couples (array, package) as defined in the Variants table in the Detail Specification.

Array Designation	TH1099E TH1M099E	TH1156E TH1M156E	TH1242E TH1M242E	TH1332E TH1M332E
Array size	99K	156K	242K	332K
Package				
MQFP-T352	X	X	X	X
MQFP-F256	X	X	X	
MQFP-F196	X			

2. Design
See Paragraph 4.1 Notes 1 and 2.

The design manual and the ASIC library data books cover design at the Atmel Nantes Design Centre.

– MH1RT Design Manual ATD-TS-LR-R0232
– MH1RT 2V5 ASIC Library Data book ATD-TS-LR-R0236
– MH1RT 3V ASIC Library Data book ATD-TS-LR-R0235
– MH1RT 3V3 ASIC Library Data book ATD-TS-LR-R0238

ASIC designs are performed by the Atmel customer at their own site, with Atmel supported tools (front end) provided as a design tool kit.

3. Fabrication
See Paragraph 4.1 Notes 1 and 2

The AT56KRT Radiation Tolerant process at Atmel Rousset is a 0.35 µm CMOS, 4 metal, Ti, TiN and AlCu process.

4. Assembly
See Paragraph 4.1 Note 3

Atmel Nantes assembles the MH1RT devices at E2V Grenoble. This Technology Flow covers the following capabilities. Solderability testing for MCGA packages is included.

Die attach for MQFP package is Cyanate Ester (JM7600).

Package	Die Attach	Wire Bond	Lid Seal	Leads
MQFP	Cyanate Ester (JM7600)	Ultrasonic Wedge, 32 µm Al	Brazed Sealed with Au/Sn Alloy	Au Plated

5. Test

See Paragraph 4.1 Note 3

TCVs and SEC

The TH1156E matrix is used for both test vehicles.

(a) Test Vehicle V37
The V37 is a buffer test vehicle representative of the range of buffers available for performance testing in the MQFP 256 package.

(b) Test Vehicle V38
The V38 is developed for performance and radiation testing in the MQFP 256 package. It tests the following library elements;

– LVDS input and output buffers
– PCI 3V and 5V output buffers
– PLL (125 MHz and 250 MHz)
– DPRAM memory cell for GENESYS tool

(c) SEC
The standard evaluation circuit for reliability testing is the 65609E.

(d) The use of Transition Delay Fault (TDF) vectors are recommended.

6. Radiation Characteristics

The MH1RT family has been developed to fulfil the following characteristics in terms of radiation tolerance:

– Tested up to 2000 Gy(Si)
– No Single Event Latch-up below a LET Threshold of 70MeV/mg/cm^2
– Availability in the library of SEU hardened cells

The radiation capability of the MH1RT family has been tested during development and evaluated in total dose and for single event effects to confirm the stated characteristics. Lot radiation verification testing is performed if specified by the procurer's purchase order requirements.

4.2 ATMEL FRANCE: ATC18RHA

NOTES:

1. LFoundry (LF) in Rousset ceased to supply ATC18RHA chips in December 2013
2. A second source of supply, UMC has been successfully added to the scope of Technology Flow qualification for this technology by Atmel.
3. New designs and fabrication after January 2014 make use of the UMC source.

4.2.1 Contact Information

Address	ESCC Chief Inspector
Atmel Nantes SAS Route de Gachet 44300 Nantes France	Ms V. Lepaludier Tel. +33 2 40 18 1633 FAX +33 2 40 18 1946 Valerie.Lepaludier@atmel.com

4.2.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
312A	Aug. 2012	Integrated Circuits, Silicon, Monolithic, CMOS, Cell-Based Array, based on Type ATC18RHA

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/080

Atmel Process Identification Document PID 0030 (LF), PID 32 (UMC) and e2v PID DF 31S 100730 (assembly, common to both sources LF and UMC).

4.2.3 List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Atmel for use in conjunction with the ESCC Detail Specification No. 9202/080. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

ASIC Sheet	Component Type

In the case of ATC18RHA, standard components are also available. These are listed below with their full ESCC Detail Specification.

Detail Specification	Component Type
9512/004	Integrated Circuits, Silicon, 32-bit SPARC Processor, based on Type AT697F
9304/165	Integrated Circuits, Silicon, monolithic, CMOS digital, Field Programmable Gate Array, 280000 gates, based on type ATF280F

4.2.4 Technology Domain Abstract

1. Technology Flow

See NOTES under Para. 4.2

ATC18RHA standard cells family is designed with a 0.18µm radiation hard CMOS technology. This offering is based on 6 metal layers at 1.8V +/-0.15V for the core and 3.3V +/-0.3V for the periphery. This family features arrays with up to 6.5 Mgates and 544 pads. With its high speed performance, its low supply current and its radiation hard level, the ATC18RHA is suitable for digital applications working in radiation intensive environment. The Technology Flow Definition domain covers the design, fabrication, assembly and testing of the ATC18RHA standard cells family.

	Scope	Site
Design Centre	Matrix Sizes: ATC18RHA95_216: 1.1 Mgates ATC18RHA95_324: 2.2 Mgates ATC18RHA95_404: 3.5 Mgates ATC18RHA95_504: 5.5 Mgates ATC18RHA95_544: 6.5 Mgates AT697F : 0.85Mgate ATF280F : 280 Kgates	Atmel Nantes BP 70602 44306 Nantes Cedex 3 France
Wafer Fabrication	Process Flow: AT58KRHA	Up to December 2013: LFoundry Zone Industrielle 131106 Rousset Cedex France
		From January 2014: UMC FAB8S Hsin-Chu Taiwan
Assembly	Packages: - Multilayer Quad Flat Pack 100, 160, 196, 256, 352 pins - Land Grid Array 349, 472 and 625 pins - MCGA 349, 472	E2V Grenoble BP 123 38521 Saint-Egrève Cedex France

Test		
	Lot Formation Wafer Acceptance Inspection - SEM - Wafer Lot Acceptance In-process Inspection Test Testing Flow Sampling Plans Test Procedures - Test Vector Generation - Test Program Validation Customer Source Inspection Qualification Testing Lot Acceptance Support Qualification Test Plan/Report Technology Characterization Reliability Monitoring	Atmel Nantes BP 70602 44306 Nantes Cedex 3 France
	Incoming Inspection Final Test - Credence, Type Octet - Sapphire Screening External Visual Inspection	Atmel Nantes Atmel Nantes BP 70602 44306 Nantes Cedex 3 France

(a) Basic Information

– CMOS technology AT58KRHA
– 40 to 70 kgates per mm² - Up to 6.5M gates
– Double supply operation
  - Periphery power supply 3.3V
  - Core power supply 1.8V
– Low supply current :
  Operating maximum value: 85nW/gate/MHz with a duty cycle at 20%
– I/O Interfaces:
  - Cold sparing
  - High speed LVDS (655 Mps) and LVPECL
  - PCI
– 544 pads (+ 8 pads power only)
– Embedded memories: Compiled and Synthesized
– EDAC library
– Radiation (LF and UMC):
  - No Single Event Latch-Up below a LET Threshold of 95 MeV/mg/cm² at ambient & high temperature
  - SEU hardened DFF's to 30 MeV/mg/cm2
  - Tested up to 300 KRad (Si), Radiation Level is 100 KRads (Si).
– Matrices / Device Types – per individual custom ASIC sheets and ESCC Detail Specification 9202/080

(b) Component Types

This table presents the available couples (matrix, package) as defined in the Detail Specification.

	ATC18RHA 95_216	ATC18RHA 95_324	ATC18RHA 95_404	ATC18RHA 95-504	ATC18RHA 95-544	AT697F	ATF280F
MQFP-T352		X	X	X			X
MQFP-F256	X	X	X	X		X	X
MQFP-F196	X	X					
MQFP-160	X	X					
MQFP-100	X						
LGA 625 AIN					X		
LGA 625				X	X		
LGA 472			X	X			X
LGA 349		X	X	X		X	
MCGA 472			X	X			X
MCGA 349		X	X	X		X	

2. Design
The design manual and the ASIC library data books cover design at the Atmel Nantes Design Centre.

– ATC18RHA Design Manual ATD-DE-GR-R0212
– ATC18RHA Buffers library databook ATD-TS-LR-R0252
– ATC18RHA Cells library databook ATD-TS-LR-R0251
– ATC18RHA Memory cells library databook ATD-TS-LR-R0254
– ATC18RHA specific library databook ATD-TS-LR-R0253

All ASIC designs will be performed by the customer at the customer site, with Atmel supported tools (front end).

3. Fabrication
The ATC18 Radiation Tolerant process at UMC is a 0.18 µm CMOS, 6 metal, Ti, TiN and AlCu process.

4. Assembly
Atmel Nantes assembles the ATC18RHA devices at E2V Grenoble. This Technology Flow covers the following capabilities.

Package	Die attachment	Wire ond	Lid seal	leads
MQFP	Cyanate ester	Ultrasonic Wedge, 32 µm Al	Brazed Sealed	Au plated
LGA and MCGA	(JM7000)		with Au/Sn Alloy	X

5. Test
Atmel Nantes tests the ATC18RHA devices at Atmel Nantes.

(a) TCVs and SEC
The choice of test vehicles to qualify for LF and UMC supplier were agreed with the ESCC Executive and included devices called V40,V47, V52, AT697 and others.

(b) The use of Transistion Delay Fault (TDF) vectors are recommended.

4.3 KONGSBERG NORSPACE, NORWAY

4.3.1 Contact Information

Address	ESCC Chief Inspector
Kongsberg Norspace AS Knutsrødveien 7 N-3189 Horten Norway	Mrs Cecilie Berg Tel: (+47) 3303 2700 Fax: (+47) 3303 2800 email: cecilie.berg@norspace.no

4.3.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
313A	Aug. 2011	SAW filters (transversal band pass/resonator/notch/low loss impedance element)

Applicable Documents

ESCC Generic Specification No. 3502; ESCC Detail Specification Nos. 3502/002

Norspace Process Identification Documents:

PID534 SAW Device Assembly with flow NORSF-A1
PID630 SAW Crystal Manufacturing with flow NORSF-C1

4.3.3 List of Qualified Components

For each design a detail specification is produced by Kongsberg Norspace. Where the SAW component is not proprietary to the customer the detail specification is published in ESCIES as a supporting document. Available detail specifications are found in the table below.

	Component Type
3502/022	SAW Filters, Hermetically Sealed, Surface Mount, Frequency Range 10 MHz - 4 GHz

4.3.4 Technology Flow Abstract

1. Technology Flow

The Technology Flow covers the design, fabrication, assembly, screening, in-process control and testing of the Norspace SAW filters manufactured within the NORSF-C1 and NORSF-A1 processes. The design, crystal manufacturing, assembly, screening and testing is performed in the Norspace facility at Knudsrødveien 7 in Horten, Norway.

Technology Flow	Scope
Design	Norspace specification Ko 03.00
Crystal manufacturing	Process flow NORSF-C1 on purchased SAW-grade surface polished wafers. Wafer materials: Quartz (SiO_2), Lithium niobate ($LiNbO_3$), Lithium tantalate ($LiTaO_3$), Langasite ($La_3Ga_5SiO_{14}$) Wafer dimensions: 3” diameter 0.5 mm thick 3” diameter 1.0 mm thick 4” diameter 1.5 mm thick
Assembly	Process flow NORSF-A1. Crystal dimensions: from 1.7 mm x 3.1 mm up to 8 mm x 76 mm. Packages: –Gold plated Fe-Ni-Co-alloy flat packs. From 4 up to 50 leads with ceramic or glass feedthroughs. External wings for screw attach on some types Package dimensions: From 8 mm x 8 mm up to 85 mm x 12 mm. –Gold plated Fe-Ni-Co-alloy flat packs with Cu-W base, 4 or 6 leads and ceramic feedthroughs. Package dimensions: From 11 mm x 11 mm up to 7 mm x 21 mm. –Gold plated ceramic Leadless Chip Carrier (LCC) package, 10 solder pads. Package dimension: 5 mm x 7 mm.

Technology Flow	Scope
Screening and Test	Process flow NORSF-A1. –Incoming inspection –In-process inspection –100% Wafer probe electrical test –100% Visual inspection –Final production tests –Customer Source Inspection –Screening –Burn-in and electrical measurements –Test procedures –External visual inspection –Qualification testing

(a) Basic Information
The SAW devices are passive devices and typically require external tuning. Frequency range: From 10 MHz up to 4 GHz.

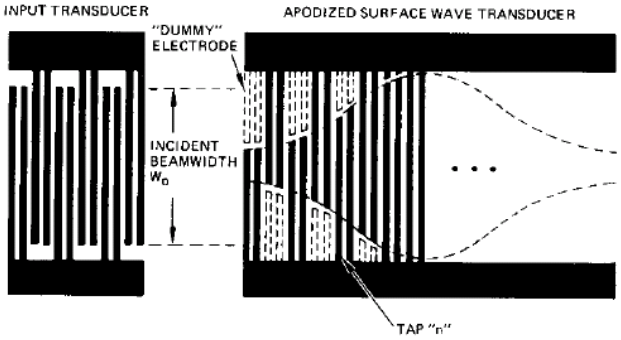
Max operating temperature range: -30 / +85 ℃ (maximum), -20 / +70 ℃ (typical).

Input power: design sensitive.

(b) Component Types
- Transversal band pass SAW filters with frequencies up to 4 GHz.
- SAW Resonator filters
- SAW Notch filters
- Impedance element filters with low loss

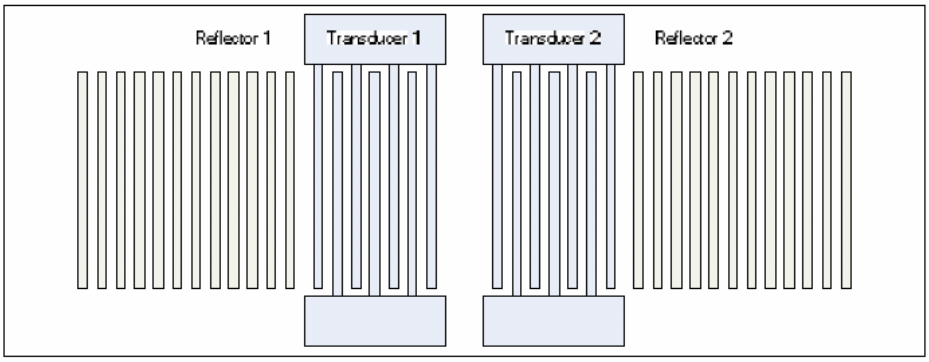
2. Design
The design programs are in-house developed procedures and libraries. Each new design is custom made for the application by Norspace design engineers. The design centre is in Horten, Norway.

(a) Transversal band pass SAW filters
The transversal filters consist of one input transducer and one output transducer, see figure below. The transducers are interdigital transducers formed by a metal pattern on a piezoelectric material (wafer). The transducers can be withdrawal weighted and/or length (apodization) weighted. The detailed weighting functions are calculated in a dedicated filter synthesis software and used as input to the mask layout software. The simulation of the filter response is performed by a dedicated SAW Analysis software.



(b) Resonator filters

The resonator filter consists of input and output transducers as described above. These are normally unweighted. The transducers are backed by reflectors, see figure below. The reflectors are l/4 wide etched grooves or metal fingers. The same software is used for simulation of the transducers and reflectors.

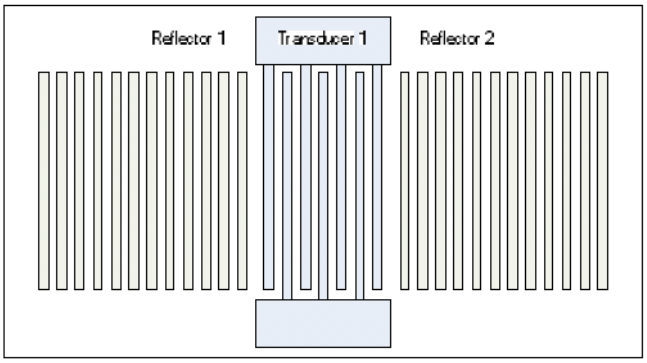


(c) SAW Notch filters

The notch are based on single port resonator elements, so called impedance elements (see below).

- Impedance element filters with low loss

  Impedance element filters are constructed from one port SAW resonators. The one port SAW resonators consist of one interdigital transducer backed by one reflector on each side, as shown in the figure below.



2. Fabrication
The NORSF-C1 process at Norspace comprises

- SAW crystal manufacturing on SAW grade polished single crystal wafers from quartz, $LiNbO_3$, $LiTaO_3$ and $La_3Ga_5SiO_{14}$ (langasite)
- Externally purchased SAW wafers
- SAW wafer thickness between 0.5 mm and 1.5 mm
- Photolithography with line widths down to 0.3 m. No upper limit.
- Metallization performed with Al or Cr/Al. Metal thickness 400 to 10 000 Å.
- The process can manufacture SAW elements of band pass, resonator or notch type with centre frequencies in the range 10 MHz to 4 GHz.

3. Assembly
Norspace assembly flow NORSF-A1 technology flow covers the following capabilities:

Package	Die Attach	Wire Bond	Lid Seal	Leads
Flatpack/LCC. Au plated. CuW base/ Fe-Ni-Co alloy or ceramic with Fe-Ni-Co alloy seal ring.	Silicone rubber	Ultrasonic ball- wedge, 25 µm Au wire	Resistance seam sealing. N2 atmosphere.	Au plated

4. Test
Measurements are performed using a Vector Network Analyzer (VNA).
All equipment in the electrical test set-up shall have the same characteristic impedance. The S-parameters are measured on the VNA and transferred to a PC for post-processing and analysis. Before testing the VNA and its test cables must be calibrated as specified in the manual for the instrument (full 2-port calibration).

Test vehicles used for qualification: SQF-3800, SLC-4320.

Test vehicles used for maintenance: SQF-3800, SLC-3900, or similar devices.

5. Radiation
- The devices are regarded as radiation insensitive within a small drift in centre frequency and phase allowed for in the design margins.
- Radiation testing has been performed successfully up to 50 MRad(Si) for quartz and 1 MRad(Si) for LiNbO3, LiTaO3 and Langasite.

Qualified wafer materials: Quartz, $LiNbO_3$. $LiTaO_3$, Langasite ($La_3Ga_5SiO_1$

4.4 VISHAY S.A. FRANCE

4.4.1 Contact Information

Address	ESCC Chief Inspector
Vishay S.A. Division SFERNICE 199, Boulevard de la Madeleine CS71159 F-06003 Nice Cedex 01 France	Mr. L. Cresson Tel: +33 4 93 37 27 88 FAX: +33 4 93 37 28 77 EMAIL: laurent.cresson@vishay.com

4.4.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
287D	Feb. 2009	Thin Film Technology for Chip, Wraparound, Single and Network Resistors, Fixed, Based on Types P for Single Chip, PRA and CNW for Resistor Networks

4.4.3 Applicable Documents

ESCC Generic Specification No. 4001

ESCC Detail Specification Nos. 4001/023, 4001/025

Vishay S.A. Process Identification Document PID PID-TFD P PRA CNW

4.4.4 List of Qualified Components

NOTE: the Established Reliability Level R is evaluated according to ESCC specification 26000.

Characteristics: Type PHR, Variants 01 to 08, 13 and 14 are qualified:

Detail Specification	Style	Critical R (kΩ)	Rated Dissipation (W)	Limiting Element Voltage (V)	Type Variant
4001/023	0402	18	0.050	30	13; 14
	0603	12.25	0.100	35	01; 05
	0805	45	0.125	75	02; 06
	1206	40	0.250	100	03; 07
	2010	45	0.500	150	04; 08

Variant	Style	Resistance Range (Note 1)		Tolerance (±%) (Note 2)	Temperature Coefficient (10^{-6}/°C) (Note 2)	Weight (g)
		Min (Ω)	Max (MΩ)			
01, 05	0603	10	0.200 (0.160 for TC « C »)	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.003
02, 06	0805	10	0.250	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.004
03, 07	1206	10	1.000	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.01
04, 08	2010	10	3.000	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.03
13, 14	0402	10	0.100 (0.067 for TC « C »)	0.01; 0.02; 0.05; 0.1	±5; ±10; ±25	0.002

NOTES

1.

Variant	Style	Critical Resistance (KΩ)
01 – 05	0603	12.25
02 – 06	0805	45
03 – 07	1206	40
04 – 08	2010	45
13 - 14	0402	18

2.

Resistance (Ω)	Avalaible Tolerances (±%)	Series
10 ≤ R < 50	0,1	Any value in the resistance range
50 ≤ R < 100	0,05 and 0,1	
100 ≤ R < 250	0,02; 0,05 and 0,1	
R ≥ 250	0,01; 0,02; 0,05 and 0,1	

OHMIC RANGE (Ω)	TEMPERATURE COEFFICIENT (ppm/°C)	ESCC CODE
10 to < 20	E: 25 (-55 °C; +155 °C)	2
20 to < 50	E : 25 (-55 °C ; +155 °C) Y : 10 (-55 °C ; +155 °C) Z : 5 (+22 °C ; +70 °C)	2 1 0
≥ 50	E : 25 (-55 °C ; +155 °C) Y : 10 (-55 °C ; +155 °C) Z : 5 (+22 °C ; +70 °C) C : 5 (-55 °C ; +155 °C)	2 1 0 9

Characteristics: Type PFRR, Variants 09 to 12 and 15 are qualified

Detail Specification	Style	Critical R (kΩ)	Rated Dissipation (W)	Limiting Element Voltage (V)	Type Variant
4001/023	0402	32	0.050	40	15
	0603	25	0.100	50	09
	0805	80	0.125	100	10
	1206	90	0.250	150	11
	2010	80	0.500	200	12

Style	Resistance Range (Ω)	Tolerance (±%)	Temperature Coefficient TC($\pm 10^{-6}$/°C)
0402; 0603; 0805; 1206; 2010	From 100 to ≤ 100K	0.05; 0.1	10; 25
0603; 0805; 1206; 2010	From 100 to ≤ 261K	0.05; 0.1	10; 25
0805; 1206; 2010	From 261K to ≤ 301K	0.05; 0.1	10; 25
1206; 2010	From 301K to ≤ 1M	0.05; 0.1	10; 25
2010	From 1M to 3M01	0.05; 0.1	10; 25

Characteristics: Type PRAHR/CNWHR,, Variants 01 to 42 are qualified

Detail Specification	Style	Critical R (KΩ)	Rated Dissipation (W/resistor)	Limiting Element Voltage (V/resistor)	Type Variant Same Ohmic Values	Type Variant Different Ohmic Values
4001/025	PRA100	12.25	0.100	35	01 to 07	22 to 28
	PRA135	56.25	0.100	75	08 to 14	29 to 35
	PRA182	100	0.100	100	15 to 21	36 to 42

Style	Resistance Range (Ω)	Tolerance (±%)		Temperature Coefficient TC(±10^{-6}/°C)	
		Absolute	Relative	Absolute	Relative
PRA100; PRA135; PRA182	From 100 to 200K	0.1; 0.5; 1	0.05; 0.1	10	3; 5
PRA135; PRA182	From 200K to 250K	0.1; 0.5; 1	0.05; 0.1	10	3; 5
PRA182	From 250K to 1M	0.1; 0.5; 1	0.05; 0.1	10	3; 5

Number of Resistors per Array: 2 to 8

NOTES:

1. Note that gold finish variants are not intended for de-golding and tinning.
2. The electrical ranges of these ESCC QML Qualified components variants are listed in the ESCC Detail Specifications and in the Qualified Part List (REP005) document available on the ESCIES website, https:// escies.org.

4.4.5 Technology Flow Abstract

1. Technology Flow

The thin film technology for chip, fixed, wraparound, single and network resistors are designed on types based on P for single chip, PRA for 2 to 8 resistors of similar value and CNW for 2 to 8 resistors with at least two different values with the same form factor as PRA.

Technology Flow	Scope	Site
Design Centre	Single resistor chips in 0402 0603, 0805, 1206 and 2010 formats 2 to 8 resistors of similar value in formats 0603, 0805 and 1206 2 to 8 resistors with at least 2 different values with the same form factor, 0603, 0805 or 1206	Vishay S.A. Division SFERNICE 199, Boulevard de la Madeleine CS71159 F-06003 Nice Cedex 01 France
Fabrication	Film deposition Photolithography Thermal treatment Passivation Thermal stabilization and control	As above

Assembly	Laser trim Protective layer Termination and Test	As above
Test	Chart F2, F3 and F4 Periodic Testing	As above

(a) Basic Information

The technology consists of:

- Substrate: High purity alumina (99.5%)
- Resistive Layer: Nickel chromium
- Passivation Layer: Silicon Nitride
- Protection: Epoxy and Silicone
- Termination: Nickel barrier
- Processes: Thin film deposition
- Finish: SnPbAg or Au

Critical resistance by style:

- P 0402 FR:32 k
- P 0603 FR:25 k
- P 0603 HR:12.25 k
- P 0805 FR: 80k
- P 0805 HR: 45 k
- P 1206 FR: 90 k
- P 1206 HR: 40 k
- P 2010 FR: 80k
- P 2010 HR: 45 k
- PRA 100: 12.25 k
- PRA 135: 56.25 k
- PRA 182: 100 k

(b) Component Types

The available formats are defined in the variants table in the Detail Specifications. Variants with established reliability in accordance with Basic specification No. 26000 are designated with an ''FR" suffix here for convenience. Variants 09, 10, 11 and 12 have established reliability level 'R' at 60% confidence level.

6. Design

The design manuals covers the design rules and limits:

- HP-BE/001 (Maîtrise de la conception)
- HP-BE/004 (Données technologiques, Régles d'implementation, Performances)

Critical design characteristics:

- Minimum metal width: 10 µm
- Power dissipation lower than 250mW/mm^2
- Current density lower than 7000 A/mm^2
- Electrical field lower than 5V/ µm

3. Fabrication/Assembly

The manufacturing flows and procedures are described in section 4 of Vishay S.A.PID.

4. Test

Complete test sequence as detailed in ESCC Generic 4001 and the relevant Detail Specifications is conducted by Vishay S.A.

The deletion of the Third Harmonic Control requirement from ESCC Detail Specification No. 4001/023 for thin film wraparound technology is documented in reference report MAT/ 3HC/07.02 revision 3 dated 2007-06-20.

For variants with established reliability the efficiency of the Overload Test is increased with the implementation of a resistance change rejection criteria of 500 ppm and approved by TRB decisions on 2007-04-04.

5. Radiation Characteristics

The resistors covered in this technology domain is considered insensitive to radiation effects.

5 PROCESS CAPABILITY APPROVALS

5.1 THALES ALENIA SPACE, TOULOUSE, FRANCE. HIGH FREQUENCY HYBRID LINE

The Process Capability Approval (PCA) of the Hybrid Line of Thales Alenia Space (TAS), Toulouse, France has been certified by ESA in accordance with the requirements of ESCC Basic specification No. 2566000.

The associated PID includes TAS' manufacturing, assembly and test operations which have been approved for the supply of Hermetic Hybrid products for use in ESA space systems as a Category1, Option 2 Manufacturer, in accordance with ECSS-Q-ST-60-05C Rev.1

5.1.1 Contact Information

Address	ESCC Chief Inspector
Thales Alenia Space 26, Av. J.-F. Champollion BP33787 31037 Toulouse Cedex 1 France	Mr. M. Lambert Tel. +33 5 3435 6338

5.1.2 Process Capability Approval

Current PCA Certificate No.	Certified since:	Type Designation
332	May 2015	High Frequency Hybrid Line

5.1.3 Capability Abstract

The associated Process Identification Document (PID) is Ref. 39.731.284/924,Issue 08/-.

This PCA covers the TAS-Toulouse activities on manufacturing, tuning, testing, inspection and Quality Assurance of High-Frequency Hermetic Hybrid technologies, used for high power and low power modules of TAS space equipment and sub-systems.

According to the PID, the hermetic modules are manufactured by encapsulation, of several types of active and passive components, inside customized hermetic package : MMICs, ASICs and digital/analog ICs, Bare transistors, Diodes, Capacitors, Resistors, Inductors and transformers, Thermistors, Thin-Film and Thick-Film circuits.

Wires and ribbons are used for interconnection between the dies, and between dies and substrates or package.

Hermetic cavities are generated with lid sealing under inert gas atmosphere. Depending of the application, the hermetic package is metal-based or HTCC based, with glass or ceramic for DC or RF feedthroughs.

Then, modules are screened, according to the PID and to the generic procurement specification ECSS-Q-ST-60-05C Rev. 1.

The repair provision conditions (element replacement, re-bonding, de-lidding …), as well as the criteria for lot rejection are also given in the PID, in accordance with ECSS-Q-ST-60-05C Rev. 1.

The procurement of passive and active components, materials and mechanical parts are performed following internal procurement specifications and incoming instructions, as detailed in PID. The associated internal tests include bondability tests as well as user-LAT tests, as required by ECSS-Q-ST-60-05C Rev. 1.

For Hybrid Circuit Lot Acceptance Test (Hybrid LAT), TAS-Toulouse follows “Option 2”, as defined in ECSS-Q-ST-60-05C Rev. 1. For this purpose, TAS-Toulouse has defined, for the Manufacturing Hybrid Line :

The generalization of Statistical Process Control of the manufacturing means,

The implementation of an Hybrid Line Management under the control of a Technology Review board (TRB). Organization, missions and responsibilities of this TRB is defined in an internal TAS instruction.

The implementation of Standard Evaluation Circuits (SECs), used for LAT acceptance. Several different SECs are requested to cover the whole range of hybrid technologies. These SECs are Flight Model Hybrids, sampled, and summited to destructive acceptance tests, in accordance toPID and ECSS-Q-ST-60-05C Rev. 1.