Aerospace & Defense BU

ECI Days 2016

SPARC 32-bit Success Story

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Atmel

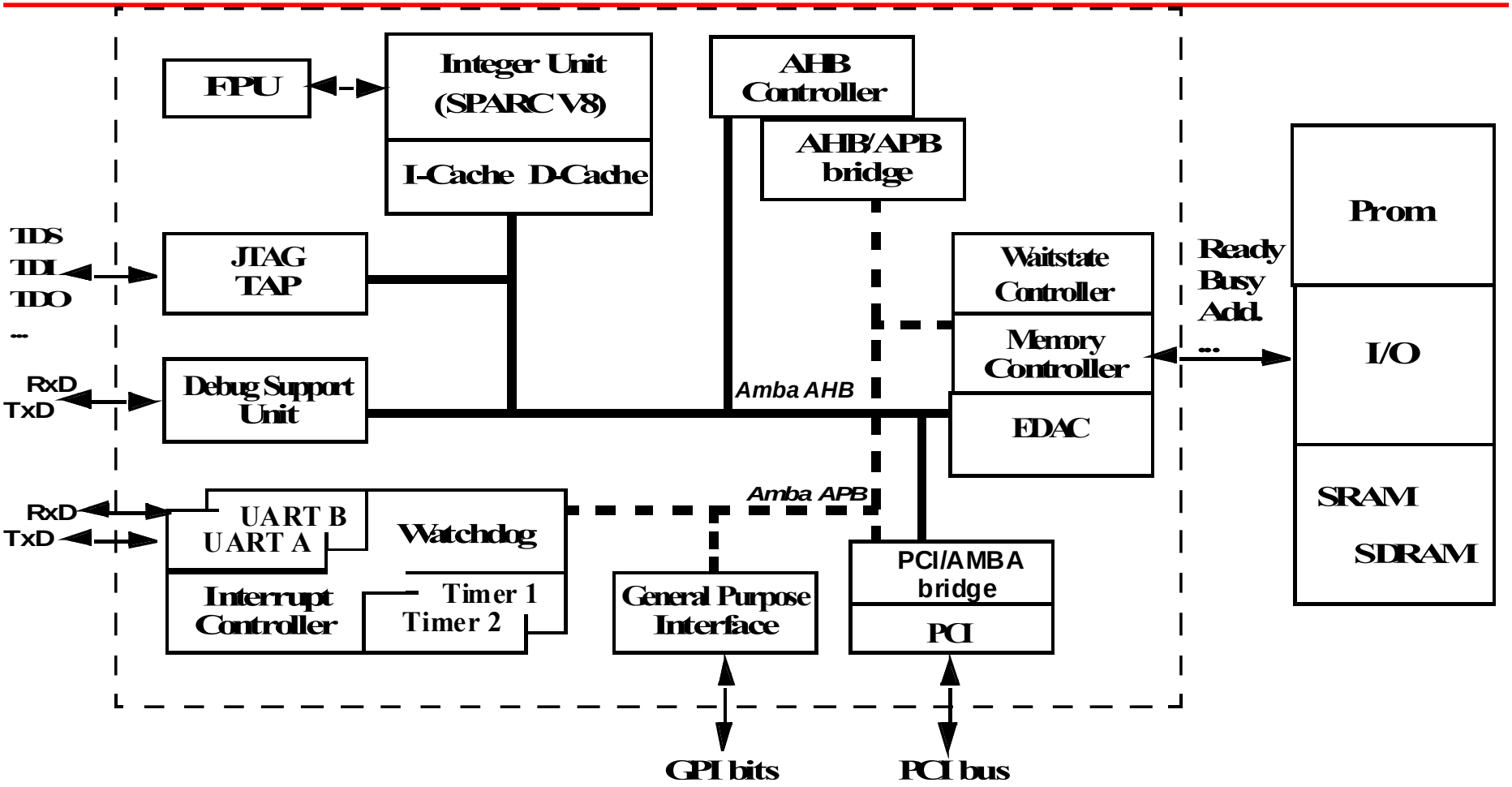
AGENDA

1. SPARC Vision
2. AT697E and AT697F
3. SPARC derivatives
4. Next Steps

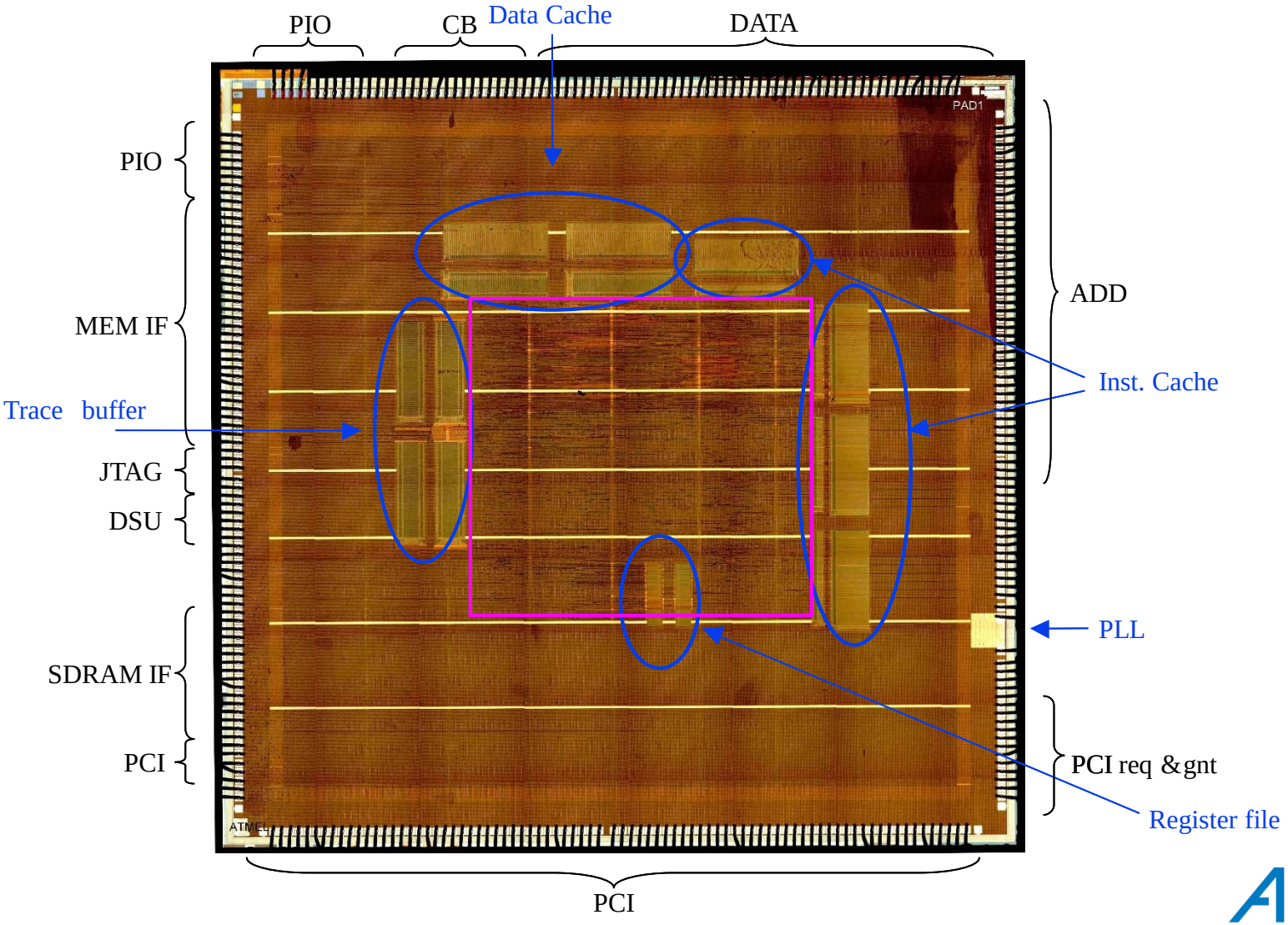
Sparc 32-bit Architecture Success Story

- Start in 1994, agreement between SUN and Matra MHS with CNES support
  - 3 Chips: 691 – 692 – 693
- 1 Chip TSC695 (SPARC V7) with ESA and CNES support to AMHS in 1999
  - Worldwide adoption of SPARC architecture for Space
- Second generation AT697E and F (SPARC V8) with ECI to ATMEL in 2005
- And many, many ASICs with LEONx core on ATC18RHA (180nm LF and UMC, ATMEL process)

AT697 block diagram



AT697 Die View



AT697E performance

- **Performance at 100MHz**
  - 86 MIPS (Dhrystone 2.1)
  - 23 MFLOPs (Whetstone)
  - SDRAM interface speed impacted by the bus load
    - On AT697-EVAB (2 SRAM and 1 SDRAM banks) : 65 MHz maximum
- **Power consumption**

150 MIPs/W

  - 7 mW / MHz
    - At 100 MHz and for high activity : core at 0.5 W, I/O at 0.2 W

AT697E radiation performance

- **Total Ionizing Dose**
  - Parts fully functional at 200 krad (Si)
  - 3.3V I/O standby current increases after 100 krad (Si), and recovers after high temperature annealing
  - These results allow to use these AT697E parts for space mission requiring a maximum of 60 krad (Si)

- **Single Event Effects**
  - No Single Event Latchup (SEL) at 95 MeV/mg/cm2 – max voltage – 125°C for a fluence of 1 E7 particles/cm2
  - Very good Single Event Upset/Transient (SEU/SET) protection

AT697F rationales

- **Prototype devices: AT697E and Flight devices: AT697F**
- **ATC18RHA library**
  - To allow successful total dose test up to 300 krad (Si)
  - To ensure appropriate process reliability monitoring (through SEC test vehicle)
- **Bug removal**
  - All known bugs has been corrected (see AT697E errata sheet)
- **Removal of existing functions**
  - 16-bit mode PROM/RAM interface (no EDAC support)
  - PCI single transaction mode
- **Addition of new functions**
  - Addition of Two Memory Block Protection Units (TSC695F compatible)
- **Pinout compatible with AT697E**

AT697F improvements of existing functions

- **Many feedbacks from customers during AT697E validation phase and first boards developments**
- **Improvements**
  - Asynchronous assertion of BRDYN
  - Use of the BRDYN for PROM area
  - Extending the timers to 32-bits
  - Addition of four external interrupts
  - AHB trace buffer halt
  - New 8-bit memory EDAC scheme
  - Write to 8-bit PROM with EDAC enabled
  - PCI device configuration boot pin made readable
  - PCI configuration registers made AHB readable in satellite mode
  - Higher capacitive load capability.
  - Higher ESD protection 2000V (250V for AT697E)
- **SDRAM interface speed**
- **Fault tolerance by design (LEON2FT)**

3.4 Results / Critical parameters / Conclusion

- **Results**
  - Characterization has been performed on one typical silicon lot
  - Timings results fully match with STA data
  - Parametrical results are on line with ATC18RHA libraries specification

- **Critical parameters**
  - Main clock Domain frequency :
    - 100MHz at limits in worst case conditions (Process Slow , Vcc Min, hot temperature)
    - Test program will screen out of specification parts

- **Conclusion**
  - According characterization results and final specification , the AT697F test program has been released to production
  - Supply chain is on line with the demand (test and burn-in capacities)

Radiation Considerations

- ***AT697F Single Event Effects Testing***
  - *SEL : No latchup found at 62MeV.cm²/mg, VCCmax, 125°C Fluence= 2.0E07 part/cm²*
    - *→ LU Cross section < 5E-8cm²*
  - *SEU: Every RHBD technique EDAC, parity, TMR was tested and showed its efficiency. Only few MBU at high LET may interest the user.*
  - *The SEU low sensitivity is enhanced with good practises like cache occupancy management.*
  - *No functional disruption found.*
  - *SET : The TMR technique allows a very good filtering of the SETs in the combinational logic network.*
  - *Proton : Very low sensitivity to 63MeV*

Application – Software Development Platform

Existing Software Tools

- Compiler
  - •Bare-C Cross-compiler
  - •RTEMS Cross-compiler

- Debugger
  - • GRMON debug monitor
    target debug through serial DSU or PCI interface
  - • Vision debugger

- Simulator/Emulator
  - • TSIM simulator
  - • LEON probe emulator

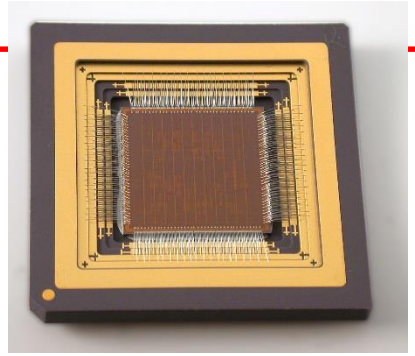
- •Real Time Operating Systems
  - • RTEMS
  - • VxWorks
  - • eCOS
  - • Snapgear Embedded Linux (uClinux)

ATMEL SPARC V7 / V8 Flight Heritage

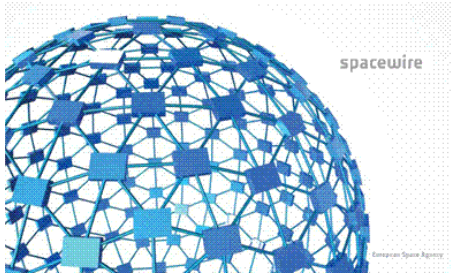
- **Unique Flight Heritage**
  - 3 chips set
    - 2500 FM delivered
  - SPARC V7 TSC695
    - More than 4000 FM already delivered, since 2003
  - SPARC V8 AT697
    - More than 2000 FM already delivered, since 2011

- **Atmel Processors SPARC V7 and V8 are used worldwide**

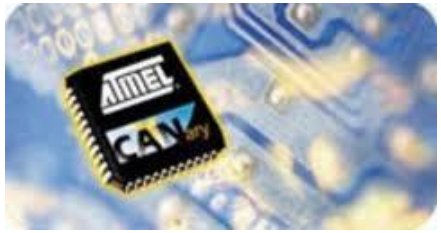
AT7913 Spacewire Remote Terminal Controler



- **SPARC V8 Processor - LEON2-FT 50Mhz**
  - 4Kinstruction cache, 4K data cache
- **Package CQPFP 352 or MCGA 349**
- **Highly integrated peripherals**
  - Digital ADC/DAC
  - Redundant CAN 2.0 with DMA
  - FIFO interface with DMA
- **Spacewire**
  - 2 links with RMAP
  - LVDS
  - Up to 200Mbit/s data rate



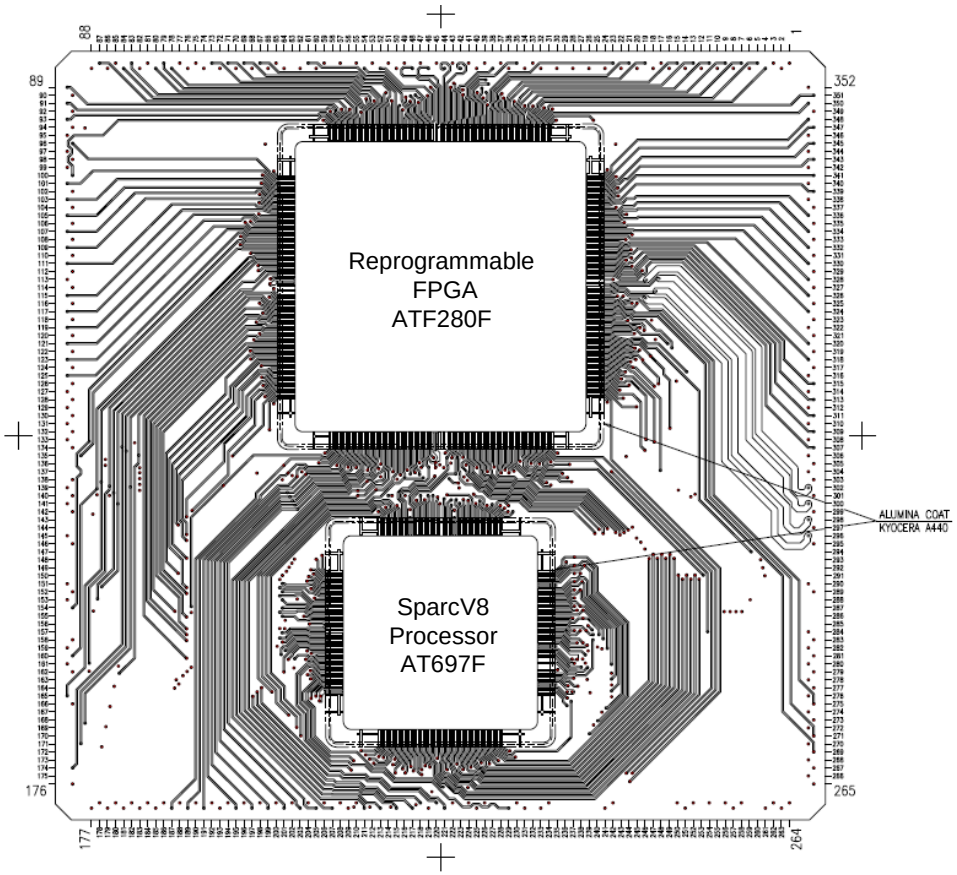
- **Onchip Memory 64KBytes EDAC protected**
- **Radiation**
  - Tested up to 300Krad
  - No single event latchup below LET 80 MeV/mg/cm2
- **Operating range**
  - 3.3V +/- 0.30V for I/O
  - 1.8V +/- 0.15V for Core
  - -55°C to 125°C



- **QML-Q, QML-V and RHA grade**

ATF697FF Reconfigurable Processor

- **Combined Rad Hard Processor + FPGA**
  - **SPARC V8 Processor**
    - AT697F LEON2-FT 100Mhz
    - Powerful & Low Power
  - **Reconfigurable unit**
    - ATF280F SRAM based FPGA (280K)
    - Mapped on SPARC Memory Bus
    - Internal PCI link
- **Multi-Chip Package CQPFP 352**
- **Ready for Spacewire**
  - 4 LVDS tranceivers & receivers
- **Radiation**
  - AT697F and ATF280 Legacy
- **Operating range**
  - 3.3V +/- 0.30V for I/O
  - 1.8V +/- 0.15V for Core
  - -55°C to 125°C
- **QML-Q, QML-V and RHA grade**



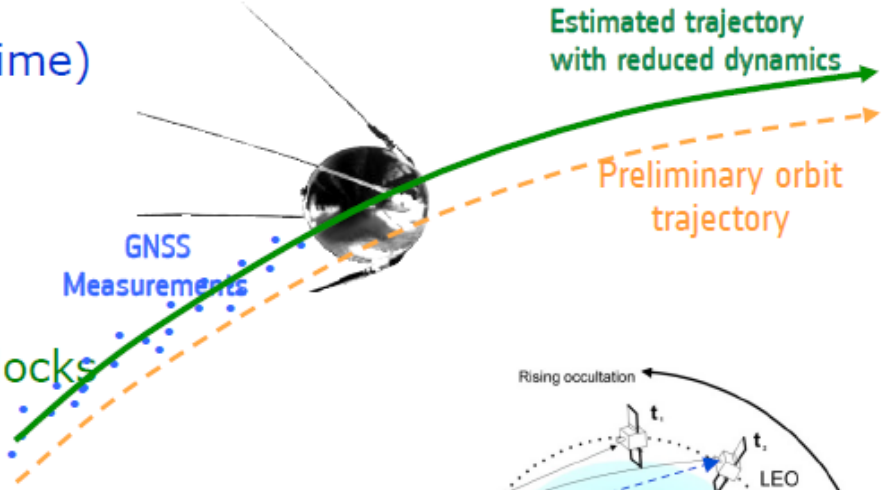
AT7991 Worldwide Market

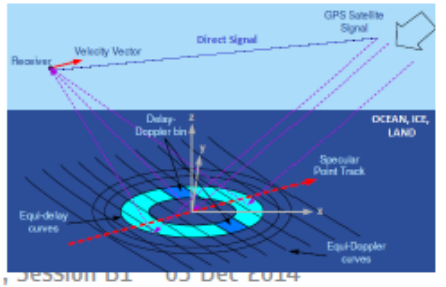
- **On-board Navigation Receivers**
  - As a platform sensor to determine Position/Velocity/Time
  - As an EO/scientific instrument payload (RO, POD, …)

- **The only multi-standard device on the market**
  - GPS
  - Glonass
  - Galileo
  - Beidou

Applications

- On-Board Navigation (Position, Velocity, Time)
  - Continuous availability
- Precise Orbit Determination (POD)
  - Post-processing to correct GNSS Tx clocks
  - 2cm level proven (GOCE)
- Scientific Instruments
  - Radio Occultation
    - AGGA based: Carrier phase measurements (like POD)
    - Refractivity causes Bending Angle => Temp., Pressure, Humidity
  - GNSS-Reflectometry (PARIS, GEROS, TDS-1, CYGNSS)
    - specific ASIC needed (not AGGA)





Overview of AGGA-4

GNSS module

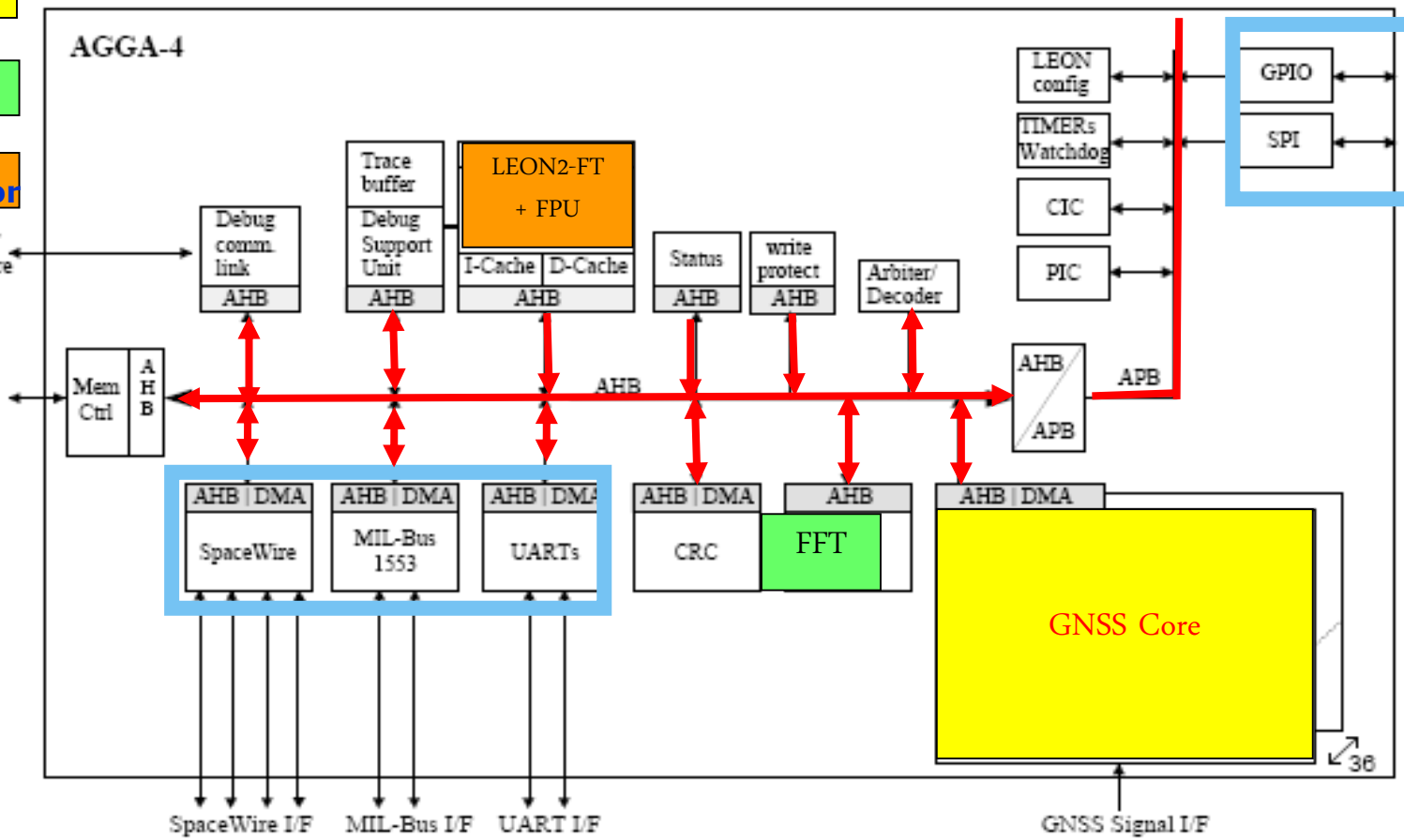
FFT module

LEON μ-processor

external I/F

AMBA I/F

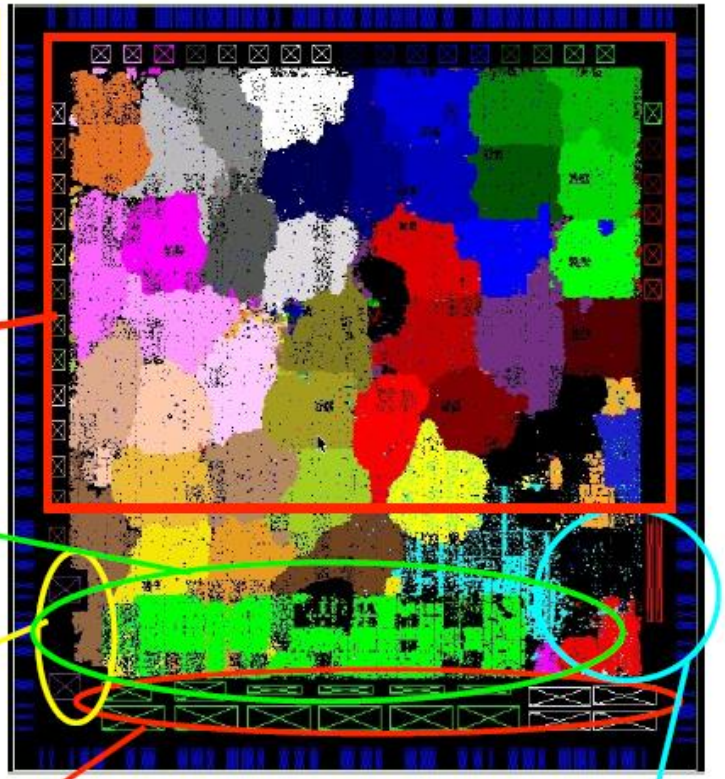
DMA I/F



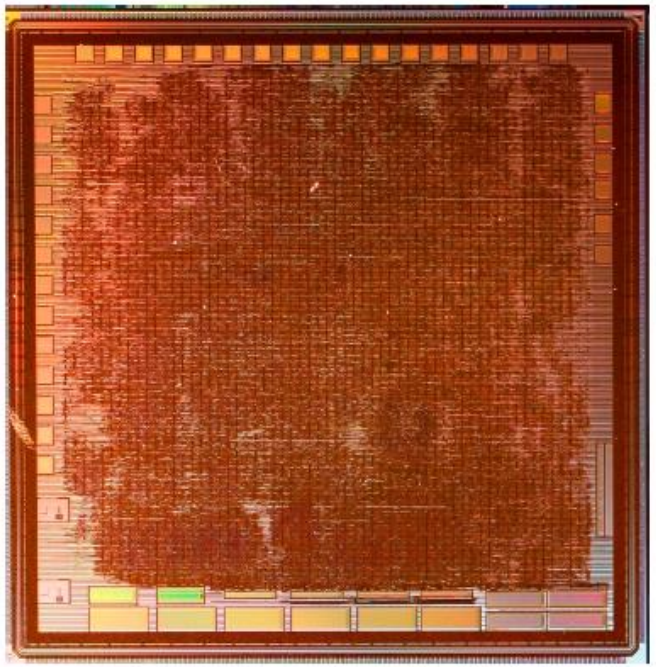
Legend:
GIC: GNSS Interrupt Controller
CIC: Communication Interrupt Controller
PIC: Primary Interrupt Controller

AGGA4 ASIC

Floorplan



Die



GNSS core : 2.7 Mgates

Clocks + I/F + Back End: 1.9 Mgates

Design : 4.6 Mgates

Pads+others : 1.4 Mgates

Total : 6 Mgates + 352 pins CQFP

(Die size 13x13 mm, incl. Pads)

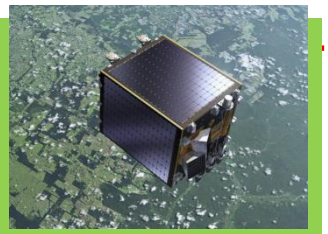
Atmel's SPARC V8 Flight Heritage

Colombus
2008

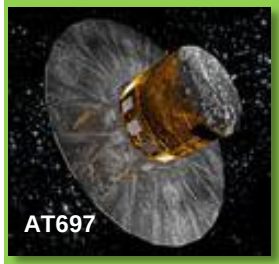
Proba2
2009

JUNO (Nasa)
2011

SPOT6
2012



Proba-V
2013



Gaïa
2013

SWARM
2013

Alphasat
2013

Sentinels
2014

SMAP (Nasa)
2014

MMS (Nasa)
2015

Bepi-Colombo
2015

Exomars
2017

SVOM/Eclair
2018

Solar Obiter
2018

CONCLUSION

- 601 – 602 – 603 chipset is phased out
- We are still selling TSC695
- We are selling AT697
- We are selling AT7913
- We start selling AT7991 (AGGA4b – GNSS)
- We prepare the next succes story with ESA, CNES, DLR, …