



Presenter: Sandi Habinc  
General Manager  
Cobham Gaisler AB



## What we do

- Cobham protects lives and livelihoods with its differentiated technology and know-how, operating with a deep insight into customer needs and agility. Cobham offers an innovative range of technologies and services to solve challenging problems in harsh environments across commercial, defence and security markets, from deep space to the depths of the ocean, specializing in meeting the growing demand for data, connectivity and bandwidth.
- Employing more than 11,500 people on five continents, Cobham has customers and partners in over 100 countries, with market leading positions in: wireless, audio, video and data communications, including satellite communications; defense electronics; air-to-air refuelling; aviation services; life support and mission equipment.

## Some numbers

- Annual revenue \$2.9B in 2015
- \$147M company funded R&D in 2014
- Employ more than 11,500 people on five continents

**The most important thing we build is trust**

# Serving Dynamic Markets

## Four Sectors

**COBHAM**

### Aviation Services

Outsourced aviation services for military and civil customers world-wide through military training, special mission flight operations, outsourced commercial aviation and aircraft engineering

- Air Traffic Display Systems
- Electronic Warfare Training
- Fly-In Fly-Out Services for the Natural Resource Industry
- Helicopter Services
- Maritime Surveillance and Border Protection
- Regional Airline Services for Qantas



### Mission Systems

Provides safety and survival systems for extreme environments, nose-to-tail refuelling and wing-tip to wing-tip mission systems for air and rotor crafts, and remote controlled robots and fully-equipped bomb disposal vehicles for homeland security and military applications

- Advanced Restraint Systems
- Air-to-Air Refuelling Systems
- On Board Inert Gas Generation Systems
- On Board Oxygen Generation Systems
- Unmanned Systems
- Weapons Carriage and Release



### Communications & Connectivity

End-to-end avionics; law enforcement and national security solutions; wireless communication and test equipment for public safety and building infrastructure; and satellite communication equipment for land, sea and air applications

- Antenna Systems for Communication, Navigation, EW and Radar
- Cockpit and Cabin Communications
- Composite Technologies
- Public Safety and Wireless Communications for Infrastructure
- Satcom Equipment for Aerospace, Land and Maritime
- Wireless Surveillance Technology
- Wireless and Radio Test Solutions



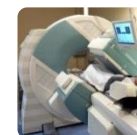
### Advanced Electronic Solutions

Provides mission critical, differentiated components and systems that protect and enhance lives, specializing in radio frequency and microwave electronics for defense and commercial applications

- AESA Sensors
- Avionics and Radar Technology
- Data Link Systems
- Electronic Warfare Systems
- High-reliability Microelectronics
- Integrated Circuit Design and Assembly
- Radiation Test Services



## Three Business Units



### Integrated Electronic Solutions

- Antenna Solutions for Airborne Communications, Navigation & Identification (CNI), Ground Mobile, Launch Vehicles & Missiles/Munitions, Motion Control Product & Systems
- Electronic Warfare, Electronic Support Measures, Direction Finding, Radar Warning
- Multi-function Assemblies
- Precision Gimbals and Gimbal Systems
- RF Transmission: High Performance RF Cables and Waveguide
- Flat Plate Antennas
- Rotary Joints/Rotating Subsystems
- Actuators/DC Motors
- Stabilized Platforms
- High Power, Solid State Transmitters

### Microelectronic Solutions

Microwave and RF Components, Modules and Subsystems, including:

- Integrated Microwave Assemblies (IMA)
- Line Replaceable Units
- Signal Source, Synthesizers and Frequency Converters
- Switches and Switching Subsystems
- Passive and Active Control Components
- AESA panels
- Digital Receiver Exciters

Applications include:

- Electronic Warfare, Electronic Support Measures and Precision Guided Weapons
- Radar (Land, Sea, Air)
- Tactical Missile Systems
- Space (Launch, Bus, Payload)
- Data Links

### Semiconductor Solutions

- Standard HiRel ICs – SPO:  $\mu$ Processor, Memory, Interconnect & Power, SBCs
- ASICs - IAD (Industrial, Space & Defense)
- ASICs - SMP (Security & Medical Products)
- Electronic Manufacturing Services (EMS): Build-To-Print (BTP) CCA & MCM, Supply Chain, Filters, Radiation Services & Trusted

Product Brands:

- Cobham Gaisler
- Cobham RAD

Official name since 10 December 2014

- Located in Gothenburg, Sweden
- Fully owned subsidiary of Cobham plc
- Management team with 60 years combined experience in the space sector:
  - Sandi Habinc: Managing Director
  - Per Danielsson: Senior Advisor
  - Jan Andersson: Director of Engineering
- 25 employees with expertise within microelectronics and software design
- Complete design facilities in-house for ASIC and FPGA development







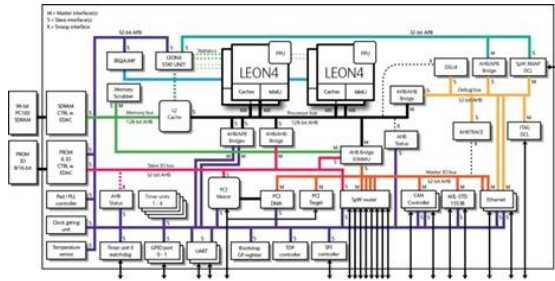
**To provide processors that enable  
new scientific missions and  
allow new ways to utilize space  
constellations for commercial use.**

# Cobham Gaisler Processor Solutions

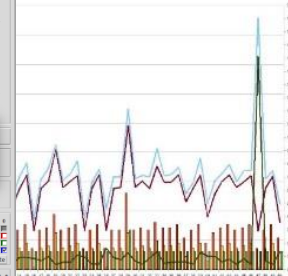
**COBHAM**

One-Stop-Shop

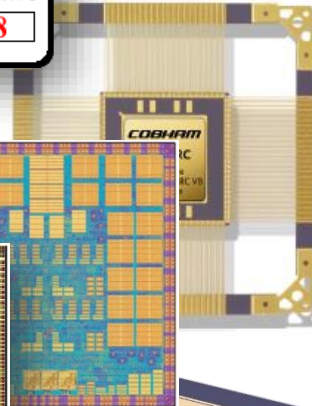
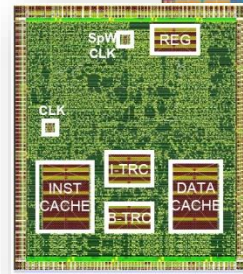
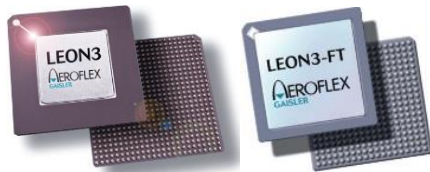
## Synthesizable IP Core Library



## Simulators, Debuggers, Operating Systems, Compilers



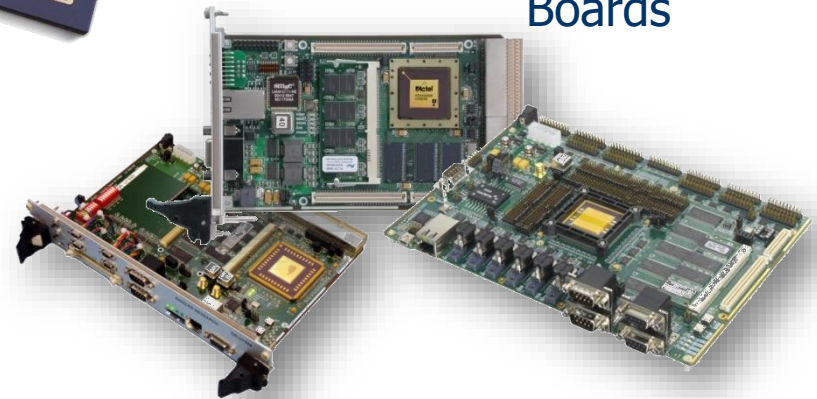
## FT FPGA Processors



## FT LEON3/LEON4 Processor Parts



## System Testbeds



## Development Boards

# SPARC/LEON Processor Background

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An open non-proprietary standard for space

- Availability to the European space market in 1990
  - 8-bit processors, like 80S32 and 8086
  - 16-bit RISC processors, like MIL-STD-1750, MDC281, MA31750
  - Motorola 68020, 32-bit CISC – Ariane 5 OBC (Launcher)
  - Intel 386, 32-bit CISC – Columbus Laboratory OBC (ISS)
- European Space Agency (ESA) studies
  - RISC Evaluation Study (Saab Space), 1990
  - RISC Architecture and Technology (Sagem), 1990
- Selection criteria for a new architecture
  - Widely supported, Open architecture, License free
- SPARC V7 was selected
- SPARC in Space
  - Atmel has shipped more than 8'500 flight parts since 1994
  - Cobham has shipped more than 1'300 flight parts since 2007
  - Unique situation with a multitude of silicon sources
  - 25 years of experience, large installed base



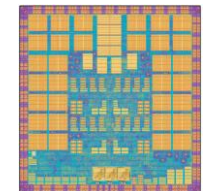
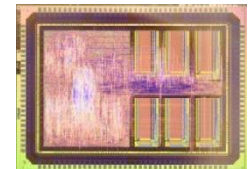
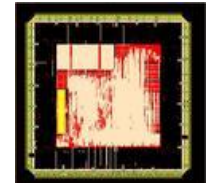
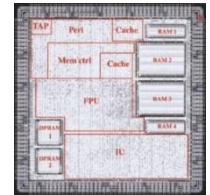
**SPARC**



# LEON Processor History

Evolution of a SPARC V8 solution over time

- **LEON1 processor core**
  - Developed at the European Space Agency (ESA) by Jiri Gaisler in 1997
  - SPARC V8 32-bit architecture / five stage pipeline
- **LEON2 processor core**
  - Developed at Gaisler Research (S) under ESA funding in 2002
  - AMBA AHB and APB on-chip bus
  - Debug Support Unit (DSU)
  - GNU LGPL, freely available source code
- **LEON3 processor core**
  - Completely new development at Gaisler Research (S) in 2004
  - SPARC V8 32-bit architecture / seven stage pipeline
  - GNU GPL / commercial dual licensing
- **LEON4 processor core**
  - Completely new development at Aeroflex Gaisler (S) in 2010
  - Wider internal bus structures, L2 cache, higher performance
- **LEON5 processor core**
  - Completely new development at Cobham Gaisler (S) in 2017
  - Specification phase started in 2016

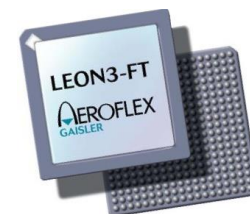
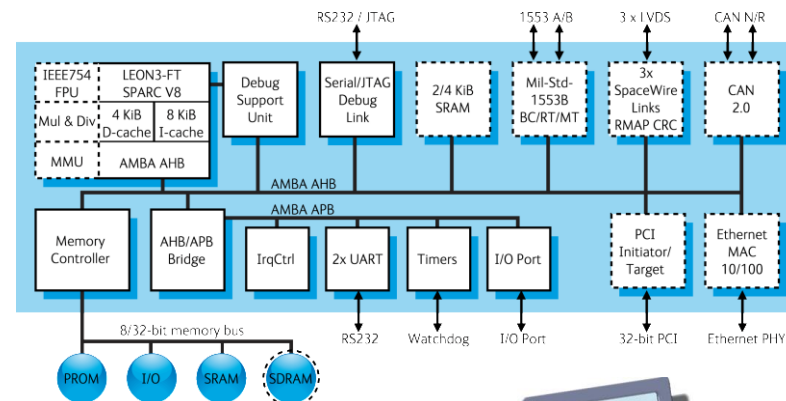


# FPGA LEON3FT RTAX-S/SL & RT3PE

Quick-to-Market – pre-programmed FPGAs based on Gaisler IP cores

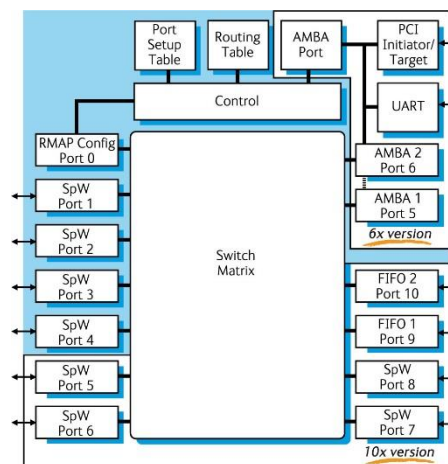
- 32-bit SPARC V8 processor in a pre-programmed RTAX2000S & RT ProASIC3 FPGAs

- LEON3FT processor core
- 8 KiB Instruction Cache / 4 KiB Data Cache
- Hardware multiply and divide
- SPARC Reference Memory Management Unit
- On-chip debug support unit with 4 KiB trace buffer
- IEEE-754 single/double precision Floating Point Unit
- Fault tolerant design detects & corrects errors (SEU) in on-chip memory without performance penalty or software interrupt
- 20 MIPS and 4 MFLOPS @ 25 MHz



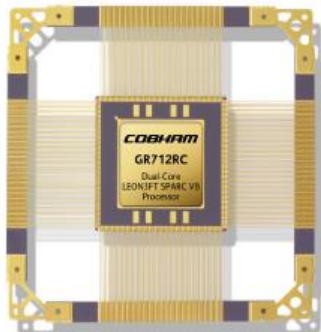
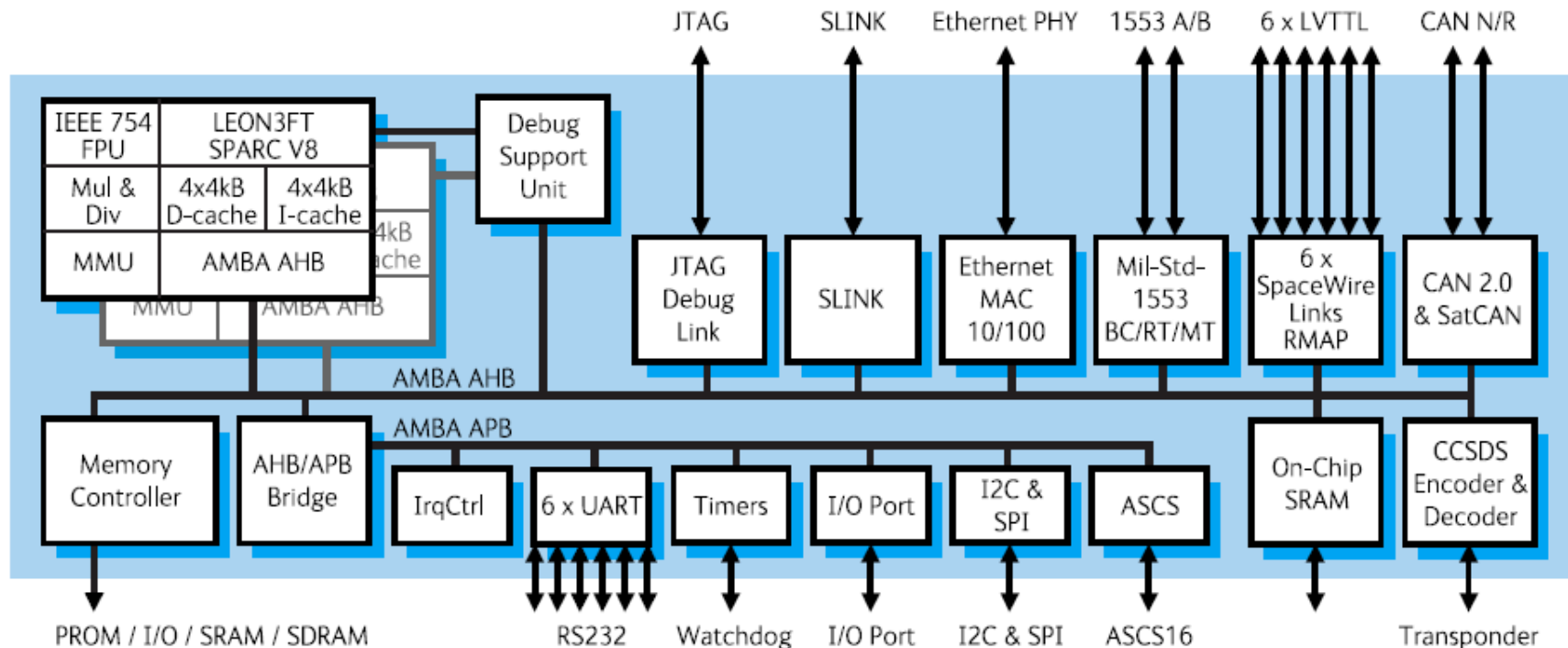
- 10-port SpaceWire router in RTAX2000S/SL FPGAs

- Compliant with ECSS-E-ST-50-12C
- Configuration port using RMAP ECSS-E-ST-50-52C
- Wormhole Routing / Non-blocking switch-matrix
- Path, Logical and Regional Logical addressing
- Group Adaptive Routing / Packet Distribution
- Support for on-chip or off-chip LVDS
- 200 Mbit/s in both directions per link



# GR712RC Dual-Core LEON3FT Processor

Dual-core processor with flight heritage



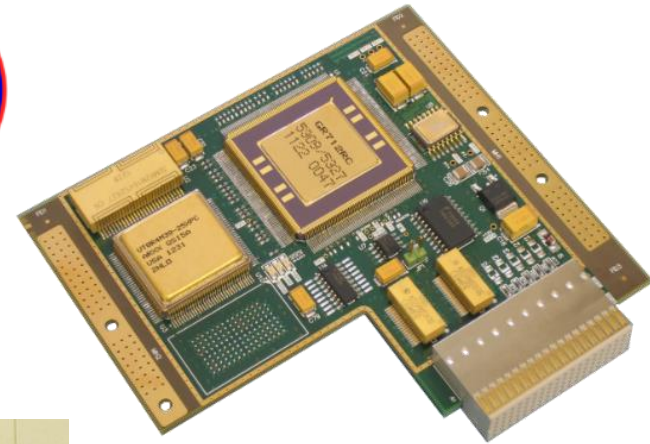
- TowerJazz 180 nm CMOS technology: Ramon RadSafe cell library
  - TID 300 Krad(Si); SEL: LET > 118 MeV/cm<sup>2</sup>/mg; 1.8V core, 3.3V I/O voltage
- Power consumption (typical): 15 mW / MHz (dual core, MMU, FPU)
- Dual Core LEON3FT Fault-tolerant processor (SMP)
  - 32 KiB cache with 4 parity bits per word
- CQFP240, 0.5 mm pitch, 32x32 mm, hermetically sealed
- Assembly by HCM/SERMA in France

# MASCOT On-Board Computer - 2014

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GR712RC first flight

- The MASCOT lander was launched as a passenger on the Hayabusa-2 asteroid probe on 3<sup>rd</sup> of December 2014
- The On-Board Computer is based on the GR712RC dual-core LEON3FT processor using SpaceWire with RMAP to implement internal redundancy and communication with payloads



 **TELESPAZIO VEGA**  
DEUTSCHLAND  
A Finmeccanica / Thales Company

 **PENDET**  
ELECTRONIC DESIGN

 **DLR**

 **HIREL DESIGN**

 **AEROFLEX**  
GAISLER

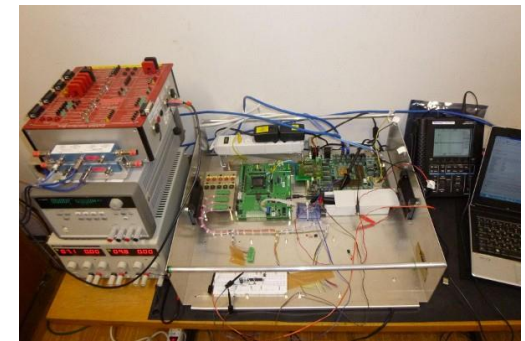
*5th International SpaceWire Conference 2013, Gothenburg, Sweden*

*<http://2013.spacewire-conference.org/downloads/SpW2013ProceedingsFinal.pdf>*



## GR712RC second flight

- The GR712RC Dual-Core LEON3FT processor is integrated in the Electronics Unit of the CaSSIS (Colour and Stereo Surface Imaging System) developed by the University of Bern, Switzerland. CaSSIS was launched on the ExoMars 2016 mission on 14<sup>th</sup> of March 2016.
- Mission details:
  - The ExoMars 2016 mission is a cooperation between ESA and the Russian Space Agency, Roscosmos.
  - The ExoMars 2016 mission consists of the Trace Gas Orbiter (TGO) and an entry, descent and landing demonstrator module, known as Schiaparelli.
  - ExoMars 2016 was launched on 14<sup>th</sup> of March 2016 from Baikonur cosmodrome in Kazakhstan.
  - CaSSIS (Colour and Stereo Surface Imaging System) flies on the TGO and will image and characterize features on the martian surface that may be related to trace-gas sources such as volcanoes.
  - The CaSSIS instrument was been successfully switched on and the first images of Mars and stars have been processed.
- [www.cassis.unibe.ch](http://www.cassis.unibe.ch)
- [www.gaisler.com/gr712rc](http://www.gaisler.com/gr712rc)

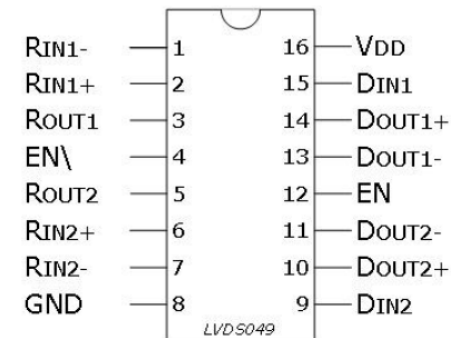
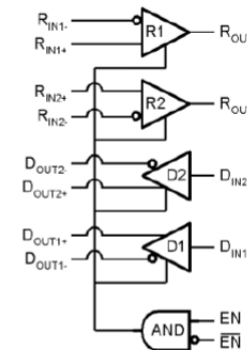
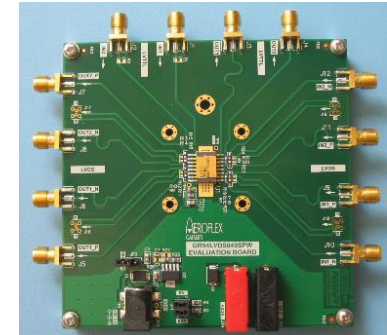
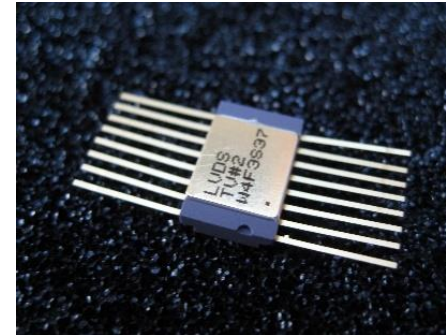


*Courtesy of University of Bern and ESA*

# European LVDS transceiver development

## GR54LVDS049 – dual transceiver

- European LVDS Driver Development and ESCC Evaluation and Qualification
- ECI - ESA contract no. 4000105762
- TIA/EIA-644 compliant LVDS input/output
- Up to 400 Mbps switching rates
- 3.3V single supply
  - 3.3V LVTTTL compatible input / output
  - 5V tolerant TTL inputs
- Overvoltage tolerant (transients)
  - Supply: -0.5V / 4.6V
  - LVTTTL: -1V / +6V
  - LVDS: -5V / 6V
- ESD robustness - 8 kV HBM ESD Level
- Receiver Extended Common Mode Input: -4V/+5V
- Radiation performance
  - TID hard > 300 krad(Si)
  - SEL immune > 118 MeV-cm<sup>2</sup>/mg
  - SEU/SET immune > 80 MeV-cm<sup>2</sup>/mg
- Receiver with Active Failsafe Operation
- Cold Spare inputs and outputs
- CFP16 package (same pinout as DS90LV049Q)



# European LVDS transceiver development

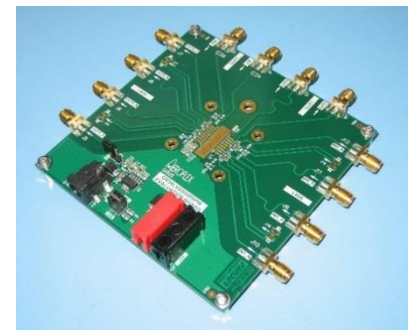
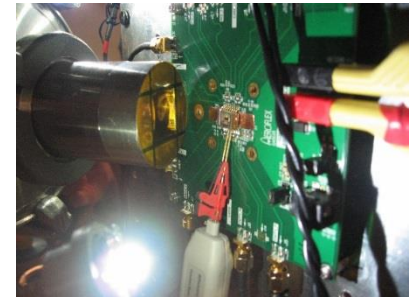
## Activity overview

- European LVDS Driver Development and ESCC Evaluation and Qualification
- ECI - ESA contract no. 4000105762
- Consortium: Cobham Gaisler (SE), IMEC (BE), Hires (FR)
- Technology: UMC 180nm, based on DARE180+ library
- Objective: design, manufacture and qualification
- Three phases: specification, prototype, production/qualification
- Currently completing prototype testing
- Redirection in scope: no 4x4 cross-point repeater
- Final product: GR54LVDS049 – dual transceiver (2+2)
- Additional designs included in last phase to start in Q4 2016
- Tape-out in December 2016 (full wafer shared with GR716)
- ECSS 9000 Lot Validation in December 2017
- Contract completion in December 2017

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**imec**

**HIREX**  
ENGINEERING  
www.hirex-engineering.com



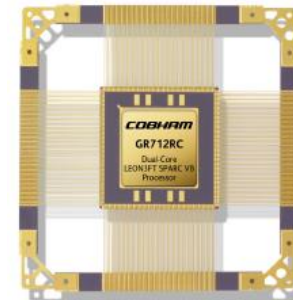
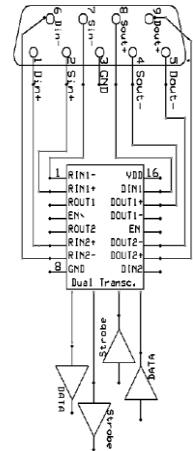
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- Providing LVDS signals for GR718B ports 17 & 18

- LVDS enhancement vs GR718B

- Providing LVDS signals for GR712RC SpaceWire ports (2 to 6 links)

- 



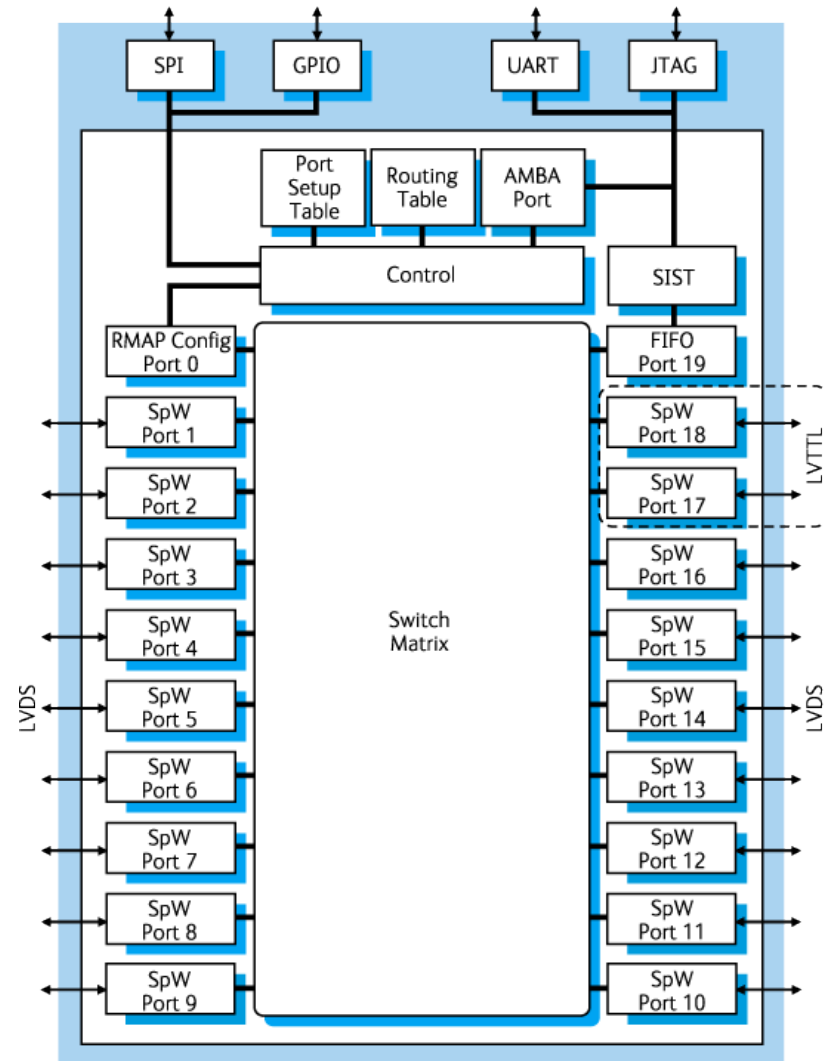
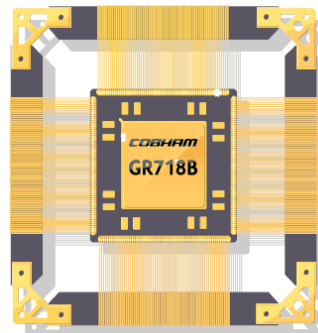


- Re-use of design blocks from the GR54LVDS049 development
- Adding the following designs to the same wafer mask:
  - Quad Driver (GR54LVDS031)
    - Pin-compatible with 031-types available on the space market
  - Quad Receiver (GR54LVDS032)
    - Pin-compatible with 032-types available on the space market
  - Dual Transceiver with Power-Down feature (GR54LVDS049PD)
    - Same pin-out, different enable pin(s) also control power-down
  - 2 x 2 Crosspoint/Repeater (GR54LVDS049XP TBC)
    - Targeted as LVDS repeater for SpaceWire devices like GR718B
    - Possibly DS90CP22/PI90LVB022/SN55LVCP22 equivalent functionality
- All in the same CFP16 package as GR54LVDS049
- Prototypes expected in ~Q3 2017
- ECSS 9000 qualification pending funding

# GR718B – 18-port SpaceWire Router

GSTP funded design – ECI funded qualification

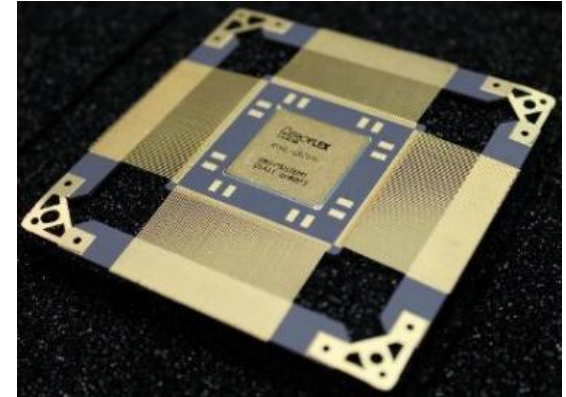
- Lot validation of 18x SpaceWire Router – GR718
  - ECI - ESA contract no. 4000113030
  - 200 Mbps full-duplex SpaceWire link speed
  - Power consumption:
    - 18 links @ 200 Mbps – 3 W
    - 8 links @ 200 Mbps – 2 W
  - Total Ionizing Dose: up to 300 krad (Si)
  - Single-Event Latch-Up (SEL)
    - $LET_{TH} > 118 \text{ MeV-cm}^2/\text{mg}$
  - Supply voltage 1.8 V and 3.3 V
  - 180 nm UMC / DARE180+ library
  - Package CQFP256
- 
- Support for SpW Rev.1
  - Distributed Interrupts
  - SpaceWire-D
  - Packet Distribution
  - SpW Plug & Play



# GR718B – 18-port SpaceWire Router

## Activity overview

- Lot validation of 18x SpaceWire Router – GR718
- ECI - ESA contract no. 4000113030
- Objective: manufacture and qualification
  - full-wafer manufacture
  - lot validation (single step qualification)
  - final product: GR718B
- Consortium: Cobham Gaisler (SE), IMEC (BE), Microcross (UK)
- Technology: UMC 180nm, DARE180+ library
- GR718 was designed in a GSTP activity, manufactured and prototyped using an MPW service
- GR718B is an enhanced version and was taped-out on a full wafer
- Contract completion in March 2017



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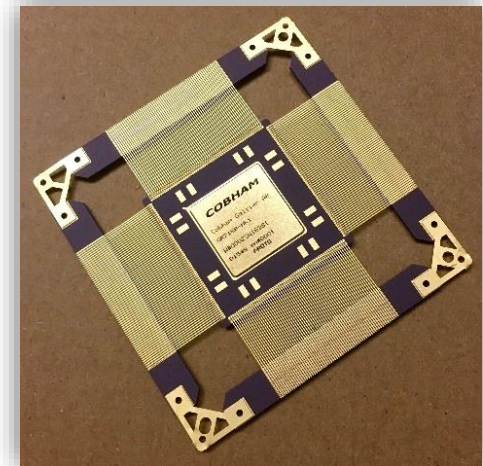


**microcross** components

# GR718B Schedule

As of 19 August 2016

<u>GR718B – (rev. B)</u>	<u>Status</u>	<u>Milestone</u>	<u>Comments</u>
Updated design (rev. B)	<i>Completed</i>	<i>Q1 2015</i>	
Layout / Tape-out (rev. B)	<i>Completed</i>	<i>Q3 2015</i>	<i>August 2015</i>
Wafer foundry (rev. B)	<i>Completed</i>	<i>Q4 2015</i>	<i>12 October 2015</i>
Package manufacturing	<i>Completed</i>	<i>2013</i>	
Prototype assembly	<i>Completed</i>	<i>Q4 2015</i>	<i>November</i>
Prototype electrical testing	<i>Completed</i>	<i>Q1 2016</i>	<i>March</i>
Prototype re-validation testing	<i>Completed</i>	<i>Q4 2015</i>	<i>December</i>

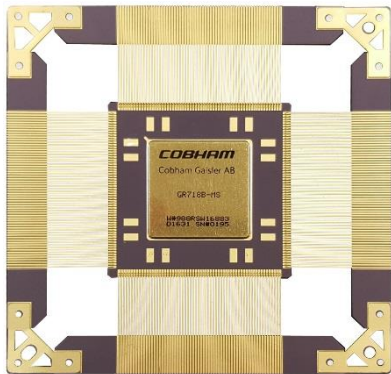




# GR718B Schedule

As of 19 August 2016

<b>GR718B – (rev. B)</b>	<b>Status</b>	<b>Milestone</b>	<b>Comments</b>
SEE testing		<i>Q2 2016</i>	<i>done</i>
TID testing		Q4 2016	RAD Europe
IBIS model		<i>Q2 2016</i>	<i>done</i>
<b>Space level assembly</b>		<i>Q3 2016</i>	<i>done</i>
<b>Space level screening</b>		Q4 2016	<i>started</i>
<b>Space level qualification (Group A, B, C and D)</b>		Q4 2016	HTOL in Q1 2017
<b>Space level flight part delivery</b>		Q1 2017	Delivery possible before HTOL in Q4 2016

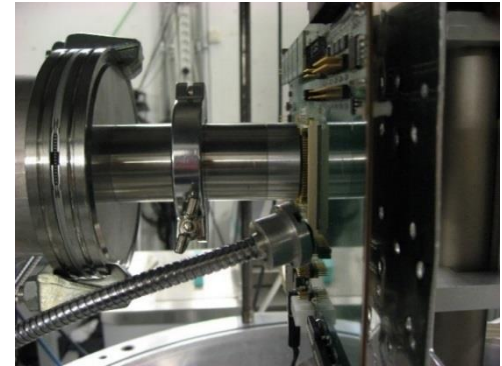


*Picture of flight part from space level assembly*

# GR718B – SEE radiation results

## SEU/SET results GR718B

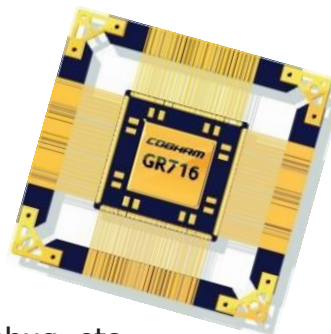
- The GR718B SpaceWire Router SEU/SET testing with HI ( $10 < \text{LET} < 57 \text{ MeV.cm}^2/\text{mg}$ ) at ESA's RADEF facility.
- Original silicon (GR718 from MPW):
  - SEL immune at  $\text{LET} > 118 \text{ MeV.cm}^2/\text{mg}$ .
  - PLL: SET immune for  $F_{\text{in}} > 25 \text{ MHz}$ .
- GR718B improvements: fewer SEUs and SETs than the GR718
- MTBE for SEUs  $> 7$  years (GEO orbit, quiet conditions)
  - Worst case configuration: 200 MHz SpW, minimum supply, no error correction scheme
  - This corresponds to a bit error rate (BER) below  $5\text{E-}17$  (compliant with the SPW standard of  $1\text{E-}12$ ).
- The majority of these rare errors will be handled either by the SpW protocol or a CRC scheme at packet level.
- Paper presented at RADECS 2016



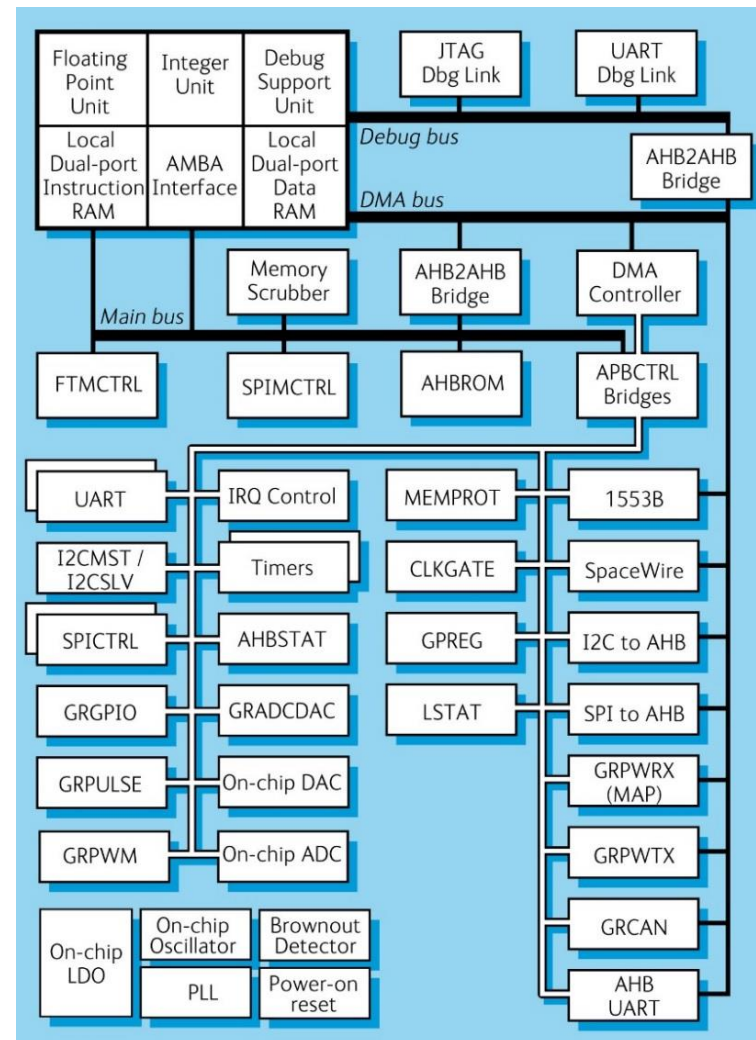
# GR716 – LEON3FT Microcontroller

## ESA microcontroller development

- LEON3FT - Fault-tolerant SPARC V8 processor, 50 MHz
  - 16-bit instruction set support to improve code density
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- SpaceWire interface with time distribution support, 100 Mbps
  - LVDS Driver and Transmitter
- MIL-STD-1553B interface
- CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- ADC 11bits @ 200Ksps, 4 differential or 8 single ended
- DAC 12bits @ 3Msps, 4 channels
- Mixed General purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm
- ESA funded development of prototypes in Q2 2017
- Qualification decision pending – requires funding



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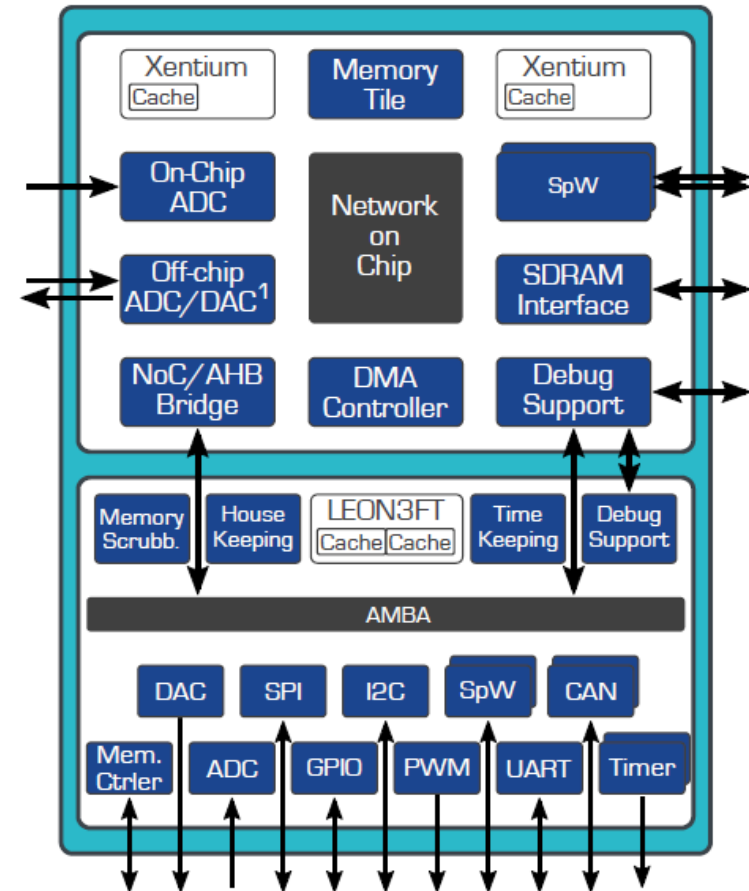


# GR732 - Scalable Sensor Data Processor

**COBHAM**

## ESA DSP development

- 2x Recore Systems Xentium Fixed-Point VLIW DSP
  - 32-bit DSP cores, with parallel functional units
  - 16 kB Instruction (Code) Cache Memory
  - 32 kB Tightly-Coupled Memory
  - 64 kB Memory Tile
  - Network-on-a-Chip (NoC) interconnect
- 1x Cobham Gaisler LEON3 Fault-Tolerant SPARC V8
  - Single general-purpose 32-bit processor core
  - 16 kB Data and Memory Cache Memories
  - Memory Management Unit
  - High-Performance IEEE-754 Floating Point Unit
  - Debug Support Unit and Trace Buffers
- Memory and Error Detection & Correction Support
- Input/Output Interfaces
  - 4x SpaceWire with RMAP target, up to 200 Mbps
  - 2x CAN 2.0B, up to 1 Mbps
  - 16 GPIO, PWM, UART, SPI, I2C
  - Parallel Chip-to-Chip Communication Interface
  - Time-keeping and Distribution
- Low-speed ADC, 13-bit, 833ksps
- Low-speed current DAC, 12-bit
- High-speed ADC, 15-bit, 100 Msps
- 352 pin QFP, 48 mm x 48 mm
- ESA funded development of prototypes in Q3/Q4 2017, flight and qualification in 2018



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**RECORE**



**ARQUIMEA**

**ThalesAlenia**  
Space  
A Thales / Finmeccanica Company

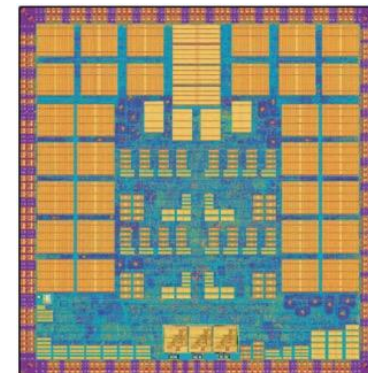


# GR740 – Quad-Core LEON4FT Processor

**COBHAM**

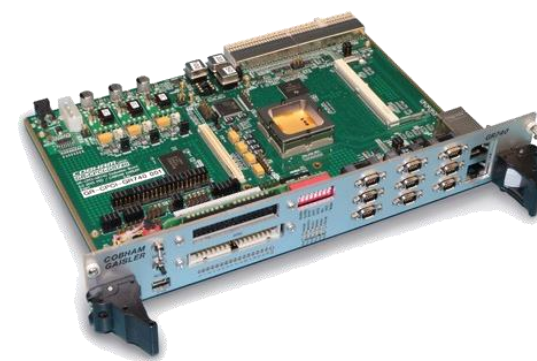
## Status update

- 250 MHz quad-core LEON4FT rad-tolerant device
- ESA Next Generation Microprocessor activity
- LGA625 / CGA625 package
- ST 65nm bulk CMOS process
- Tested prototype parts: now!
- Evaluation boards with proto parts: now!
- Accepting orders for evaluation boards, but have shipped all boards!
- Presentations at MAPLD/SEE, SpW conference, JAXA conf. ...
- Worst-case frequency of 250 MHz validated in production tests
- >380 MHz operation over temperature range tested
- Total power consumption (including I/O) at 40°C:
  - 1x CPU: 1.35 W; 4x CPU: 1.85 W (1700 DMIPS)
- Benchmark results to be published in October
- Qualification partially funded: ECSS9000/QML-V/Class-S



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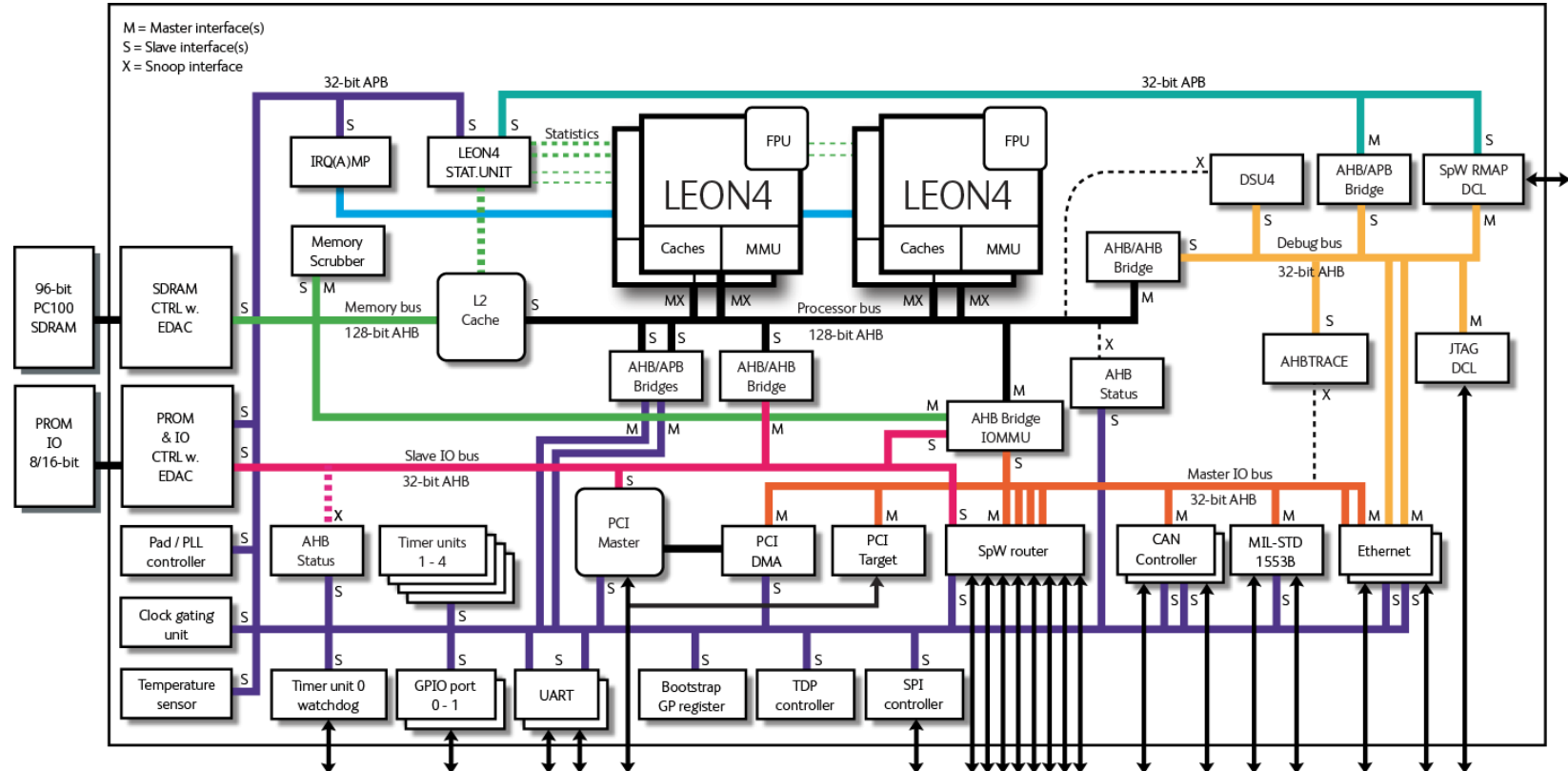
**ST**  
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# GR740 - Quad-Core LEON4FT - architecture

GR740 – designed for multi-processing

- Quad-core LEON4FT with dedicated FPU and MMU
- 128-bit L1 caches connected to 128-bit AHB bus
- 2 MiB L2 cache, 256-bit cache line, 4-ways
- 64-bit PC100 SDRAM memory I/F (+32 checkbits)
- 8-port SpaceWire router with 4 internal ports
- 32-bit 33 MHz PCI interface
- 2x 10/100/1000 Mbit Ethernet
- Debug links: Ethernet, JTAG, SpaceWire
- MIL-STD-1553B, CAN 2.0B, 2 x UART, SPI master/slave, GPIO, Timers & Watchdog



- Cobham Gaisler aims at providing components for the space market
  - Single-Core LEON3FT Microcontroller GR716
  - Dual-Core LEON3FT Processor GR712RC
  - Triple-Core Xentium / LEON3FT Digital Signal Processor GR732
  - Quad-Core LEON3FT Processor GR740
  - SpaceWire Router GR718B / LVDS GR54LVDS049/031/032
- The ECI program is of outmost importance for Cobham Gaisler
  - ECI vs GSTP vs TRP
  - Sweden is a small country with a small GSTP budget
  - No actual production in Sweden, only intellectual capital
  - Production is made in France, Italy, Belgium, United Kingdom etc., thus sales of components benefits many countries in the end
  - Important to have ESA involvement in qualification
- The SPARC/LEON success story and the importance of second-source(s)
  - Never before have there been so many alternative sources for a common processor architecture, a unique situation in space
  - SPARC is an open and free computer architecture
  - Continuous road map that started already in 1990 – 25 years of experience