ESTEC's Materials and Electrical Components Laboratory capabilities on testing passive components

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INTRODUCTION

The European Space Agency has its own Materials and Electrical Components Laboratories, located at ESTEC, in Noordwijk (The Netherlands). Highly qualified test engineers and state-of-the art test equipment constitute the main asset of this laboratory, whose customers are the ESA projects. Although a wide range of Electrical, Electromechanical and Electronic (EEE) components have been tested during the many years of existence of this laboratory, passive components constantly play a key role in the laboratory's backlog. Failure Analysis (FA), Constructional Analysis (CA) and Destructive Physical Analysis (DPA) on passive components like capacitors, connectors, relays, resistors and many others are part of the daily testing at the laboratory. The specialized laboratory's capabilities in testing passive components and many appropriate examples of tests carried out in the past will be presented, for example: infrared (IR) techniques for investigating short circuits in capacitors, C-mode scanning acoustic microscopy (C-SAM) for investigating possible defects in capacitors, microsection and Scanning Electronic Microscope (SEM) techniques for film precision resistors, non-destructive techniques like X-ray computerized tomography (CT) scan for obtaining 3D virtual models of multilayer capacitors, Focused Ion Beam (FIB) techniques for exposing dendrites causing short circuits, among many others that will be debated and discussed.

ESA's Materials & Electrical Components Laboratory guarantees an optimal choice of electrical components, materials and processes for ESA missions and external projects, considering the unique environmental challenges involved in building for space, additionally investigating failures to ensure similar issues do not occur on future missions. This encompasses all aspects of reliability analysis, failure analysis and radiation effects characterisation. The Labs' expertise is made available to support all ESA missions, ESA technology programs, standardization and qualification activities, and collaborative activities with the wider European space community. The Lab's research findings have also led to an authoritative database of materials, hardware and processes qualified for space applications, as well as guiding the establishment of industrial production standards.

The laboratory's customer focus is aimed at time critical, non-routine activities, that require independent and impartial approach, acting as a reference laboratory. The EEE component section conducts the core functions or test flow mentioned below:

- Failure analysis (FA): investigation aimed at exposing the failure mode in a component and trying to identify the root cause originating the failure. A frequently asked question is whether the failure is a one-off problem or a lot reliability concern.
- Destructive physical analysis (DPA): series of inspections, tests and analyses performed on a sample of components to verify that the material, design and workmanship used for its construction, as well as the construction itself, meet the requirements of the relevant specification and are suitable for the intended application.
- Constructional Analysis (CA): series of inspections which primary aim is to provide an early indication of a component's constructional suitability for meeting the specified performances of the space project application. Constructional analysis usually implies more intensive testing that destructive physical analysis.
- Miscellaneous investigation (MI): any set of individual tests performed during the aforementioned FA, CA or DPA test flows.
- Radiation Analysis (RA): set of tests aimed at exposing the components to radiation in order to assess their performance and reliability at specific radiation doses.

01 XRAY

The lab currently possesses redundant X-ray capability. This is a key capability in the field of non-destructive testing. There are two X-ray instruments with computerized tomography (CT) capabilities. One of them has two x-ray tubes: one up to 180kV for high resolution images and another one up to 300kV, for high density samples. A powerful computer cluster connected to this instrument allows for relatively quick CT reconstructions.

The number of applications of X-ray investigation for failure and constructional analysis is enormous. For instance, it is a powerful tool in order to get information about the internal structure of relays (Fig. 1 to Fig. 3 refer).

Fig. 1 X-ray view of a high voltage relay

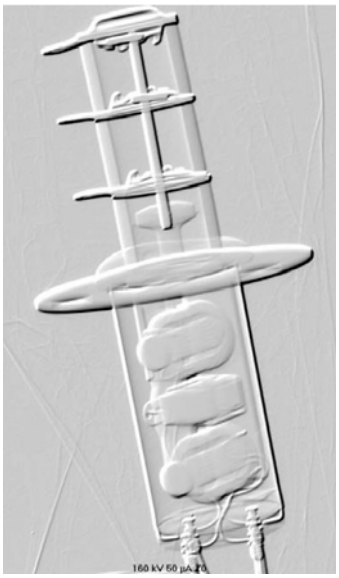

Fig. 2 Relief enhanced version

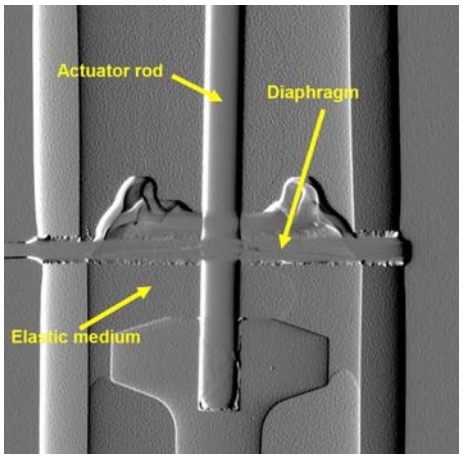

Fig. 3 Detailed view identifying different parts of the relay

In most of the investigations carried out in the lab, this is a decisive tool in order to detect the failure location. For instance, in the following flex circuit submitted to the lab for failure analysis investigation:

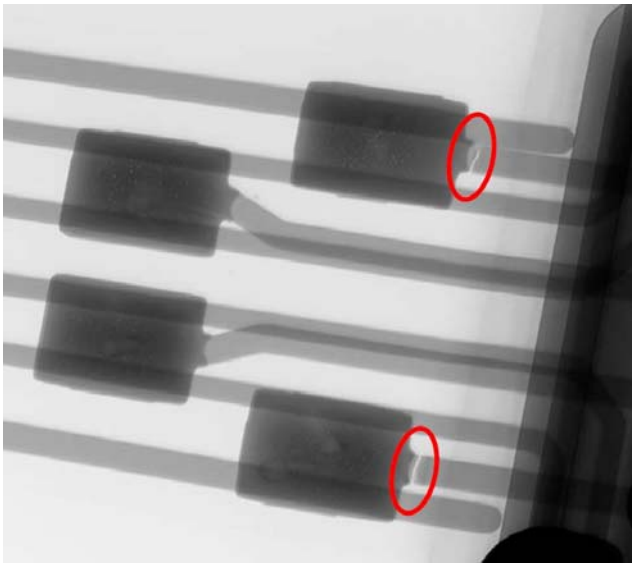

Fig. 4 Quick identification of failure mode thanks to x-ray

A view of a flex circuit soldered onto a connector is shown in Fig. 4: the fillet formed onto the flexible circuit by the epoxy resin around the connector reaches very close to the first row of soldering pads on the flexible circuit, concentrating any bending stress on a length of flexible circuit only. The x-ray image in Fig. 4 clearly shows open circuits at the location where they exit the soldering pads, close to the epoxy resin fillet.

Some interesting unexpected features were found when performing x-ray investigations in a set of tantalum capacitors submitted to the lab for a constructional analysis. Fig. 5 illustrates anode risers in the multi-slug design that were found to be bent. Furthermore, Fig. 6 shows that some slugs in the multi-slugs designs were bent too. These matters were not considered to constitute an immediate threat on the part, but it was recommended to discuss them with the manufacturer in order to fully understand their origin and long term potential reliability effects.

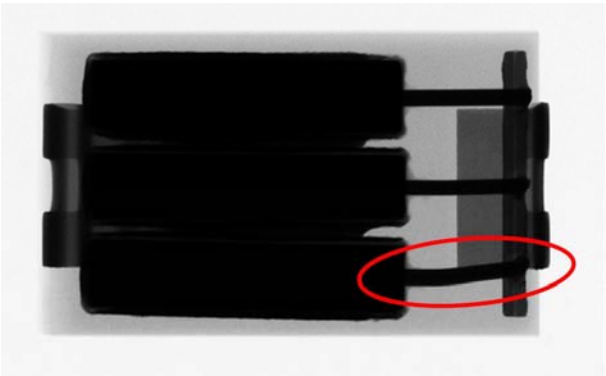

Fig. 5 Anode risers in tantalum capacitor

Fig. 6 Bent slugs in the same type of tantalum capacitor

02 CT SCAN

The real power of the X-ray tool lies on the possibility of performing computerized tomography (CT) scans. For instance, three connectors were delivered to the laboratory for performing a failure analysis investigation, mentioning a loose centre contact assembly which was recessed too deeply in the shell. These parts were triaxial connectors designed to be inserted into round multi-pin connector assemblies. One of the samples had an external crimp length of 11mm, where the specification states only 6mm. Fig. 7 illustrates the wrong crimp length on the first part (at the top) and a correct crimp length of 6mm on the other two parts (at the bottom). This wrong long crimp caused several cracks on the connector outer shell (see Fig. 9). In addition to this, this same sample had a centre assembly set back in the body by 0.38mm (see Fig. 8).

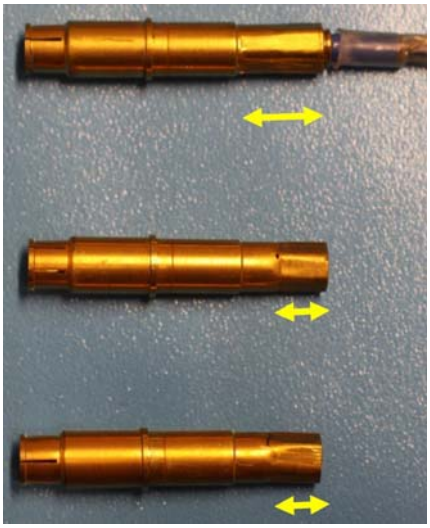

Fig. 7 Wrong crimp length on top part

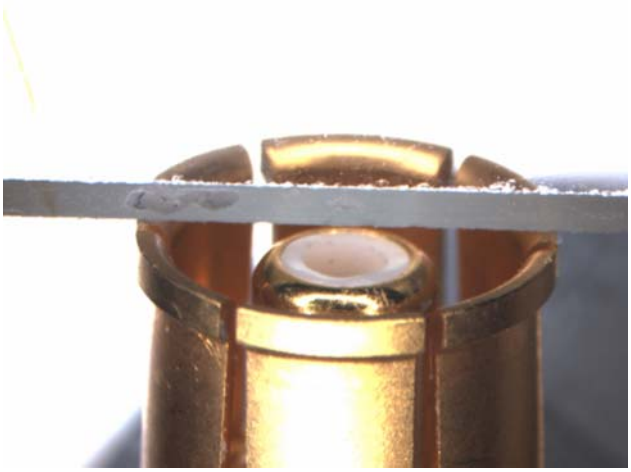

Fig. 8 Recessed centre assembly on top part of Fig. 7

Several CT scans were performed on this part, focussing on its front-end and rear-end (or cable end, Fig. 10 refer). One of the big advantages of this technique is the possibility of doing virtual sections of the parts. Fig. 11 illustrates the body cracking associated with the over-long crimp in the reference sample, labelled as “Indicator 1”. Note that a 6mm long correct crimp would have been confined to an end region of the body with a deliberately reduced wall thickness to facilitate the deformation (see the red arrows in Fig. 11). By extending the crimp length, a much thicker wall was deformed and immediately next to the outer surface section change, the forces used resulted in through cracks.

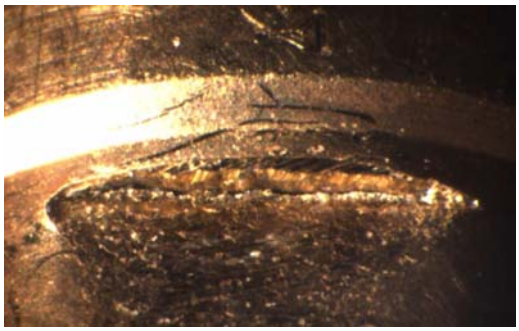

Fig. 9 Cracks on the outer shell of the connector

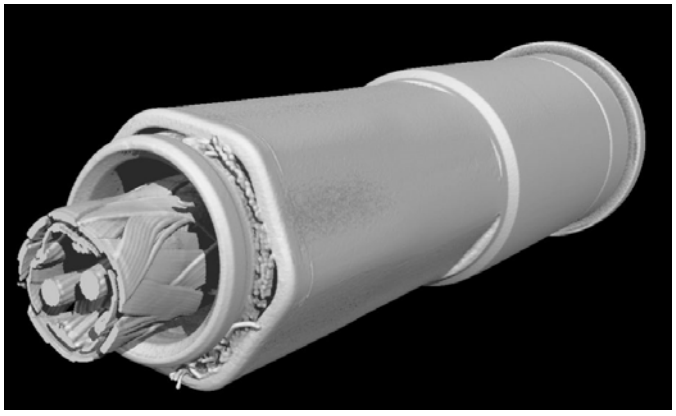

Fig. 10 3D model CT scan

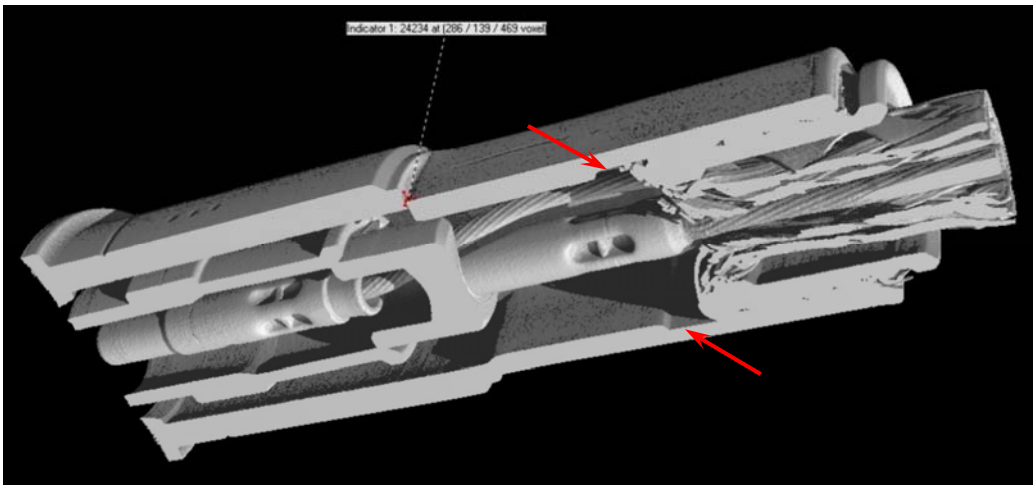

Fig. 11 Red arrows show the correct location for end of crimp length

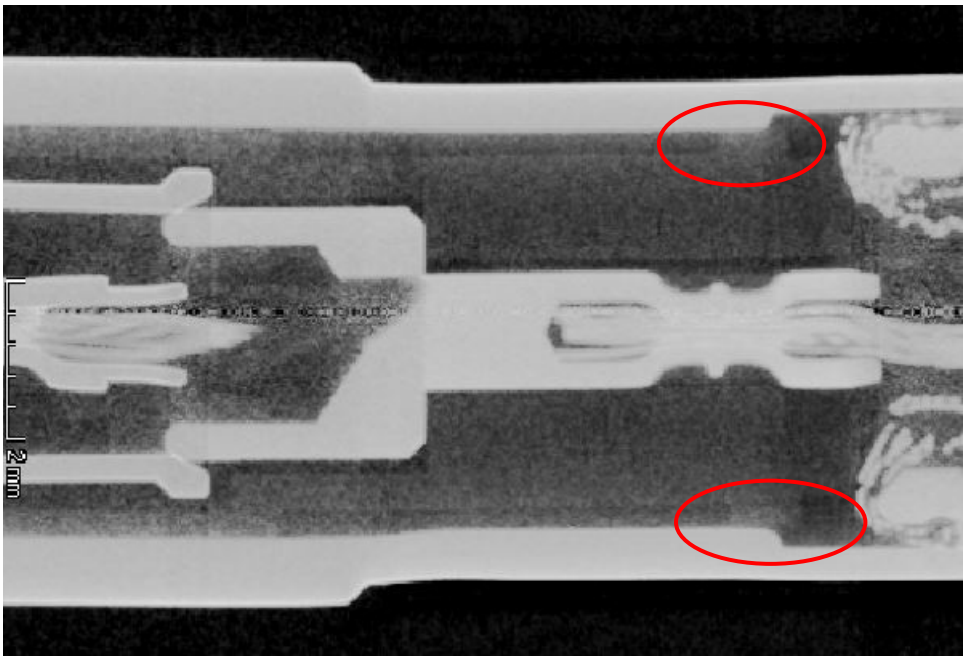

Fig. 12 Red circles highlight the PTFE insulator flange incorrectly positioned

Fig. 13 The PTFE insulator exposed

Obviously, X-ray techniques are not suitable to show images of internal non-metallic components of any part. However, with a proper setup of the x-ray instrument and of the reconstruction techniques, it is not impossible to see interesting features. This way, the CT scans revealed that a split polytetrafluoroethylene (PTFE) insulator used to assemble the connector was incorrectly placed inside the connector. The flange on this insulator faced the rear-end of the assembly, which is simply the opposite direction outlined in the specification. Fig. 12 shows a contrast enhanced image of the section in Fig. 11 in which the flange of the PTFE insulator can be identified. This caused the rearward displacement of the centre pin assemble. Subsequent destructive testing exposed the PTFE insulator. Fig. 13 illustrates that the flange was deformed from the original circular form into hexagons. This demonstrated that the insulator flange was incorrectly placed within the crimp deformation area.

The CT scan tool has also proven to be a big help while investigating the failure mode of a multilayer chip capacitor that was submitted to the lab together with three unused samples of the same batch and date code as the failed one. The failed part was massively cracked and the lab was asked if the cracking caused the electrical failure or was only a consequence.

An optical microscope image of the crack seen on the top surface of this capacitor is illustrated on Fig. 14. CT scan allows for virtual sections of the part, one of which is shown in Fig. 15, where a plan view tomographic section on the principal delamination plane can be identified. The main cracks of this capacitor are illustrated in the tomographic model in Fig. 16.

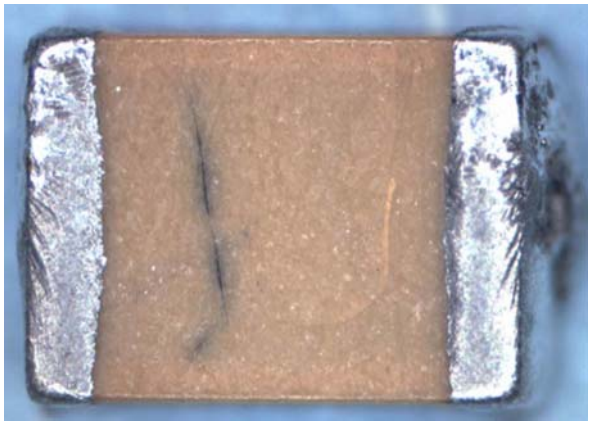

Fig. 14 Top view of the failed capacitor

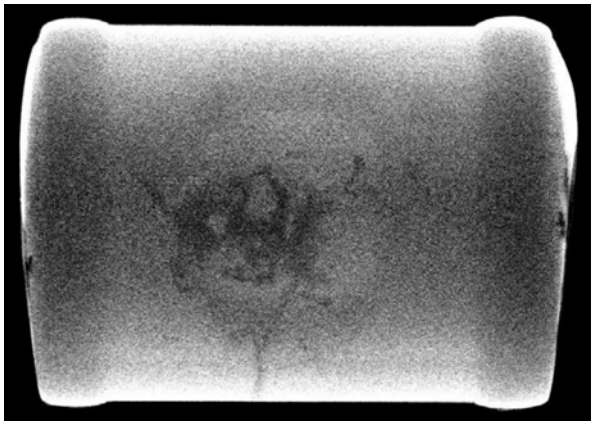

Fig. 15 A tomographic section on the delamination plane

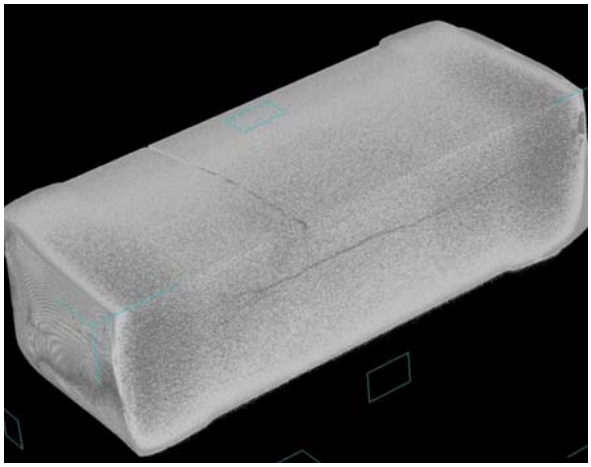

Fig. 16 Main cracks in the capacitor

As other unused parts were provided with this failed capacitor, these were also sectioned, and some relatively large pores were discovered between the electrodes. Some of them were larger than the requirements expressed by the procurement specification: dielectric thickness shall not be reduced by more than 50% by voiding.

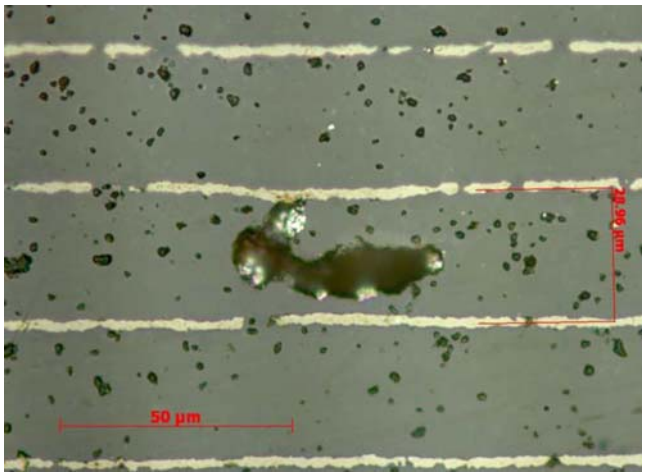

Fig. 17 Optical microscope section of a void found in an unused capacitor

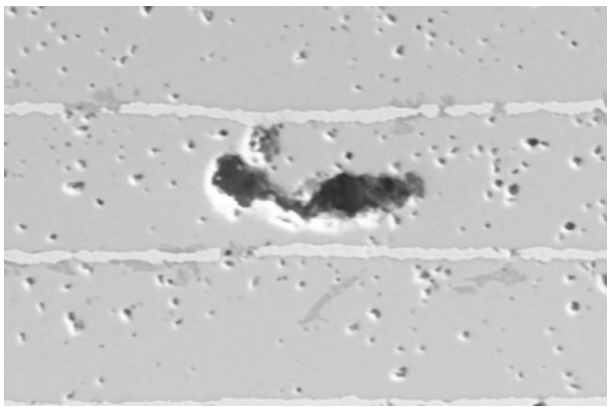

Fig. 18 Secondary electrons SEM view

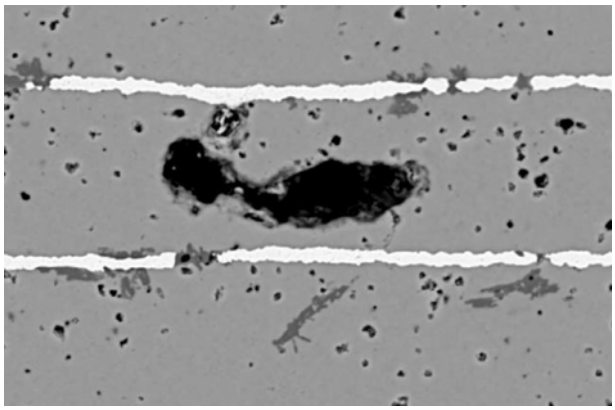

Fig. 19 Backscattered electrons SEM view

An optical microscope image of one particularly large pore, a secondary electron SEM image of the same pore and a backscattered electron SEM image of it are shown, respectively, on Fig. 17 to Fig. 19. The Everhat-Thornely Detector (ETD) image gives an impression of the depth of the void. The Backscattered Detector (BSD) image shows the edges of the void more clearly and gives more materials contrast. This pore is comparable in size to the inter-electrode spacing. In case an internal void reaches between adjacent plates, that would guarantee eventual failure. This information produced enough evidence to provide two possible explanations of the cracking pattern:

1) The cracks originated from an electrical short circuit associated with excessive porosity close to the parts centre causing layer delamination followed by a top surface crack as the internal stress resulted in surface strain sufficient to exceed the ceramics mechanical elongation limits.
2) The crack from the top surface to the centre was the original fault possibly caused by a worn pick and place tool. This crack extended to the capacitors neutral axis and electrical failure by moisture access and short circuit occurred later causing the delamination effect.

In any case, most likely the parts contained porosity on a scale sufficient to cause failures by moisture, short circuiting between electrodes. So it was the electrical failure that caused the crack.

To illustrate the power of the CT scan tool, Fig 20 illustrates a CT scan of a relay. This model allowed for a quick detection of the pivot bar being bent (Fig 21 refer). All this information can be gathered without performing any destructive testing.

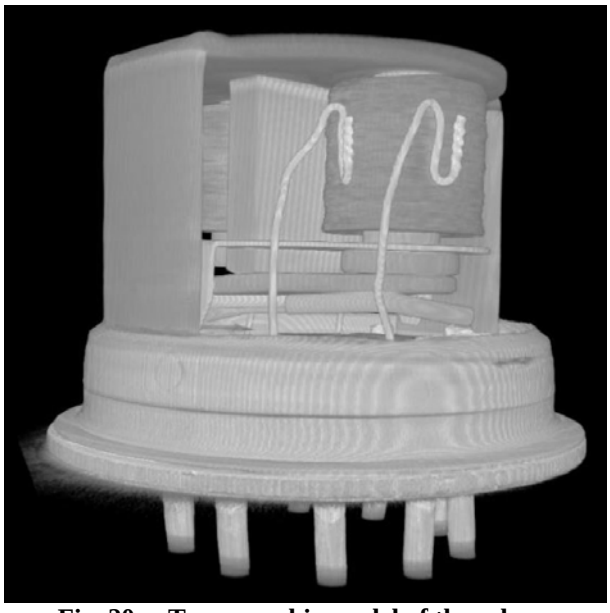

Fig. 20 Tomographic model of the relay

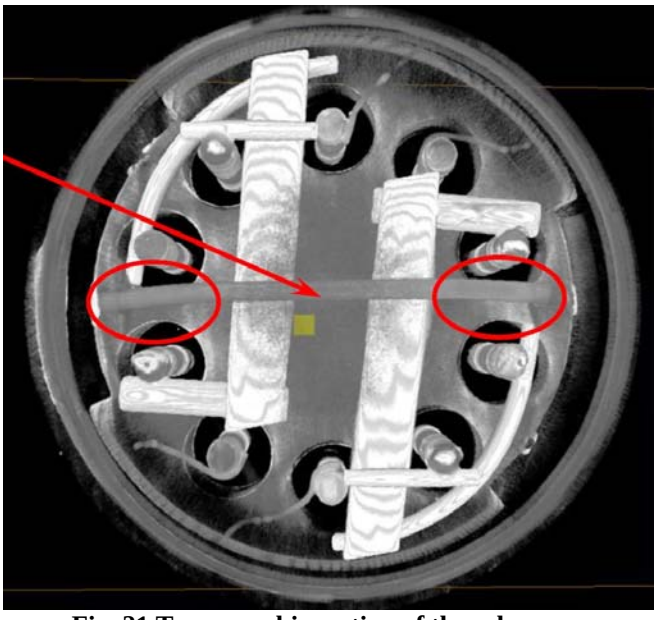

Fig. 21 Tomographic section of the relay

03 IR TECHNIQUES

The lab currently owns an infrared (IR) camera, with InSb detector and frame rate of 5Hz to 100Hz (full frame 2425@48x4). This camera offers the possibility of upgrading to a Lock-in Thermography option.

The infrared imaging technology has frequently helped our lab engineers to spot failure location in passive components in past failure analysis investigations.

Failure of a ceramic chip capacitor: for instance, a ceramic chip capacitor was delivered to the lab for failure analysis. It failed producing a short circuit when installed in an instrument. The first action was to check the part electrically. The short circuit was confirmed and submitted to hot spot detection test. Fig. 22 shows the IR image of the part when unbiased, as opposed to Fig. 23 when the part is biased. The red circle highlights the spread of lighter colour.

The IR technique has some limitations. It was decided that it was best to remove the termination metal, in order to get better IR images. Only the metal from the sides was removed. The end metal was left in place to provide continued electrical contact. Fig. 24 and Fig. 25 show a clearer breakdown area, highlighted in the ovals.

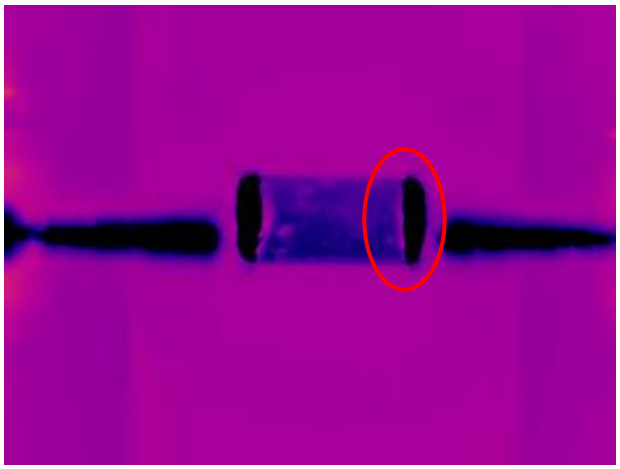

Fig. 22 IR image of the unbiased capacitor

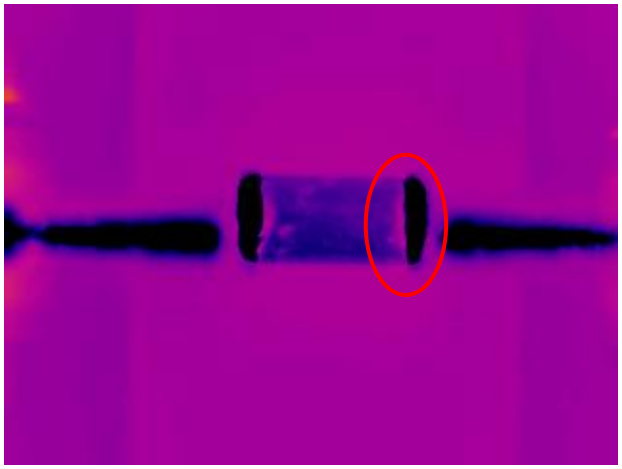

Fig. 23 IR image of the biased capacitor

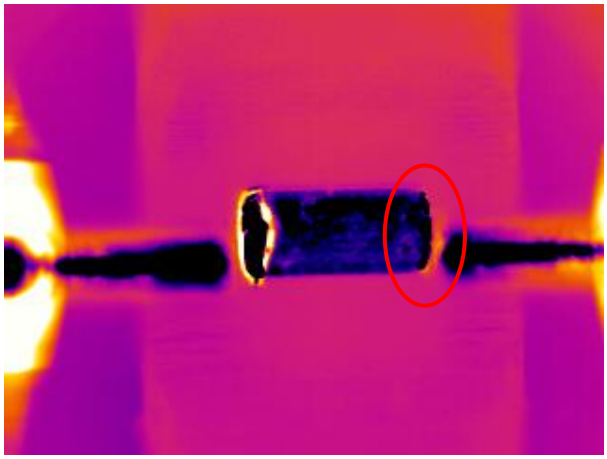

Fig. 24 Termination metal removed: unbiased

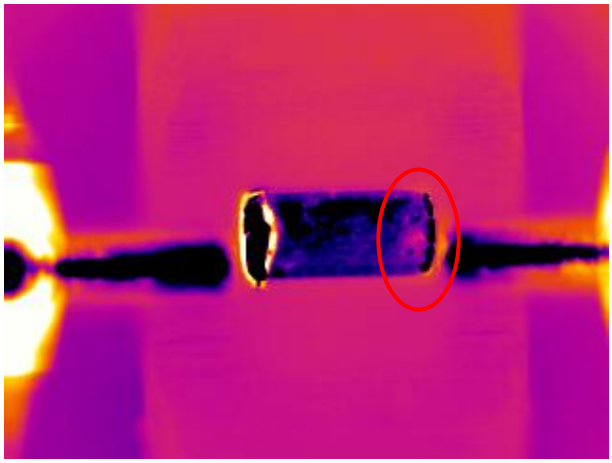

Fig. 25 Termination metal removed: biased

Failure on a tantalum capacitor: IR techniques proved to be very useful when investigating a short circuit failure in a tantalum capacitor delivered to the laboratory. IR was employed to attempt to isolate the thermal dissipation point which should lead to better pinpointing the short circuit path. The capacitor was exposed to IR both biased and unbiased. When a hotspot was detected, the capacitor was sectioned in the plane where the hotspot was found in order expose the failure site. This was done iteratively three times. At the first stage of locating the hot spot, the overall

temperature of the part could be seen to rise, but a barely perceptible early warming point could be detected in the top surface. The top surface was therefore thinned to remove the concealing plastic. Fig. 26 and Fig. 27 show the results of repeating the IR images with the top plastic thinned. The bottom edge was then thinned to the point indicated by the yellow line in Fig. 27. The edge view is shown in Fig. 28 and Fig. 29, unbiased, and then biased, after the thinning of the edge. The circled area shows the target area for the next sectional plane. Fig. 32 shows an optical view corresponding with the IR image of Fig. 30 and Fig. 31. The failure was then located and exposed in the area pointed by the IR images. With the help of SEM and EDX analysis, a point of contact between the silver cathode metal and the bulk Tantalum was found (see Fig. 33).

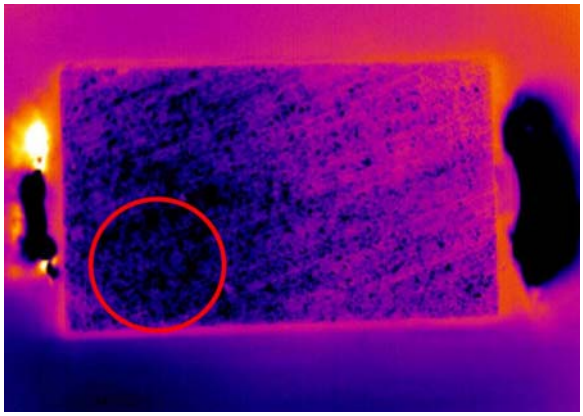

Fig. 26 Top surface thinned - unbiased

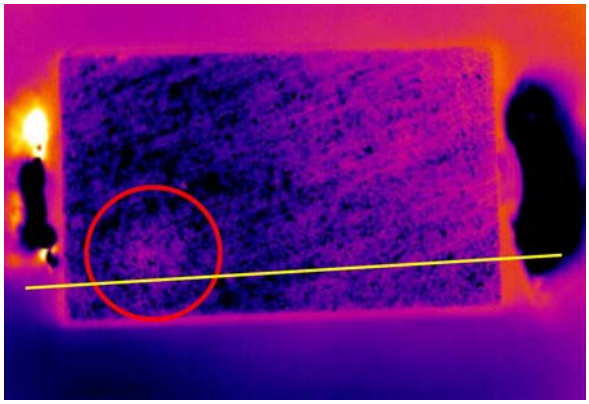

Fig. 27 Top surface thinned - biased

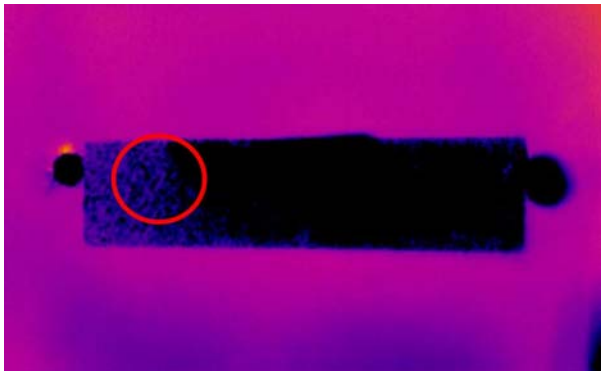

Fig. 28 Further thinning - unbiased

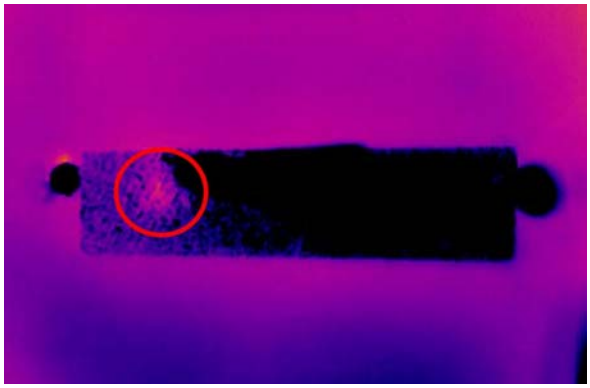

Fig. 29 Further thinning - biased

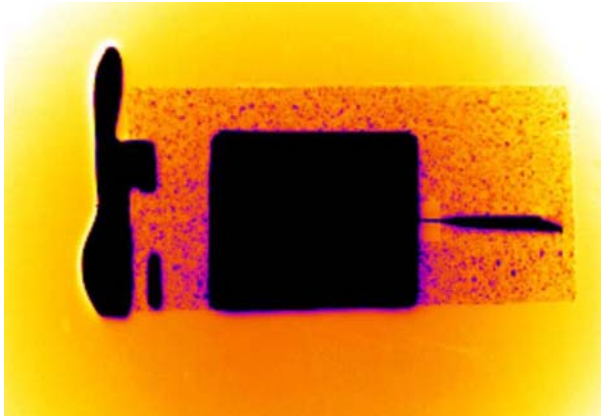

Fig. 30 Third section plane - unbiased

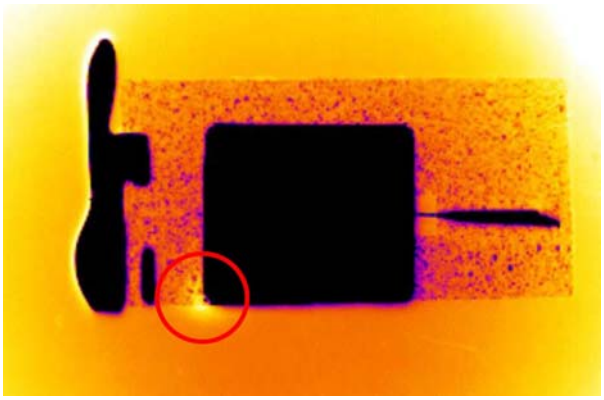

Fig. 31 Third section plane - biased

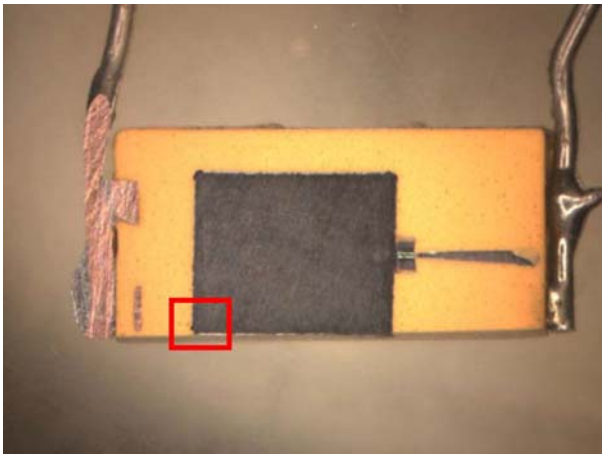

Fig. 32 Optical view of Fig. 30 and 31

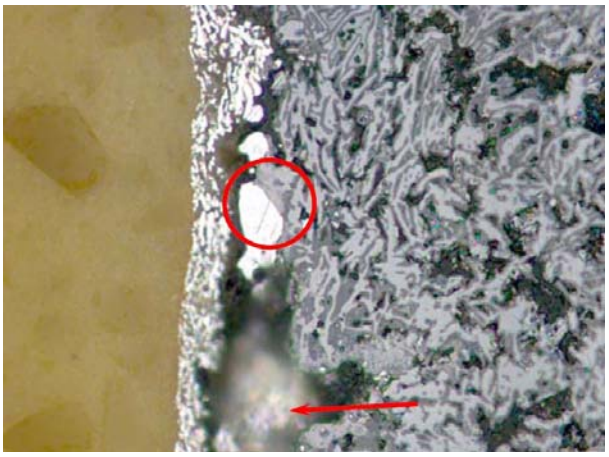

Fig. 33 Short circuit path between cathode and tantalum

These techniques help for failure localization, which is a big help micro-sectioning the part afterwards in the exact location where the NDT techniques predicted the failure might be. This way the failure can be localized and therefore exposed.

04 CSAM

The C-SAM is a reflection-mode instrument that operates on a pulse-echo principle and produces detailed layer-by-layer information on the defects in an object. The C-mode Scanning Acoustic Microscope uses high-frequency ultrasound to travel through layers of an object: if the object has good material continuity and good bonding between layers, there is very little sound wave obstruction. However, if the object contains defects, then the sound wave is obstructed and a contrast will appear in the acoustic image. This is one of the non-destructive tools frequently used in the lab to identify cracks, air gaps, delaminations, porous areas or other anomalies in EEE components.

Some examples on how the C-SAM has been used in the past in the lab are described below.

A series of polyester capacitors was submitted to the lab for a thorough investigation of specific design elements. Among others, possible delaminations between the case and the potting epoxy. The C-SAM did not detect any delaminations in these capacitors.

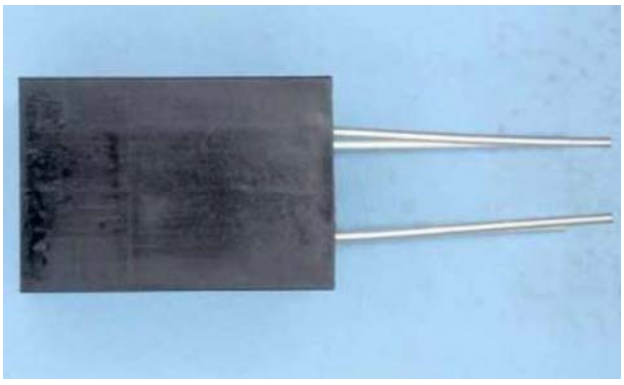

Fig. 34 Optical top view of polyester capacitor

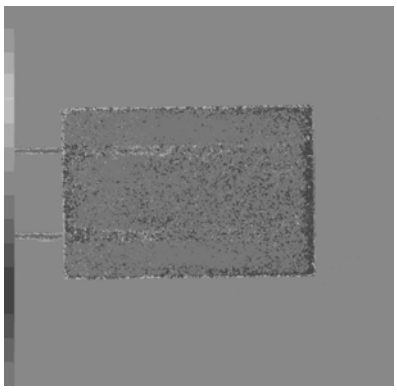

Fig. 35 CSAM image of polyester capacitor

In order to check the validity of this investigation, deliberate delamination was created to verify the technique, **Fig. 36** refer.

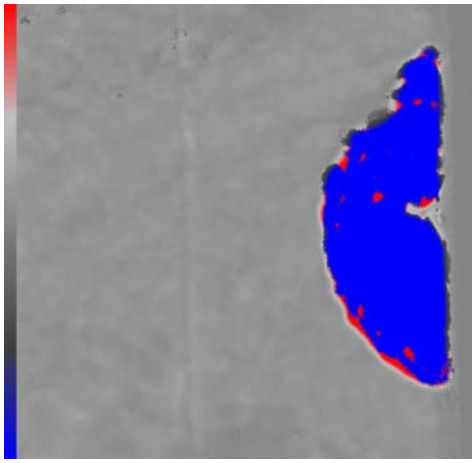

Fig. 36 Intentioned delaminations

This technique has helped to detect some defects in a tantalum, solid electrolyte surface mount chip capacitor that was investigated in the lab.Fig. 37 shows the bottom view of the capacitor and Fig. 38 shows the CSAM image of the bottom layer of the capacitor.

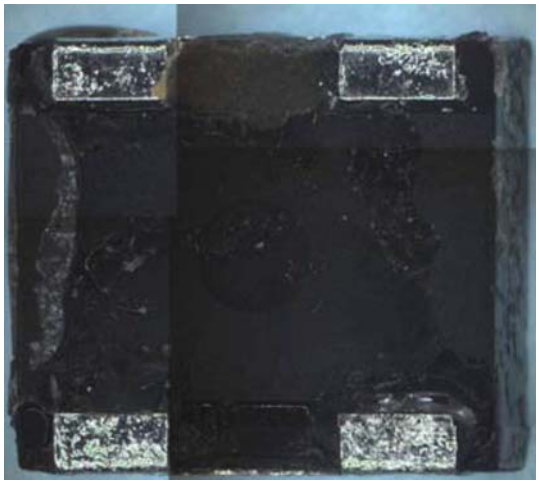

Fig. 37 Optical bottom view of the capacitor

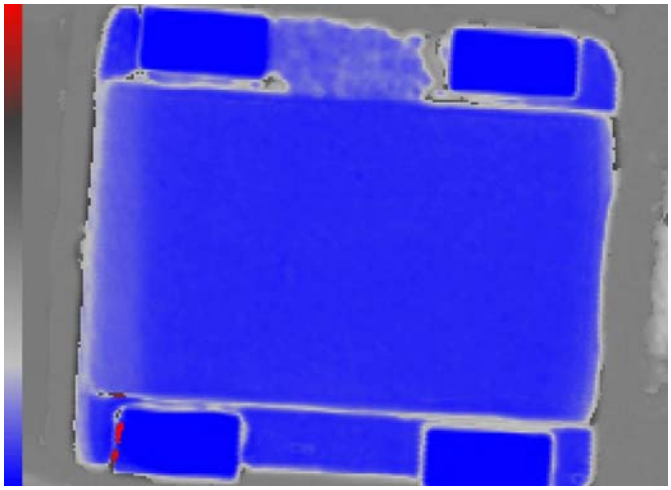

Fig. 38 CSAM image of the bottom layer of the capacitor

Red areas in Fig. 39 illustrate the CSAM image of the interface between the tantalum and the moulding resin. Instances of poor adhesion and delamination in this interface are clearly visible. This is not uncommon, though, in resin moulded parts. No evidence that such defects extended along the entire part body was found during C-SAM analysis.

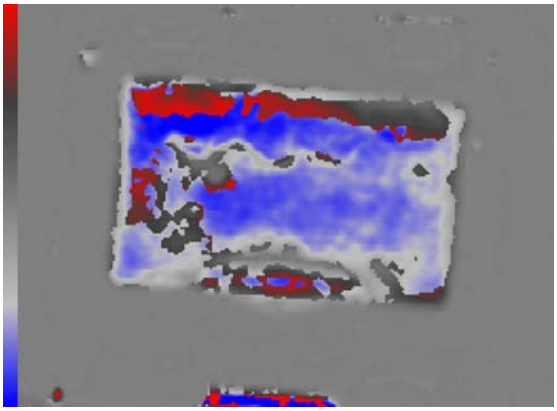

Fig. 39Delaminations at the resin to tantalum core interface (red areas)

05 MICROSECTION

Several techniques are used in the lab for performing microsections on the parts that are investigated. This is a way of exposing internal areas of particular interest, especially when trying to show a failure site.

One multilayer chip capacitor was delivered to the lab for failure analysis investigation. Electrical measurements demonstrated an anomaly in the capacitor at lower frequencies. The part (Fig. 40) was potted in epoxy resin and microsectioned (Fig. 41). Two different cracks can be seen in this section (see red arrows in Fig. 41):

1) One crack on the top left corner, a typical of the type of crack normally associated with thermal stress cracking, but is thought to have no effect on the performance degradation noted in this instance.

2) A defect characterised through a delamination of the bottom plate which made a transition to the next plate up in the structure, by way of a crack, and was effectively continuous from terminal to terminal. This is also thought to be a possible thermally generated defect.

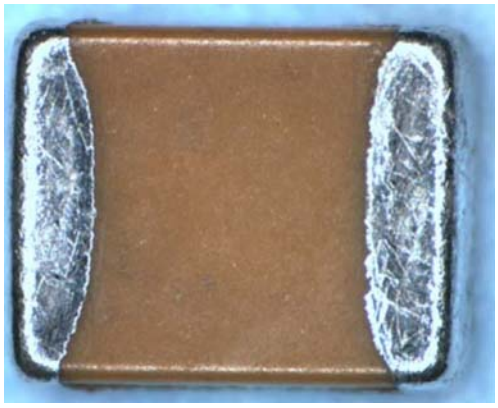

Fig. 40 Top view of failed capacitor

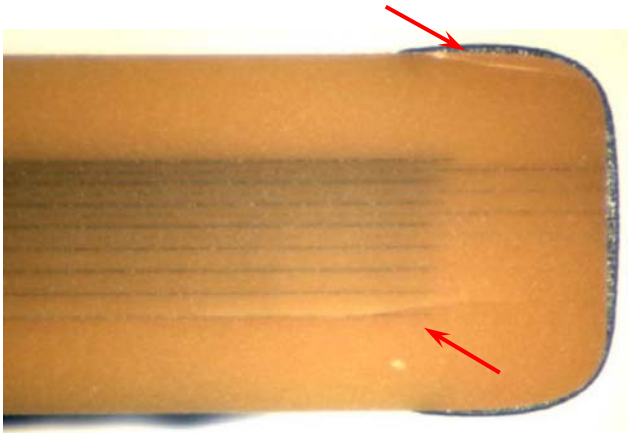

Fig. 41 Cracks (red arrows) detected in sectioned part

Two other capacitors, unrelated to the one mentioned above, were sent for failure investigation to the lab. Some cracks were observed on their surface (Fig. 42 and Fig. 43 refer):

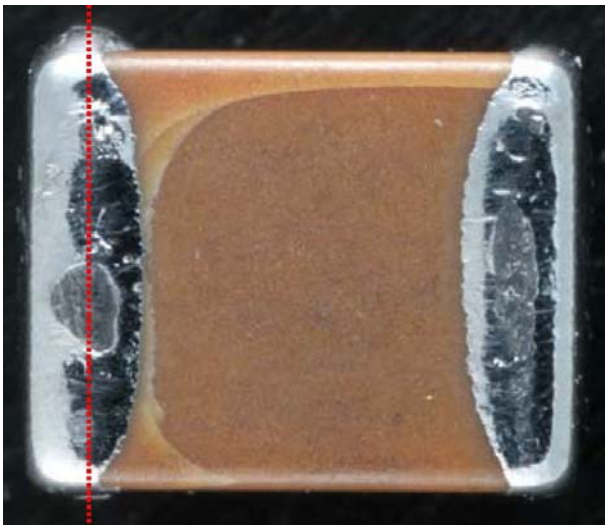

Fig. 42 Capacitor 1 general view

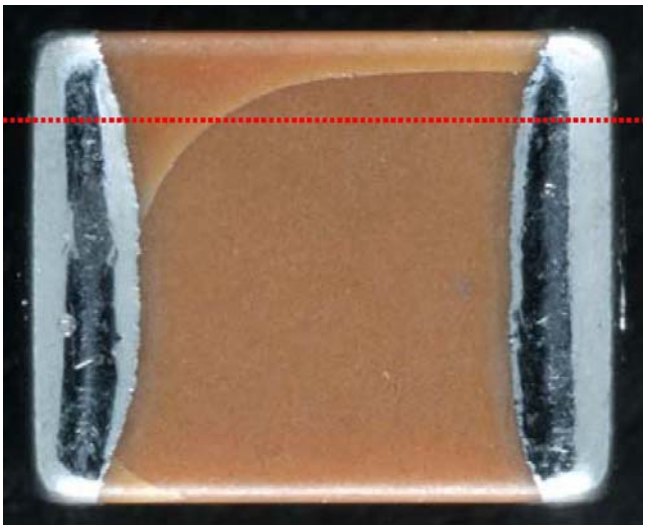

Fig. 43 Capacitor 2 general view

The shape of the cracks observed in the received samples is typical of thermal-shock induced damage, no external mechanical damage (like dents or scratches) could be observed in correspondence with the cracks. These two parts were potted in resin and cross sectional views of the samples were obtained by grinding and polishing along the red dotted line indicated in Fig. 42 and 43.

The cross-sectional views (Fig. 44 and 45) proved that the cracks observed during the visual inspection are not just cosmetic, since they connect two or more electrodes, and these electrodes to the surface, and to one of the terminations.

The shape of these cracks are typical of thermal-shock induced damage and strongly supports the conclusion that these cracks have been induced by some thermal shock experienced during the pre-tinning process. The fact that no external mechanical damage (like dents or scratches) could be observed in correspondence with the cracks is also in line with this conclusion. Moreover, the micro-section evaluation showed that these cracks are not just cosmetic surface damage but they reach to the plates and the termination, and they can be hidden under the metallization of the terminations, thus potentially affecting components without showing on the surface.

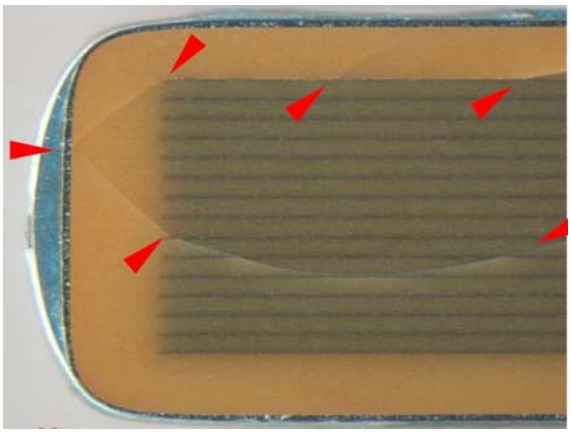

Fig. 44 Cross-sectional view of capacitor 1

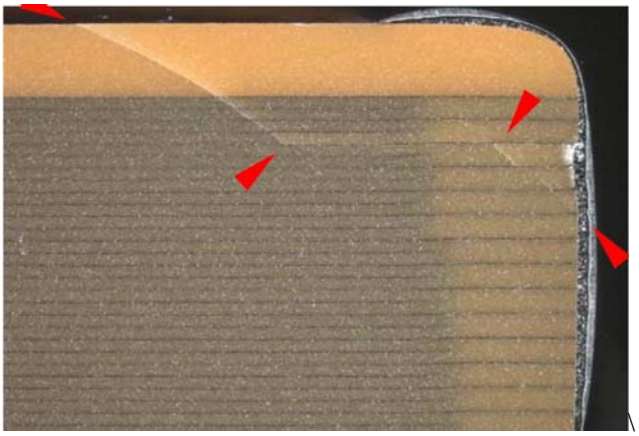

Fig. 45 Cross-sectional view of capacitor 2

06 SEM AND FIB

The lab currently possesses four field effect gun Scanning Electron Microscopes (SEM).

This tool can be used for many different purposes. For instance, for investigating two capacitors that were delivered to the lab in order to investigate the appearance of tin whiskers after 500 temperature cycles.

The inspection revealed several tin whiskers at different growth stages (Fig. 46):

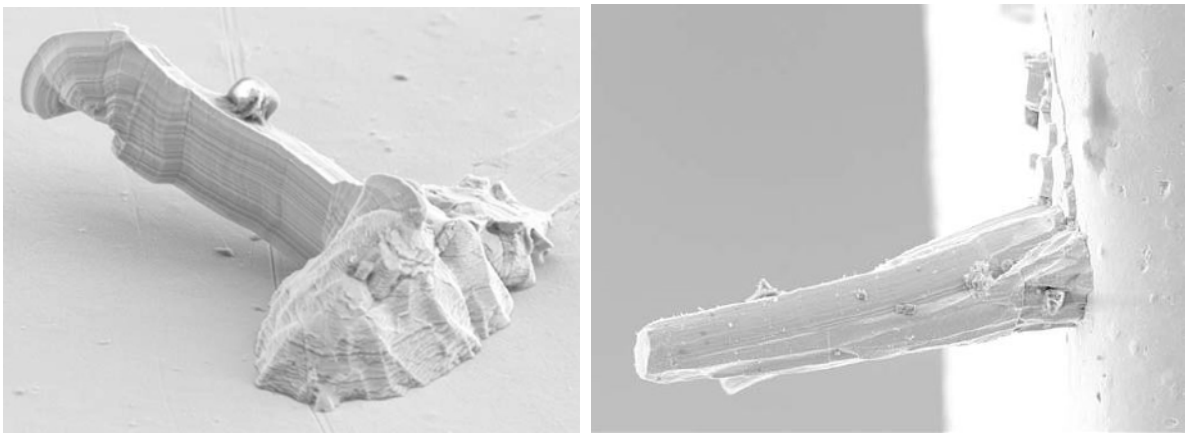

Fig. 46 Examples of tin whiskers found in the capacitor

On another investigation, three thin film resistors were submitted to the lab for qualification testing. One of these resistors (Fig. 47 refer) showed two cracks on its substrate the length of which exceeded the maximum allowed by the specification.

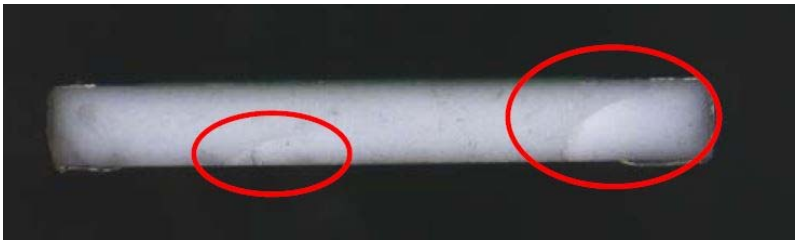

Fig. 47 Cracks along the side of the substrate of the thin film resistor

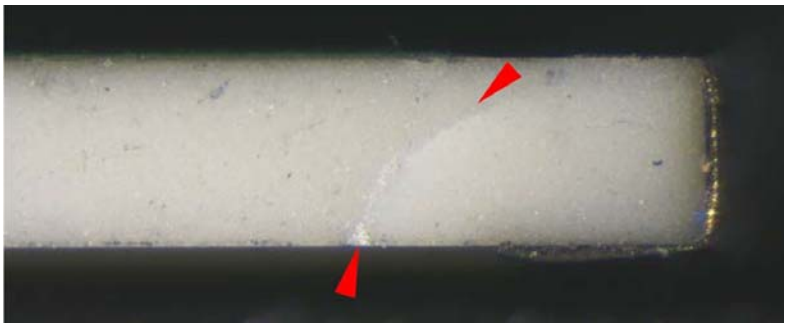

Fig. 48 Zoomed view of the longest crack in Fig. 47

Two FIB cuts (Fig. 49) were performed along the crack shown in Fig. 48:

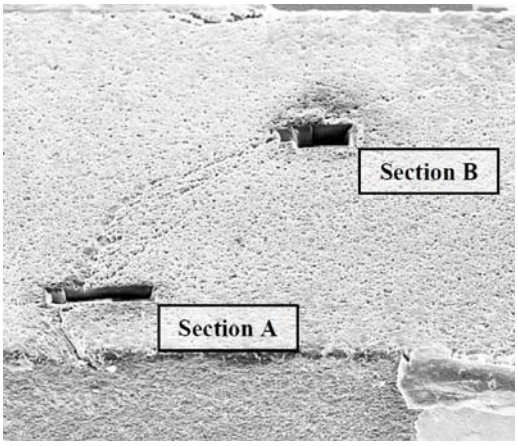

Fig. 49 SEM view of the FIB sections along the crack in Fig. 48

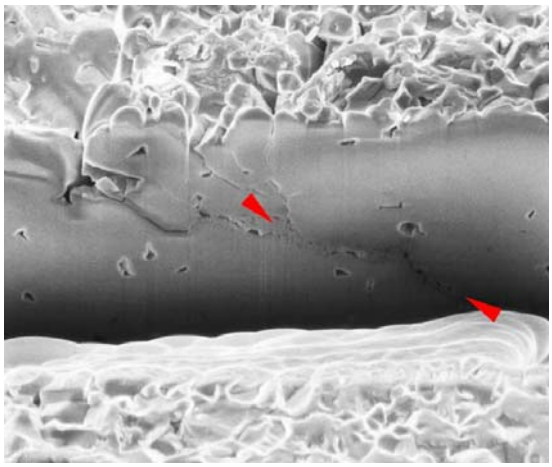

Fig. 50 SEM view of FIB section A

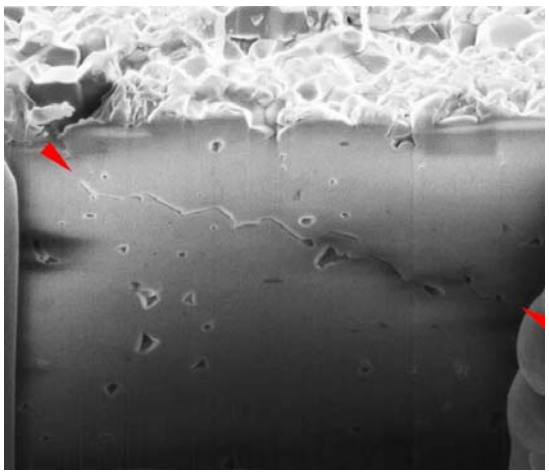

Fig. 51 SEM view of FIB section B

The red arrows in Fig. 50 and 51 indicate the crack propagating within the bulk material. This demonstrates that the crack is propagating inside the bulk material and allowed for a precise measurement of its length, which is out of the specification limits.

A very interesting failure investigation carried out in the lab was performed on an electronic component, in which two of its three leads were unintentionally internally short circuited. The package material was kovar, with three leads attached to the package body through a glass seal. On each of the parts examined, there was a notable reduction in the diameter of the lead, where it is not enclosed in the glass of the seal. The reduction is of the order of 20 microns overall. Additionally, the etching solution used for electroplating crept down the interface between the glass and the lead to a depth approaching 150 microns, well below the glass meniscus surface down the sides of the lead. The nickel plating was therefore deposited into this gap to an equivalent depth. In the area where the dendrites were formed there was therefore a nickel seed layer which could support a pure nickel dendrite formation. The concept is illustrated below (Fig. 52 refer):

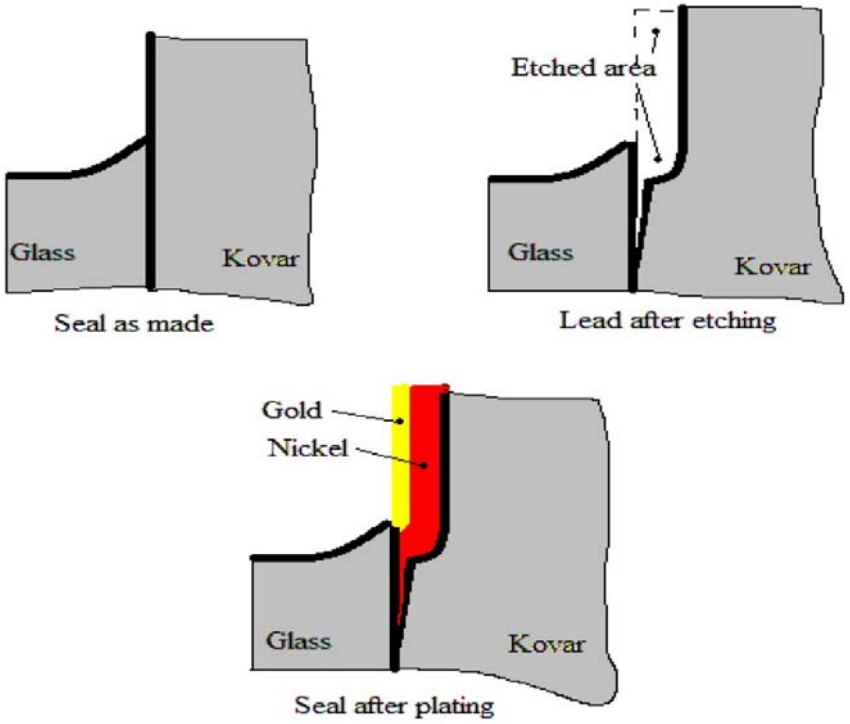

Fig. 52 Process of formation of a nickel seed layer

This was demonstrated by the EDX analysis produced the following results (Fig. 53):

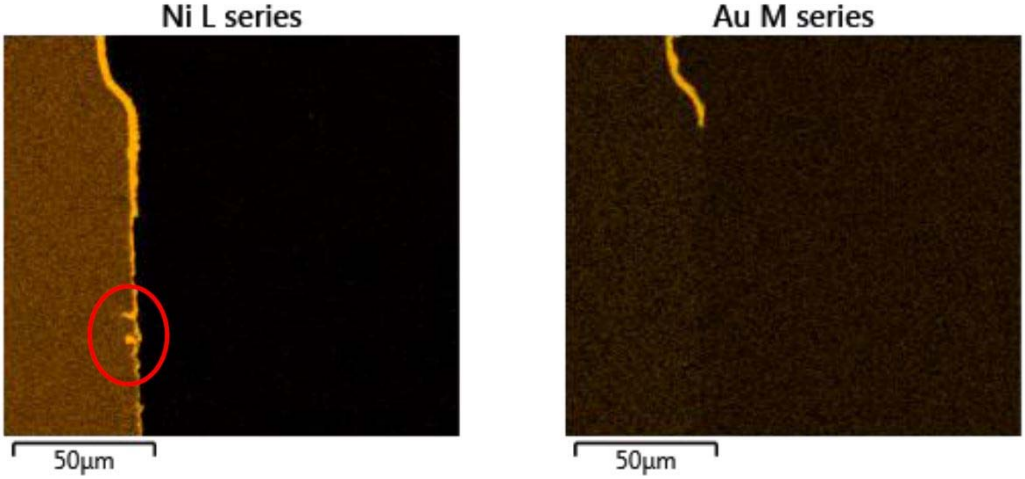

Fig. 53 EDX analysis right at the meniscus area

Nickel is the external layer of the leads inside the glass seal. Some of these packages presented a crack in the glass seal. Time and a proper chemical activator caused a linear growth of the nickel through the crack in the glass seal: a dendrite. Eventually, this led to a short circuit in the package and a subsequent component failure. The mechanism causing the cracks in the glass seal could not be discovered.

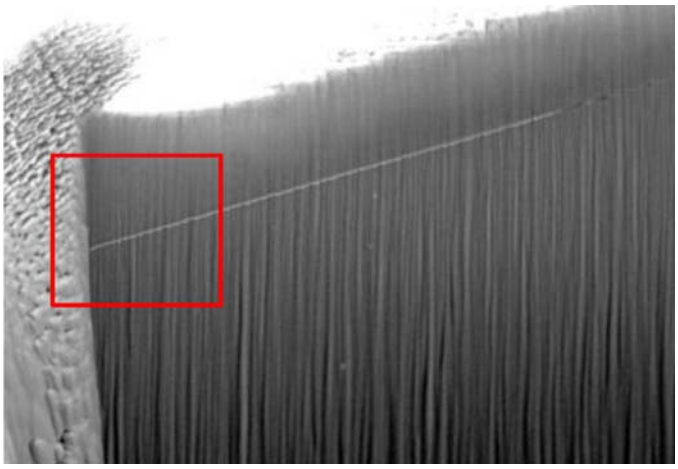

Fig. 54 FIB cut exposing the dendrite

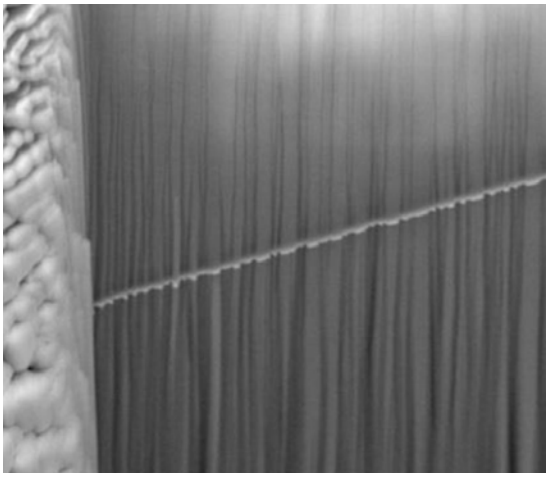

Fig. 55 Zoomed image of dendrite in Fig.54

REFERENCES

All the cases exposed in this paper have been based on ESTEC's Material and Electrical Components Laboratory confidential reports. Therefore, they cannot be referenced here.

AUTHOR

Joaquín José Jiménez Carreira has a Telecommunications Engineering Master Degree by the High School of Engineers at the University of Seville (Spain). He worked during seven years at the Parts Laboratory Department at ALTERTECHNOLOGY TÜV Nord S.A.U., Seville (Spain), performing all kinds of complete test flows on EEE components for aerospace qualification, mainly for ESA projects, including radiation test campaigns, RF/MW component testing, internal trainings and direct technical support to external customers. In September 2014 he took up his current position as EEE component engineer at ESTEC's Materials and Electrical Components laboratory (Noordwijk, the Netherlands), mainly performing DPAs, CAs and FAs test flows.