Large deformable MEMS mirror array

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What does that mean?

2D Tilting capability
+/- 4.5° @ 150V DC

Silicon based
Electrostatic actuation

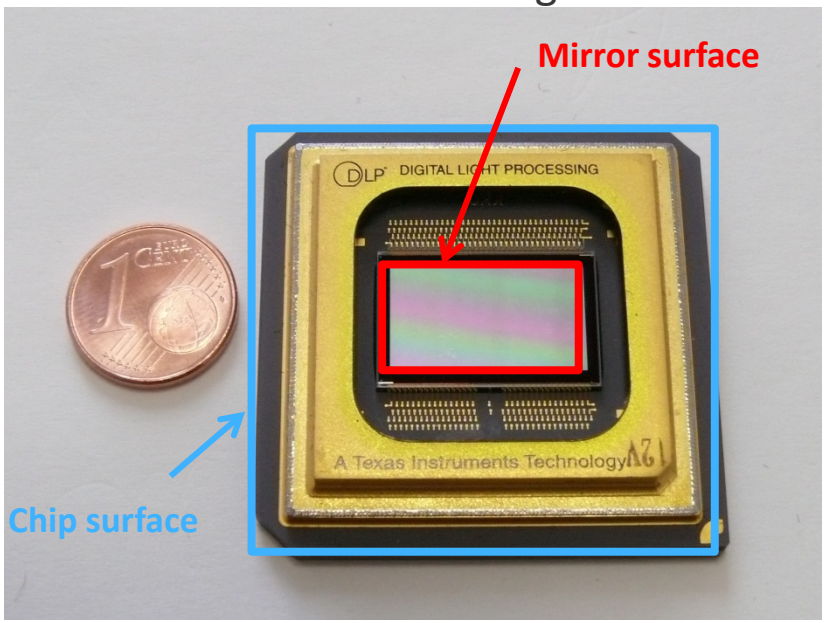
Large Deformable MEMS Mirror Array

High reflectivity

High fill factor
Large surface

Why doing this development?

- No product available for supporting high optical power load (>1kW/m2) or harsh environment
- Surface limited by packaging
- Fill factor limited for large surface



<u>The famous DLP from Texas Instrument</u>

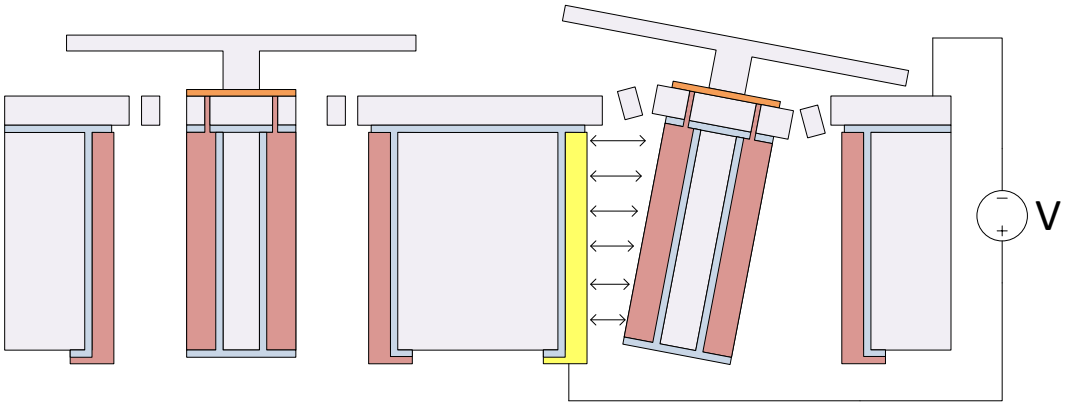
- Leader of the Micro Mirror Array market
- 1D tilting
- Around 25% of surface covered with mirror
- Maximum temperature supported by the mirror: 150°C (about 1W IR laser in air)
- Not compatible at cryo temperatures

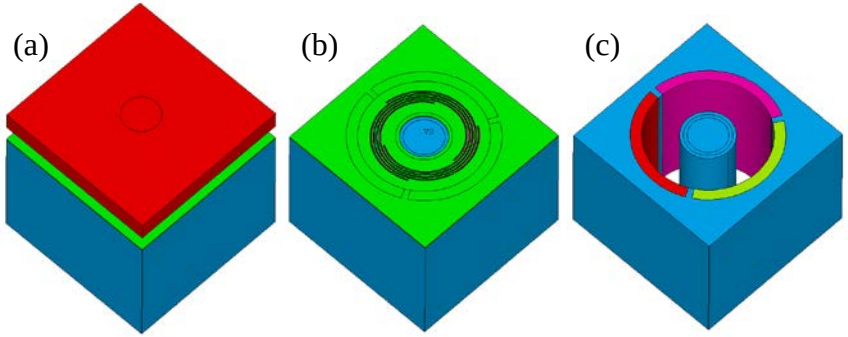
Objectives and applications

- Objectives
  - 2D tilting mirror possibility (no actuation in this study)
  - Large mirror surface (14x14mm) containing 400 mirrors
  - Low packaging surface (<16%)
  - Vertical integration of the electrical interconnections
  - Backside interconnections of the chip to BGA or POGO pin (spring loaded pin)
  - No glueing. Magnetic clamping.
  - Possibility of extended array by juxtaposition of the MMA
- Applications
  - Beam shaping
  - Adaptive optics

Concept - Actuation

- DC Electrostatic actuation up to 150V (4.5° mechanical)

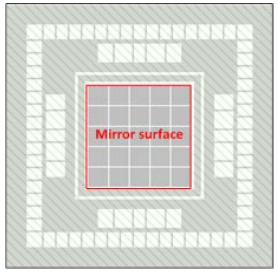




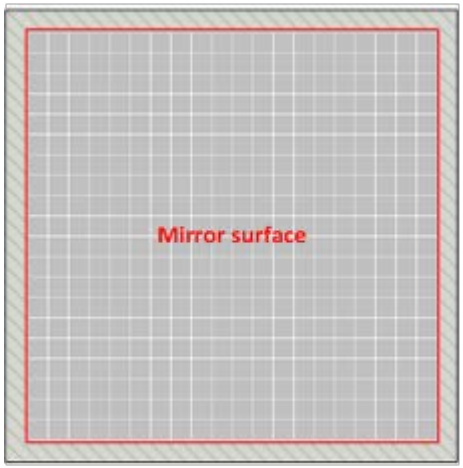
Concept – Mirror surface

- Previous concept by *Ataman et al.* was based on:
  - 5x5 mirror array
  - Fill factor of 12 % for the mirror and packaging surface
  - Fill factor of 88% for the mirror surface

8x8mm

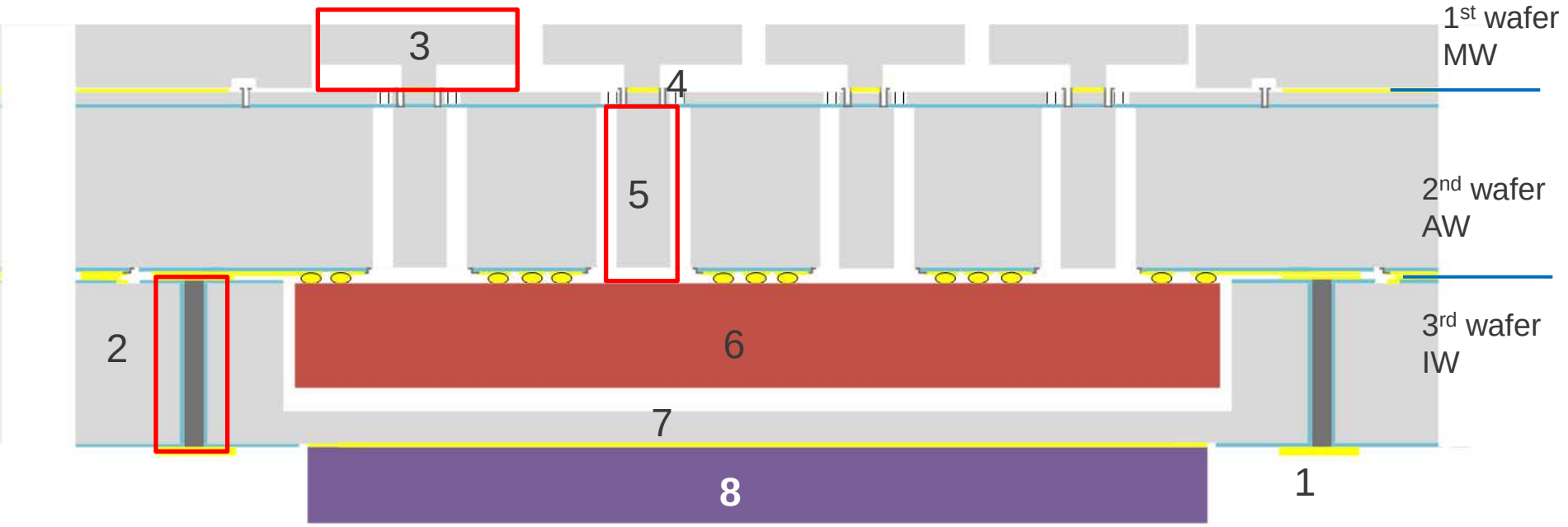


- Improved concept based on:
  - 20x20 array
  - Fill factor of 80% for the mirror and packaging surface
  - Fill factor of 88% for the mirror surface



14x14mm

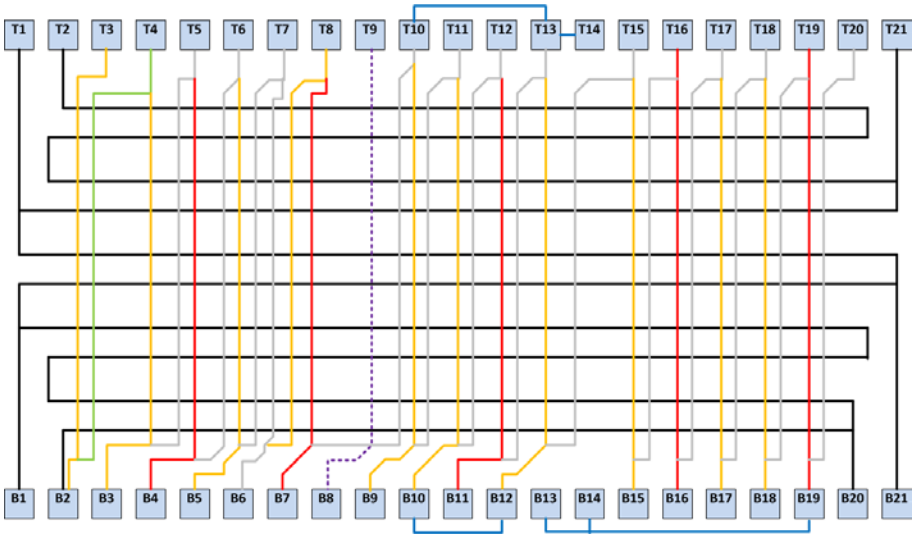
Concept – MMA architecture

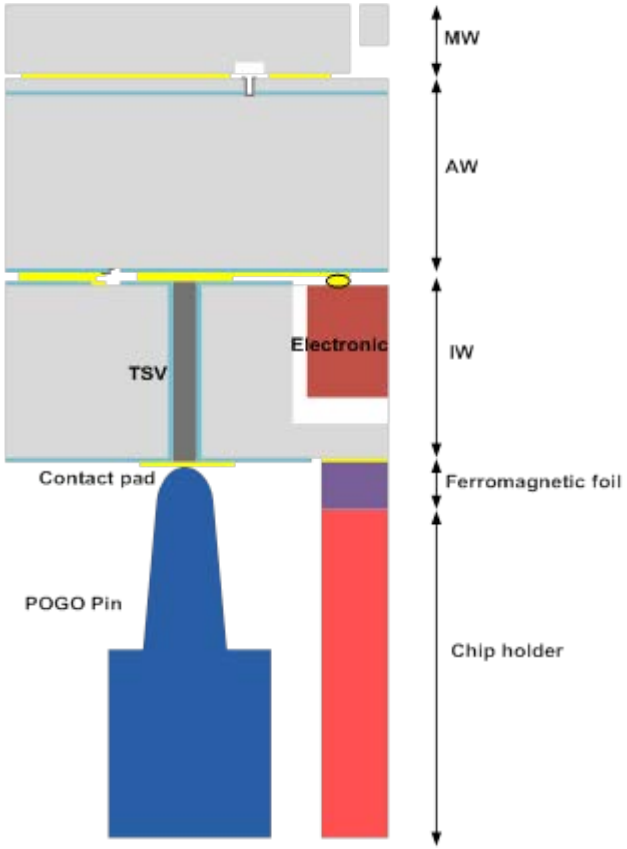


- 1: Electrical contact pads
- 2: TSV
- 3: Mirror
- 4: Suspension
- 5: Moving/Central electrode
- 6: Electronics
- 7: Capping
- 8: Ferromagnetic foil
- MW: mirror wafer
- AW: Actuator wafer
- IW: Interconnect wafer

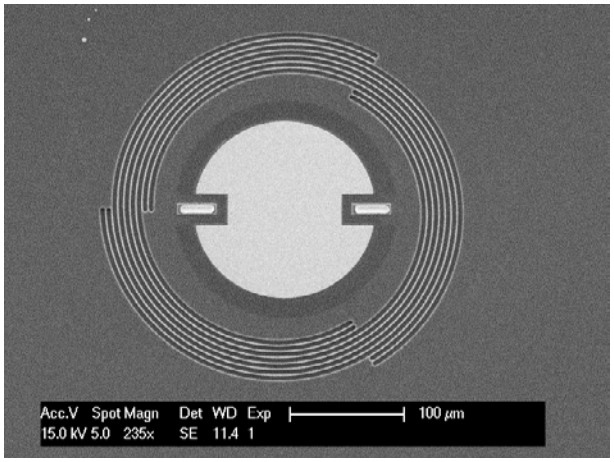
Concept - Interconnections

- Electrical chains to test interconnections
  - 1475 bumps
  - 42 TSVs
  - 31 vertical lines
  - 10 horizontal lines

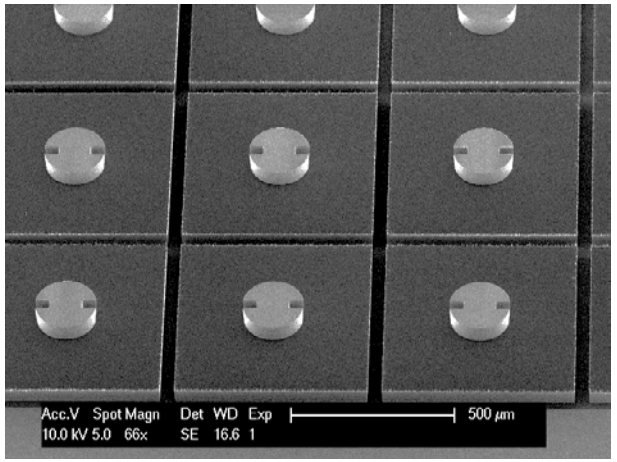




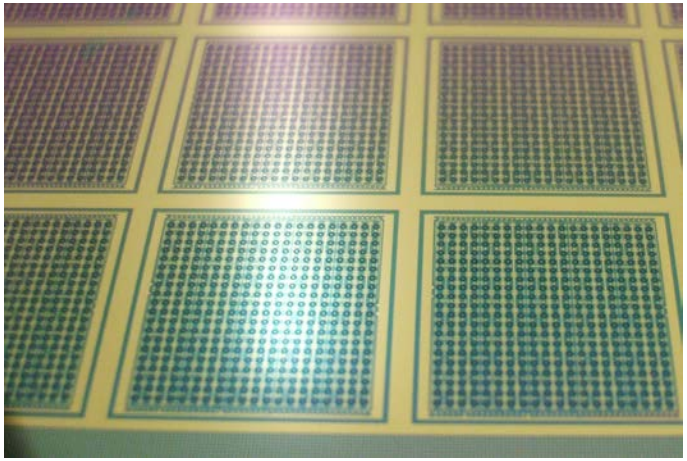
Fabrication “screen shots”



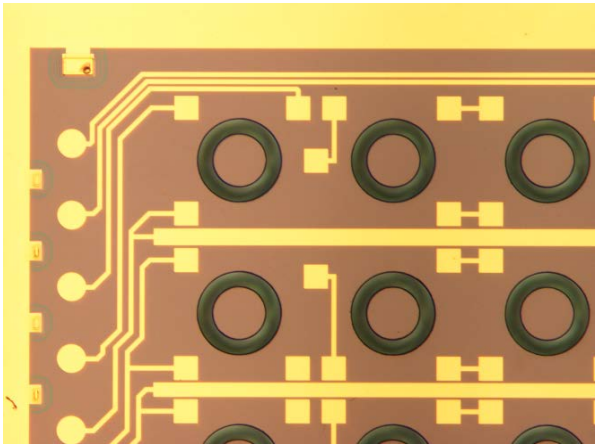
Suspension and bonding pad



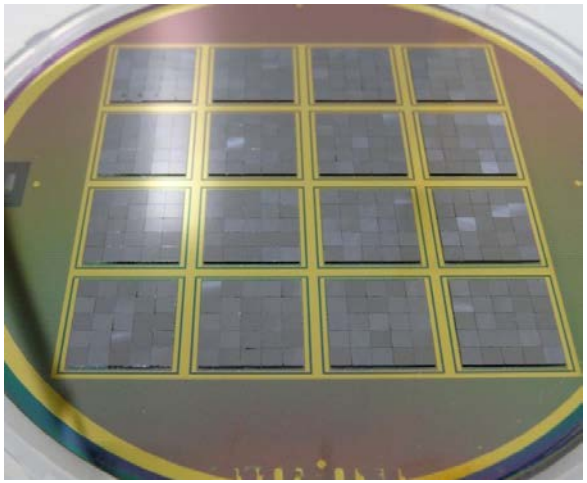
Mirror from backside



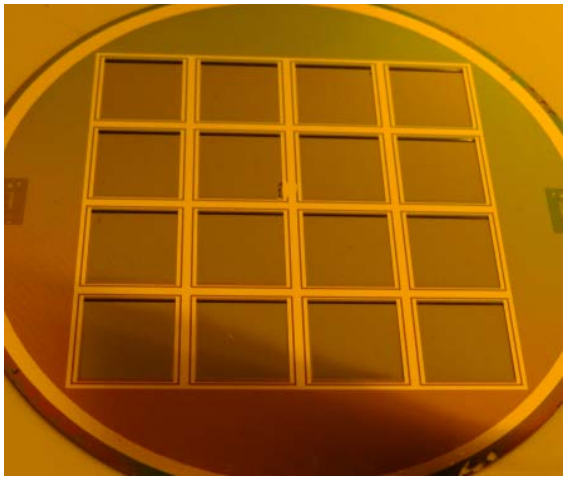
Electrodes side



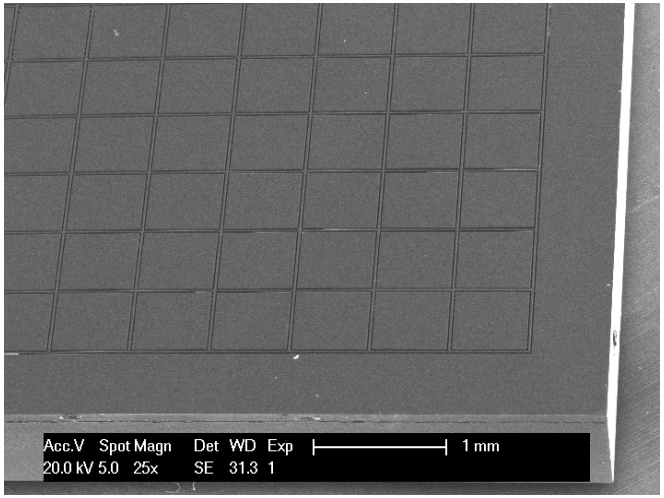
Fabrication «screen shots»



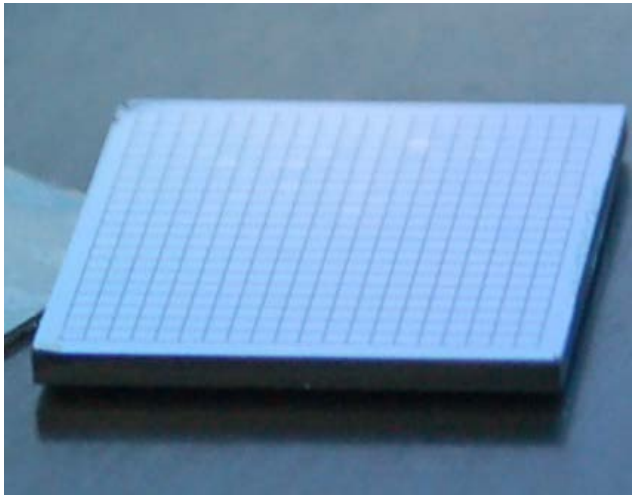
Electronics side



Cavity and interconnects wafer



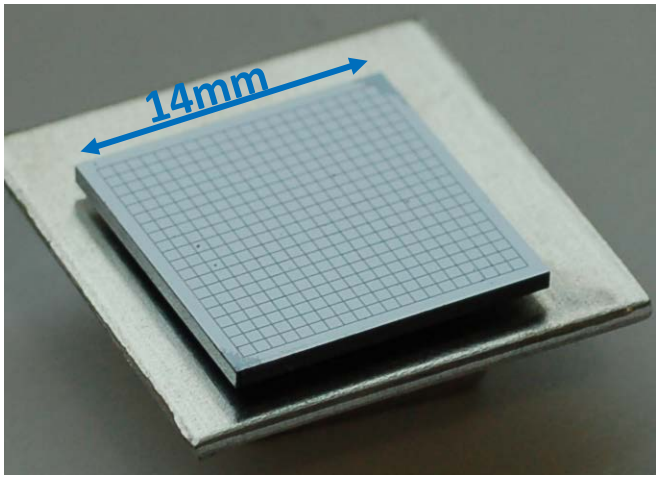
Mirror surface

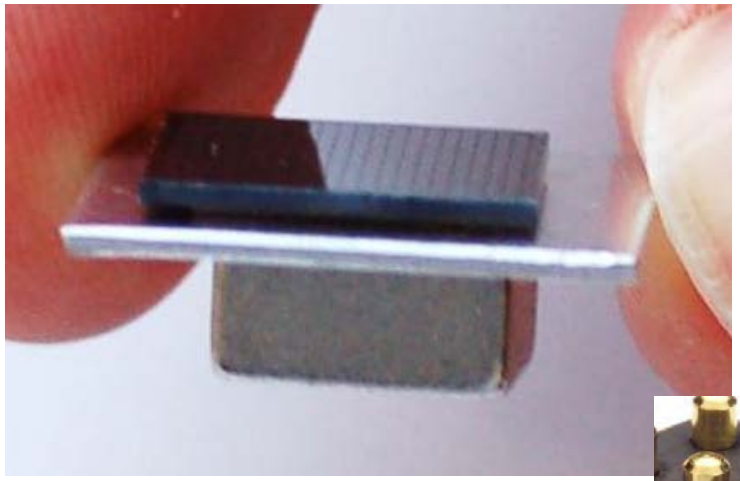


Mirror chip

Results – Magnetic clamping

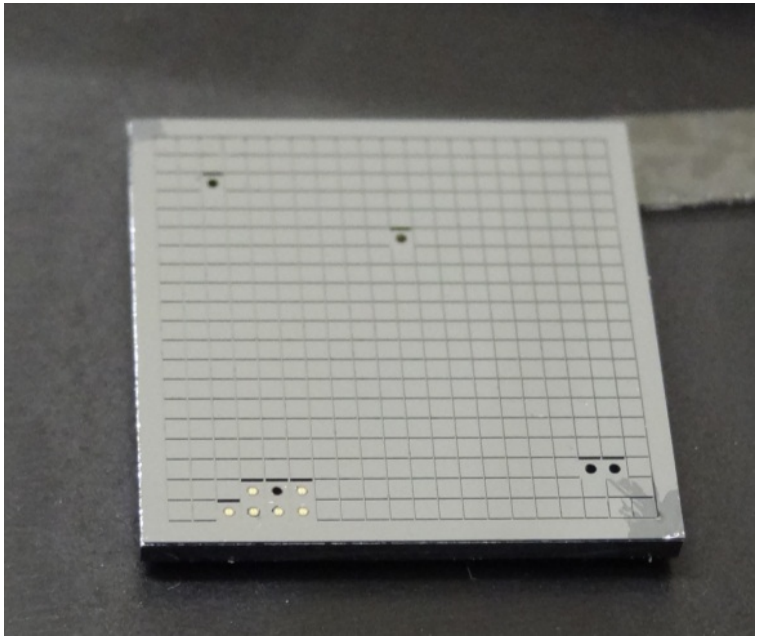
- Magnetic clamping with a 1mm Al foil in-between

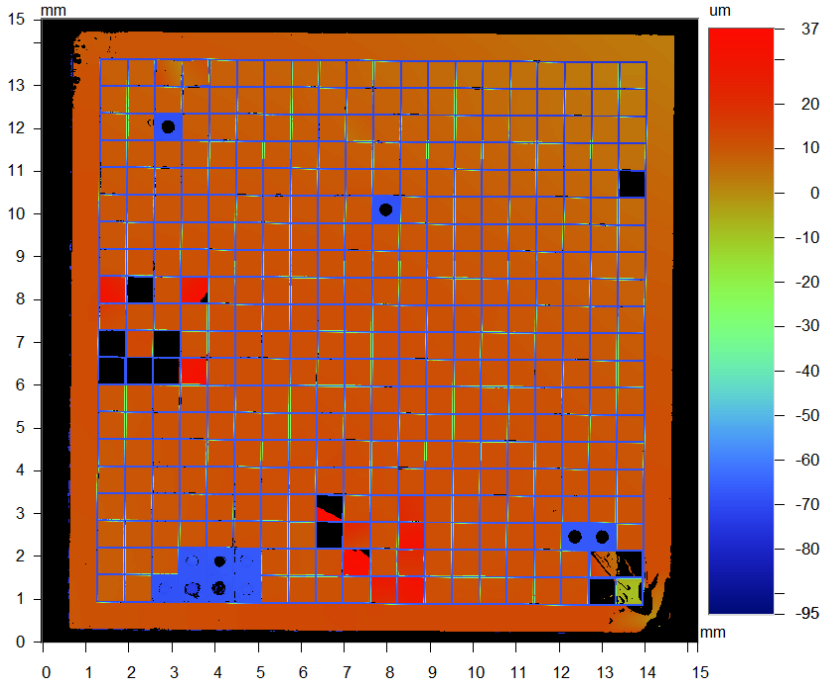




Thickness/ magnet config.	Experiment	Fine mesh Simulations	Error percentage
1000 µm / 10X10 mm²	9.4 N	9.3 N	1%
1000 µm / 20X20 mm²	31.9 N	29.3 N	8%

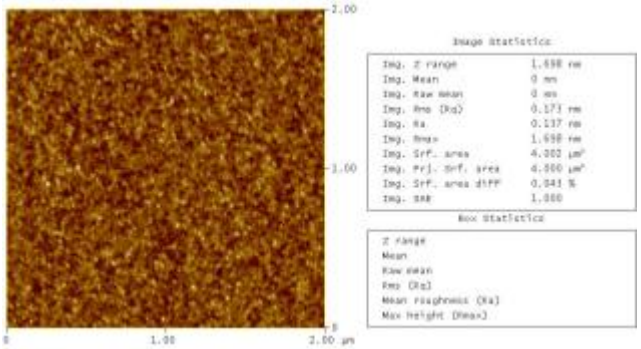
Results - Pretilt



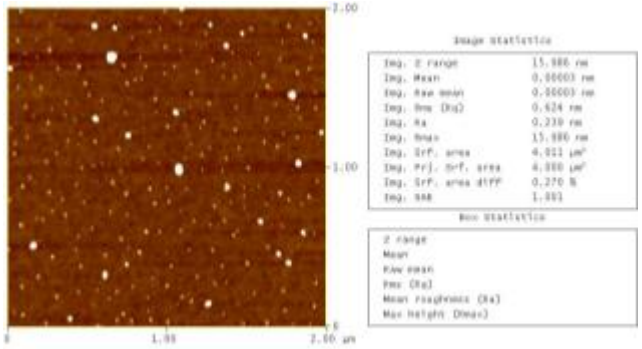


0.06° of average pretilt

Results – Surface roughness

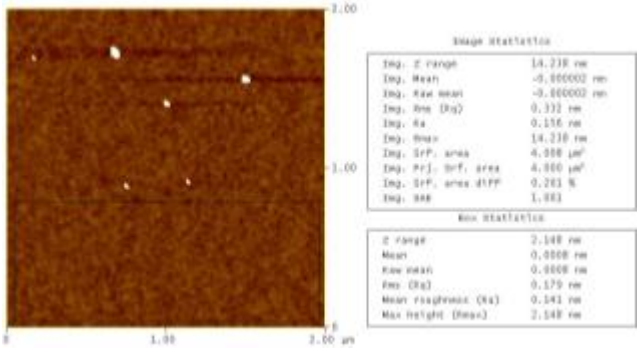


Samples a - HF vapor
0.17nm RMS

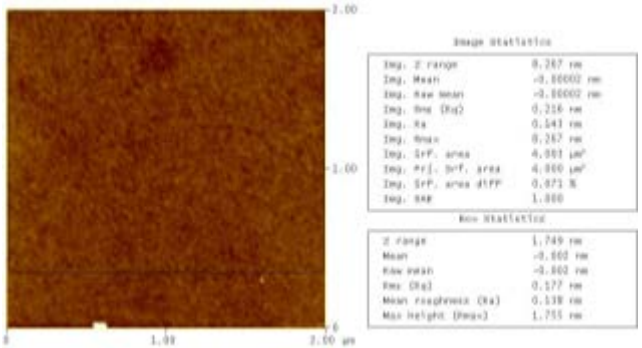


Samples b – HF vapor
0.6nm RMS

After release
Roughness <1nm



Samples c after thermal treatment
Roughness decrease from 15 to 50%



Samples d – Liquid release
0.17nm RMS

After treatment
Roughness <0.5nm

Results – Electrical measurements

- Chains measured at different process steps
  - After electronics assembly
  - After triple stack assembly
  - After dicing
  - After release

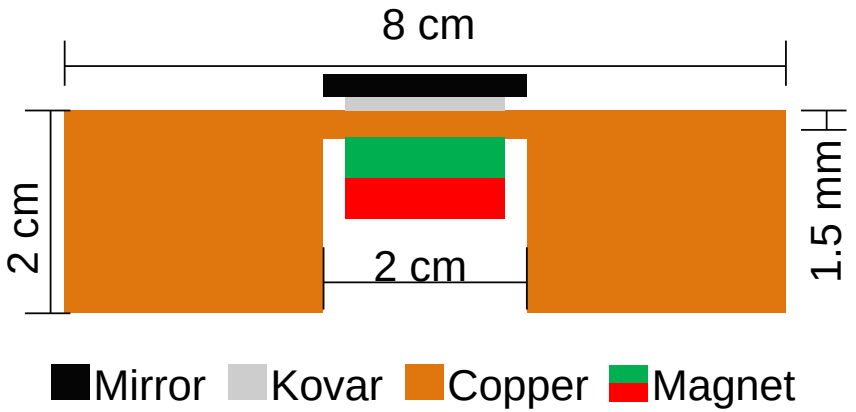
No effects from the process on measured resistance

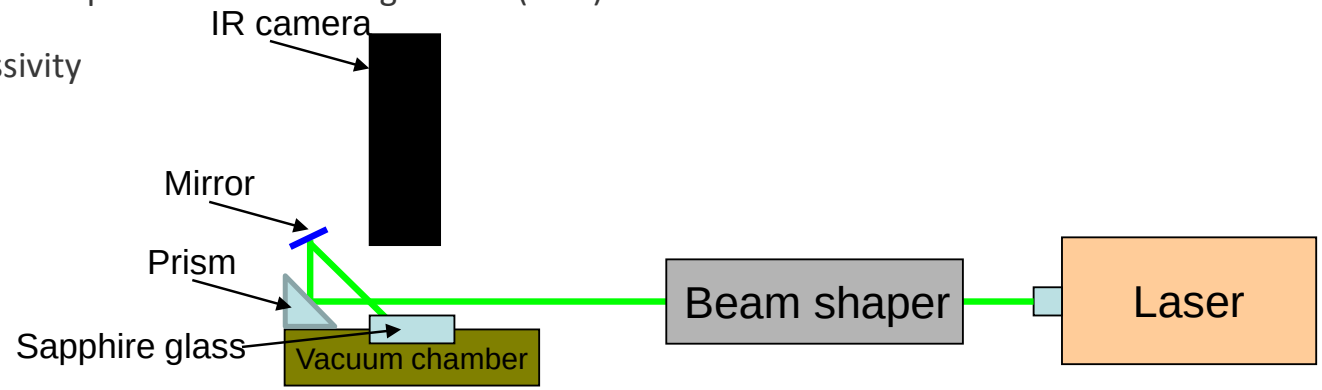
1475 bumps
42 TSVs
31 vertical lines
10 horizontal lines

- No defects on TSV or wafer to wafer contacts
- Defects on the ASIC/AW interface but less than 0.2%
- Full chains measured
- Total resistance from pin to electronics lower than 100Ω but more investigation will be required for a better understanding (min value 15Ω, max value of 150 Ω)

Results - Thermal measurements

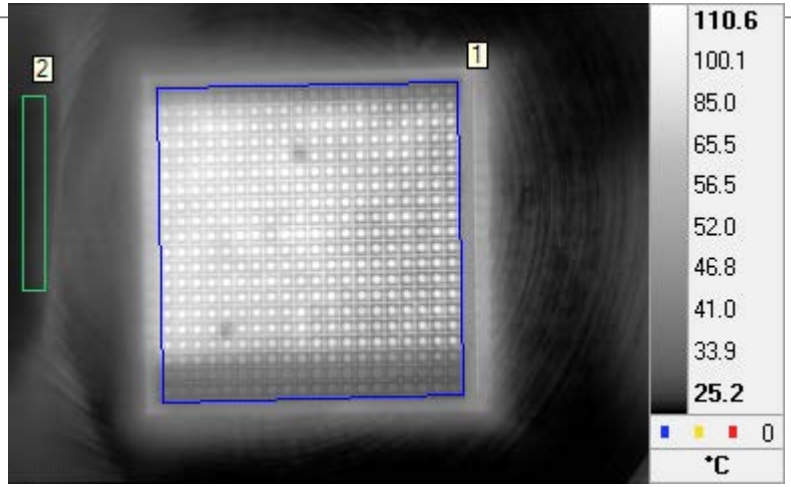
- Setup
  - Cedip Jade III MW" Infra-Red (IR) camera
  - 2W 532nm green laser
  - Beam shaper with 1 cm^2 square profile with a focal point of 70 cm
  - Mounting on 1mm thick Cu and magnetic clamping
- Calibration
  - Transmitted laser power for the configuration (40%)
  - Sample emissivity

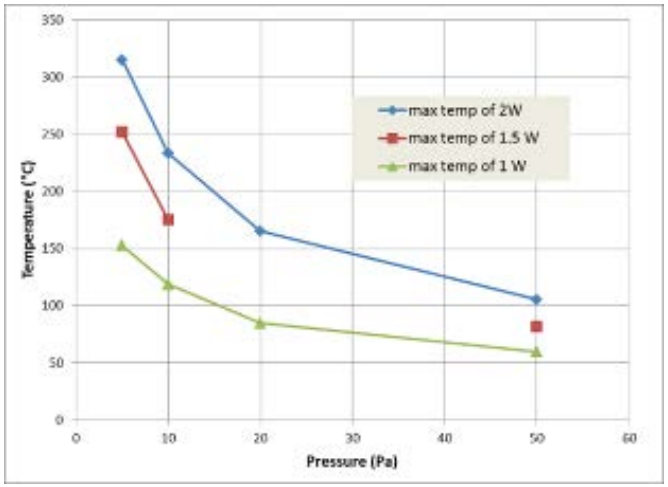


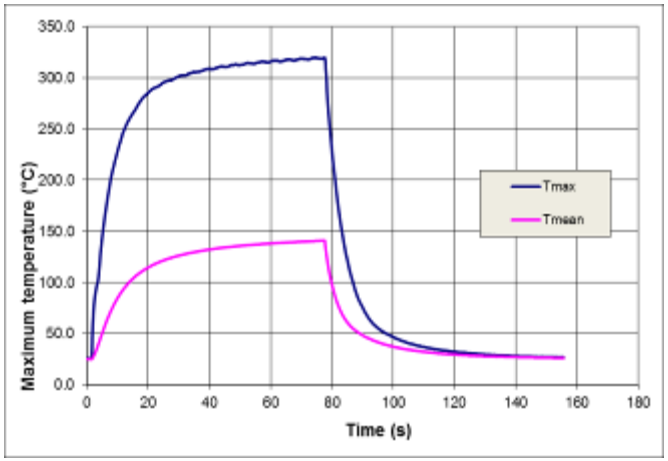


Results - Thermal measurements

- Results
  - 105°C at 50Pa with 6.1kW/m^2
  - Stress test at 1 Pa → 400°C
  - Time constant extracted
  - Temperature higher at MMA center than at the edge

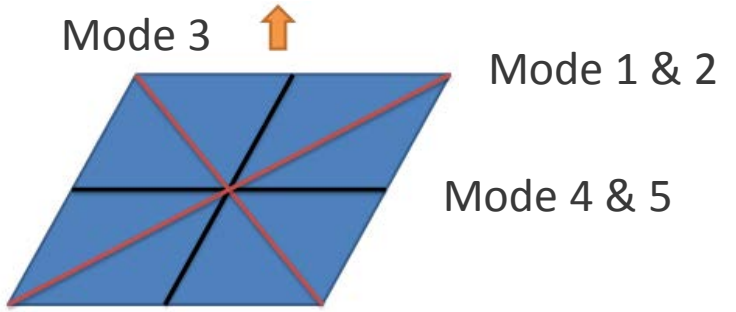


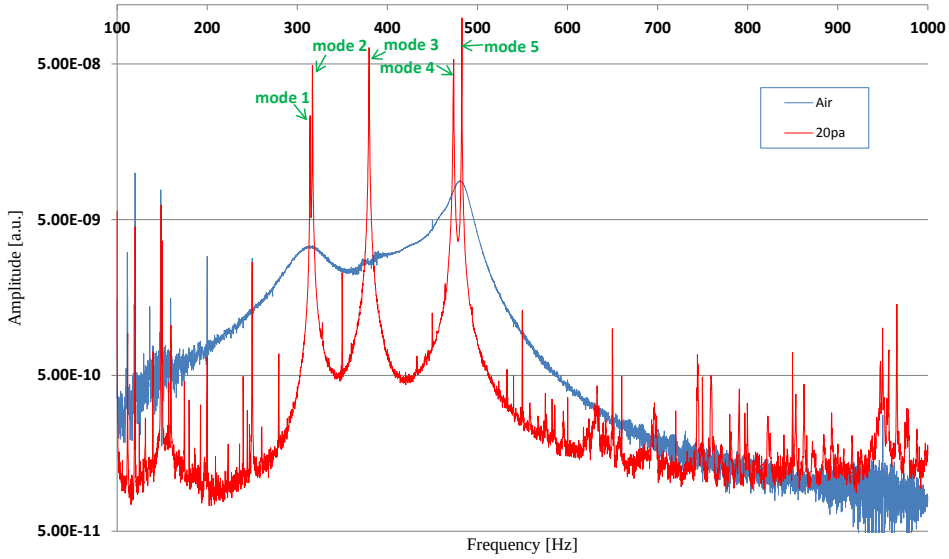


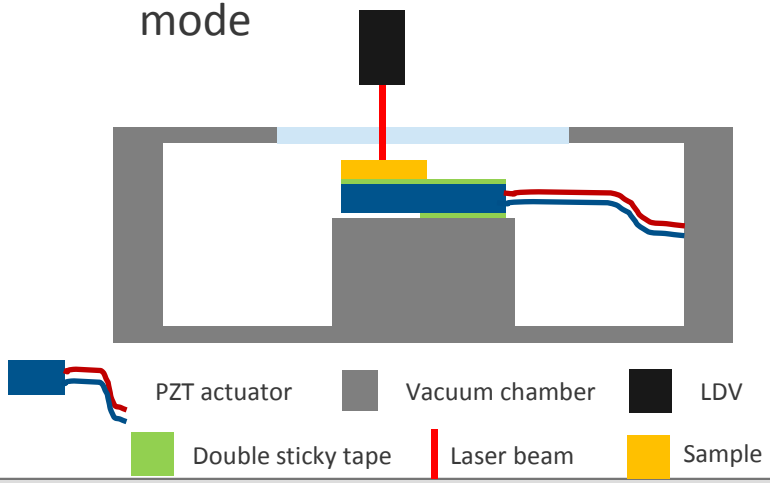


Results – Mechanical performance

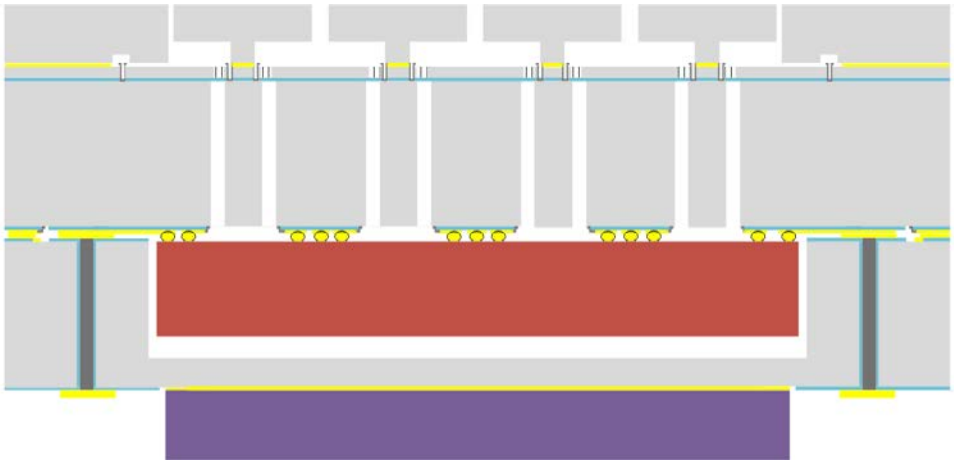
- Laser doppler vibrometer
- PZT external excitation
- Frequency response for different pressure
- 5 peaks detected under vacuum
- Q factor of 300 at 20Pa for the 3rd mode







Flexibility



- Mirror part
  - Continuous surface
  - Shape
  - Size
  - Coating (from UV to IR)
- Actuation part
  - Electrodes shape (flat, comb drive)
  - Flexible membrane
- Packaging
  - With or without ASIC
  - Clamping technology

Summary

- Novel wafer level fabrication process and packaging for large Micro Mirror array.
- High fill factor thanks to the high vertical integration level.
- “Infinite surface” by adding chip side to side.
- High optical power load compatible.
- High temperature compatible.
- Achievable tilt above 4° mechanically in 2D.
- Low surface roughness.
- High flexibility in optical coating (last process step).
- Integrated electronics.

Questions?