optocap

9th ESA MNT Roundtable
System-in-Package of MEMS and Electronic Components

Stephen Duffy

Agenda

- Background
- Objectives
- Project details
- General packaging background
- MEMS SiP Overview
- Design and Process considerations

Background

- Microelectronic mechanical systems (MEMS) small size and low power consumption represent attractive advantages for the use of MEMS device in satellites and space crafts.
- Packaging technology is a key element for the development of the MEMS concept into a MEMS device product capable to be fabricated and commercialized.
- Even though MEMS devices are now widespread in day-to-day high-tech devices such as smartphones and cars, demonstrations of its reliability in space applications requires further developments.

Objectives

- The objective of this activity is to demonstrate a packaging solutions for the 3D packaging of MEMS devices. MEMS devices and the respective ASIC controllers are packaged in both stack and side-by-side configurations.
- The System-in-Package (SIP) demonstrator will be fabricated during this activity and will be submitted to a test phase to assess the viability of the packaging options that are to be employed.
- In this presentation the design and assembly processes considerations of the SiP demonstrator are presented.

Project Details

- ESA funded project to design and build a MEMS based System in Package demonstrator and assess the maturity of the available technologies and potential applicability to space systems.

- The project consists of the following companies;
  - Optocap Ltd – responsible for the package design and assembly of the MEMS SiP demonstrator modules.
  - ESS (formerly Theon) – responsible for the ASIC and MEMS devices
  - Lusospace – responsible for the testing and qualification

The purpose of micro-electronic packaging

- Environmental Protection
  - Mechanical protection
  - Isolation from moisture, oxygen etc. as required
  - Protection from unwanted electrical (EMC) or optical influences

- Electrical Connectivity
  - Allows small device to interface to next level
  - Provides power connection for device operation

- Thermal
  - Provides optimised thermal pathway

Specific challenges with MEMS Packaging

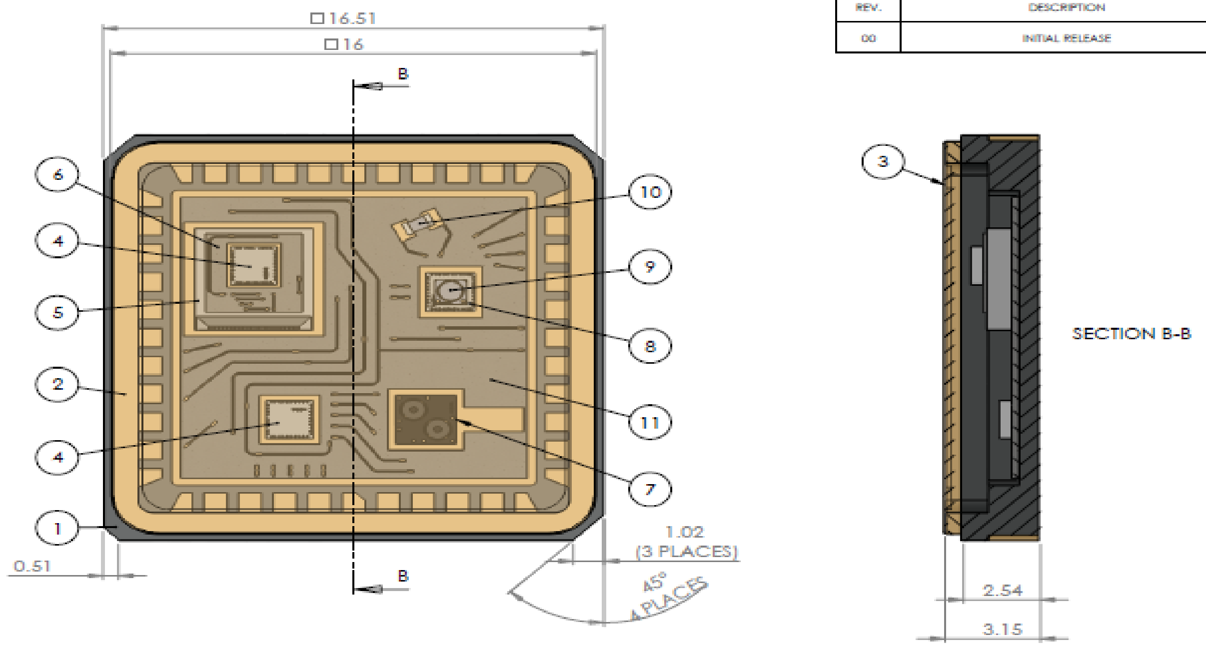
- No surface contact in “active” area – special handling techniques
- Some MEMS devices require hermetic or vacuum packaging
- Some MEMS devices must have the active area in contact with the environment which may limit reliability of other components
- Package must often be specifically designed for the device so no common standards
- Effects of moisture/gas ingress
- Integration of windows
- Outgassing from packaging material/plating
- MEMS may require isolation from adhesives, solvents etc. used in standard packaging processes
- Impact of stress can impact MEMS device operation

Benefits of System in Package(SiP)

- Provision of full system functionality in small form factor
- Allows integration of dissimilar chip technologies e.g. CMOS logic on Si with III/V RF components
- Can accommodate optical and MEMS devices with required peripheral components
- Can include vertical interconnection, “die stacking”
- External package is typically custom and may be hermetic

MEMS SiP Demonstrator Overview

REV.	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	29/04/2014	1985



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	IRK44F2-5489C	44 Pin Ceramic Package	1
2	IRK44F2-5489C	Package Lid Seal Ring	1
3	DRG-001-1136-00	Package Lid	1
4	TH111A	ASIC	2
5	THXLM011	MEMS Accelerometer	1
6	DRG-001-1134-00	Interposer	1
7	141-364	MEMS Pressure Sensor	1
8	TH112	ASIC	1
9	Pressure Sensor 2	MEMS Pressure Sensor	1
10	Capacitor	Capacitor	1
11	DRG-001-1134-00	Tracked Substrate	1

DIMENSIONS ARE IN MM
TOLERANCES:
ANGULAR ±1 DEG
ONE DECIMAL PLACE ±0.1
TWO DECIMAL PLACES ±0.05
THREE DECIMAL PLACES ±0.005
UNLESS OTHERWISE STATED

PROPRIETARY & CONFIDENTIAL

THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF OPTOCAP Ltd. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT WRITTEN PERMISSION FROM OPTOCAP Ltd IS PROHIBITED.

APPROVALS	NAME	SIGNATURE	DATE
AUTHOR	S.ROBERTSON		
Q.A MANAGER	J.BORLAND		
ENGINEERING MANAGER	B.ASHBY		
OPERATIONS	G.WHYTE		

MATERIAL	DRAWING NUMBER	REV	DRAWING NAME	
N/A	ASY-001-117	00	LUSOSPACE SIP DEMONSTRATOR ASSEMBLY	
FINISH	**3D MODEL NUMBER**	**REV**	**SHEET**	**SIZE**
N/A	ASY-001-117	00	1 OF 1	A3

Module Overview

- Purpose is to provide 3 different die attach approaches.
  - One die set with the MEMS and associated ASIC mounted on the same plane,
  - One die set with the ASIC stacked on top of the associated MEMS with the use of an interposer between components
  - The additional die set would see the MEMS mounted directly on top of the associated ASIC with only a nonconductive epoxy between components.
  - The ASIC for the new die set requires a connection to an external capacitor so the location of the capacitor also needed consideration in the new layout proposal.

Main SiP components – Pressure Sensor

Table 4 – ESS's Pressure Sensor ESCP2-0002.0-ADRR functional parameters.

Parameter		Specifications	Interface
Range	[bar]	0.4-2	Capacitance [C] (amplitude)
Full Scale span capacitance	[pF]	2.67	
Non-Linearity	[%FS]	10.8 (Raw)	
Total Error (calibrated)	[%FS]	±0.08@25ºC	
Resolution	[µbar]	15	
Repeatability	[%]	<0.05	
Die dimensions	[mm^3]	2 × 2 × 0.4	

Table 5 – ESS's Pressure Sensor ESCP3-0002.0-ADRR functional parameters.

Parameter		Specifications	Interface
Range	[bar]	0.5 - 4	Capacitance [C] (amplitude)
Base Capacitance	[pF]	15.5	
Full Scale span capacitance	[pF]	1	
Die dimensions	[mm]	1 × 1.1 × 0.4	

Main SiP components – Accelerometer

Table 6 – ESS's Accelerometer functional parameters for the XLM10/11.

Parameter		Specifications	Interface
Range	[g]	10	Capacitance [C] (amplitude)
Scale Factor	[fF/g]	3	
Non-Linearity	[%FS]	0.4	
Brownian-Noise	[µg/Hz$^{0.5}$]	32	
Resonance	[KHz]	3.1	
Cross Axis sensitivity	[%]	2	
Die dimensions	[mm^3]	4.2 × 3.9 × 0.8	

Main SiP components – ASIC

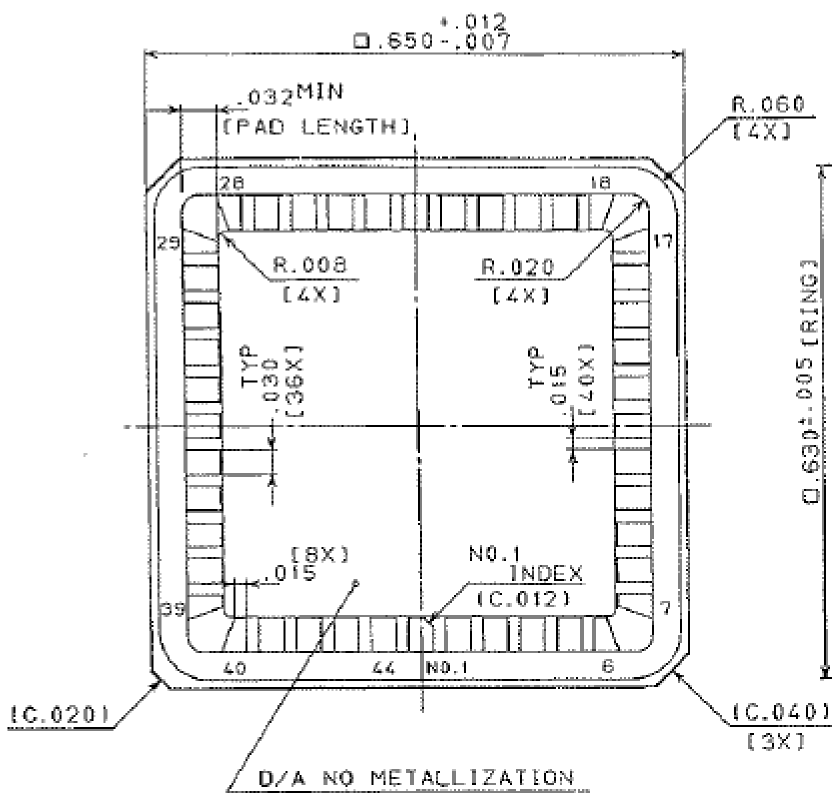
The ASIC performs the signal conditioning of the measurement readouts from each MEMS sensor. One ASIC per sensor is required. The specification of ESS's signal condition is presented in Table 7.

Table 7 – ESS's signal conditioning TH111 and ESS112 specs.

<table>
<tr><th colspan="2">Parameter</th><th>Specifications TH111</th><th>Specifications ESS112</th><th>Interface</th></tr>
<tr><td colspan="2">Temperature sensor readout</td><td>32-bit</td><td>32-bit</td><td rowspan="2">Differential and Single-ended Analogue</td></tr>
<tr><td>Resolution</td><td>[ENOB]</td><td>Up to 15.4</td><td>19</td></tr>
<tr><td>Internal Oscillator</td><td>[Hz]</td><td>TBD</td><td>TBD</td><td rowspan="3">SPI</td></tr>
<tr><td>Operating Temperature</td><td>[ºC]</td><td>-40 to 85</td><td>-40 to 85</td></tr>
<tr><td>Power supply</td><td>[V]</td><td>3.3</td><td>3.3</td></tr>
<tr><td>Die dimensions</td><td>[mm^3]</td><td>1.56 × 1.56 × 0.4</td><td>1.56 × 1.64 × 0.4</td><td rowspan="2">10-bit PWM</td></tr>
<tr><td colspan="4">Offset cancelation proficiency</td></tr>
</table>

Main SiP components – Package

- The 44 Pin LCC (Lead Chip Carrier) package was selected to simplify package assembly on automated equipment.
- It was also selected for the cavity depth it provided. The total stack height of the devices significantly reduced the number of “off the shelf” package options available.
- The package selected provides ~700 µm clearance between the top surface of the Accelerometer ASIC and the bottom surface of the package lid. The wire bond loops will be in the region of 250 µm in height (lower if reverse bonding is used) so there should be no risk of the wires shorting to the package lid.
- Package also has a kovar ring frame to enable hermetic sealing.



Draft Assembly Process

Step	Process	Equipment	Materials	Comments
1	Incoming inspection	Stereo microscope (10-40x magnification)	All components	Tested to mil-std 883 (latest revision) or ESA/SCC Basic Specification No. 20400: Internal Visual Inspection (as req'd)
2	Package bake		Ceramic package	16 h @ 200°C Vacuum <100 mTorr
3	Die attach	Palomar 3500 auto die bonder.	Package, Substrate, Interposer, MEMS ×3, ASIC ×3 Epoxy (TBD)	Capable of +/-35 µm placement accuracy. Pick & place force control down to 1 g.
4	Visual inspection	Stereo microscope (10-40× magnification & 200× if required)	Package assembly	Tested to mil-std 883 (latest revision) or ESA/SCC Basic Specification No. 20400: Internal Visual Inspection (as req'd)
5	Die attach cure	Convection oven	Package assembly	Cure schedule depends on epoxy selection.
6	Wire bond	Palomar CBT8000 auto wire bonder	Package assembly, 25 µm Au wire	
7	Wire bond inspection	Stereo microscope (10-40× magnification & 200× if required)	Package assembly	Inspected to mil-std 883 (latest revision)
8	Moisture bake	SSEC	Package assembly, Lid	16 h @ 80°C
9	Seam seal	SSEC	Package assembly, Lid	Sealed with He10%:N2 environment. Gas pressure can be varied to suit application.
10	Fine leak test	Adixen ASM	Lidded package assembly	Tested to mil-std 883 (latest revision)
11	Gross leak test	Atrium 6000 bubble tank	Lidded package assembly	Tested to mil-std 883 (latest revision)
12	Final Inspection	Stereo microscope (10-40× magnification)	Package assembly	Tested to mil-std 883 (latest revision) or ESA/SCC Basic Specification No. 20400: Internal Visual Inspection (as req'd)

Design and Process Considerations

- Multichip architectures comprise a myriad of factors that need further deep analysis.
- Merging distinct devices in a system presents challenges that impact the area overhead, power consumption and loss of performance, which ultimately reflects on the measurement integrity.
- The following slides review the key performance and reliability considerations for wire bond design layout, die attach, sealing and thermal management.

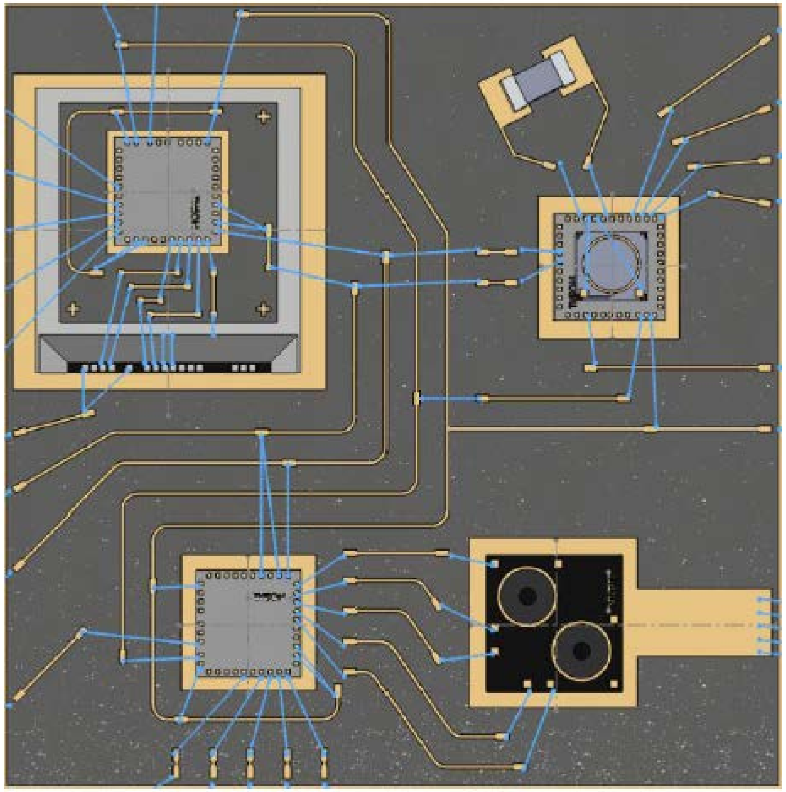
Design and process considerations – wire bonding

- **Wire Bonding**
- The wire interconnect layout is critical and needs to address a couple of key points.
  - Consideration has to be given to the crosstalk phenomenon.
  - The proposed MEMS and ASIC device shave a pad configuration which suits when the components are mounted on the same horizontal plane. Mounting on the same horizontal plane would enable direct bonding between the two components without wire interconnects crossing over. Stacking the components or mounting in the vertical plane introduces wire layout complications in particular for the pressure sensor.
  - The wire bond interconnects need to meet certain DFM (Design for Manufacture) guidelines to ensure it is suitable for manufacture. These guidelines include wire length, loop height and wire angle (from perpendicular).
  - To address these concerns several layout proposals have been reviewed to ensure the optimum die and wire interconnect layout was achieved.

Design and process considerations – wire bonding

- To improve the wire bond interconnect layout while maintaining the approach of stacking the Accelerometer MEMS and its associated ASIC, a ceramic interposer was introduced.

- This approach eliminates the crossing wire bond interconnects while minimises the length and simplifying the loop formation.



Design and process considerations – signal cross-talk and distortion

- The sources of crosstalk occur due to proximity of the active structures of both dies, this takes place from the MEMS sensor electrodes to the CMOS module, hence the interconnection plays a significant role in signal integrity. The interconnects parasitic effects result in a propagation delay alongside a crosstalk-induced delay and noise.

- Non-ideal interconnects are still an issue to account for, meaning that countermeasures against crosstalk must be developed on design level and in form of technology optimization.

- The next step for this layout was to mitigate the risk of electrical crosstalk. To do this the track and gap ratio on the tracked ceramic substrate and interposer had to be increased . The track and gap ratio was set at 50 μm track: 400 μm gap. This maximised gap to reduce parasitic capacitance.

- Where possible common contacts were created between the 3 ASIC's to minimise the number of tracks.

- The use of 90degree corners in the track layout was avoided to prevent signal distortion.

Design and process considerations – Die Attach

- Consideration has to be given to the subsequent processes and in particular to wire bond. The proximity of the interposer pads to the ASIC must be such that the wire bond tool can access the interposer bond pads without colliding with the ASIC. The design of the interposer and tracked submount allows for relaxed tolerance on the placement accuracy of the die to within +/-100 μm

- Selecting the correct die attach epoxy is crucial. A thixotropic low modulus epoxy is required to ensure minimum flow after dispense and to minimise stress once cured. There are various options available for selection which will address specific requirements. For this package where mechanical stress is expected to play a role in the device performance a low stress material can be selected.

Hermetic sealing – Part 1

- A hermetic enclosure is required to provide isolation of the MEMS and ASIC from external environmental influences.
- The hermeticity of the package is subject of different failure sources, such as stress, seal robustness and moisture permeation. Moisture penetration would not affect the MEMS devices themselves but might change the value of the parasitic capacitance of the tracks and wire bonds. This effect is crucial in the case of capacitive devices such as the accelerometer and pressure sensors used in this activity.

Hermetic sealing – Part 2

- The hermetic sealing technique to be used for the SiP demonstrator package will be the parallel seam seal method.
- A Kovar ring which has been brazed onto the ceramic package by the package manufacturer is used as a sealing surface.
- A Kovar lid will be seam sealed onto the ceramic package. A known positive pressure will be sealed into the package which combined with the MEMS Pressure Sensor, will be used to determine leak rate from the sealed package.
- The challenge will be to ensure the leak rate can be detected by the MEMS Pressure Sensor over a reasonable time frame.

Hermetic sealing – Part 3

- Sealing a vacuum inside the package cavity is an option but this would limit testing of the package hermeticity.
- Fine leak checking requires the presence of a tracer gas within the package cavity (typically 10% He in N2). The fine leak test detects the gas using mass spectroscopy and calculates the leak rate.
- The sealing is performed in a pressurised chamber and is typically set to 1.5 atm but can be varied slightly if required. For the SiP demonstrator a pressure of 1.5 atm will be targeted.

Thermal and Stress management

- There is limited thermal and mechanical data on the MEMS and ASIC device. As a result an accurate and meaningful finite element analysis (FEA) cannot be performed.
- It is certain that mechanical stress will have an impact on the MEMS device but there is currently no specification or limit to target when designing and analysing the package assembly.
- Performing the FEA would provide data but the data would not be useful until a performance threshold can be found.
- The performance threshold is the point at which the MEMS device no longer provides useful information due to heat or stress. The same is true for the thermal analysis. The thermal simulation will indicate the temperature during operation but this data would not be useful until a performance threshold can be found.
- To collect this data 6 de-risk package assemblies have been manufactured. Slide below shows the details of the de-risk samples.

De-Risk builds – Epoxy evaluation

- Both the adhesive shrinkage and thermal conductivity are relevant to the overall thermal signature of the SiP. To de-risk the epoxy selection 6 packages were assembled using 2 different epoxy options

- Epotek H70E-4 is a thixotropic material selected to reduce the risk of the epoxy flowing over the bonding surface into areas it is not wanted, specifically wire bond pads on the tracked ceramic and interposer which would prevent application of the wire bond interconnects.
- Ablebond 2030SC is a snap cure epoxy selected for its lower stress

Physical Property	Ablebond 2030SC	Epotek H70E-4
Glass Transition Temp (Tg)	80°C	80°C
Coefficient of Thermal Expansion (CTE) below Tg	31×10^{-6} in/in/°C	17×10^{-6} in/in/°C
Coefficient of Thermal Expansion (CTE) above Tg	158×10^{-6} in/in/°C	77×10^{-6} in/in/°C
Thermal Conductivity	2.3 W/mK	0.57 W/mK
Dielectric Constant (1 kHz)	n/a	4.81
Weight Loss @ 200°C	0.48%	0.57%

De-risk builds - Package material evaluation

- The package materials have been selected with consideration to the heat generated by the MEMS devices and associated ASICs as well as the mechanical stress introduced.

- The heat generated by the MEMS and ASIC is considered negligible with drive current for the devices being in the 10’s of mA range.

- Mechanical stress is considered as a parameter which could have an impact on the device performance. The Accelerometer in particular could be affected by mechanical stress in the assembled package. With this in mind the materials were selected to mitigate the risk of device performance issues related to thermo-mechanical stress in the package assembly.

- The package itself has a lower thermal conductivity than the other materials but it has been selected as an industry standard package material which has a CTE closely match to that of silicon.

- The 6 de-risk package assemblies have been assembled using an Alumina package to provide test data on the device performance over a temperature range while mounted to this material. Refer to the de-risk section of this document for more information on the de-risk activity.

Thermal and CTE properties of components

Component	Material	CTE (10^{-6}/K)	Thermal Conductivity (W/mK)
Accelerometer MEMS	Silicon (Si)	3	151
Pressure Sensor MEMS	Silicon (Si)	3	151
ASIC	Silicon (Si)	3	151
Interposer	Aluminium Nitride (AlN)	4.5	170
Tracked Submount	Aluminium Nitride (AlN)	4.5	170
Package	Alumina (Al_2O_3)	6.7	17

Conclusion

- The design guidelines and assembly process flows for a MEMS SIP package have been evaluated and defined.
- Further evaluation will be performed once the test vehicles have been assembled later in 2014.