WE LOOK AFTER THE EARTH BEAT

# 9th ESA MNT Round Table Development and Exploitation of a Miniaturised IMU Capability

imec optocap esa ESTEC

GarField MICROELECTRONICS matrics ltd

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THALES ALENIA SPACE CONFIDENTIAL

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# Topics



- Introduction and MinIMU Overview
  - Development Aims and Objectives
  - MinIMU Team
  - MinIMU Requirements
- Front End ASIC (FEA)
  - FEA Description and Development Approach
  - FEA Design Drivers and De-Risking Activities
- MinIMU Module Packaging
  - Module Packaging Description and Development Approach
  - Module Design Drivers and De-Risk Activities
- Applications and Exploitations
- Conclusions

# Introduction

- The MinIMU programme is utilising a range of European technologies and capabilities to demonstrate a component level Inertial Measurement Unit (IMU) for a range of space applications.
- The motivation for the programme is to offer to the space community the benefits of cost reduction and low mass/volume/power already demonstrated successfully within terrestrial applications.

The MinIMU team is:

| | |
|---|---|
| SEA | Project Lead, FEA digital design and prototype testing. |
| Optocap | Module design and manufacture |
| Garfield-Matrix | FEA Analogue Functions design |
| IMEC | FEA layout and manufacture. |
| ESA | Technical Support and TRP funding. |

# MinIMU Motivation

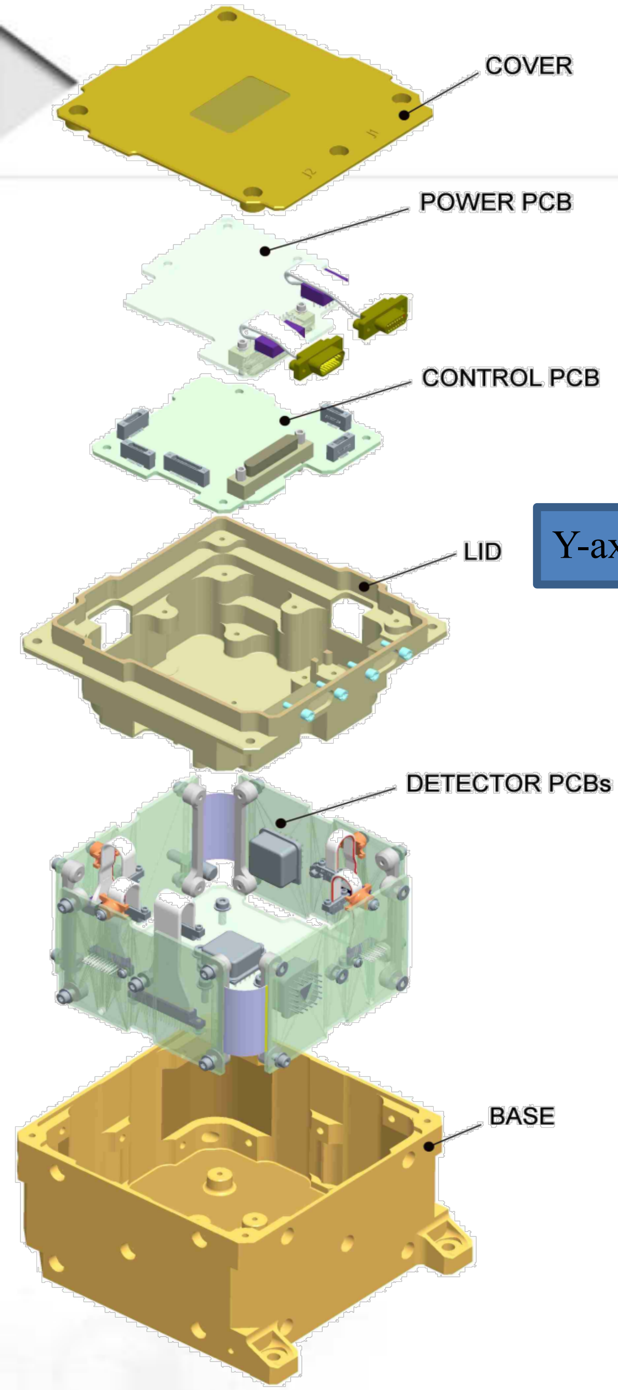


- A small, low power 3-axis gyro unit has already been developed for space based on MEMS detector technology..
  - The MEMS Rate Sensor (MRS)
  - SiREUS standard product (from SELEX-GALILEO) using MRS design and supplied to SENTINEL-3, MTG.....

- Unit mass/volume/cost dominated by:
  - Discrete electronic components (analogue).
  - Large packaging of space FPGA/ASIC components.
  - Unit assembly and test.

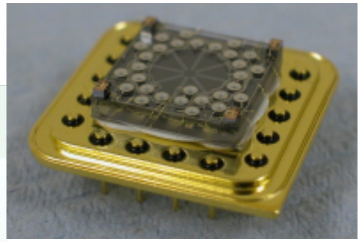
- Terrestrial/commercial sensors achieve significant recurring cost benefit,as well as mass/ volume reduction from mixed-signal ASIC technologies and integrated packaging.
  - But not directly compatible with the space domain/standards.

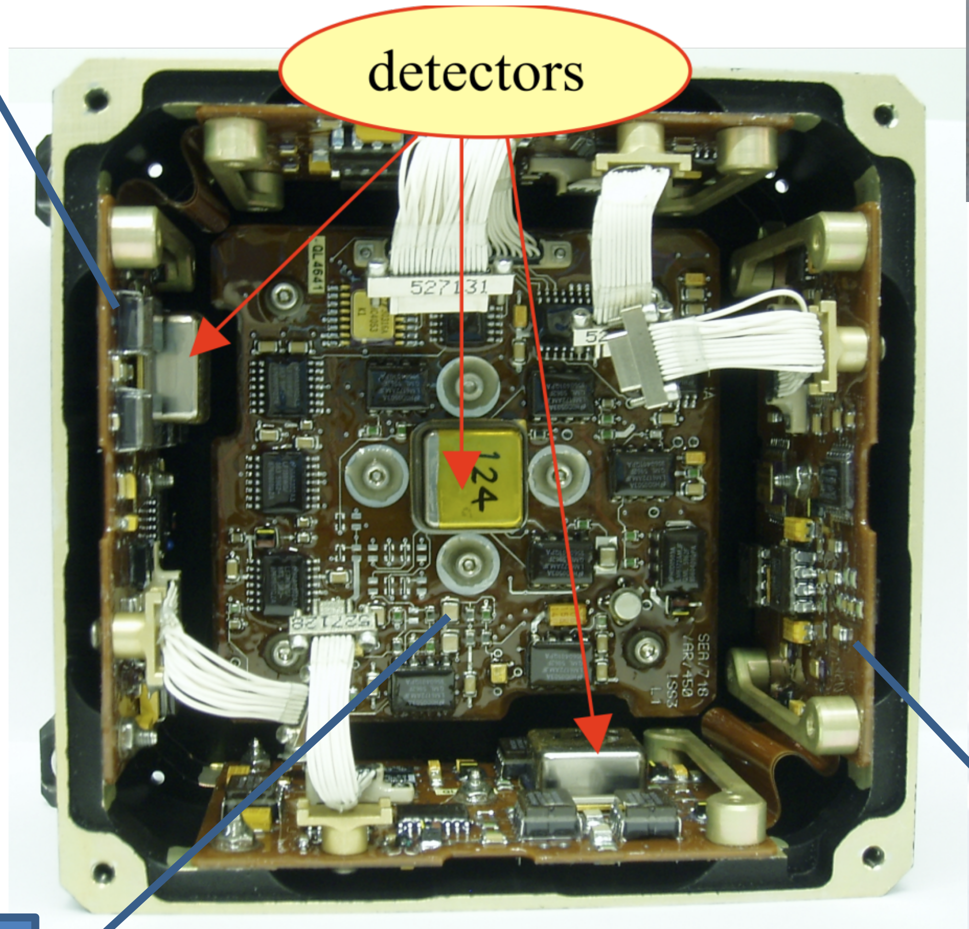
# MEMS Rate Sensor (MRS)

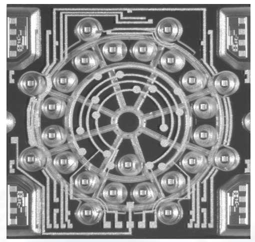



Key contributors to MEMS gyro unit mass/volume/cost are:

- Detector PCBs discrete electronics
- PSU PCB in discrete (ITAR free) form.

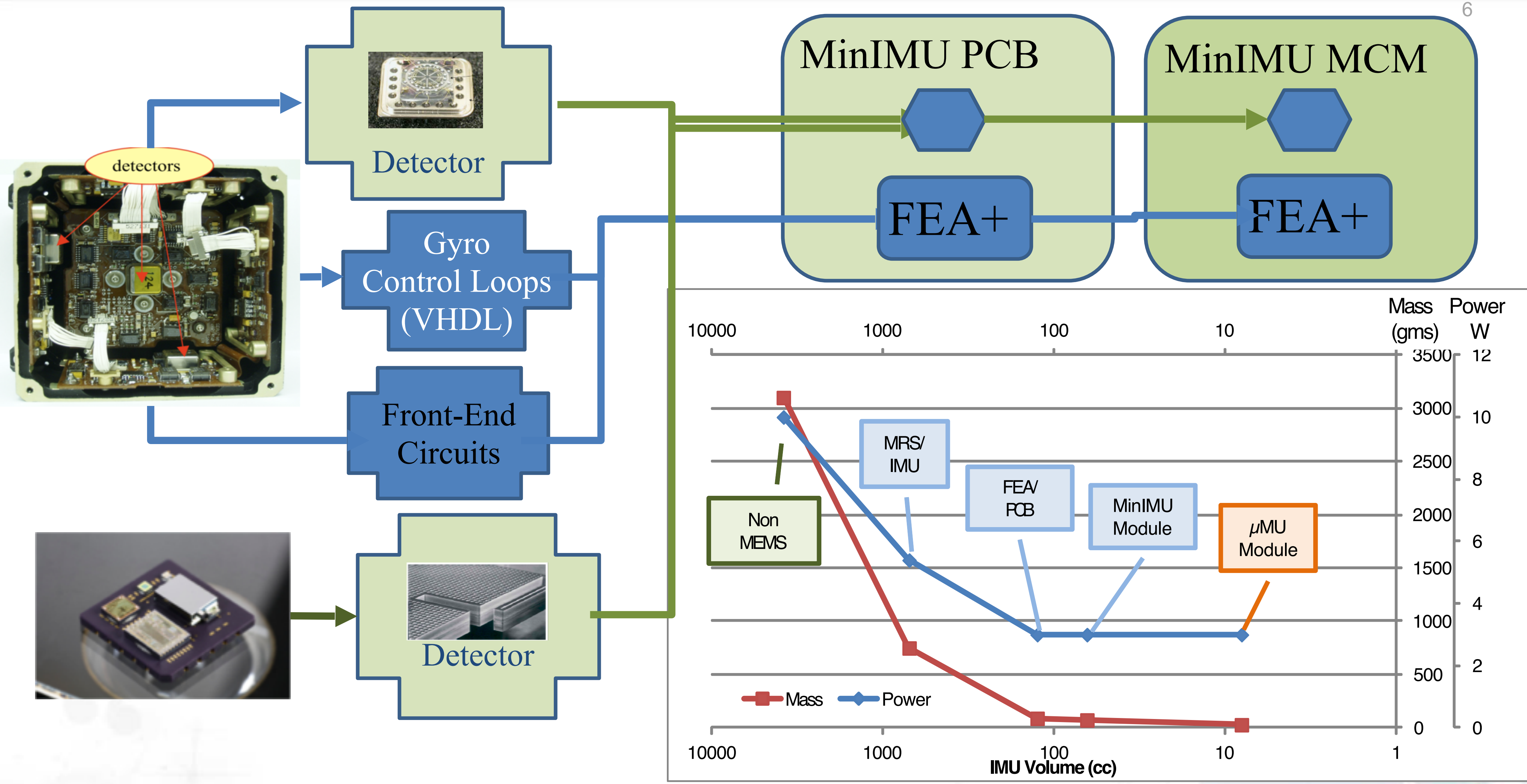




# MEMS IMU Technology Route Map





# MinIMU - The Enabling Technologies



- The MinIMU development is therefore predicated on two main enabling technologies:
  - Mixed Signal ASIC in a Radiation Hardened form capable of integrating all analogue, digital and power functions for a single IMU axis.:
    - High Voltage capability needed (>30V).
    - Non-volatile storage.
    - Single power rail, standard user interface, minimal external components
    - European.
  - Multi-chip Component Packaging
    - Accelerometer and gyro die in a single package
    - Availability of MEMS detectors in "die" form
    - Management of power dissipation from Front End ASIC
    - Packaging suitable for PCB mounting or mechanical structure mounting

- Performance similar to discrete version implementations:
  - Gyro: +/- 20 deg/sec, 10-20 deg/hr bias stability, 1000 ppm SF error,
  - Acc: +/- 20g, 45 ug bias stability, 1000 ppm SF error

- Cost target of < 25 Keuro/axis.

# Programme Schedule



- Programme initiated Feb 2013
- Requirements and Trade-Off Review May 2013
- PDR Nov 2013
- CDR August 2014
- FEA Prototype Manufacture Feb/Mar 2015
- MinIMU prototype manufacture - Sept 2015
- MinIMU prototype TRB - Feb 2016

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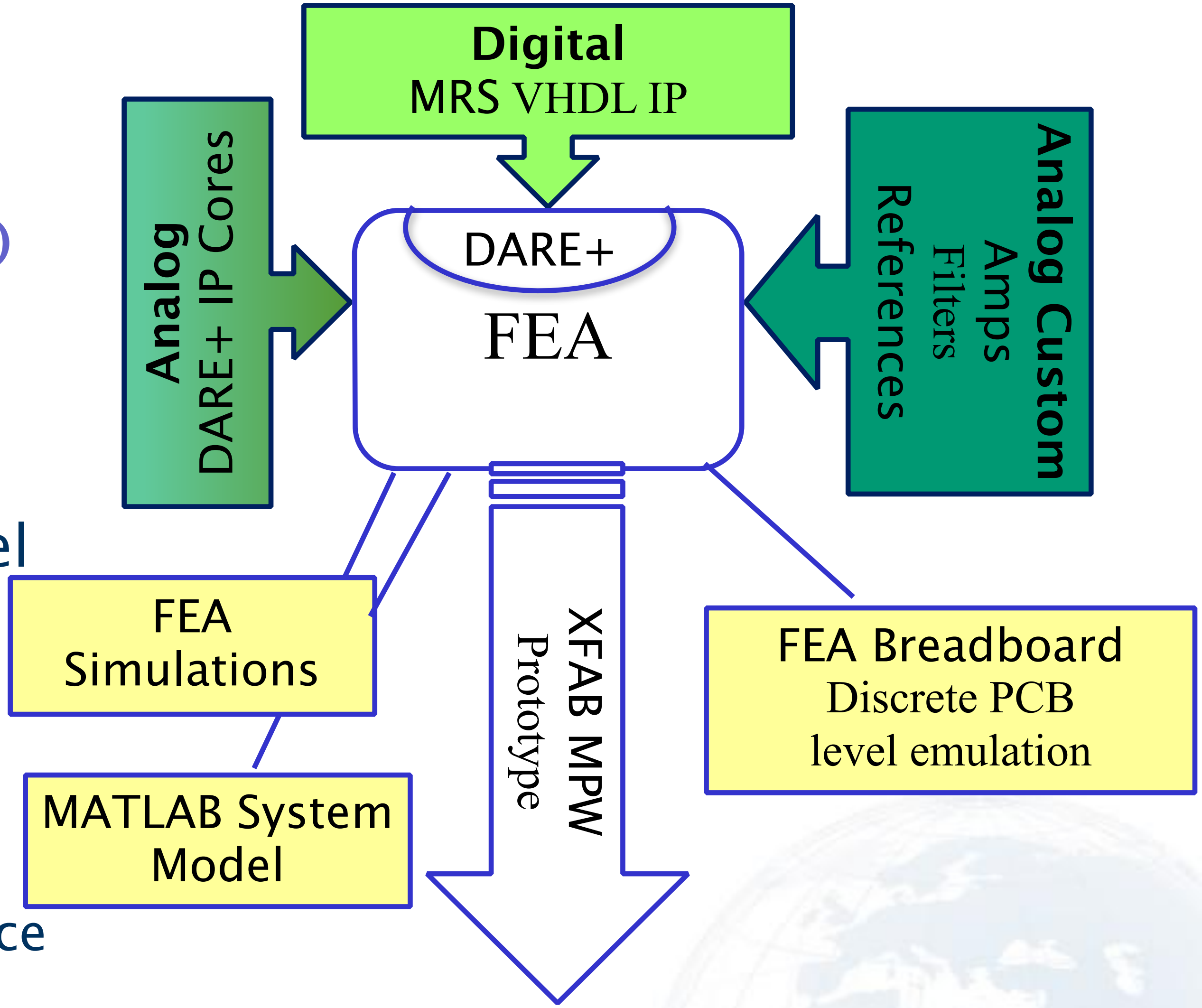
# MinIMU FEA Design and Development



- FEA design will maximise:
  - MRS (digital) VHDL
  - Analog IP CORES (ICSense)
  - DARE+ library (IMEC)
- Component level simulations and system level modelling.
- Discrete/PCB Breadboard
  - Confirm functionality
  - Provide baseline performance for comparison

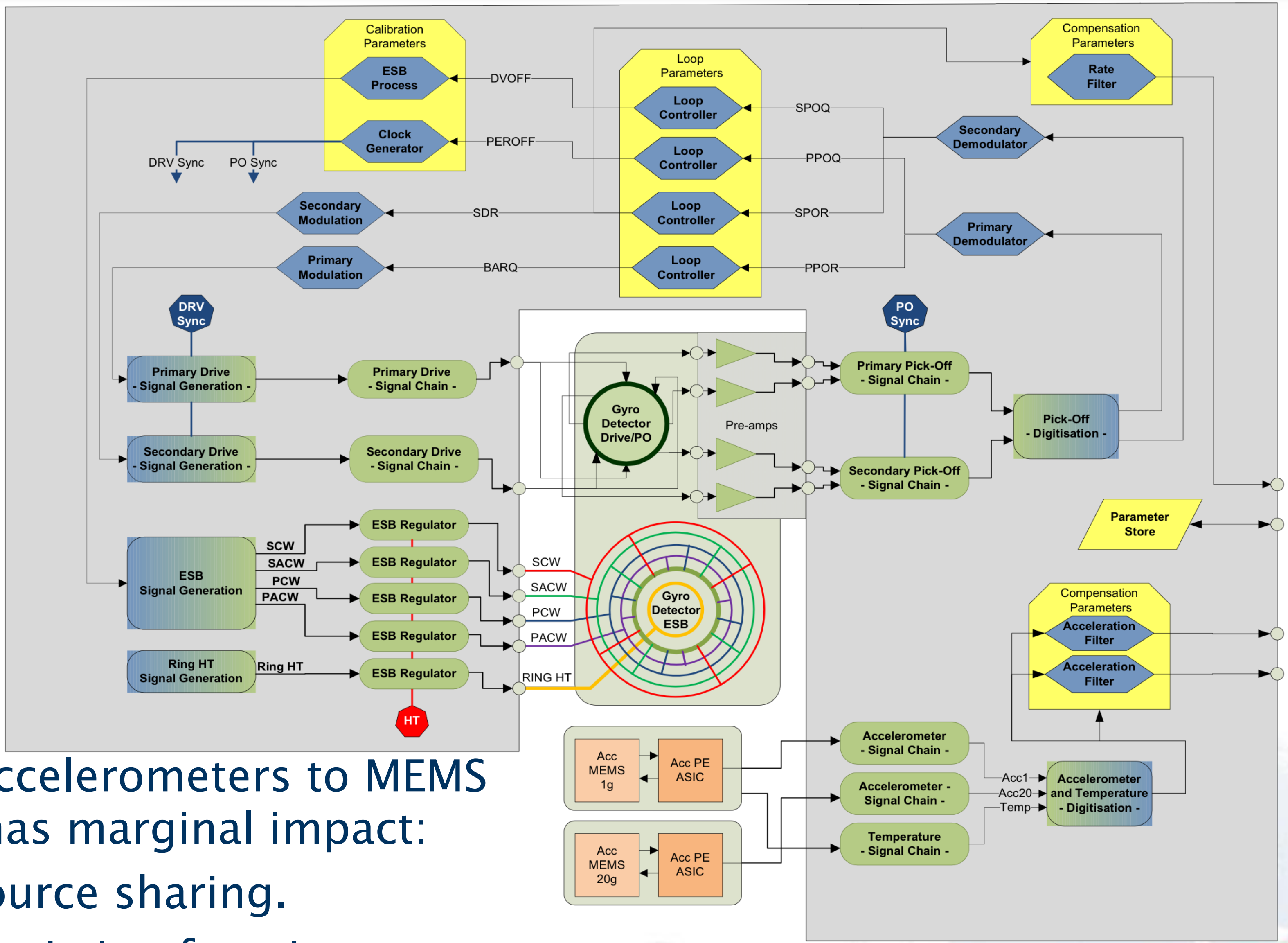


# MinIMU Electrical Architecture

MEMS Detectors:

- Gyro: **SSSL**
- Acc:
  - **ESS/Theon**
  - Colibrys

(Acc interface dual compatible at FEA level.

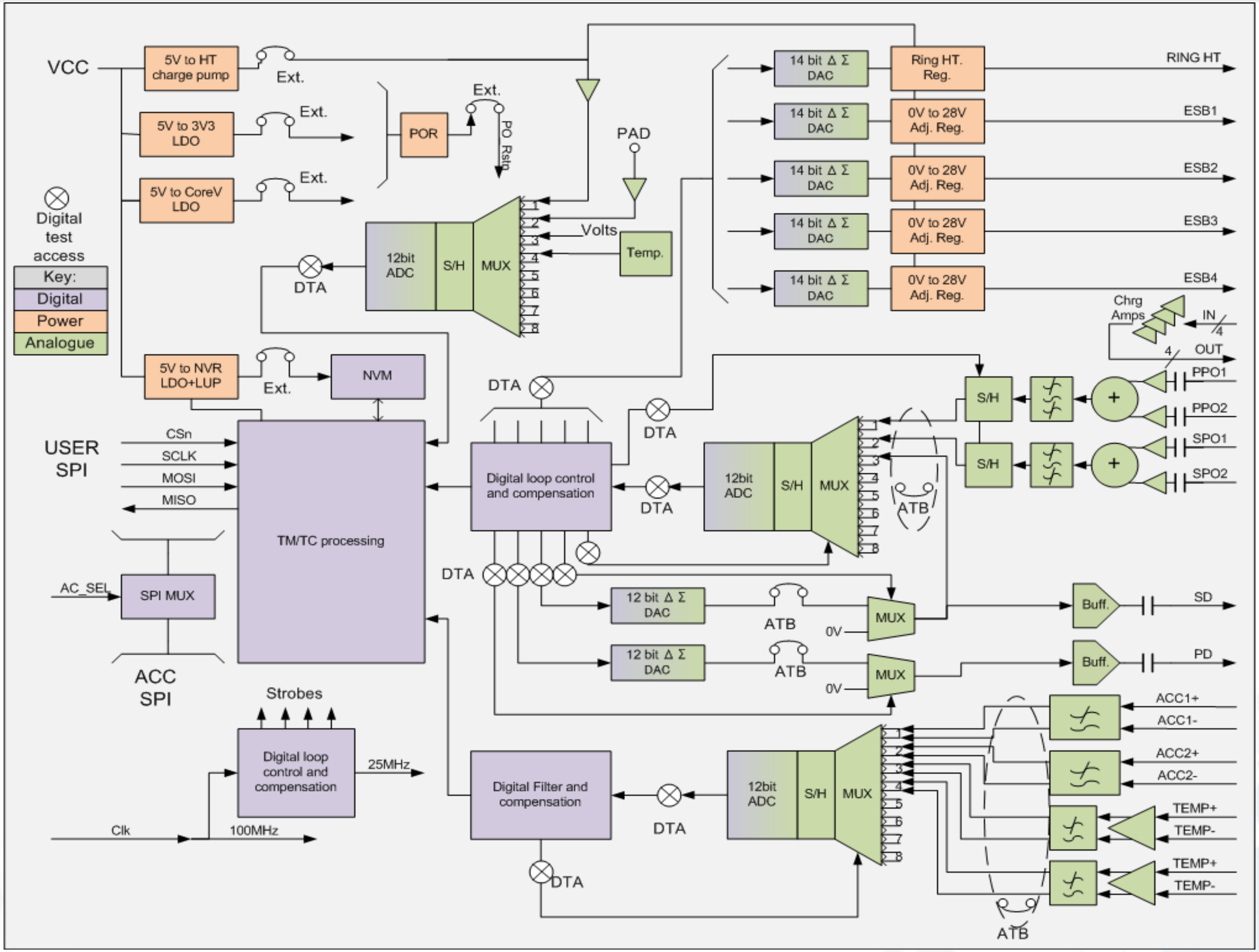



Addition of MEMS accelerometers to MEMS gyro architectures has marginal impact:

- Significant resource sharing.
- Duplication of existing functions.

# MinIMU FEA overview





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# FEA Technology/Foundry Selection



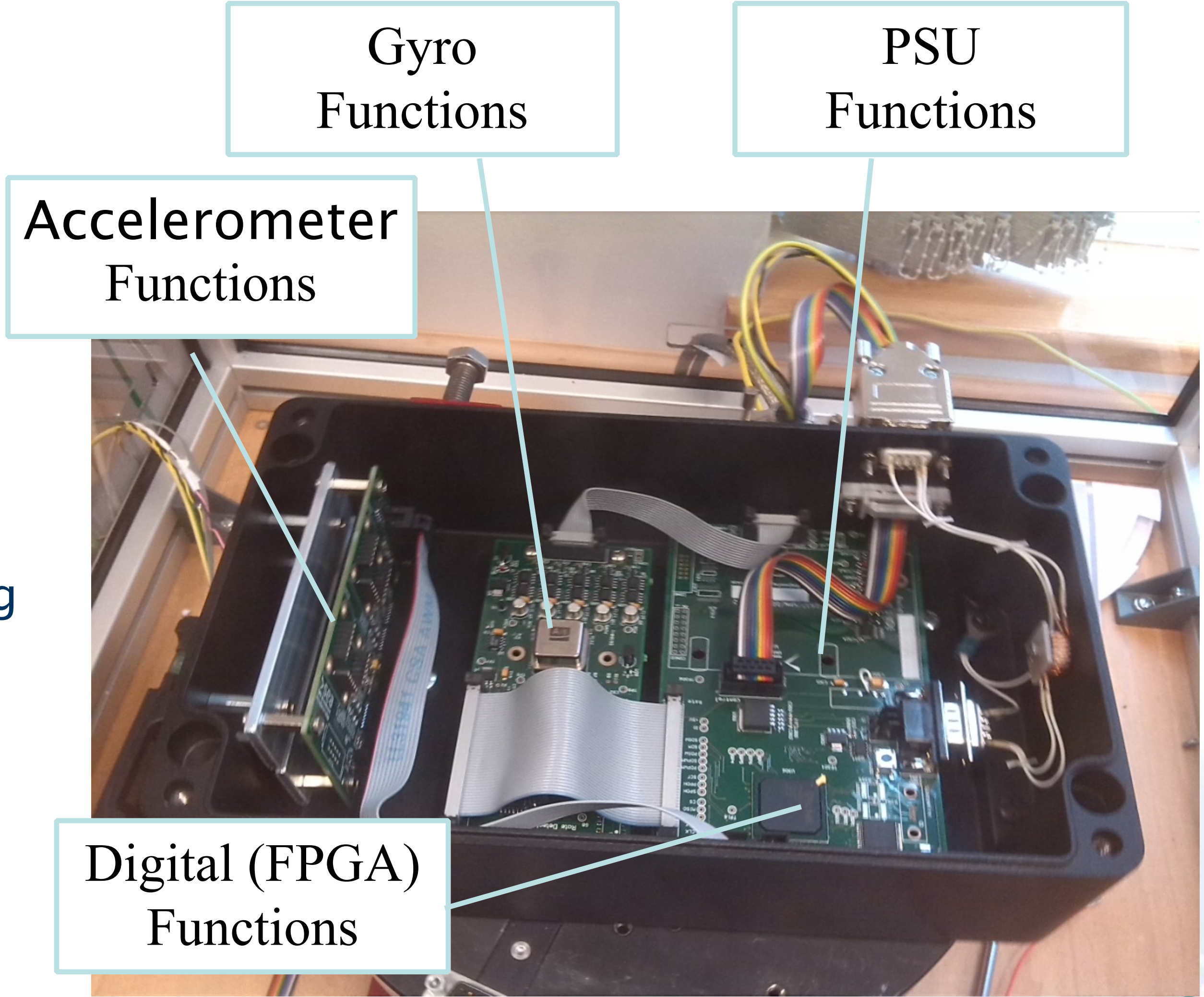
| Foundry | Technology | Rad hard library | High Voltage | PROM |
|---|---|---|---|---|
| Austriamicrosystems | 0.35um (H35) | no | 50V | EEPROM |
| Austriamicrosystems | 0.18um (H18) | no | 20V | ? |
| On-Semi | 0.35um (I3T50) | no | 50V | FREEPROM, OTP |
| On-Semi | 0.35um (I3T80) | no | 80V | OTP |
| TowerJazz | 0.18um | RAMON REDCAT | 5V | ePolyfuse, YFlash |
| TSMC | 0.18um (CV018LD) | no | 32V | FLASH, OTP |
| UMC | 0.18um (L180) | DARE | 5V | None |
| X-FAB | 0.18um (XH018) | DARE Aug 2014 | 45V | eFlash and OTP |

- XFAB 0.18 um (XH018) selected to provide HV capability, non-volatile storage and DARE library support

# FEA Breadboarding

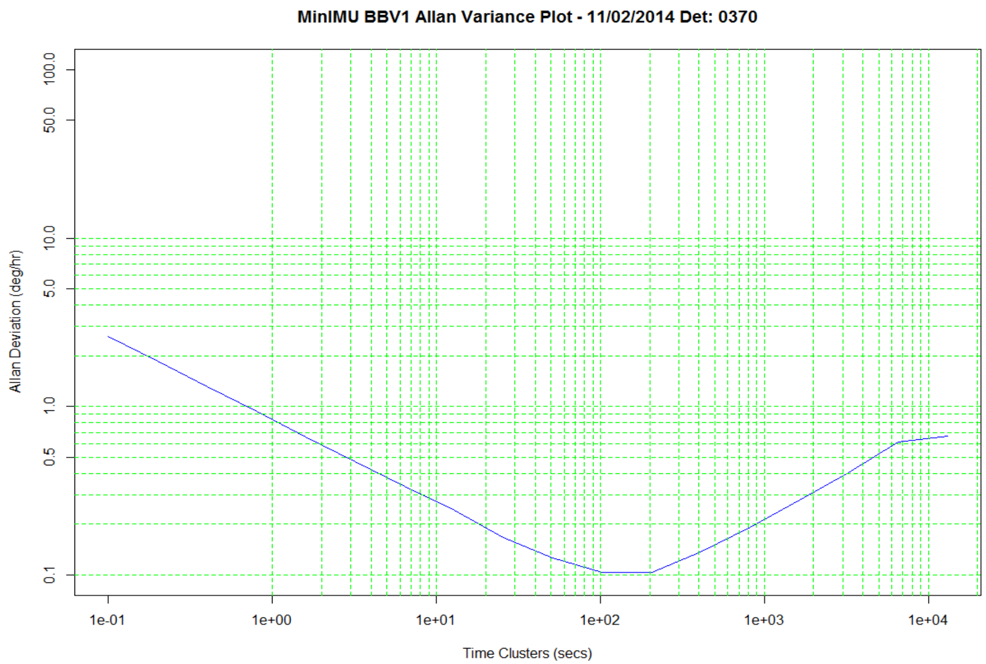


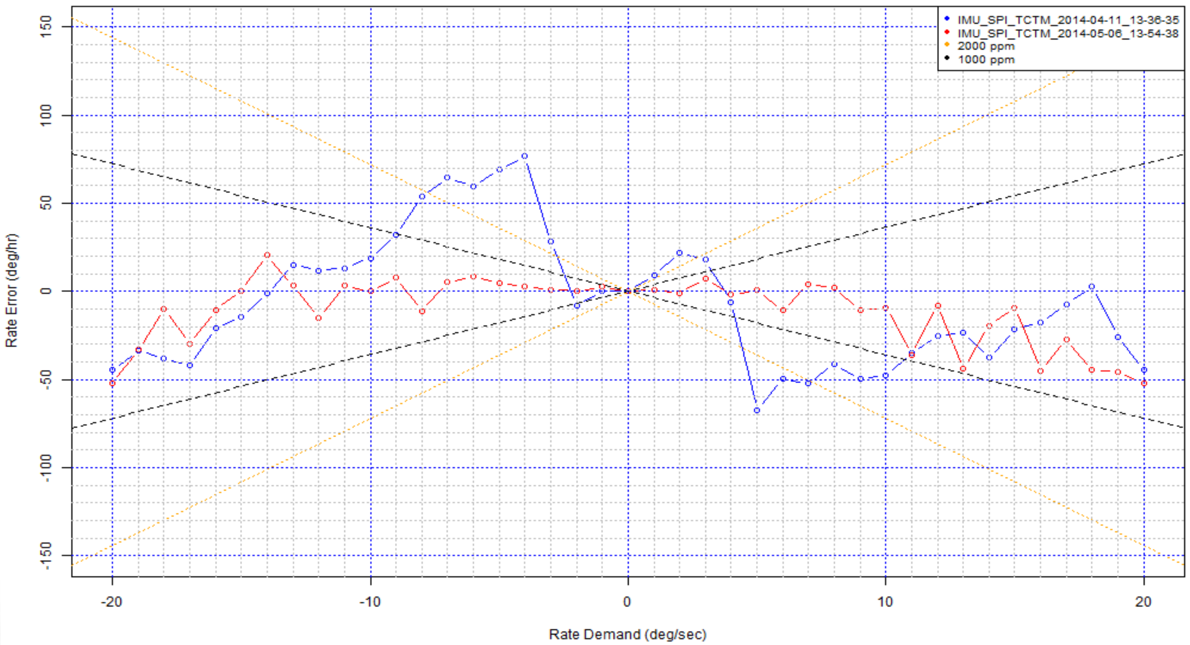
- FEA Breadboard completed and tested for gyro functions
- Performance drivers......
  - Delta-Sigma DACs
    - ESB 14 bit
    - Sec/Pri drive 12 bit
  - 13 bit ADC
  - 3V analogue stages
  - Power distribution/filtering
  - Filter ASIC margins
- Duplicate breadboard delivered to ESA for parallel/comparative testing
- Accelerometers on order.
- Test results to date confirm:
  - Viability of design
  - Performance close to existing MRS.
- Further testing to support detailed FEA designs.



# Breadboard Test Results and MinIMU Expectations

- Bias stability and Angular Random Walk similar to discrete MEMS gyro.
- Rate noise at 10–50 Hz sampling higher than in discrete MEMS implementation.
- Noise expected to be better in ASIC implementation.




- Scale Factor non-linearity dominated by Sigma-Delta drive DAC performance.
  - Optimising drive range to gyro range shows improvement to within 1000 ppm.
  - DAC performance expected to be better in ASIC implementation.



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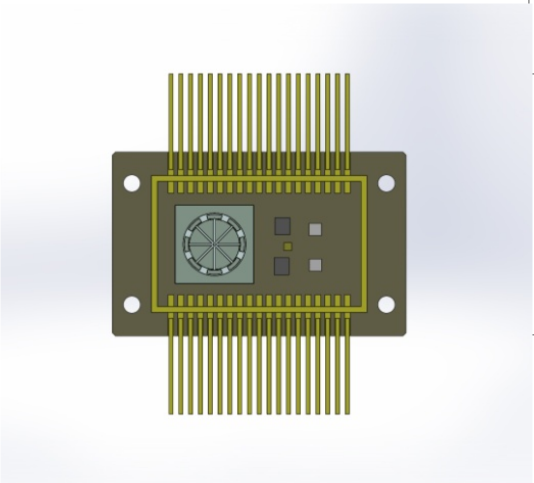
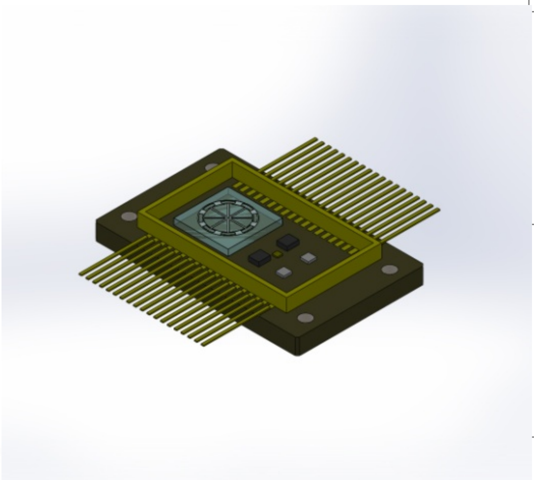
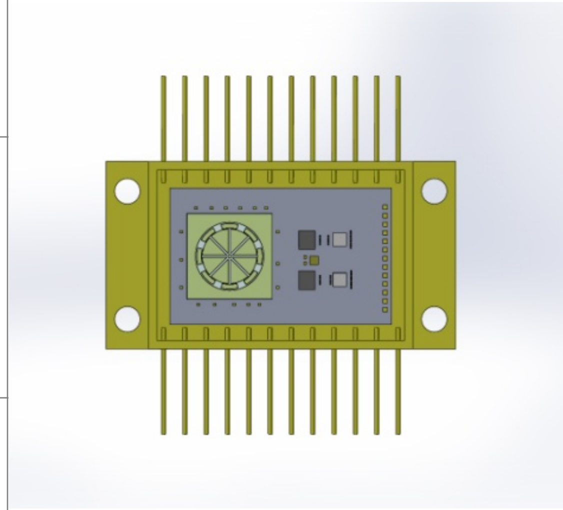
# MinIMU Packaging Trade-Off.

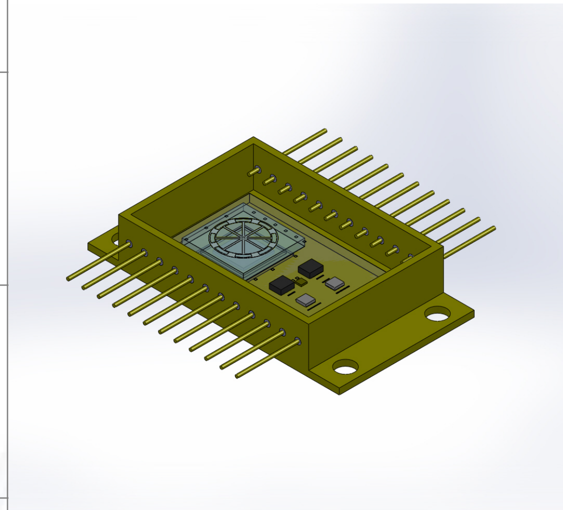






| Package Features | Key Drivers |
|---|---|
| Single or dual cavity | Thermal management<br>Signal path length<br>Reference planes<br>Package size and weight<br>Manufacturability |
| Through hole or side mounted pins | Package size and weight<br>Mounting options<br>Reliability<br>Acc. ASIC calibration |
| Metal or ceramic package construction | Reliability<br>Misalignment stability<br>Thermal management<br>Reference planes |
| Package with or without mounting flanges | Mounting options |
| Assembly materials | Reliability<br>Misalignment stability<br>Manufacturability |

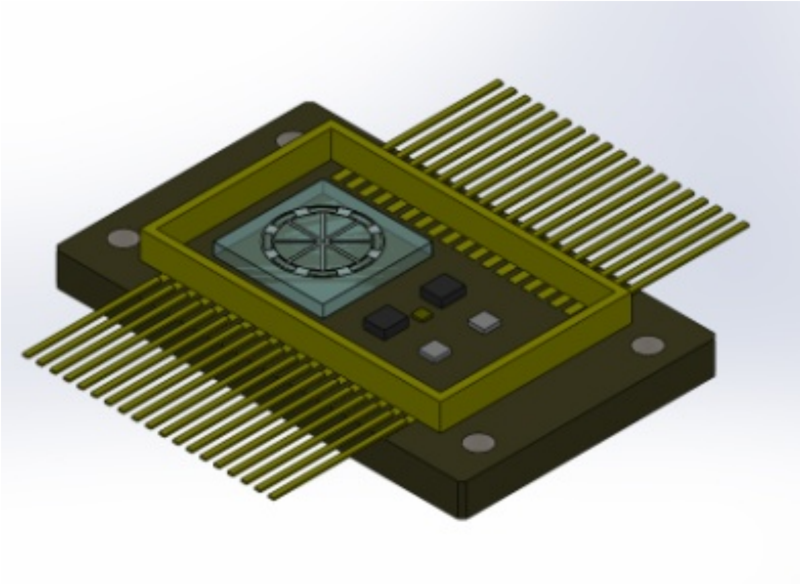




- Key points of trade off review for final package selection:
  - Thermal performance – the FEA  is mounted directly below the gyro to minimise the effect of thermal expansion on the gyro performance.
  - Signal path – FEA to gyro interconnections are balanced and as short as possible.
  - Reference surfaces – package layout minimises the tolerance stack-up between the package base reference plane and the MEMs mounting plane.
  - Package layout – side pins allow for both bulkhead and PCB mounting. Dual cavity allows for lowest possible package weight and size.
  - Device misalignment stability – use of CTE matched materials for package construction will minimise the stress on the MEMs components due to thermal effects.
  - Reliability – both options utilise industry standard packaging assembly techniques and materials and will provide a good base for long term device reliability.

# Baseline Packaging





- Dual Cavity
- 38 pin
- Mass..16 gms
- Volume..37.5 x 23.5x5.5 mm

# Packaging De-Risking Activities



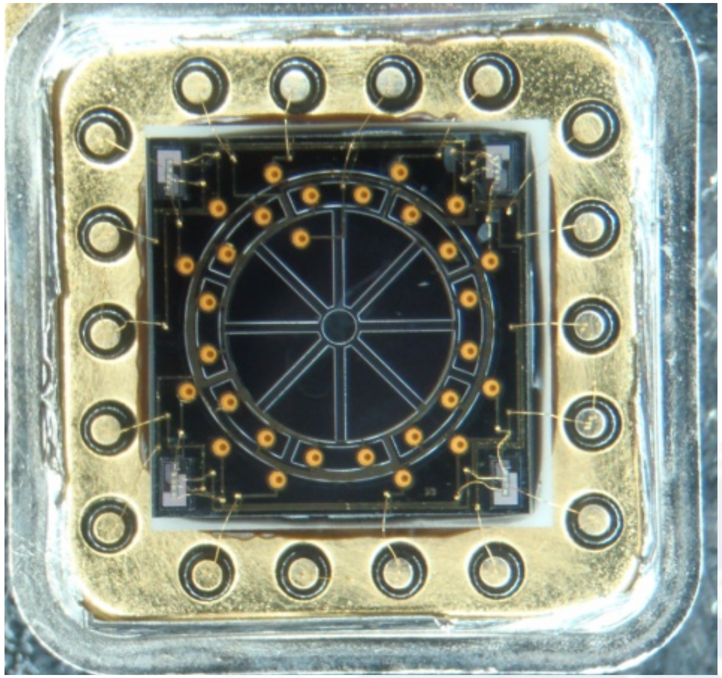
Three areas of packaging identified as potential risk areas:

1. Shock/vibration causing stressing/cracking for ceramic package hole mounting.
2. Detector mounting/planarity.
3. De-packaging of existing gyro detectors and re-mounting (prototype only).

De-risking activities in place to mitigate risk being carried forward into the prototype build.

For item 1 representative ceramic piece-parts have been manufactured and are currently in test.

For item 2 and 3 early, functional detector prototypes (mechanically representative) have been de-packaged and cleaned, re-assembled onto a ceramic substrate and re-mounted into detector can package for re-testing.

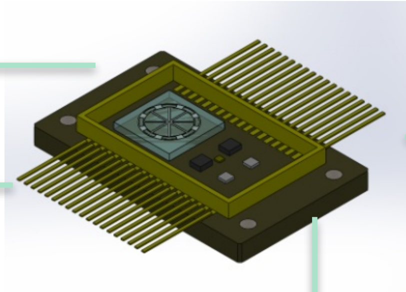


# Topics

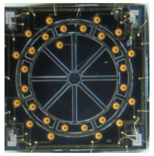
# Applications and Technology Exploitation



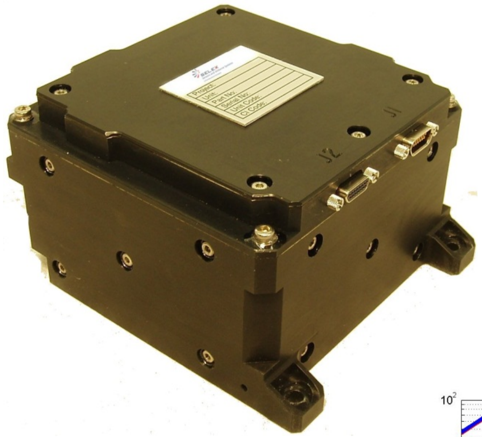
ESS20g/1g
Proximity ASIC



SGH15



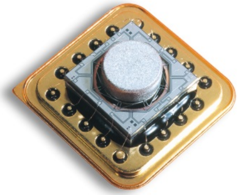
*SGH15*
- *ARW = 0.047°/√hr*
- *Bias Instability (Flicker Rate) = <1°/hr*



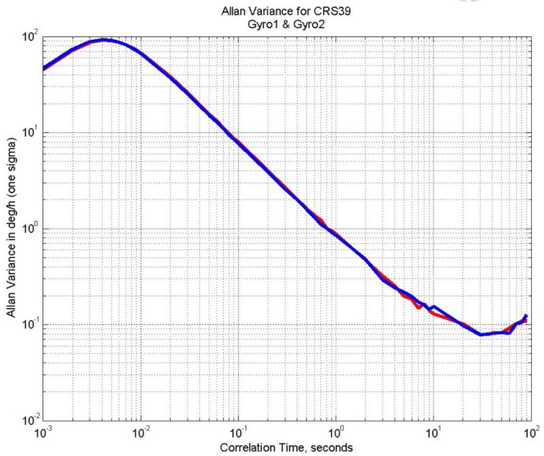
Single Axis IMU "MinIMU" Programme

FEA (die)

FEA (CQFP)



SGH03




*SGH03*
- *ARW = 0.0083°/√hr*
- *Bias Instability (Flicker Rate) = 0.08°/hr*

Lowest Mass/Volume

Planetary Exploration IMUs (eg. Rovers, ....).

Lowest Cost

uGyro Modules integration into avionics units (eg. OBCs, RIUs)

uGyro 3-axis Unit

FDIR + ?

# Conclusions



- Development of a Miniaturised IMU demonstrator was initiated in Feb 2013 with an aim to:
  - Provide a component level IMU function (single axis)
  - Offer the mass/power/volume/cost advantages of the terrestrial applications to the space domain.

- Key enabling technologies identified and baselined at PDR:
  - Mixed signal ASIC (European: XFAB 0.18 um)
    - With supporting DARE+ library and IP COREs
  - Multi-Chip Module packaging (dual cavity ceramic).

- Significant heritage from preceding MEMS Rate Sensor and accelerometer developments.

- FEA prototype fabrication planned for early 2015

- Emerging exploitation of FEA with new SSSL detector for lowest cost uGyro applications integrated into existing space units.

WE LOOK AFTER THE EARTH BEAT

# Thank You
# for your Attention
# Questions?