SINGLE EVENT EFFECTS
RADIATION TEST REPORT

Part Type : SP100V

Package : TO-3

N-Channel Power MOSFET

SGS Thomson

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TABLE OF CHANGES

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	Original Issue

TABLE OF CONTENTS

FIGURES

TABLES

I. ABSTRACT

Under ESA/ESTEC contract n° 13413/98/NL/MV covering "Radiation Evaluation of Power MOSFET Devices from Different European Manufacturers", a large number of commercial Power MOSFET device types were radiation assessed. Results from these assessments, primarily focused on the radiation sensitivity of the MOSFETs to Total Ionizing Dose (TID) and Single Event Effects (SEE), are reported in individual TID and SEE reports. Below summary table list manufacturer and evaluated types, and give references to the various reports issued.

Manufacturer	Type	TID Report	SEE Report
Philips	PHP50N06T	ESA_QCA990901T_C	ESA_QCA990901S_C
Philips	BUK456-200A	ESA_QCA990902T_C	ESA_QCA990902S_C
Motorola	MTP50N06VL	ESA_QCA990903T_C	
Motorola	MTW32N20E	ESA_QCA990904T_C	
Motorola	MTP50N06V	ESA_QCA990905T_C	
Siemens	BUZ100S	ESA_QCA990906T_C	ESA_QCA990906S_C
Siemens	BUZ100SL	ESA_QCA990907T_C	ESA_QCA990907S_C
Siemens	BUZ341	ESA_QCA990908T_C	ESA_QCA990908S_C
SGS-Thomson	SP60	ESA_QCA990909T_C	ESA_QCA990909S_C
SGS-Thomson	SP100V	ESA_QCA9909010T_C	ESA_QCA9909010S_C
SGS-Thomson	SP200V	ESA_QCA9909011T_C	ESA_QCA9909011S_C
Siemens	SPP1N60S5	ESA_QCA9909012T_C	ESA_QCA9909012S_C
Philips	BUK7508-55	ESA_QCA9909013T_C	ESA_QCA9909013S_C
Harris	HUF75639P3	ESA_QCA9909014T_C	ESA_QCA9909014S_C

II. INTRODUCTION

This report presents the results of a heavy ion Single Event Effects (SEEs) test program carried out on SP100V N-Channel Power MOSFET from SGS Thomson Semiconductor
Devices were tested at the European Heavy Ion Irradiation Facility (HIF) at Cyclone, Université Catholique de Louvain, Belgium.

This work was performed for ESA/ESTEC under ESA Contract No 13413/98/NL/MV dated 25/01/99

III. DOCUMENTS

III.1 APPLICABLE DOCUMENTS

AD1. Hirex Engineering proposal ref. HRX/98.3475 Issue 1, "Radiation Evaluation of Power MOS Devices from Different European Manufacturers"
AD2. ESA memorandum Appendix 1 to ESTEC/Contract No 13413/NL/MV

III.2 REFERENCE DOCUMENTS

RD1. Power MOS samples SGS letter ref. BE/PB/98187ce01
RD2. Single Event Effects Test method and Guidelines ESA/SCC basic specification No 25100
RD3. The Heavy Ion Irradiation Facility at CYCLONE, UCL document, Centre de Recherches du Cyclotron (IEEE NSREC'96, Workshop Record, Indian Wells, California, 1996)

IV. DEVICE INFORMATION

IV.1 DEVICE DESCRIPTION

N-Channel Power MOSFET, 100 Volts, 16 A encapsulated in TO-3 package

IV.2 PROCUREMENT OF TEST SAMPLES

Delivered by ESA

IV.3 PREPARATION OF SAMPLES

Devices have been delidded by Hirex Lab.

IV.4 SAMPLES CHECK OUT

A functional test sequence has been performed on delidded samples to check that devices have not been degraded by the delidding operation.

IV.5 DEVICE MARKING

Device marking is provided in Figure 1

Figure 1 – Device marking

Technology :	Strip-based process
Die metallization	Aluminum
Die dimensions (approximately, mm²)	2,6 x 2,4

Further details on die description are provided in "Comparative Description and Analysis of Various Power MOSFETs", ESA document ref. ESA_QCA9909015_C (Hirex ref. HRX/99.4775) / ESA Contract No 13413/98/NL/MV dated 25/01/99.

V. DEVICE TEST DEFINITION

V.1 PREPARATION OF TEST HARDWARE AND PROGRAM

Overall device emulation, SEE, data storage and processing were implemented using an in-house test hardware and application specific test boards.

The generic in-house test equipment is driven by a PC computer through a RS232 line. All power supplies and input signals are delivered and monitored by the in-house equipment which also stores in its memory the output data from the device throughout the specific test board.

The application specific test board allowed to interface the standard test hardware with the device under test, in order to correctly emulate the relevant part, to record all the different type of errors during the irradiation and to set output signal for processing and storage by the standard test equipment.

At the end of each test run, data are transferred to the PC computer through the RS232 link for storage on hard disk or floppies.

V.2 GENERIC TEST SET-UP

Generic device test set-up is presented in Figure 2.
This set-up is constituted of the following units:

- A PC computer (to configure and interface with the test system and store the data),
- An electronic rack with the instrumentation functions provided by a set of electronic modules,
- A mother board under vacuum which allows for the sequential test of up to 10 devices.
- A digital oscilloscope to store analog SEE waveform

SEE Test functional diagram is shown in Figure 3.

V.2.1 Mother board description (Ref. IL140A)

The motherboard acts as a standard interface between each DUT test board and the control unit :
For each slot, the following signals can be considered:

- 4 inputs signals
  - Drain Source programmable power supply
  - Gate Source programmable power supply
  - Simulation signal
  - Heater control signal
- 1 output signal
  - 1 fast analog output signal

- IL140 board has been designed to comply with both PSI and Louvain test facilities .
- Each device needs a dedicated plug-in test board compatible with IL140 mother board.
- The number of slots is limited to 10: Up to 10 TO220 DUT test boards can be plugged or 5 TO3 DUT test boards.
- Operation is multiplexed and only one slot is powered at one time.

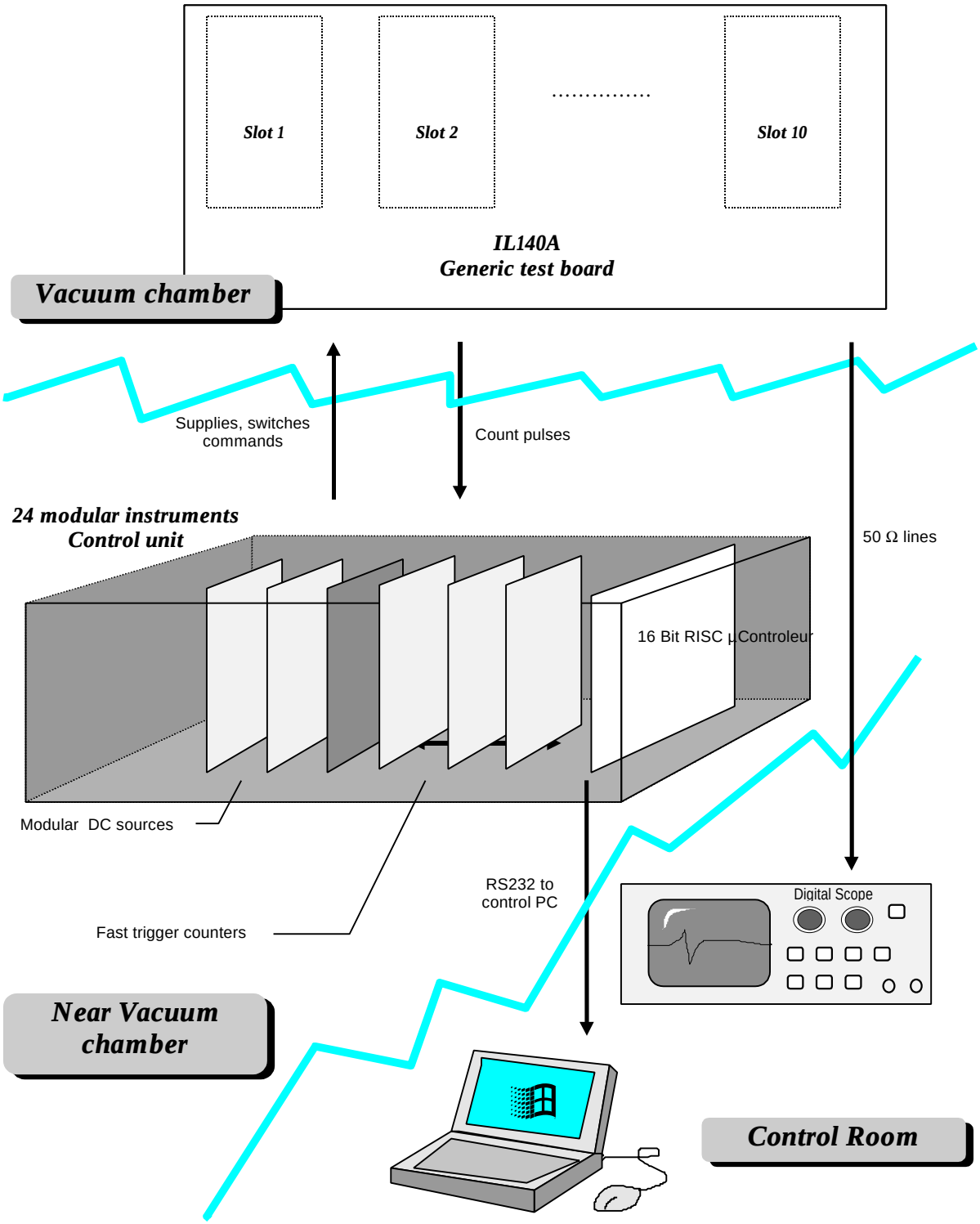

Figure 2 - Generic Test Set-up

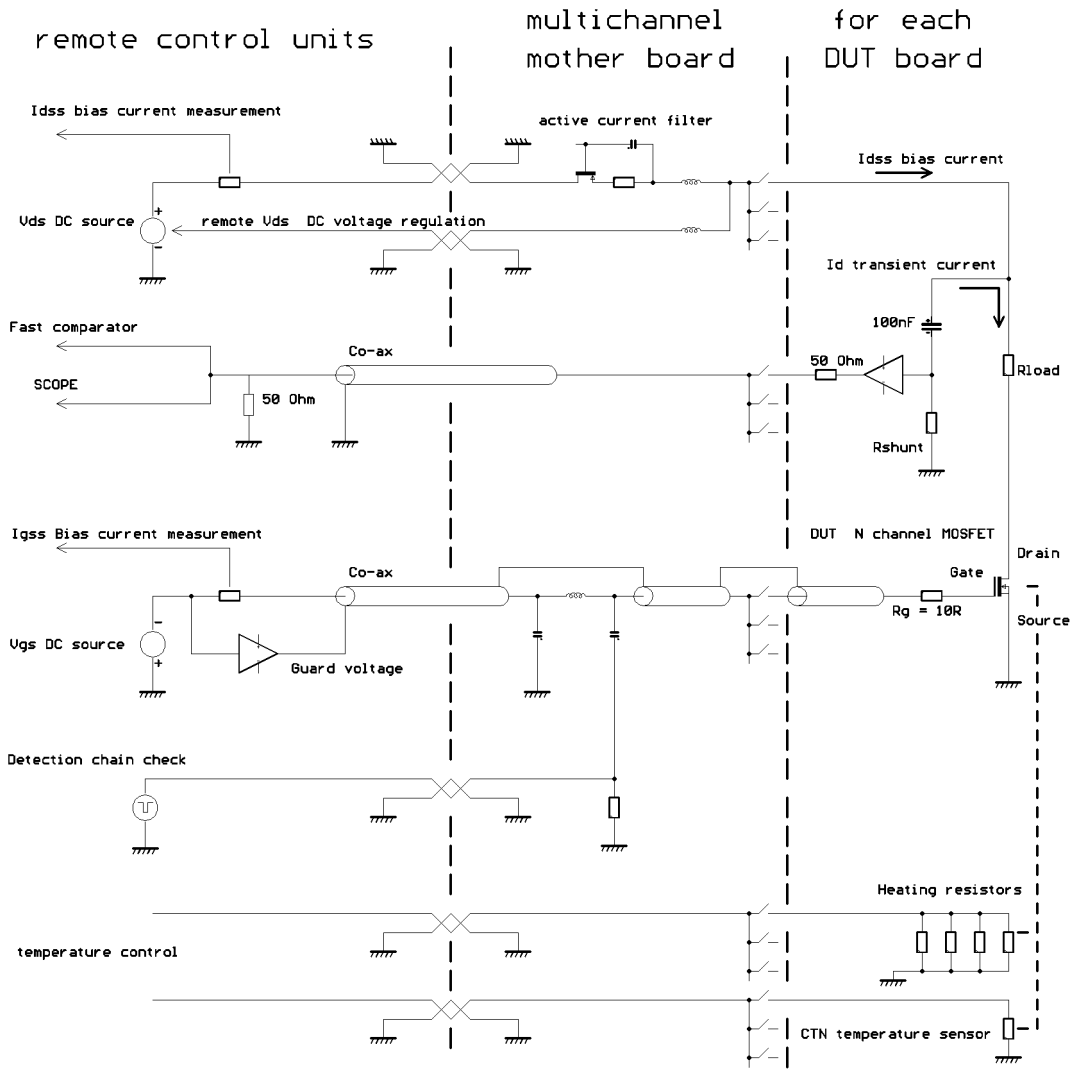

Figure 3 – Functional diagram for SEE Test

V.2.2 DUT Test board description

The device under test is mounted on a specific PCB board which again is connected to the motherboard.
Two different DUT boards have been designed which can be fitted with either a TO2xx plastic package device or with TO3 metal package device.
On each individual DUT board, a limiting current serie resistance and a shunt resistor are mounted for SEB pulse measurement.
To prevent the destructive burn-out of the DUT when the parasitic Bipolar Junction Transistor (BJT) is triggered on by a strike, the DUT Drain is biased with a capacitor and a limiting current resistor mounted on each DUT board. This is to limit the amount of energy available as well as the maximum transient current value.
For testing at elevated temperature, each board is equipped with surface mount heating resistors plus a CTN thermistor for temperature control.

V.3 TEST CONFIGURATION

Test set-up which has been used for the present test report, allows for the detection of both Single Event Burn-out (SEB) and Single Event Gate Rupture (SEGR) effects

V.3.1 Single Event burnout (SEB)

SEB can be observed with the MOSFET in the off mode.
To get non destructive SEBs, selected test principle was to limit as much as possible the energy which could flow into the DUT when the parasitic bipolar transistor enters second breakdown.
To achieve this goal, a resistor Rload (see Figure 3) in serie with the DUT drain limits the current which can flow from the bias circuit (capacitor of 100nF, see Figure 3). In that case the only available energy which can flow into the DUT without any external current limitation is the one stored into the output DUT capacitance C_{DS}.
The equivalent circuit when an SEB is triggered is shown in Figure 4.
Observation of VDS transients is done at Rshunt which form a resistor divider with Rload.

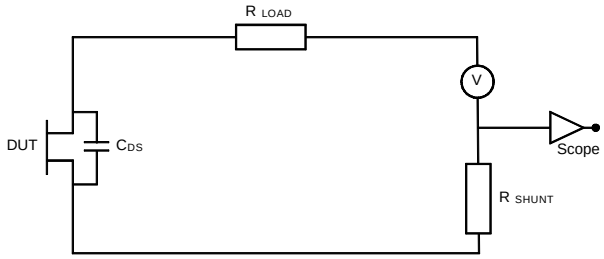

Figure 4 – Equivalent circuit for SEB including the parasitic capacitor of the MOSFET.

Actual resistor values for the test results presented in this report are shown in the Table 1 here below.

Symbol	Value
R_{load}	2,5 kohms
R_{Shunt}	25 ohms

Table 1 – Test circuit resistor values

Events are counted thanks to a programmable threshold comparator of 50MHz bandwidth. Moreover the monitoring of changes in the leakage dc current Idss will allow to check for eventual permanent degradation.

Temperature effect may be evaluated as each DUT single board is provided with surface mount heating resistors and a thermistor mounted on the back side of the board, which give the ability of testing at elevated temperature.

V.3.2 Single Event Gate Rupture (SEGR)

SEGR is a destructive effect which can be observed with the MOSFET in the off mode. Monitoring of the IGSS current allows for the detection of a SEGR which corresponds to a permanent degradation of the gate current.
This requires the measurement of µamp current amplitude under high impedance. Test board design is compatible with the accelerator environment by the use of a complete guard ring.
Fluence is recorded during each run by monitoring with a modular counter, the TTL signal delivered by an on-line Beam Detector. Information on the reached fluence at the time of an eventual SEGR occurrence can then be retrieved by analysis of the run data.

VI. TEST FACILITIES

VI.1 HEAVY IONS

Test at the cyclotron accelerator was performed at Université de Louvain (UCL) in Louvain la neuve (Belgium) under HIREX Engineering responsibility.

VI.1.1 Beam Source

In collaboration with the European Space Agency (ESA), the needed equipment for single events studies using heavy ions has been built and installed on the HIF beam line in the experimental hall of Louvain-la-Neuve cyclotron.
CYCLONE is a multi particle, variable energy, cyclotron capable of accelerating protons (up to 75 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU. For these ions, the maximal energy can be determined by the formula :

$$110\ Q^2/M$$

where Q is the ion charge state, and M is the mass in Atomic Mass Units.

The heavy ions are produced in a double stage Electron Cyclotron Resonance (ECR) source. Such a source allows to produce highly charged ions and ion "cocktails". These are composed of ions with the same or very close M/Q ratios. The cocktail ions are injected in the cyclotron, accelerated at the same time and extracted separately by a fine tuning of the magnetic field or a slight changing of the RF frequency. This method is very convenient for a quick change of ion (in a few minutes) which is equivalent to a LET variation.

VI.1.2 Beam Set-up

VI.1.2.1 Ion Beam Selection

The LET range was obtained by changing the ion species and incident energy and changing the angle of incidence between the beam and the chip.
For each run, information on the beam characteristics is provided in Table 2.

VI.1.2.2 Flux Range

For each run, the averaged flux value is provided in Table 2.

VI.1.2.3 Particle Fluence Levels

Fluence level was comprised between few x10E4 and 5 x10E5 ions/cm²

VI.1.2.4 Dosimetry

The current UCL Cyclotron dosimetry system and procedures were used.

VI.1.2.5 Accumulated Total Dose

For each run, the computed equivalent cumulated doses received by the DUT sample, is provided here below:

S/N	Dose (rads)
#001	3,04 E 2
#003	3,28 E 2
#005	7,43 E 2
#006	3,70 E 2
#014	2,68 E 2
#015	0,04 E 2

VI.1.2.6 Test Temperature Range

Runs have been performed at room temperature with the exception of few runs . However few runs were performed at elevated temperature to check the effect of temperature on SEB error cross section.

VII. HEAVY IONS RESULTS

VII.1 SP100V TEST RESULTS

Krypton and Argon ions have been used with respectively an LET of 34 and 14.1 MeV/mg/cm². Results per run are presented in Table 2.

At Vds of 60V, the difference in terms of SEB error cross section which can be observed for runs A014 and A018 on one side and runs B011 and B012 on the other side, may be explained by the difference in the comparator threshold magnitude.

Temperature effect can be observed with runs #A018, #A021 and #A022 results, performed respectively at ambient, 50 and 65 °C on the same sample and for the same VDS rating : SEB cross-section value decreases when the temperature value increases. This is in line with what has been already reported in various experiment results on power MOSFETs.

Main outcomes can then be summarized as follows :

With Krypton (34 MeV/mg/cm²) and device biased with a fixed Gate Source Voltage (VGS) of –2V :

- Devices are SEB free when VDSS. does not exceed 55 % of maximum rating.
- Devices are not sensitive to SEGR when VDSS does not exceed 60% of maximum rating.

With Argon (14.1 MeV/mg/cm²) and device biased with a fixed Gate Source Voltage (VGS) of –2V :

- Devices are SEB free up to 100% VDSS rating.
- Devices are not sensitive to SEGR (up to 100% VDSS rating)

With Argon, when devices are tested at a VDSS rating up to 70%, the maximum gate source voltage which can be applied without occurrence of SEGR event is -15V (limit of the present test).

VII.2 TYPICAL SEB WAVEFORM

Figure 5 show a typical example obtained with a 100V transistor. In this figure, voltage variation across R_{shunt} can be observed for a SEB pulse waveform at two rated V_{DS} conditions, 60V and 70V.
The superposition of the simulation pulse (observed at R_{shunt}) which consist to turn on the DUT allows to compare in each case, which part of the circuit is involved:

- In the SEB case, it can be seen that drain source voltage drops to zero in a very short time, then once the energy stored in the output DUT capacitance is dissipated, the current limitation provided by R_{load} allows for leaving the burn-out sustaining condition and DUT output capacitance start to reload with a current limited by $R_{load.}$
  The very high dV/dt (> 10 000V/µs)induce a peak current greater than 2 A, which discharge the internal C_{DS} DUT capacitor in a few ns.
- In the case of simulation pulse, once the DUT is switched on, the supply current which flows into the DUT is limited by R_{load}.

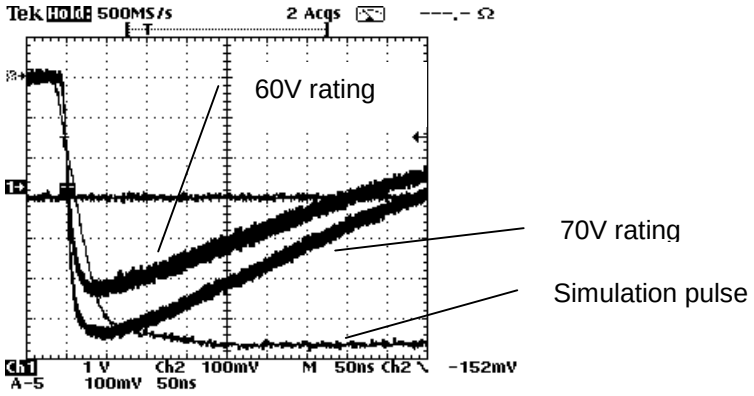

Figure 5 – Example of non destructive SEBs observed on a 100V transistor at 60V and 70V Vds ratings

VIII. CONCLUSION

SEU test have been conducted on SP100V N-channel Power MOSFET from SGS Thomson, using the heavy ions available at the European Heavy Ion Irradiation Facility (HIF), at Cyclone, Université Catholique de Louvain, Belgium.

With Krypton (34 MeV/mg/cm²) and device biased with a fixed Gate Source Voltage (VGS) of –2V :

- Devices are SEB free when VDSS. does not exceed 55 % of maximum rating.
- Devices are not sensitive to SEGR when VDSS does not exceed 60% of maximum rating.

With Argon (14.1 MeV/mg/cm²) and device biased with a fixed Gate Source Voltage (VGS) of –2V :

- Devices are SEB free up to 100% VDSS rating.
- Devices are not sensitive to SEGR (up to 100% VDSS rating)

With Argon, when devices are tested at a VDSS rating up to 70%, the maximum gate source voltage which can be applied without occurrence of SEGR event is -15V (limit of the present test).

Table 2 – Heavy Ion Test results on SP100V N-Channel Power MOSFET from SGS Thomson Semiconductor :

													SEB		SEGR			
Run	Date	S/N	Ion	LETeff	Angle	T(°C)	VDS	VGS	%VDSS	Fluence	Flux	Time	Nbr	Sigma	Nbr	Sigma	Comparator Threshold	Equivalent Pulse height
#		-	-	(MeV/mg/cm²)	(°)	(°C)	(V)	(V)	(%)	(p/cm²)	(p/cm²/s)	(s)	(-)	cm²	(-)	cm²	mV	V
VGS=-2V, Ion Krypton, LET =34 MeV/mg/cm² @ room temperature																		
A011	09/01/99	1	84-Kr	34	0	25	30	-2	30%	100163	1473	68	0				-250	-25
A012	09/01/99	1	84-Kr	34	0	25	40	-2	40%	100585	1524	66	0				-250	-25
A016	09/01/99	1	84-Kr	34	0	25	55	-2	55%	100628	1324	76	0				-100	-10
A017	09/01/99	3	84-Kr	34	0	25	55	-2	55%	101096	1218	83	0				-100	-10
B013	11/06/99	14	84-Kr	34	0	25	55	-2	55%	250600	1640	152,80	0				-500	-50
A014	09/01/99	1	84-Kr	34	0	25	60	-2	60%	100380	1673	60	537	5,35E-03			-100	-10
A018	09/01/99	3	84-Kr	34	0	25	60	-2	60%	100465	1225	82	509	5,07E-03			-152	-15
B010	11/06/99	6	84-Kr	34	0	25	60	-2	60%	500000	1290	387,60	5	1,00E-05			-500	-50
B012	11/06/99	14	84-Kr	34	0	25	60	-2	60%	199720	1560	128,03	4	2,00E-05			-500	-50
B011	11/06/99	6	84-Kr	34	0	25	65	-2	65%	180191	1400	128,71	519	2,88E-03	1	5,55E-06	-500	-50
A015	09/01/99	1	84-Kr	34	0	25	70	-2	70%	55295	1420	38,93	740	1,34E-02	1	1,81E-05	-100	-10
A019	09/01/99	3	84-Kr	34	0	25	70	-2	70%	100383	1304	77	1747	1,74E-02			-152	-15
VDS=-5V, Ion Krypton, LET =34 MeV/mg/cm² @ room temperature																		
B044	11/06/99	15	84-Kr	34	0	25	70	-5	70%	80	3580	0,02	0		1	1,25E-02	-100	-10
VGS=-2V, Ion Krypton, LET =34 MeV/mg/cm² @ elevated temperature																		
A013	09/01/99	1	84-Kr	34	0	80	50	-2	50%	101014	1554	65	0				-480	-48
A021	09/01/99	3	84-Kr	34	0	50	60	-2	60%	100878	1401	72	238	2,36E-03			-152	-15
A022	09/01/99	3	84-Kr	34	0	65	60	-2	60%	100352	1320	76	86	8,57E-04			-152	-15
A020	09/01/99	3	84-Kr	34	0	50	70	-2	70%	100648	1398	72	1637	1,63E-02			-152	-15
VGS=-2V, Ion Argon, LET =14,1 MeV/mg/cm² @ room temperature																		
A247	10/01/99	5	40-Ar	14,1	0	25	50	-2	50%	107153	7144	15	0				-152	-15
A251	10/01/99	5	40-Ar	14,1	0	25	60	-2	60%	348225	5197	67	0				-152	-15
A255	10/01/99	5	40-Ar	14,1	0	25	70	-2	70%	100233	5012	20	0				-152	-15
A259	10/01/99	5	40-Ar	14,1	0	25	80	-2	80%	100000	6667	15	0				-152	-15
A260	10/01/99	5	40-Ar	14,1	0	25	100	-2	100%	500000	8475	59	0				-152	-15
B029	11/06/99	14	40-Ar	14,1	0	25	100	-2	100%	100000	2440	40,98	0				-100	-10
VGS=-5V, Ion Argon, LET =14,1 MeV/mg/cm² @ room temperature																		
A248	10/01/99	5	40-Ar	14,1	0	25	50	-5	50%	503547	7194	70	0				-152	-15
A252	10/01/99	5	40-Ar	14,1	0	25	60	-5	60%	102749	4110	25	0				-152	-15
A256	10/01/99	5	40-Ar	14,1	0	25	70	-5	70%	103480	5446	19	0				-152	-15
VGS=-10V, Ion Argon, LET =14,1 MeV/mg/cm² @ room temperature																		
A249	10/01/99	5	40-Ar	14,1	0	25	50	-10	50%	505955	6023	84	0				-152	-15
A253	10/01/99	5	40-Ar	14,1	0	25	60	-10	60%	104705	5235	20	0				-152	-15
A257	10/01/99	5	40-Ar	14,1	0	25	70	-10	70%	104831	5242	20	0				-152	-15
VGS=-15V, Ion Argon, LET =14,1 MeV/mg/cm² @ room temperature																		
A250	10/01/99	5	40-Ar	14,1	0	25	50	-15	50%	503690	5724	88	0				-152	-15
A254	10/01/99	5	40-Ar	14,1	0	25	60	-15	60%	101828	5657	18	0				-152	-15
A258	10/01/99	5	40-Ar	14,1	0	25	70	-15	70%	105341	7524	14	0				-152	-15