TOTAL DOSE RADIATION TEST REPORT

Part Type : HUF75639P3

Package : TO-262AA

N-Channel Power MOSFET

Harris Semiconductors

Report Reference : ESA_QCA9909014T_C

Issue : 01

Date : July 1st 1999

ESA Contract No 13413/98/NL/MV dated 25/01/99

ESTEC Technical Officer: R. Harboe Sorensen

Hirex reference :	HRX/99.4573	Issue : 01	Date :	July 1st 1999
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on
Harris Semiconductors HUF75639P3 N-Channel Power Mosfet.

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1 Abstract

Under ESA/ESTEC contract n° 13413/98/NL/MV covering "Radiation Evaluation of Power MOSFET Devices from Different European Manufacturers", a large number of commercial Power MOSFET device types were radiation assessed. Results from these assessments, primarily focused on the radiation sensitivity of the MOSFETs to Total Ionizing Dose (TID) and Single Event Effects (SEE), are reported in individual TID and SEE reports. Below summary table list manufacturer and evaluated types, and give references to the various reports issued.

Manufacturer	Type	TID Report	SEE Report
Philips	PHP50N06T	ESA_QCA990901T_C	ESA_QCA990901S_C
Philips	BUK456-200A	ESA_QCA990902T_C	ESA_QCA990902S_C
Motorola	MTP50N06VL	ESA_QCA990903T_C	
Motorola	MTW32N20E	ESA_QCA990904T_C	
Motorola	MTP50N06V	ESA_QCA990905T_C	
Siemens	BUZ100S	ESA_QCA990906T_C	ESA_QCA990906S_C
Siemens	BUZ100SL	ESA_QCA990907T_C	ESA_QCA990907S_C
Siemens	BUZ341	ESA_QCA990908T_C	ESA_QCA990908S_C
SGS-Thomson	SP60	ESA_QCA990909T_C	ESA_QCA990909S_C
SGS-Thomson	SP100V	ESA_QCA9909010T_C	ESA_QCA9909010S_C
SGS-Thomson	SP200V	ESA_QCA9909011T_C	ESA_QCA9909011S_C
Siemens	SPP1N60S5	ESA_QCA9909012T_C	ESA_QCA9909012S_C
Philips	BUK7508-55	ESA_QCA9909013T_C	ESA_QCA9909013S_C
Harris	HUF75639P3	ESA_QCA9909014T_C	ESA_QCA9909014S_C

2 Introduction

A total dose radiation evaluation test of the HARRIS semiconductors HUF75639P3 N-Channel Power Mosfet has been performed with an accumulated dose of about 37 Krad(Si) at a dose rate of 75 rad(Si)/hour, in response to European Space Agency contract reference : 13413/98/NL/MV.

The purpose of this test was to evaluate total dose withstanding of this component, to investigate its suitability for being used in space applications. This test was conducted on commercial samples provided by ESTEC.
Test has been performed in accordance with Hirex proposal HRX/98.3475 issue 01.

A complete set of electrical measurements together with graphical representation of measured parameters with respect to total dose received, are provided for all samples.

SEE results for this device type can be found in SEE radiation test report: ESA_QCA9909014S_C

3 Applicable and Reference Documents

3.1 Applicable Documents

- ESA/SCC Basic specification N° 22900 issue 4
- Harris Semiconductors datasheet
- Hirex Engineering proposal: HRX/98.3475 issue 01.

3.2 Reference Documents

- MIL-STD-883: test methods and procedures for microcircuits

4 Test Samples

11 samples of the HUF75639P3 device were tested (2 groups of 5 + 1 control sample). The samples were serialized before the radiation test as indicated in the following table.

Serial Number	Allocation
1	Control
2	Bias 1
3	Bias 1
4	Bias 1
5	Bias 1
6	Bias 1
7	Bias 2
8	Bias 2
9	Bias 2
10	Bias 2
11	Bias 2

Identification of the HUF75639P3 is given below:

Part Number:	HUF75639P3	**Mask Set:**	NA
Top Marking:	75639P H819L	**Chip Marking:**	NA
Diffusion Lot:	NA	**Wafer #:**	NA
Date Code:	9819	**Project:**	Not defined

5 Experimental Conditions

5.1 Radiation Source Dose Rate and Annealing

The dose exposures were performed at CERT-ONERA. In this irradiation facility, a Cobalt 60 source is used with the possibility to vary the dose rate by simply adjusting the distance to the source.
The irradiation conditions used for this test are provided in the following table:

Irradiation Steps	Dose rate	Annealing steps	Temperature
krads	krads/h	hours	°C
0			
3.85	0,075		25
7.35	0,075		25
13.95	0,075		25
19.65	0,075		25
24.65	0,075		25
29.85	0,075		25
36.85	0,075	0	25
		24	25
		192	100

5.2 Bias during Dose Exposures and Measurements conditions

5.2.1 Bias conditions

During exposures dedicated test boards were used mounted on a special board-holder made for irradiation. The test board allowed to bias the devices in accordance with the electrical circuit provided in Figure 1. Two bias conditions were used so called Bias 1 and Bias 2.
Bias 1 corresponds to a gate stress of VGSS equals 12 Volts. Bias 2 corresponds to drain to source stress equals 80% of BVDSS.
During annealing steps the same stress conditions were applied at room and 100°C temperatures respectively.

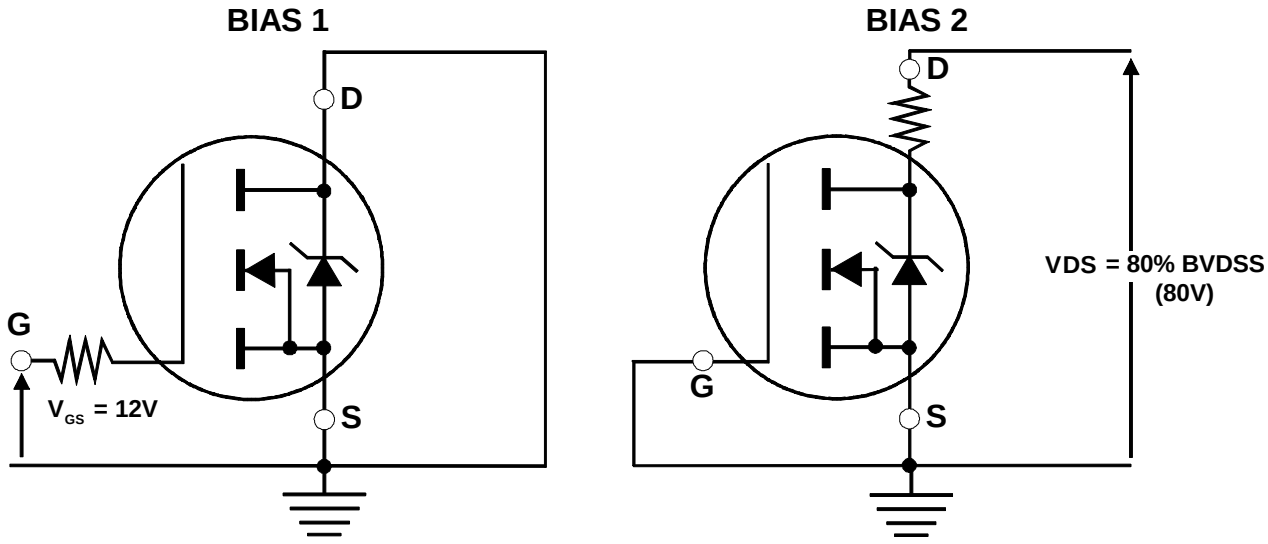


Figure 1 : Bias Conditions during Irradiation Exposures and Annealing

5.2.2 Electrical Measurements

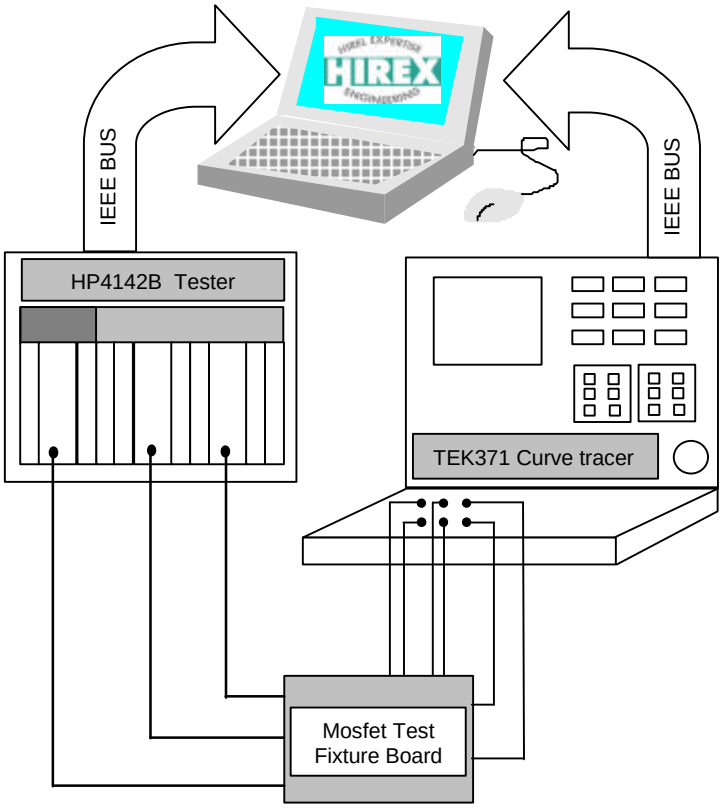
Mosfet transistor test program principle is provided in Figure 2. Due to the great number of samples to be measured (test campaign was conducted on 14 part types at the same time) and the time interval constraints required for performing measurements after each exposure and annealing step, It was decided to automate low power and high power measurements.

Two instruments were used to cover low power and high power measurements respectively.
HP4142B was used for breakdown voltage, gate and drain leakage currents, and threshold voltage measurements.
Tektronix TEK371 high power curve tracer was used for R_{DSON} measurements.

A dedicated test fixture was designed to ensure proper switching of instruments. In addition a faraday cup was used to ensure optimum conditions for low level measurements.

Test program has been written in Visual Basic on a PC computer. HPIB commands were sent to each instrument via IEEE bus, in order to measure a given parameter with specified conditions.
Results were automatically loaded in an Excel worksheet and compared in real time to specification limits. This allowed for real time data analysis in particular when failures were recorded.

Figure 2 : Mosfet transistor test program principle



Electrical parameters test conditions and limits used for performing this test are given in the following table.

Symbol	Test Parameter	Test Conditions	Min limit	Max limit	Unit
BVDSS	Drain to Source breakdown voltage	VGS=0V, ID=0.25mA	100		V
VGSTH	Gate to Source threshold voltage	VDS>=VGS, ID=0.25mA	2	4	V
+IGSS	Positive Gate Source leakage current	VGS=+20V, VDS=0V		100	nA
-IGSS	Negative Gate Source leakage current	VGS=-20V, VDS=0V		100	nA
IDSS	Drain current	VGS=0V, VDS=90V		1	µA
RDSON	Static drain to source on-state resistance	VGS=10V, ID=53A		0.028	Ohm

Table 1 : Measured electrical parameters

6 Test Summary

A Total Ionizing Dose assessment was carried out by Hirex Engineering under ESA contract on the HARRIS HUF75639P3 N-Channel Power Mosfet.
2 groups of 5 samples each plus one control sample were used during testing. The first group was exposed to radiation using Bias 1 conditions corresponding to a gate stress of the devices. The second group of 5 samples was exposed to radiation using Bias 2 conditions corresponding to drain to source stress of the devices, equals 80% of BVDSS (80 Volts).

Based on the analysis of the results, the tolerances of this component and main conclusion are provided below.

Parametric Tolerance Level (>=Krad) - Bias 1: 39.85 [1]

Parametric Tolerance Level (>=Krad) - Bias 2: 39.85 [1]

Parametric tolerance level represents the last cumulative exposure at which no samples failed any test

[1]: Last irradiation step

Main conclusion:

No failures were recorded up to the last exposure of 36.85 Krad(Si) and annealing steps.
Even if some drifts are recorded on threshold voltage and gate and drain to source leakage currents, these parameters remained always within specification limits.

This device has shown a fairly good resistance to radiation total dose induced effects.

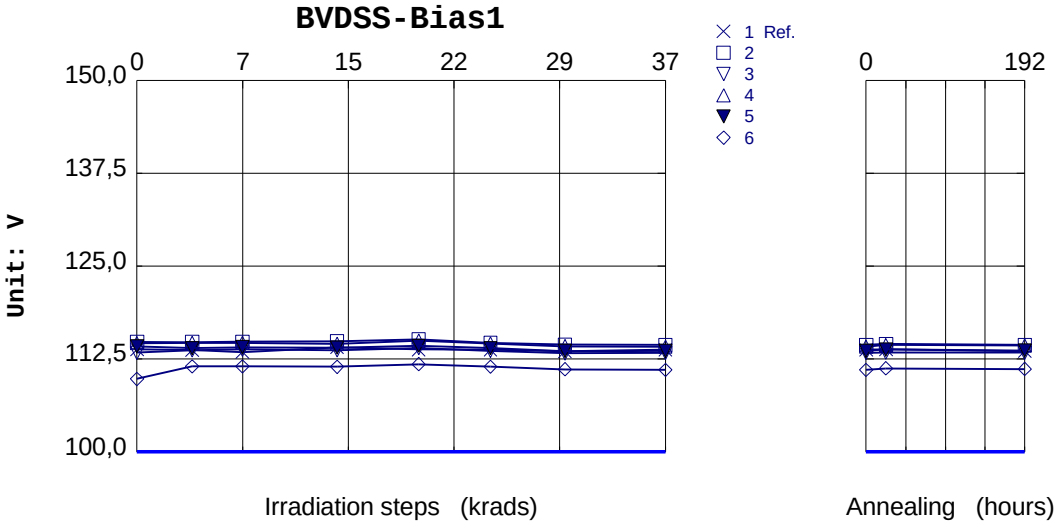
7 Test Results

Test results including tables and graphics are provided in this section for each measured parameter. To allow easy reading of data, each parameter is plotted twice, one for the first bias condition: Bias 1 and one for the second condition: Bias 2.

Parameter: Drain to source breakdown voltage: BVDSS-Bias1 **VGS=0V, ID=0.25mA**
Unit= V
Spec limit min: 100
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	1,138E +02	1,137E +02	1,134E +02	1,141E +02	1,138E +02	1,138E +02	1,135E +02
2	1,148E +02	1,148E +02	1,148E +02	1,149E +02	1,152E +02	1,147E +02	1,144E +02
3	1,133E +02	1,137E +02	1,138E +02	1,137E +02	1,140E +02	1,136E +02	1,133E +02
4	1,146E +02	1,147E +02	1,147E +02	1,145E +02	1,150E +02	1,146E +02	1,142E +02
5	1,142E +02	1,140E +02	1,141E +02	1,140E +02	1,143E +02	1,140E +02	1,136E +02
6	1,098E +02	1,115E +02	1,115E +02	1,114E +02	1,118E +02	1,115E +02	1,111E +02
Statistics							
Min	1,098E +02	1,115E +02	1,115E +02	1,114E +02	1,118E +02	1,115E +02	1,111E +02
Max	1,148E +02	1,148E +02	1,148E +02	1,149E +02	1,152E +02	1,147E +02	1,144E +02
Mean	1,133E +02	1,137E +02	1,138E +02	1,137E +02	1,140E +02	1,136E +02	1,133E +02
Sigma	2,063E +00	1,321E +00	1,335E +00	1,351E +00	1,340E +00	1,309E +00	1,316E +00

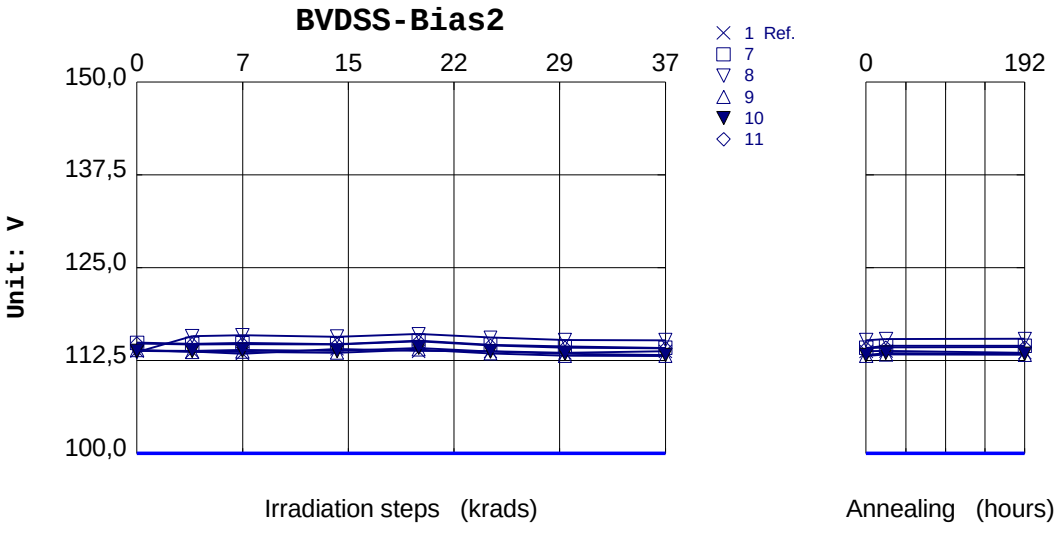
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	1,137E +02	1,138E +02	1,136E +02
2	1,144E +02	1,145E +02	1,144E +02
3	1,133E +02	1,134E +02	1,133E +02
4	1,141E +02	1,144E +02	1,143E +02
5	1,136E +02	1,138E +02	1,136E +02
6	1,110E +02	1,112E +02	1,112E +02
Statistics			
Min	1,110E +02	1,112E +02	1,112E +02
Max	1,144E +02	1,145E +02	1,144E +02
Mean	1,133E +02	1,135E +02	1,134E +02
Sigma	1,338E +00	1,325E +00	1,315E +00



Parameter: Drain to source breakdown voltage: BVDSS-Bias2 **VGS=0V, ID=0.25mA**
Unit= V
Spec limit min: 100
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	1,138E +02	1,137E +02	1,134E +02	1,141E +02	1,138E +02	1,138E +02	1,135E +02
7	1,149E +02	1,147E +02	1,149E +02	1,147E +02	1,152E +02	1,146E +02	1,144E +02
8	1,136E +02	1,158E +02	1,159E +02	1,157E +02	1,161E +02	1,156E +02	1,153E +02
9	1,139E +02	1,137E +02	1,137E +02	1,135E +02	1,140E +02	1,135E +02	1,131E +02
10	1,138E +02	1,138E +02	1,139E +02	1,138E +02	1,142E +02	1,137E +02	1,134E +02
11	1,148E +02	1,147E +02	1,147E +02	1,147E +02	1,151E +02	1,145E +02	1,142E +02
Statistics							
Min	1,136E +02	1,137E +02	1,137E +02	1,135E +02	1,140E +02	1,135E +02	1,131E +02
Max	1,149E +02	1,158E +02	1,159E +02	1,157E +02	1,161E +02	1,156E +02	1,153E +02
Mean	1,142E +02	1,145E +02	1,146E +02	1,145E +02	1,149E +02	1,144E +02	1,141E +02
Sigma	5,869E -01	8,540E -01	8,877E -01	8,671E -01	8,407E -01	8,412E -01	8,451E -01

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	1,137E +02	1,138E +02	1,136E +02
7	1,142E +02	1,145E +02	1,145E +02
8	1,152E +02	1,154E +02	1,154E +02
9	1,131E +02	1,133E +02	1,133E +02
10	1,132E +02	1,135E +02	1,134E +02
11	1,141E +02	1,143E +02	1,143E +02
Statistics			
Min	1,131E +02	1,133E +02	1,133E +02
Max	1,152E +02	1,154E +02	1,154E +02
Mean	1,140E +02	1,142E +02	1,142E +02
Sigma	8,653E -01	8,325E -01	8,799E -01

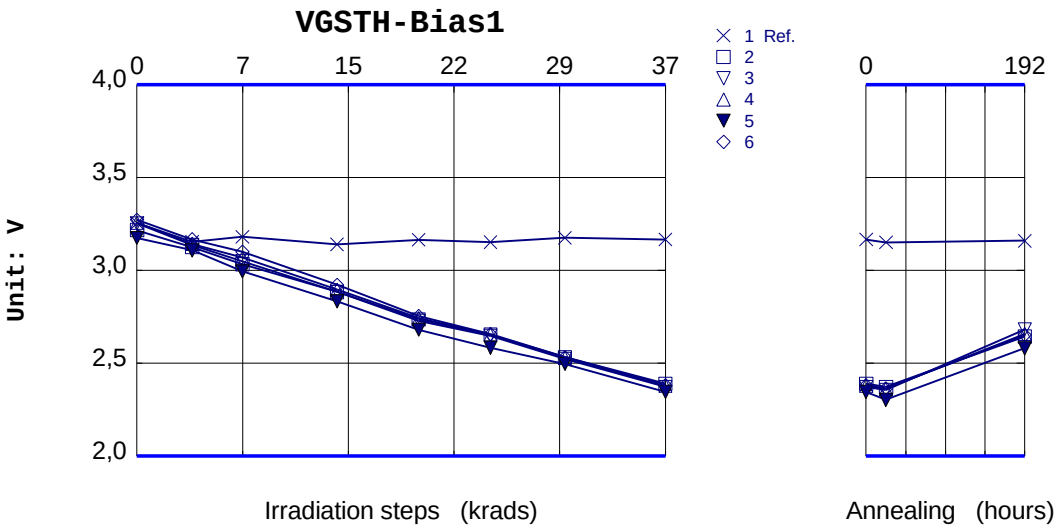


Parameter: Gate to source threshold voltage: VGSTH-Bias1 **VDS>=VGS, ID=0.25mA**

Unit= V
Spec limit max: 4
Spec limit min: 2
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	3,255E +00	3,154E +00	3,180E +00	3,140E +00	3,164E +00	3,152E +00	3,175E +00
2	3,216E +00	3,124E +00	3,032E +00	2,883E +00	2,736E +00	2,653E +00	2,533E +00
3	3,252E +00	3,136E +00	3,049E +00	2,883E +00	2,728E +00	2,647E +00	2,523E +00
4	3,257E +00	3,142E +00	3,068E +00	2,896E +00	2,742E +00	2,655E +00	2,529E +00
5	3,174E +00	3,107E +00	2,994E +00	2,833E +00	2,680E +00	2,583E +00	2,496E +00
6	3,272E +00	3,166E +00	3,100E +00	2,921E +00	2,754E +00	2,657E +00	2,532E +00
Statistics							
Min	3,174E +00	3,107E +00	2,994E +00	2,833E +00	2,680E +00	2,583E +00	2,496E +00
Max	3,272E +00	3,166E +00	3,100E +00	2,921E +00	2,754E +00	2,657E +00	2,533E +00
Mean	3,234E +00	3,135E +00	3,049E +00	2,883E +00	2,728E +00	2,639E +00	2,522E +00
Sigma	3,949E -02	2,188E -02	3,943E -02	3,221E -02	2,840E -02	3,138E -02	1,545E -02

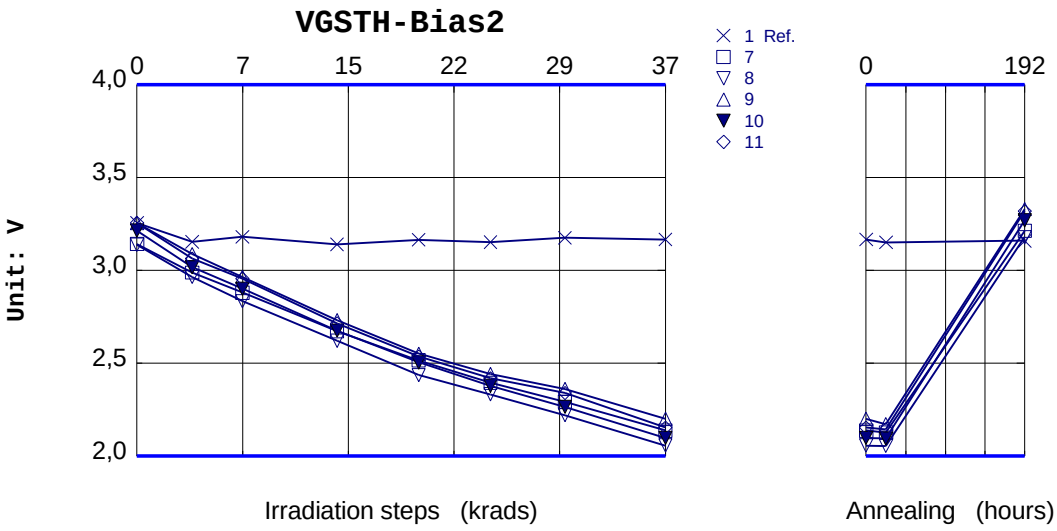
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	3,166E +00	3,150E +00	3,159E +00
2	2,390E +00	2,372E +00	2,643E +00
3	2,372E +00	2,356E +00	2,682E +00
4	2,379E +00	2,362E +00	2,657E +00
5	2,345E +00	2,302E +00	2,580E +00
6	2,380E +00	2,364E +00	2,651E +00
Statistics			
Min	2,345E +00	2,302E +00	2,580E +00
Max	2,390E +00	2,372E +00	2,682E +00
Mean	2,373E +00	2,351E +00	2,643E +00
Sigma	1,694E -02	2,793E -02	3,783E -02



Parameter: Gate to source threshold voltage: VGSTH-Bias2 **VDS>=VGS,ID=0.25mA**
Unit= V
Spec limit max: 4
Spec limit min: 2
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	3,255E +00	3,154E +00	3,180E +00	3,140E +00	3,164E +00	3,152E +00	3,175E +00
7	3,142E +00	2,988E +00	2,880E +00	2,672E +00	2,515E +00	2,395E +00	2,292E +00
8	3,137E +00	2,964E +00	2,834E +00	2,621E +00	2,436E +00	2,332E +00	2,219E +00
9	3,255E +00	3,087E +00	2,964E +00	2,731E +00	2,551E +00	2,441E +00	2,360E +00
10	3,213E +00	3,017E +00	2,901E +00	2,675E +00	2,504E +00	2,378E +00	2,264E +00
11	3,255E +00	3,063E +00	2,955E +00	2,714E +00	2,535E +00	2,418E +00	2,339E +00
Statistics							
Min	3,137E +00	2,964E +00	2,833E +00	2,621E +00	2,436E +00	2,332E +00	2,219E +00
Max	3,255E +00	3,087E +00	2,964E +00	2,731E +00	2,551E +00	2,441E +00	2,360E +00
Mean	3,201E +00	3,024E +00	2,907E +00	2,683E +00	2,508E +00	2,393E +00	2,295E +00
Sigma	5,822E -02	5,126E -02	5,418E -02	4,262E -02	4,432E -02	4,155E -02	5,679E -02

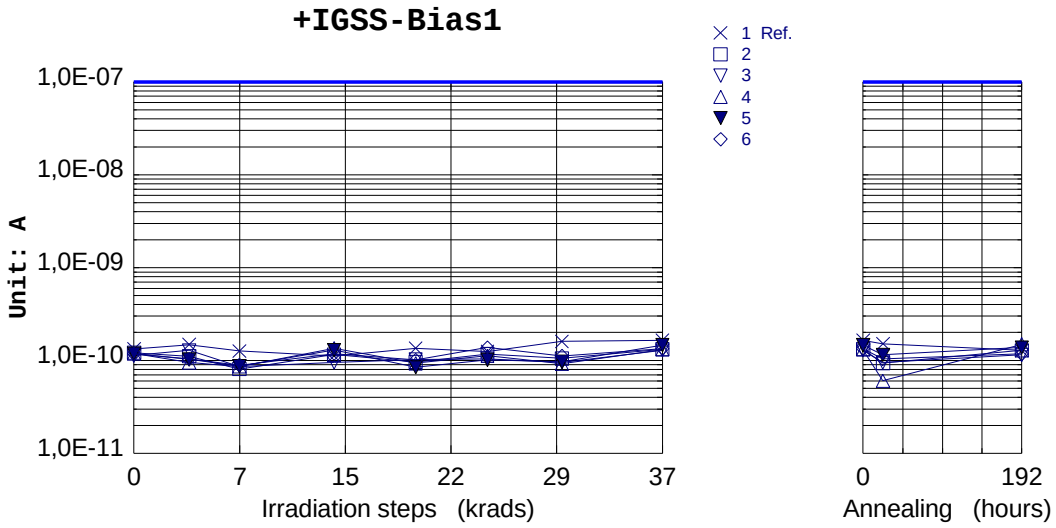
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	3,166E +00	3,150E +00	3,159E +00
7	2,137E +00	2,127E +00	3,212E +00
8	2,057E +00	2,054E +00	3,178E +00
9	2,201E +00	2,171E +00	3,330E +00
10	2,098E +00	2,094E +00	3,269E +00
11	2,153E +00	2,144E +00	3,318E +00
Statistics			
Min	2,057E +00	2,054E +00	3,178E +00
Max	2,201E +00	2,171E +00	3,330E +00
Mean	2,129E +00	2,118E +00	3,261E +00
Sigma	5,495E -02	4,510E -02	6,571E -02



Parameter: Positive Gate source leakage current: +IGSS-Bias1 **VGS=+10V, VDS=0V**
Unit= A
Spec limit max: 100E-9
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	1,337E -10	1,485E -10	1,267E -10	1,119E -10	1,356E -10	1,253E -10	1,603E -10
2	1,213E -10	1,114E -10	8,106E -11	1,156E -10	9,638E -11	1,172E -10	1,052E -10
3	1,132E -10	1,288E -10	8,660E -11	9,554E -11	1,025E -10	1,040E -10	9,576E -11
4	1,192E -10	9,552E -11	8,664E -11	1,353E -10	9,330E -11	1,126E -10	9,260E -11
5	1,183E -10	1,028E -10	8,678E -11	1,296E -10	8,450E -11	1,018E -10	9,692E -11
6	1,182E -10	1,038E -10	8,922E -11	1,188E -10	1,017E -10	1,385E -10	1,120E -10
Statistics							
Min	1,132E -10	9,552E -11	8,106E -11	9,554E -11	8,450E -11	1,018E -10	9,260E -11
Max	1,213E -10	1,288E -10	8,922E -11	1,353E -10	1,025E -10	1,385E -10	1,120E -10
Mean	1,181E -10	1,085E -10	8,606E -11	1,190E -10	9,567E -11	1,148E -10	1,005E -10
Sigma	2,969E -12	1,269E -11	3,005E -12	1,533E -11	7,309E -12	1,461E -11	7,942E -12

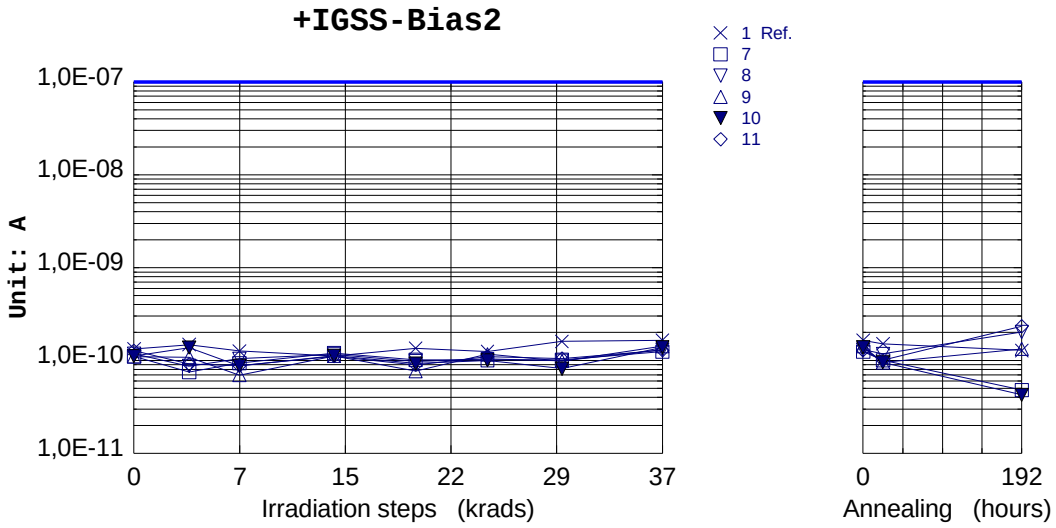
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	1,651E -10	1,513E -10	1,283E -10
2	1,324E -10	9,368E -11	1,285E -10
3	1,288E -10	9,536E -11	1,149E -10
4	1,320E -10	6,058E -11	1,497E -10
5	1,465E -10	1,150E -10	1,382E -10
6	1,344E -10	1,038E -10	1,174E -10
Statistics			
Min	1,288E -10	6,058E -11	1,149E -10
Max	1,465E -10	1,150E -10	1,497E -10
Mean	1,348E -10	9,368E -11	1,297E -10
Sigma	6,811E -12	2,035E -11	1,451E -11



Parameter: Positive Gate source leakage current: +IGSS-Bias2 **VGS=+10V, VDS=0V**
Unit= A
Spec limit max: 100E-9
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	1,337E -10	1,485E -10	1,267E -10	1,119E -10	1,356E -10	1,253E -10	1,603E -10
7	1,107E -10	7,516E -11	9,376E -11	1,201E -10	1,018E -10	1,014E -10	1,019E -10
8	1,181E -10	8,726E -11	1,043E -10	1,162E -10	9,822E -11	1,035E -10	9,924E -11
9	1,106E -10	1,084E -10	6,984E -11	1,120E -10	7,698E -11	1,166E -10	9,870E -11
10	1,115E -10	1,379E -10	8,730E -11	1,128E -10	9,266E -11	1,000E -10	8,172E -11
11	1,279E -10	9,130E -11	8,798E -11	1,113E -10	8,970E -11	1,102E -10	1,048E -10
Statistics							
Min	1,106E -10	7,516E -11	6,984E -11	1,113E -10	7,698E -11	1,000E -10	8,172E -11
Max	1,279E -10	1,379E -10	1,043E -10	1,201E -10	1,018E -10	1,166E -10	1,048E -10
Mean	1,157E -10	1,000E -10	8,864E -11	1,145E -10	9,188E -11	1,063E -10	9,728E -11
Sigma	7,474E -12	2,430E -11	1,252E -11	3,681E -12	9,570E -12	6,937E -12	9,032E -12

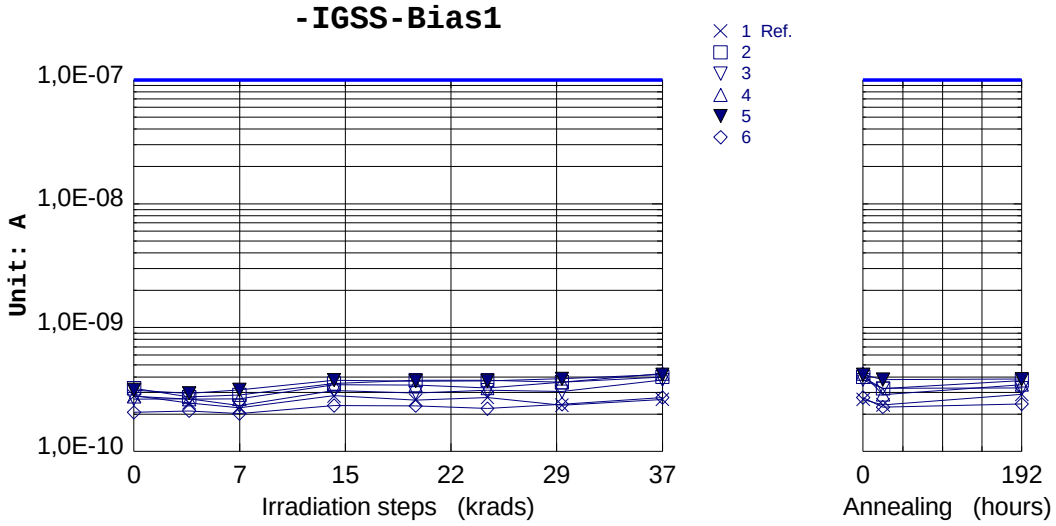
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	1,651E -10	1,513E -10	1,283E -10
7	1,246E -10	1,008E -10	4,814E -11
8	1,310E -10	1,178E -10	2,028E -10
9	1,427E -10	9,530E -11	1,334E -10
10	1,389E -10	9,568E -11	4,272E -11
11	1,285E -10	1,006E -10	2,334E -10
Statistics			
Min	1,246E -10	9,530E -11	4,272E -11
Max	1,427E -10	1,178E -10	2,334E -10
Mean	1,331E -10	1,020E -10	1,321E -10
Sigma	7,496E -12	9,173E -12	8,704E -11



Parameter: Negative Gate source leakage current: -IGSS-Bias1 **VGS=-10V, VDS=0V**
Unit= A
Spec limit max: 100E-9
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,808E -10	2,461E -10	2,251E -10	2,808E -10	2,590E -10	2,729E -10	2,362E -10
2	3,241E -10	2,750E -10	2,864E -10	3,538E -10	3,757E -10	3,753E -10	3,618E -10
3	2,651E -10	2,665E -10	2,339E -10	3,104E -10	2,957E -10	3,121E -10	3,040E -10
4	2,781E -10	2,644E -10	2,657E -10	3,464E -10	3,432E -10	3,247E -10	3,617E -10
5	3,132E -10	2,940E -10	3,137E -10	3,756E -10	3,700E -10	3,705E -10	3,865E -10
6	2,067E -10	2,127E -10	2,023E -10	2,349E -10	2,338E -10	2,213E -10	2,399E -10
Statistics							
Min	2,067E -10	2,127E -10	2,023E -10	2,349E -10	2,338E -10	2,213E -10	2,399E -10
Max	3,241E -10	2,940E -10	3,137E -10	3,756E -10	3,757E -10	3,753E -10	3,865E -10
Mean	2,774E -10	2,625E -10	2,604E -10	3,242E -10	3,237E -10	3,208E -10	3,308E -10
Sigma	4,642E -11	3,021E -11	4,364E -11	5,520E -11	5,937E -11	6,211E -11	5,915E -11

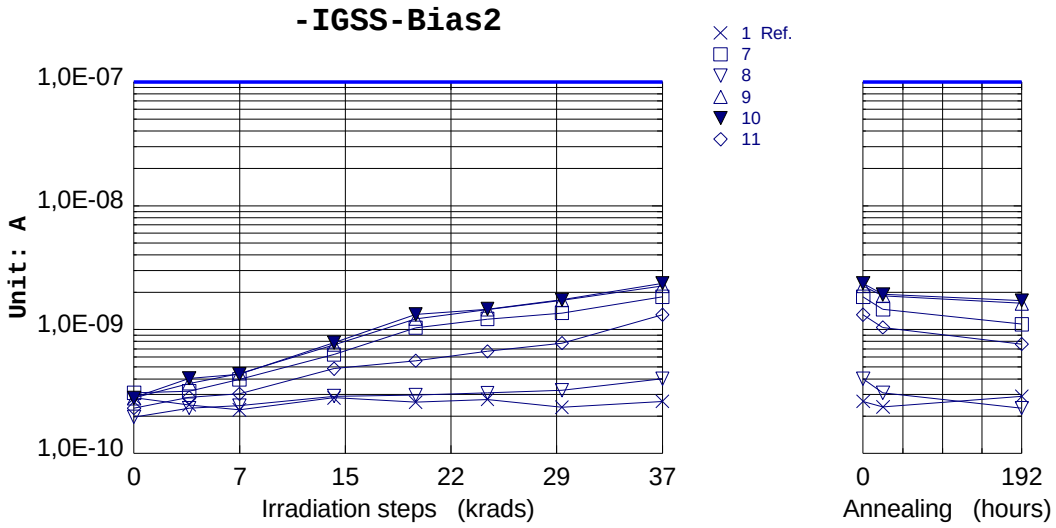
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	2,634E -10	2,377E -10	2,887E -10
2	3,993E -10	3,219E -10	3,742E -10
3	3,775E -10	3,229E -10	3,244E -10
4	4,257E -10	2,878E -10	3,463E -10
5	4,162E -10	3,802E -10	3,843E -10
6	2,716E -10	2,280E -10	2,410E -10
Statistics			
Min	2,716E -10	2,280E -10	2,410E -10
Max	4,257E -10	3,802E -10	3,843E -10
Mean	3,781E -10	3,081E -10	3,340E -10
Sigma	6,227E -11	5,576E -11	5,710E -11



Parameter: Negative Gate source leakage current: -IGSS-Bias2 VGS=-10V, VDS=0V
Unit= A
Spec limit max: 100E-9
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,808E -10	2,461E -10	2,251E -10	2,808E -10	2,590E -10	2,729E -10	2,362E -10
7	3,088E -10	3,174E -10	3,960E -10	6,281E -10	1,034E -09	1,217E -09	1,358E -09
8	1,969E -10	2,319E -10	2,428E -10	2,898E -10	2,961E -10	3,075E -10	3,242E -10
9	2,793E -10	3,678E -10	4,412E -10	7,551E -10	1,225E -09	1,452E -09	1,725E -09
10	2,810E -10	4,035E -10	4,350E -10	7,860E -10	1,326E -09	1,461E -09	1,743E -09
11	2,319E -10	2,831E -10	3,026E -10	4,833E -10	5,599E -10	6,674E -10	7,778E -10
Statistics							
Min	1,969E -10	2,319E -10	2,428E -10	2,898E -10	2,961E -10	3,075E -10	3,242E -10
Max	3,088E -10	4,035E -10	4,412E -10	7,860E -10	1,326E -09	1,461E -09	1,743E -09
Mean	2,596E -10	3,207E -10	3,635E -10	5,885E -10	8,881E -10	1,021E -09	1,185E -09
Sigma	4,463E -11	6,783E -11	8,730E -11	2,053E -10	4,428E -10	5,128E -10	6,203E -10

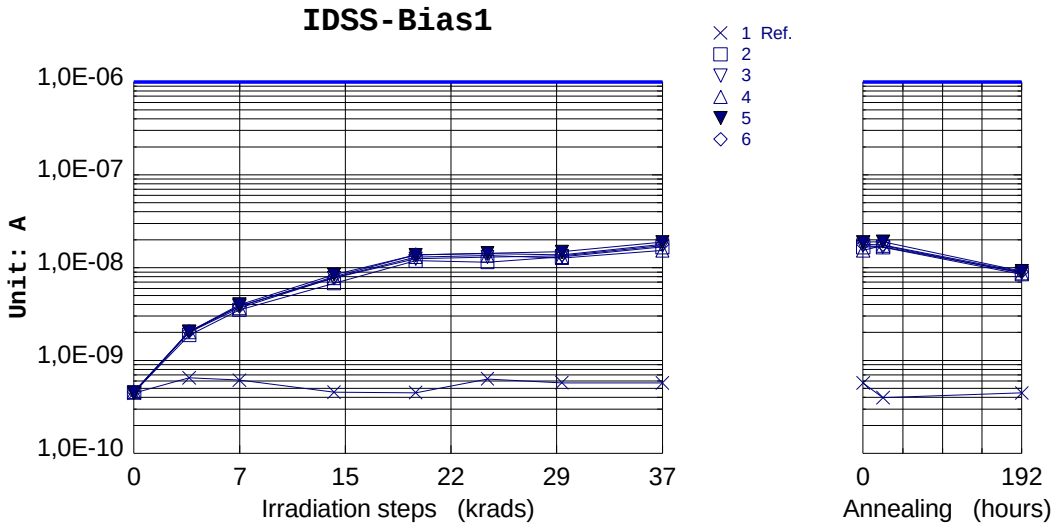
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	2,634E -10	2,377E -10	2,887E -10
7	1,837E -09	1,457E -09	1,104E -09
8	4,005E -10	3,087E -10	2,321E -10
9	2,254E -09	1,871E -09	1,626E -09
10	2,362E -09	1,919E -09	1,713E -09
11	1,319E -09	1,040E -09	7,629E -10
Statistics			
Min	4,005E -10	3,087E -10	2,321E -10
Max	2,362E -09	1,919E -09	1,713E -09
Mean	1,634E -09	1,319E -09	1,087E -09
Sigma	8,025E -10	6,675E -10	6,161E -10



Parameter: Drain current: IDSS-Bias1 VGS=0V, VDS=90V
Unit= A
Spec limit max: 1E-6
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	4,440E -10	6,499E -10	6,140E -10	4,565E -10	4,516E -10	6,351E -10	5,765E -10
2	4,532E -10	1,879E -09	3,508E -09	6,787E -09	1,189E -08	1,149E -08	1,313E -08
3	4,512E -10	2,033E -09	3,853E -09	7,724E -09	1,247E -08	1,302E -08	1,333E -08
4	4,599E -10	2,017E -09	3,675E -09	7,785E -09	1,297E -08	1,348E -08	1,272E -08
5	4,492E -10	2,051E -09	3,995E -09	8,385E -09	1,365E -08	1,431E -08	1,479E -08
6	4,600E -10	2,063E -09	3,842E -09	7,980E -09	1,381E -08	1,415E -08	1,371E -08
Statistics							
Min	4,492E -10	1,879E -09	3,508E -09	6,787E -09	1,189E -08	1,149E -08	1,272E -08
Max	4,600E -10	2,063E -09	3,995E -09	8,385E -09	1,381E -08	1,431E -08	1,479E -08
Mean	4,547E -10	2,009E -09	3,775E -09	7,732E -09	1,296E -08	1,329E -08	1,354E -08
Sigma	5,006E -12	7,451E -11	1,872E -10	5,881E -10	8,029E -10	1,132E -09	7,841E -10

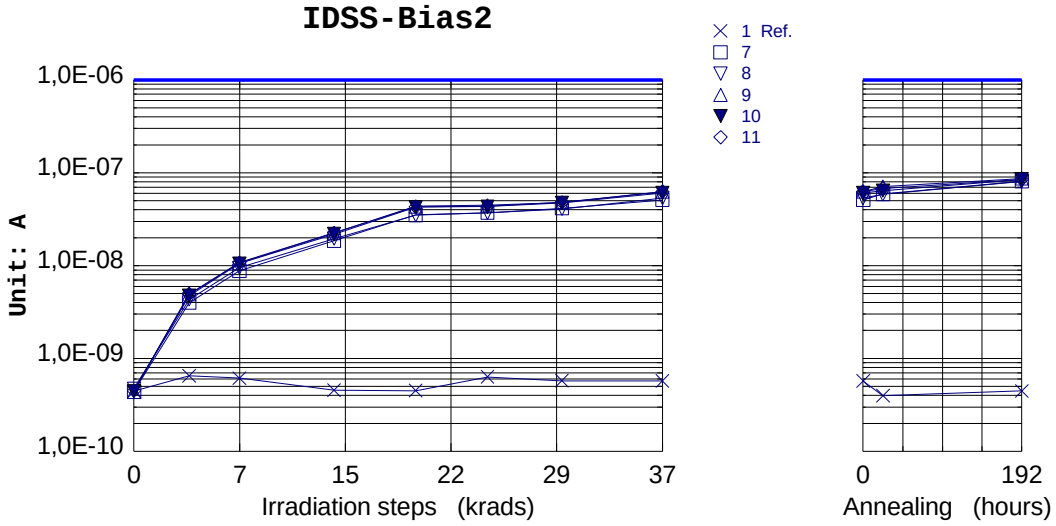
Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	5,731E -10	3,989E -10	4,469E -10
2	1,664E -08	1,657E -08	8,479E -09
3	1,726E -08	1,673E -08	8,825E -09
4	1,530E -08	1,729E -08	8,716E -09
5	1,874E -08	1,904E -08	9,192E -09
6	1,788E -08	1,761E -08	9,056E -09
Statistics			
Min	1,530E -08	1,657E -08	8,479E -09
Max	1,874E -08	1,904E -08	9,192E -09
Mean	1,716E -08	1,745E -08	8,854E -09
Sigma	1,299E -09	9,815E -10	2,809E -10



Parameter: Drain current: IDSS-Bias2 VGS=0V, VDS=90V
Unit= A
Spec limit max: 1E-6
Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	4,440E -10	6,499E -10	6,140E -10	4,565E -10	4,516E -10	6,351E -10	5,765E -10
7	4,396E -10	3,990E -09	8,810E -09	1,849E -08	3,513E -08	3,701E -08	4,137E -08
8	4,733E -10	4,318E -09	9,516E -09	1,947E -08	3,495E -08	3,694E -08	4,080E -08
9	4,398E -10	4,916E -09	1,064E -08	2,245E -08	4,350E -08	4,465E -08	4,779E -08
10	4,433E -10	4,734E -09	1,056E -08	2,184E -08	4,259E -08	4,318E -08	4,747E -08
11	4,512E -10	4,944E -09	1,079E -08	2,261E -08	4,286E -08	4,370E -08	4,793E -08
Statistics							
Min	4,396E -10	3,990E -09	8,810E -09	1,849E -08	3,495E -08	3,694E -08	4,080E -08
Max	4,733E -10	4,944E -09	1,079E -08	2,261E -08	4,350E -08	4,465E -08	4,793E -08
Mean	4,494E -10	4,580E -09	1,006E -08	2,097E -08	3,981E -08	4,110E -08	4,507E -08
Sigma	1,416E -11	4,139E -10	8,622E -10	1,872E -09	4,364E -09	3,800E -09	3,650E -09

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	5,731E -10	3,989E -10	4,469E -10
7	5,105E -08	5,911E -08	8,131E -08
8	5,322E -08	5,857E -08	8,058E -08
9	6,258E -08	7,108E -08	8,691E -08
10	6,051E -08	6,402E -08	8,496E -08
11	6,283E -08	6,755E -08	8,480E -08
Statistics			
Min	5,105E -08	5,857E -08	8,058E -08
Max	6,283E -08	7,108E -08	8,691E -08
Mean	5,803E -08	6,407E -08	8,371E -08
Sigma	5,517E -09	5,385E -09	2,672E -09



Parameter: Static drain to source on-state resistance: RDSON-Bias1 **VGS=10V, ID=53A**

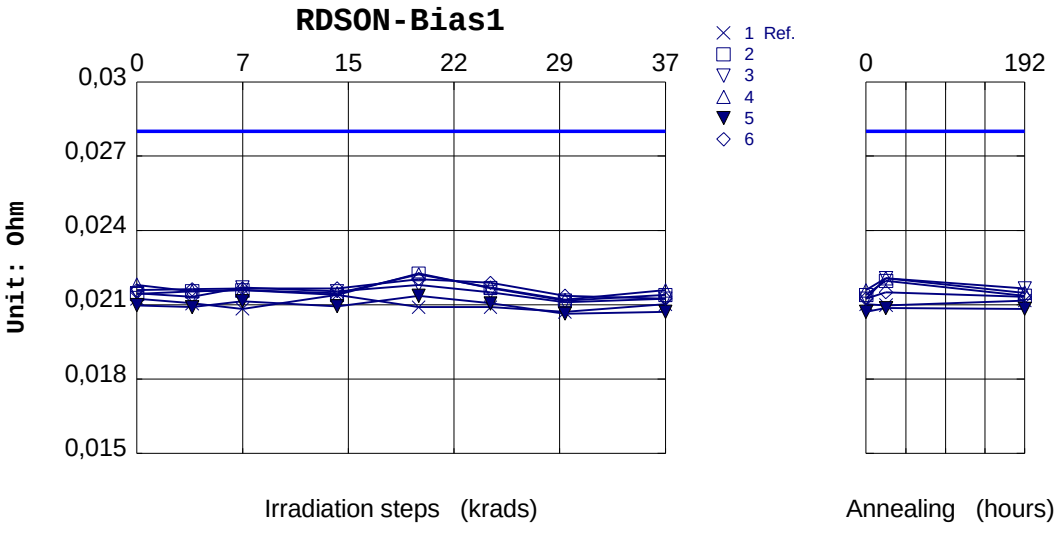
Unit= Ohm

Spec limit max: 0.028

Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,125E -02	2,106E -02	2,083E -02	2,140E -02	2,091E -02	2,091E -02	2,072E -02
2	2,143E -02	2,155E -02	2,158E -02	2,140E -02	2,226E -02	2,168E -02	2,117E -02
3	2,147E -02	2,132E -02	2,170E -02	2,155E -02	2,181E -02	2,151E -02	2,109E -02
4	2,181E -02	2,155E -02	2,158E -02	2,147E -02	2,223E -02	2,170E -02	2,121E -02
5	2,098E -02	2,091E -02	2,114E -02	2,094E -02	2,136E -02	2,106E -02	2,064E -02
6	2,158E -02	2,162E -02	2,166E -02	2,166E -02	2,204E -02	2,189E -02	2,136E -02
Statistics							
Min	2,098E -02	2,091E -02	2,114E -02	2,094E -02	2,136E -02	2,106E -02	2,064E -02
Max	2,181E -02	2,162E -02	2,170E -02	2,166E -02	2,226E -02	2,189E -02	2,136E -02
Mean	2,146E -02	2,139E -02	2,153E -02	2,140E -02	2,194E -02	2,157E -02	2,109E -02
Sigma	3,038E -04	2,928E -04	2,242E -04	2,752E -04	3,713E -04	3,143E -04	2,708E -04

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	2,102E -02	2,098E -02	2,117E -02
2	2,140E -02	2,196E -02	2,136E -02
3	2,125E -02	2,208E -02	2,166E -02
4	2,158E -02	2,208E -02	2,149E -02
5	2,072E -02	2,087E -02	2,083E -02
6	2,125E -02	2,151E -02	2,132E -02
Statistics			
Min	2,072E -02	2,087E -02	2,083E -02
Max	2,158E -02	2,208E -02	2,166E -02
Mean	2,124E -02	2,170E -02	2,133E -02
Sigma	3,229E -04	5,195E -04	3,099E -04



Parameter: Static drain to source on-state resistance: RDSON-Bias2 **VGS=10V, ID=53A**

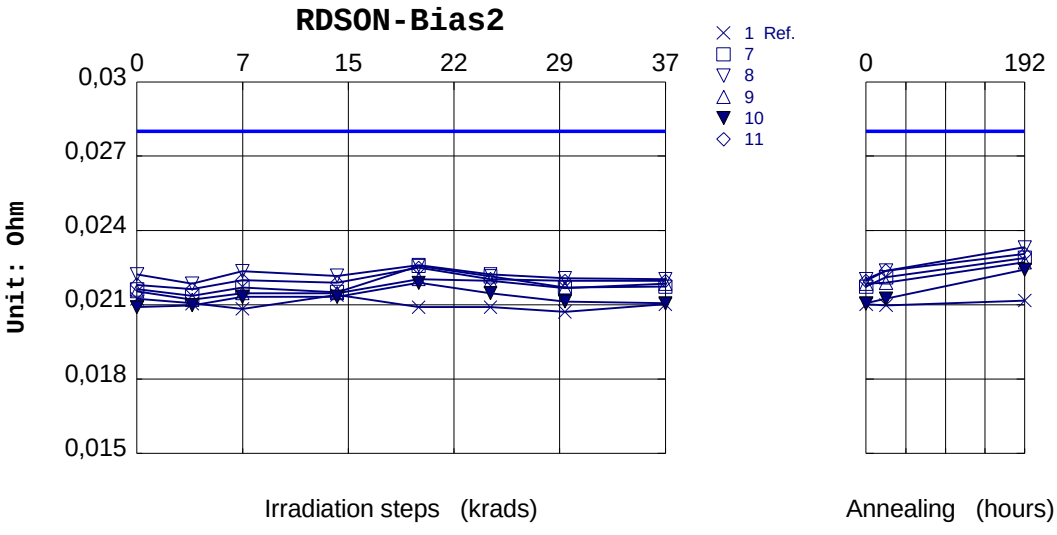
Unit= Ohm

Spec limit max: 0.028

Spec limits are represented in bold lines on the graphic.

Test Step	Initial	3,85 krads	7,35 krads	13,95 krads	19,65 krads	24,65 krads	29,85 krads
Serial #							
1 Ref.	2,125E -02	2,106E -02	2,083E -02	2,140E -02	2,091E -02	2,091E -02	2,072E -02
7	2,162E -02	2,136E -02	2,170E -02	2,151E -02	2,257E -02	2,215E -02	2,170E -02
8	2,223E -02	2,185E -02	2,236E -02	2,217E -02	2,260E -02	2,223E -02	2,208E -02
9	2,155E -02	2,121E -02	2,147E -02	2,147E -02	2,204E -02	2,196E -02	2,168E -02
10	2,091E -02	2,098E -02	2,132E -02	2,132E -02	2,189E -02	2,147E -02	2,113E -02
11	2,181E -02	2,162E -02	2,200E -02	2,189E -02	2,249E -02	2,204E -02	2,196E -02
Statistics							
Min	2,091E -02	2,098E -02	2,132E -02	2,132E -02	2,189E -02	2,147E -02	2,113E -02
Max	2,223E -02	2,185E -02	2,236E -02	2,217E -02	2,260E -02	2,223E -02	2,208E -02
Mean	2,162E -02	2,140E -02	2,177E -02	2,167E -02	2,232E -02	2,197E -02	2,171E -02
Sigma	4,796E -04	3,411E -04	4,181E -04	3,484E -04	3,307E -04	2,964E -04	3,649E -04

Test Step	36,85 krads	24 hours	192 hours
Serial #			
1 Ref.	2,102E -02	2,098E -02	2,117E -02
7	2,174E -02	2,211E -02	2,290E -02
8	2,204E -02	2,238E -02	2,332E -02
9	2,185E -02	2,189E -02	2,272E -02
10	2,106E -02	2,125E -02	2,242E -02
11	2,196E -02	2,238E -02	2,306E -02
Statistics			
Min	2,106E -02	2,125E -02	2,242E -02
Max	2,204E -02	2,238E -02	2,332E -02
Mean	2,173E -02	2,200E -02	2,288E -02
Sigma	3,925E -04	4,690E -04	3,422E -04



8 Conclusion

A total dose radiation verification test has been performed on HUF75639P3 N-Channel Power Mosfet from Harris Semiconductors up to 36.85 Krad(Si) accumulated dose.

No failures were recorded up to the last exposure of 36.85 Krad(Si) and annealing steps.
Even if some drifts are recorded on threshold voltage and gate and drain to source leakage currents, these parameters remained always within specification limits.

This device has shown a fairly good resistance to radiation total dose induced effects.

ANNEX 1 : HUF75639P3 DATA SHEET

53A, 100V, 0.028 Ohm, N-Channel UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75639.

Ordering Information

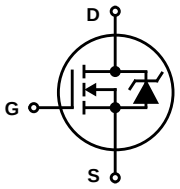
PART NUMBER	PACKAGE	BRAND
HUF75639G3	TO-247	75639G
HUF75639P3	TO-220AB	75639P
HUF75639S3	TO-262AA	75639S
HUF75639S3S	TO-263AB	75639S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75639S3ST.

Features

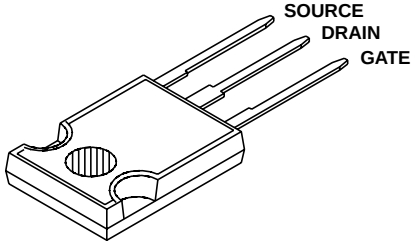
- 53A, 100V
- *Ultra Low On-Resistance*, $r_{DS(ON)} = 0.028\Omega$
- Diode Exhibits Both High Speed and Soft Recovery
- *Temperature Compensating* PSPICE Model
- *Thermal Impedance* SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

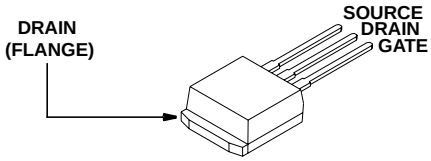


Packaging

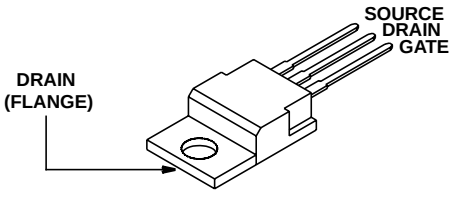
JEDEC STYLE TO-247



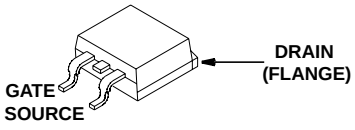
JEDEC TO-262AA



JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

Drain to Source Voltage (Note1)	V_{DSS}	100	V
Drain to Gate Voltage (R_{GS} = 20KΩ) (Note 1)	V_{DGR}	100	V
Gate to Source Voltage	V_{GS}	20	V
Drain Current			
Continuous (Figure 2)	I_D	53	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15	
Power Dissipation	P_D	200	W
Derate Above 25^oC		1.33	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure11)		100	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure10)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 90V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 80V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = 20V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 53A, V_{GS} = 10V (Figure 9)		-	0.023	0.028	Ω
Turn-On Time	t_{ON}	V_{DD} = 50V, $I_D \cong 53$, R_L = 0 .943Ω, V_{GS} = 10V, R_{GS} = 5.1Ω		-	-	110	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	60	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	ns
Fall Time	t_f			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	70	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 50V, $I_D \cong$ 53A, R_L =0 .943Ω $I_{g(REF)}$ = 1.0mA (Figures 13, 16, 17)	-	110	130	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	57	75	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	3.7	4.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure12)		-	2000	-	pF
Output Capacitance	C_{OSS}			-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	65	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.75	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^oC/W$
		TO-220, TO-262, and TO-263		-	-	62	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 53A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 53A, dI_{SD}/dt = 100A/μs	-	-	110	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 53A, dI_{SD}/dt = 100A/μs	-	-	320	nC

Typical Performance Curves

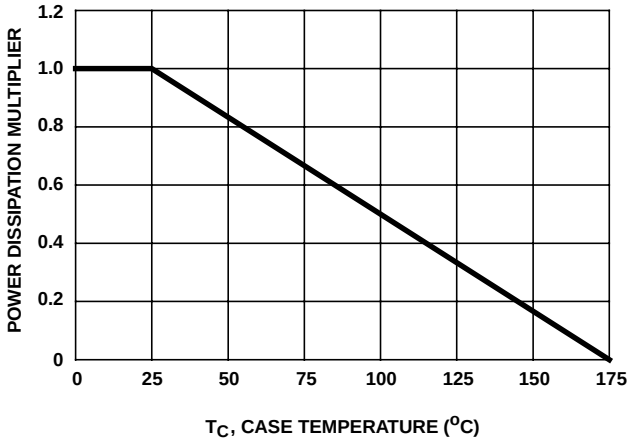


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

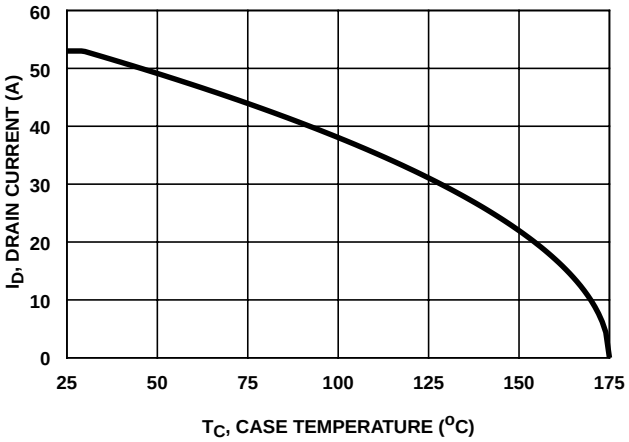


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

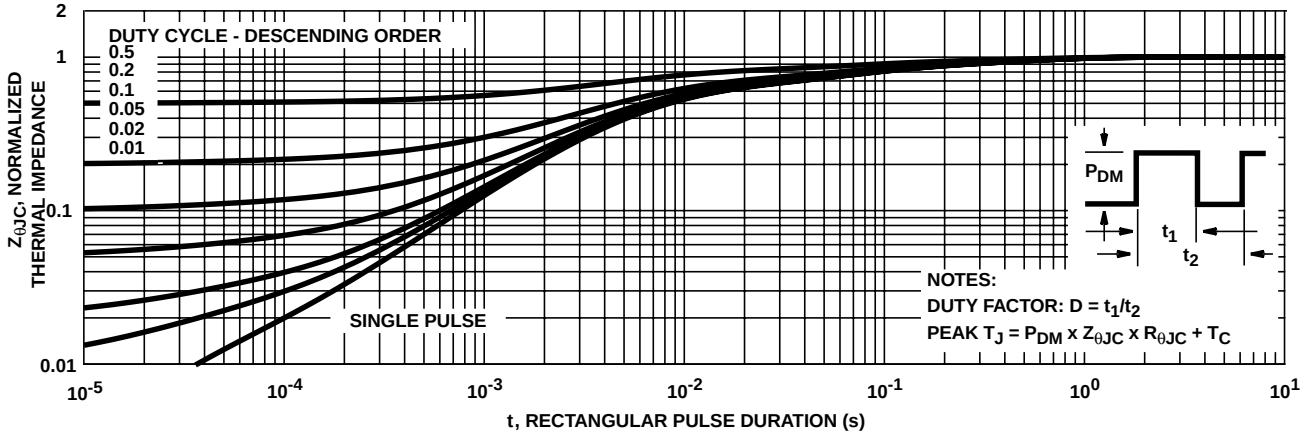


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

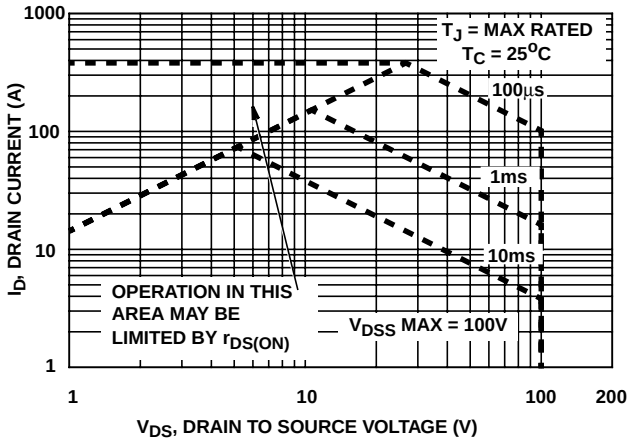


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

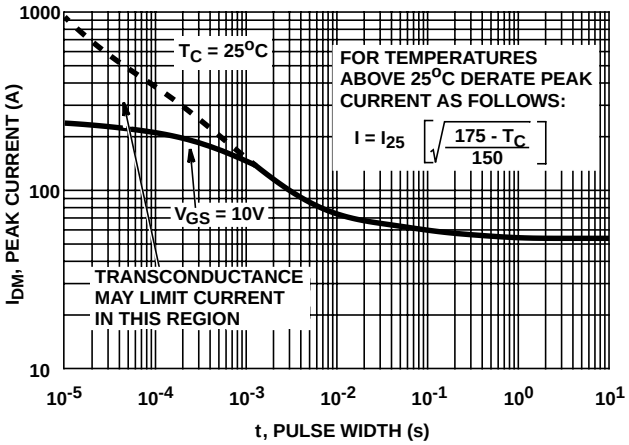
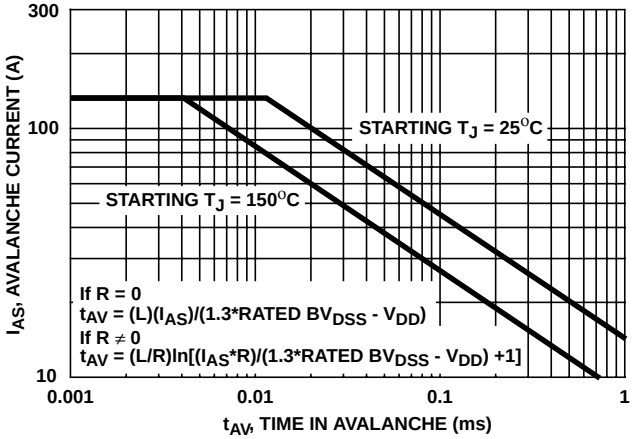


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

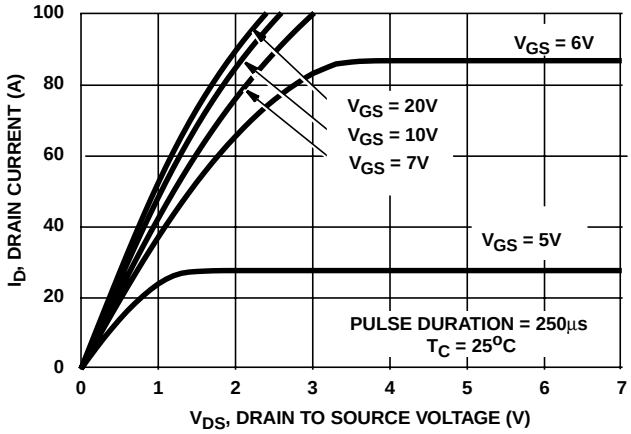


FIGURE 7. SATURATION CHARACTERISTICS

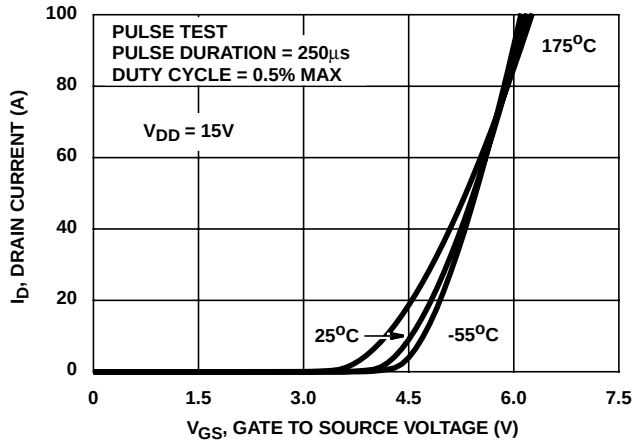


FIGURE 8. TRANSFER CHARACTERISTICS

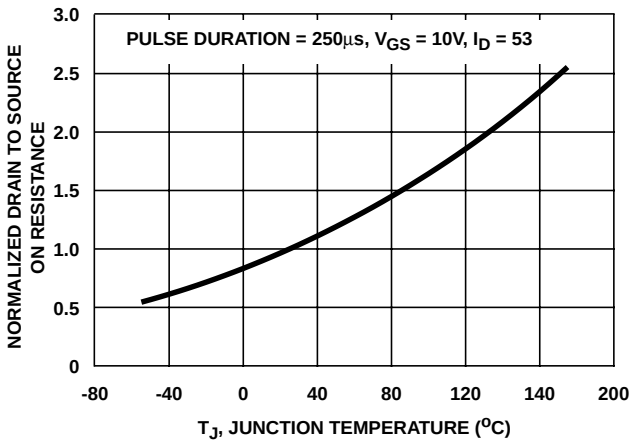


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

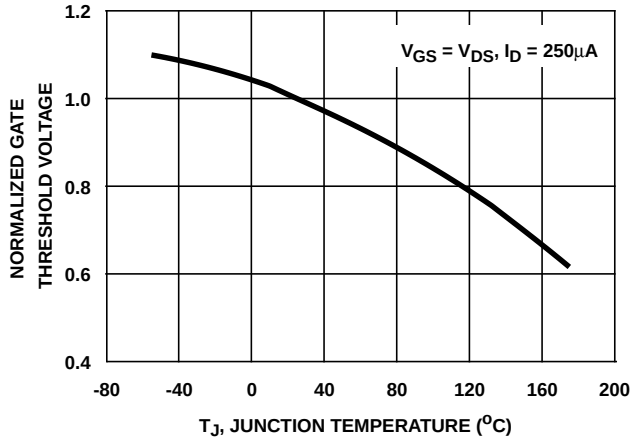


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

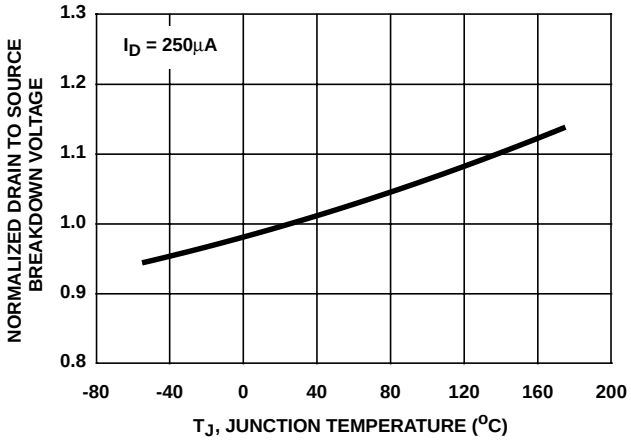


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

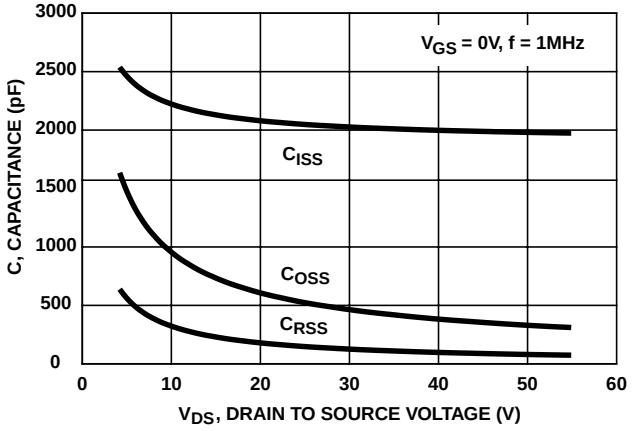
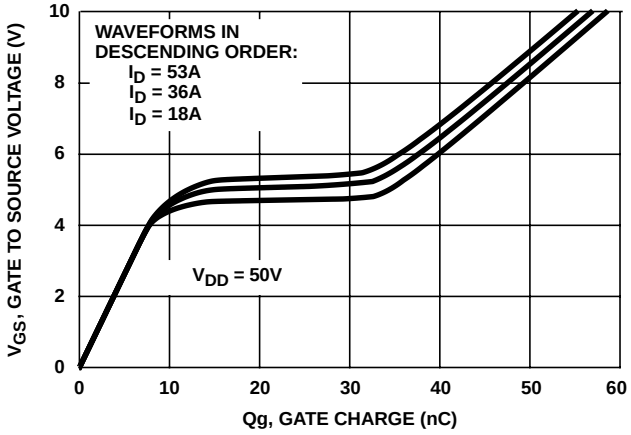


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

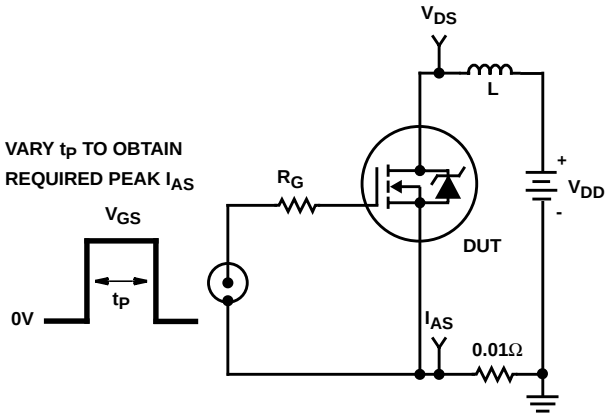


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

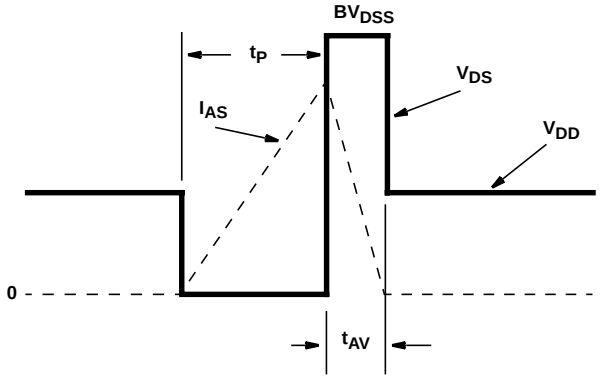


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

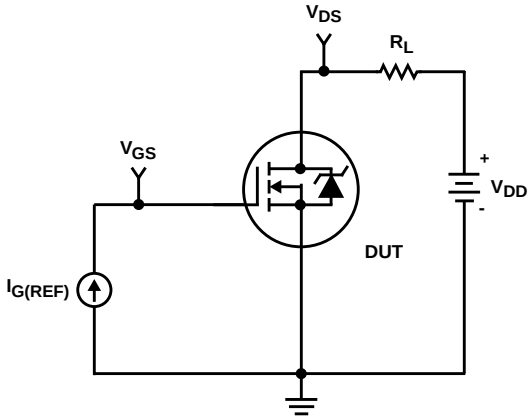


FIGURE 16. GATE CHARGE TEST CIRCUIT

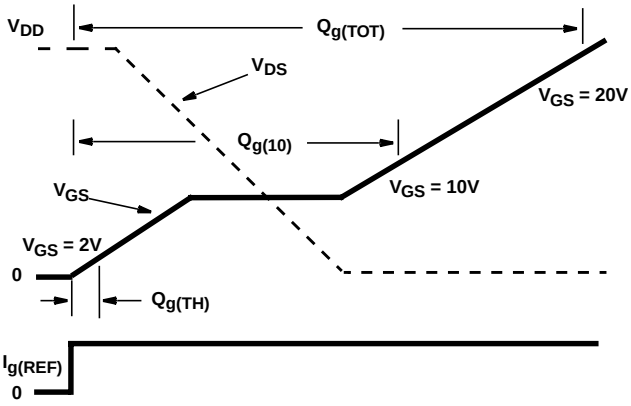


FIGURE 17. GATE CHARGE WAVEFORMS

Test Circuits and Waveforms (Continued)

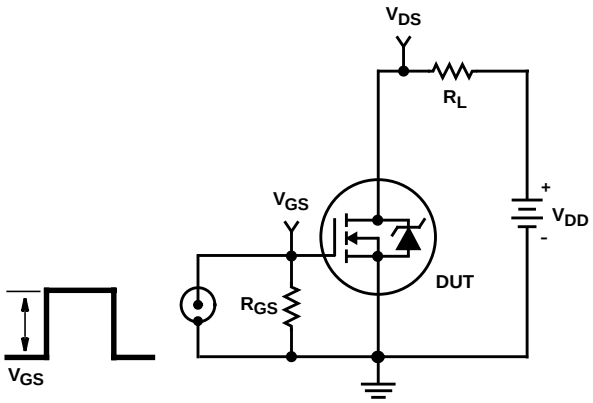


FIGURE 18. SWITCHING TIME TEST CIRCUIT

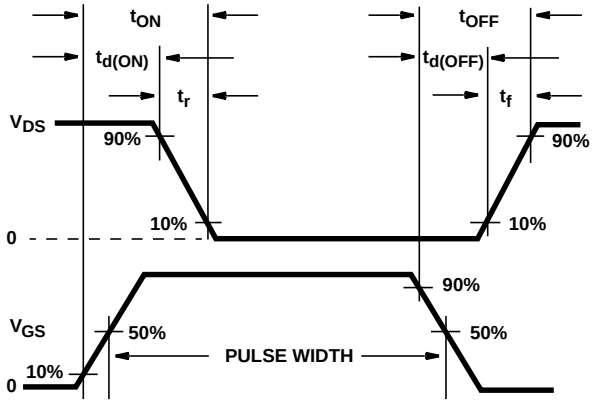
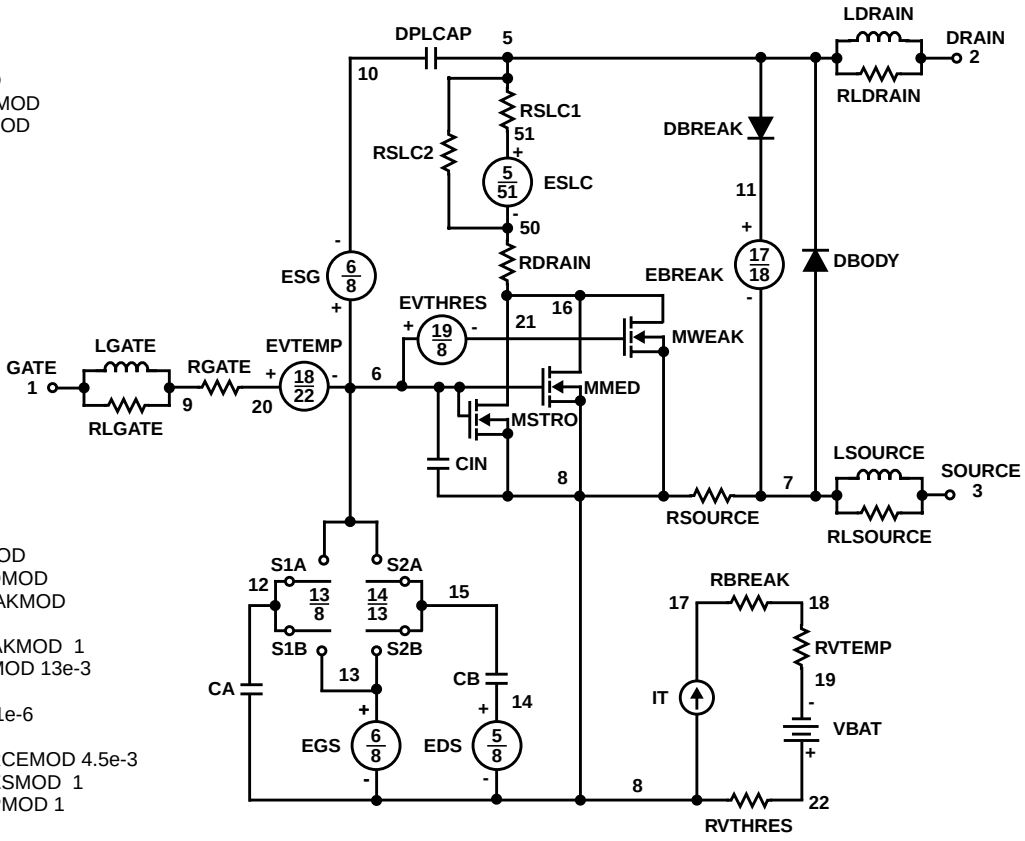


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

```
SUBCKT HUF75639 2 1 3 ;       rev OCT98
CA  12  8 28.5e-10
CB  15  14 26.5e-10
CIN  6  8 19e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 110
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 2e-9
LGATE 1  9 1e-9
LSOURCE  3  7 4.69e-10

RLGATE 1 9 10
RLDRAIN 2 5 20
RLSOURCE 3 7 4.69

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 13e-3
RGATE  9  20 .7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 4.5e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*115),4))}

.MODEL DBODYMOD D (IS = 1.4e-12  RS = 3.3e-3 XTI=4.7  TRS1 = 2e-3  TRS2 = .1e-5  CJO = 27e-10  TT = 6.1e-8 M = 0.6 )
.MODEL DBREAKMOD D (RS = 3.5e-1  TRS1 = 1e-3  TRS2 = 1e-6)
.MODEL DPLCAPMOD D (CJO = 28.5e-10  IS = 1e-30  N = 10 M = .95 vj=1.0)
.MODEL MMEDMOD NMOS (VTO = 3.5 KP = 4.8 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u Rg=.7)
.MODEL MSTROMOD NMOS (VTO = 3.97 KP = 56.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO =3.11 KP = 0.085 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG=7 RS=.1)
.MODEL RBREAKMOD RES (TC1 = .8e-3  TC2 = 1e-6)
.MODEL RDRAINMOD RES (TC1 = 1e-2  TC2 = 1.75e-5)
.MODEL RSLCMOD RES (TC1 = 2.8e-3 TC2 = 14e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -2.e-3 TC2 = -1.75e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.75e-3  TC2 = .05e-9)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -6.0  VOFF = -3.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.5  VOFF = -6.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.5  VOFF = 4.95)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 4.95  VOFF = -2.5)

.ENDS
```



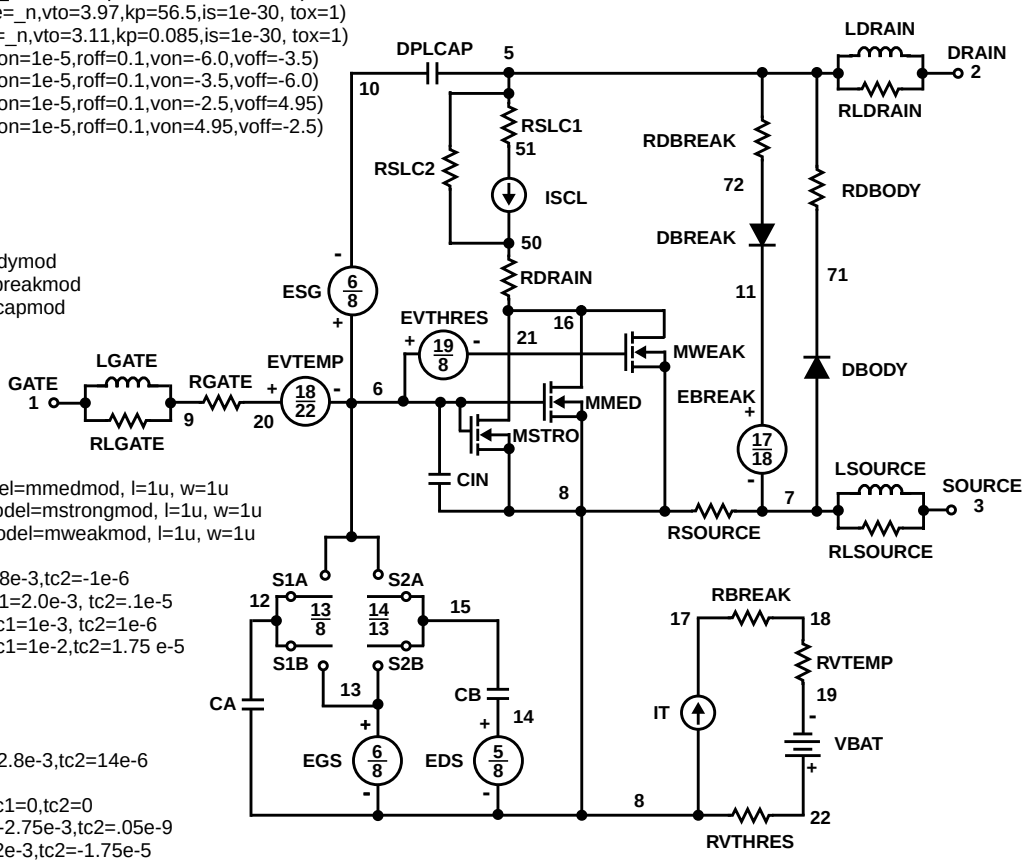
NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

nom temp=25 deg c 100v Ultrafet

REV Oct 1998

```
template huf75639 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod =  (is=1.4e-12, xti=4.7, cjo=27e-10,tt=6.1e-8, m=0.6)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo=28.5e-10,is=1e-30,n=10,m=0.95, vj=1.0)
m..model mmedmod = (type=_n,vto=3.5,kp=4.8,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=3.97,kp=56.5,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3.11,kp=0.085,is=1e-30, tox=1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-6.0,voff=-3.5)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-3.5,voff=-6.0)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-2.5,voff=4.95)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=4.95,voff=-2.5)

c.ca n12 n8 = 28.5e-10
c.cb n15 n14 = 26.5e-10
c.cin n6 n8 = 19e-10

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 2.0e-9
l.lgate n1 n9 = 1e-9
l.lsource n3 n7 = 4.69e-10

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1=.8e-3,tc2=-1e-6
res.rdbody n71 n5 =3.3e-3, tc1=2.0e-3, tc2=.1e-5
res.rdbreak n72 n5 =3.5e-1, tc1=1e-3, tc2=1e-6
res.rdrain n50 n16  = 13e-3, tc1=1e-2,tc2=1.75 e-5
res.rgate n9 n20 = .7
res.rldrain n2 n5 = 20
res.rlgate n1 n9 = 10
res.rlsource n3 n7 = 4.69
res.rslc1 n5 n51  = 1e-6, tc1=2.8e-3,tc2=14e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 4.5e-3, tc1=0,tc2=0
res.rvtemp n18 n19  = 1, tc1=-2.75e-3,tc2=.05e-9
res.rvthres n22 n8  = 1, tc1=-2e-3,tc2=-1.75e-5

spe.ebreak n11 n7 n17 n18 = 110
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/115))** 4))
}
}
```



SPICE Thermal Model

REV APRIL 1998

HUF75639

CTHERM1 TH 6 6 5.0
CTHERM2 6 5 3.0e-2
CTHERM3 5 4 1.0e-2
CTHERM4 4 3 3.0e-2
CTHERM5 3 2 3.5e-2
CTHERM6 2 TL 1.0

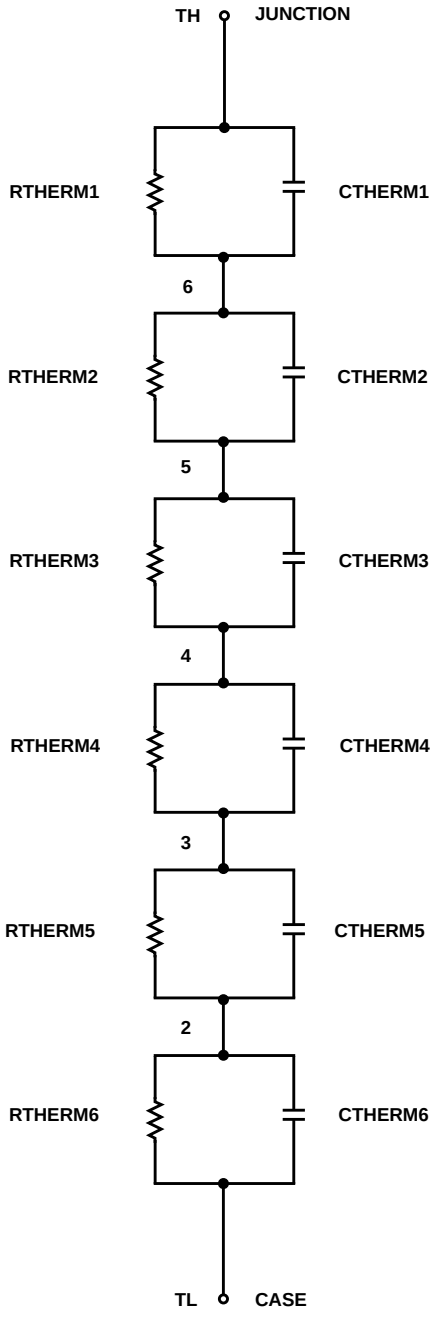
RTHERM1 TH 6 2.5e-4
RTHERM2 6 5 5.0e-4
RTHERM3 5 4 2.8e-3
RTHERM4 4 3 8.8e-2
RTHERM5 3 2 1.8e-1
RTHERM6 2 TL 5.0e-2

SABER Thermal Model

SABER thermal model HUF75639

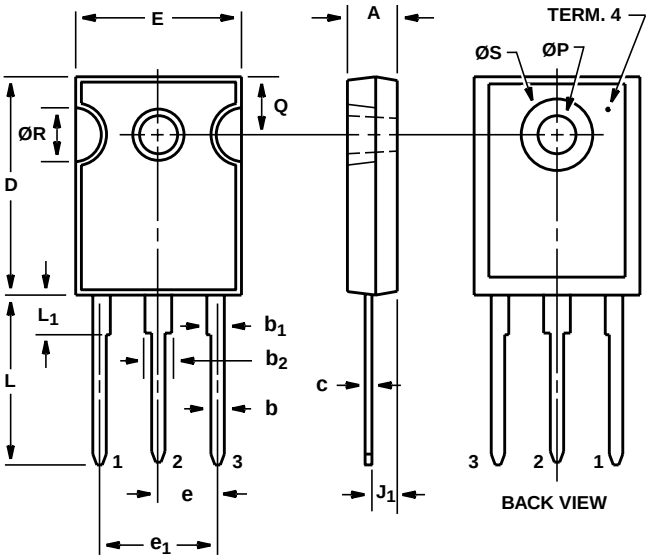
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 500e-2
ctherm.ctherm2 6 5 = 3.0e-2
ctherm.ctherm3 5 4 = 1.0e-2
ctherm.ctherm4 4 3 = 3.0e-2
ctherm.ctherm5 3 2 = .35e-1
ctherm.ctherm6 2 tl = 1.0

rtherm.rtherm1 th 6 = 2.5e-4
rtherm.rtherm2 6 5 = 5.0e-4
rtherm.rtherm3 5 4 = 2.8e-3
rtherm.rtherm4 4 3 = 88e-3
rtherm.rtherm5 3 2 = 18.0e-2
rtherm.rtherm6 2 tl = .5e-1
}



TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



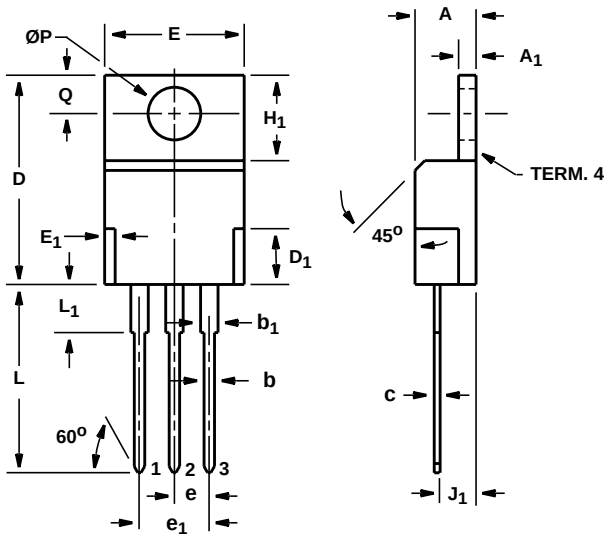
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

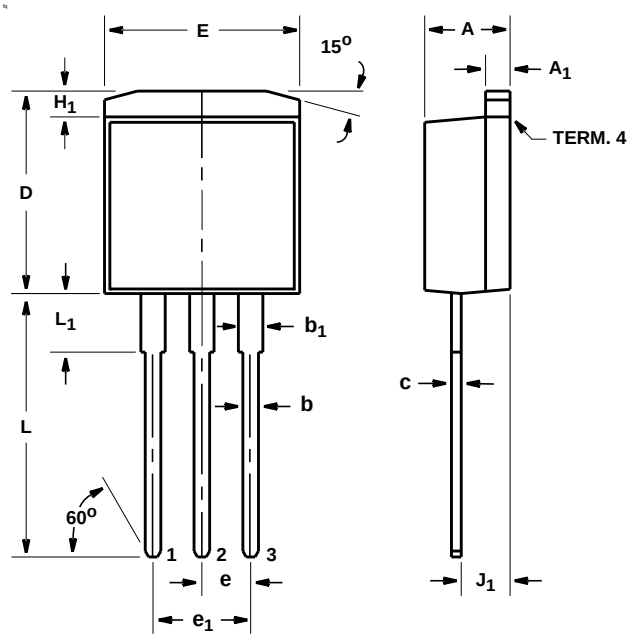


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

TO-262AA 3 LEAD JEDEC TO-262AA PLASTIC PACKAGE

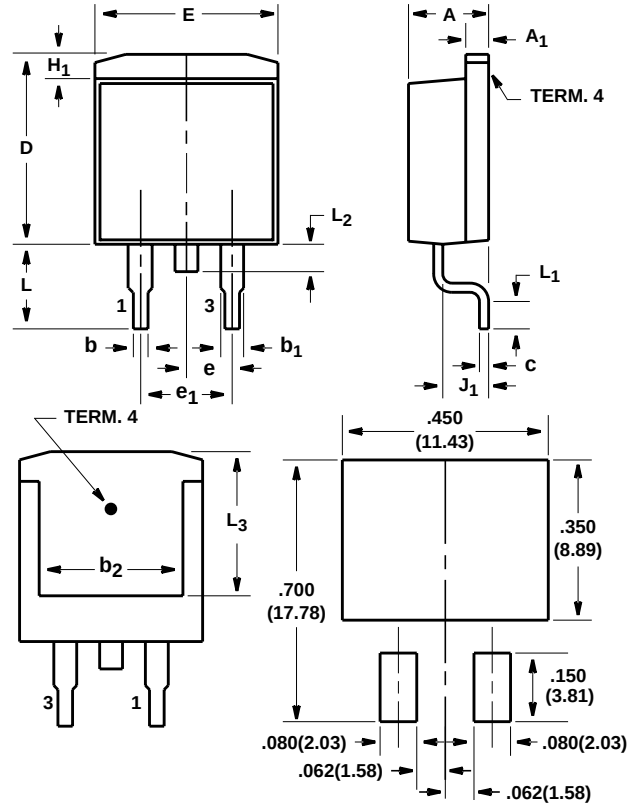


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 5 dated 7-97.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

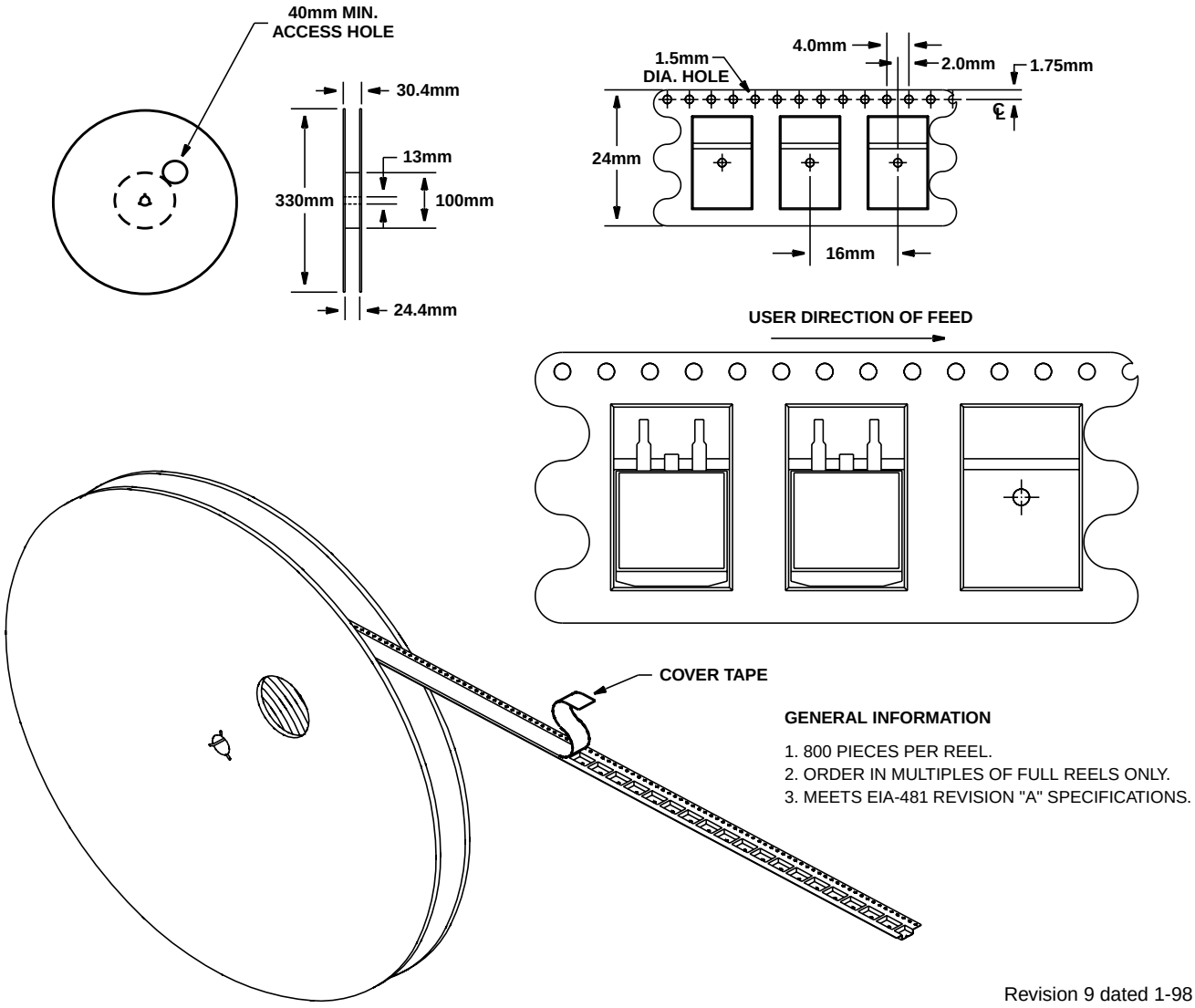
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 9 dated 1-98.

TO-263AB

24mm TAPE AND REEL



GENERAL INFORMATION

1. 800 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 9 dated 1-98

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