4 QUALIFIED TECHNOLOGY FLOWS

The following Technology Flows are qualified:

4.1 MICROCHIP ATMEL, FRANCE: MH1RT

NOTES:

1. An end of life notification affected the MH1RT process at the end of 2011, setting last delivery dates in June 2013.
2. LFoundry in Rousset ceased to supply MH1RT chips in December 2013 as well.
3. ATMEL MH1RT is therefore not available for any new designs. However, assembly and test operations (on legacy product designed and fabricated before January 2014) have remained possible beyond the scheduled last time delivery dates, within the ESCC qualified Technology Flow as described in the rest of this paragraph.

4.1.1 Contact Information

Address	ESCC Chief Inspector
Microchip Atmel Nantes SAS Route de Gachet 44300 Nantes France	Ms V. Lepaludier Tel. +33 2 40 18 1633 FAX +33 2 40 18 1946 Valerie.Lepaludier@atmel.com

4.1.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
278E Rev2	Dec. 2006	Integrated Circuits, Silicon Monolithic, CMOS Gate/ Embedded Array based on type MH1RT

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/076
Atmel Process Identification Document PID 0026, e2v PID DF 31S 100730 (assembly, common to both sources LF and UMC), HCM SYSTREL PID 11 (for columns attachment)

4.1.3 List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Atmel for use in conjunction with the ESCC Detail Specification No. 9202/076. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

ASIC Sheet	Component Type
FPK	Integrated Motor Controller for Mechanisms

4.1.4 Technology Flow Abstract

4.1.4.1 General features

The MH1RT gate array family is designed with a 0.35µm radiation tolerant CMOS technology. The offering is based on a 4 metal layer 3.6volts maximum AT56KRT process.

The family features arrays with up to 1.6 million routable gates and 596 pads. With its high speed performance, its low supply current and its radiation tolerant level, the MH1RT is suitable for digital applications working in a radiation intensive environment.

(a) Basic Information:

- 0.35 µm CMOS technology AT56KRT Process.
- High Speed Performance
  - 170 ps typical gate delay (NAND, FANOUT 2) @ 3V
  - 800 MHz typical toggle frequency @ 3.3V
- Triple Supply Operation
  - 3.3, 3 and 2.55 V operation
  - 5V compliant
  - 5V tolerant
- Low Supply Current
  - Operating Maximum Value
    0.32 µW/gate/MHz @ 2.5V,
    0.54 µW/gate/MHz @ 3V,
    0.69 µW/gate/MHz @ 3.3V
  - Maximum Stand-by Value
    4nA/gate@ 2.5V
    5nA/gate@ 3 and 3.3V
- I/O Interface
  - CMOS, LVTTL, LVDDS, PCI, USB
  - Output Currents Programmable from 2 to 24 mA, by Steps of 2 mA
  - Cold Sparing Buffers (2 µA maximum leakage current at 3.6V worst case MIL temperature)
- Radiation
  - CMOS on epitaxial layer
  - No Single Event Latch-up below a LET Threshold of 70 MeV/mg/cm^2
  - SEU Hardened Flip-flops
  - 200 Krad (Si) Radiation level tested CMOS technology

(b) Component Types
Device Types as per ESCC Detail Specification 9202/076 and individual custom ASIC sheets.

Die	Max programmable I/O's	Case	Typical Routable gates
MH1(M)099E	324	MQFP-352	519k
MH1(M)099E	324	MQFP-256	519k
MH1(M)099E	324	MQFP-196	519k
MH1(M)099E	324	LGA349	519k
MH1(M)099E	324	CCGA349	519k
MH1(M)156E	404	MQFP-352	764k
MH1(M)156E	404	MQFP-256	764k
MH1(M)156E	404	LGA472	764k
MH1(M)156E	404	CCGA472	764k
MH1(M)156E	404	LGA349	764k
MH1(M)156E	404	CCGA349	764k
MH1(M)242E	504	MQFP-352	1198k
MH1(M)242E	504	MQFP-256	1198k
MH1(M)242E	504	LGA472	1198k
MH1(M)242E	504	CCGA472	1198k
MH1(M)242E	504	LGA349	1198k
MH1(M)242E	504	CCGA349	1198k
MH1(M)332E	588	MQFP-352	1634k
MH1(M)332E	588	LGA472	1634k
MH1(M)332E	588	CCGA472	1634k

4.1.4.2 Technology Flow definition

[See Paragraph 4.1 Notes 1 and 2.]
The Technology Flow covers the design, fabrication, assembly and testing of the MH1RT standard cell ASIC family.

4.1.4.2.1 Design

The design manual and the ASIC library data books cover design at the Atmel Nantes Design Centre.

- MH1RT Design Manual ATD-TS-LR-R0232
- MH1RT 2V5 ASIC Library Data book ATD-TS-LR-R0236
- MH1RT 3V ASIC Library Data book ATD-TS-LR-R0235
- MH1RT 3V3 ASIC Library Data book ATD-TS-LR-R0238

ASIC designs are performed by the Atmel customer at their own site, with Atmel supported tools (front end) provided as a design tool kit.

4.1.4.2.2 Fabrication

See Paragraph 4.1 Notes 1 and 2

The wafer fabrication was performed in Rousset LFOUNDRY. Since Decmber 2013. LFOUNDRY in Rousset ceased to supply MH1RT chips. ATMEL MH1RT ASICs wafers are stored in Nantes based on customers demand

4.1.4.2.3 Assembly

See Paragraph 4.1 Note 3

The assembly of MH1RT devices is performed at E2V Grenoble with the following capabilities:

Die attach Cyanate Ester (JM7000)
Wire bond Ultrasonic Wedge, 32µm Al
Lid sealing Brazed with Au/Sn alloy
Leads Au plated (MQFP and LGA)

Columns attachment is performed in SERMA HCM, La Rochelle, with the following capabilities:

Columns 85Pb15Sn with Cu ribbon

4.1.4.2.4 Control and Test

See Paragraph 4.1 Note 3

The control and test of MH1RT devices is performed in Atmel Nantes. It includes Lot Acceptance, Test Flows and Test Procedures, Qualification Test and Reliability Monitoring, Screening and associated electrical tests and inspections.

4.1.4.2.5 TCVs and SEC

The die MH1156E was used for both test vehicles.

(a) Test Vehicle V37

The V37 is a buffer test vehicle representative of the range of buffers available for performance testing in the MQFP 256 package.

(b) Test Vehicle V38 – Technology SEC

The V38 is developed for performance verification and radiation testing with the following library elements;

- LVDS input and output buffers
- PCI 3V and 5V output buffers
- PLL (125 MHz and 250 MHz)
- DPRAM memory cell for GENESYS tool

The V38 is packaged in MQFP256

4.1.4.2.6 Radiation Characteristics

The MH1RT family has been developed to fulfil the following characteristics in terms of radiation tolerance:

- No Single Event Latch-up below a LET Threshold of 70MeV/mg/cm^2
- SEU hardened flip-flops
- Total dose up to 200Krad (Si)

4.1.4.3 Manufacturing sites

Design: Atmel Nantes, BP70602, 44306 Nantes Cedex 3, France
Wafer Fabrication: Lfoundry, Rousset, France
Assembly: E2V Grenoble, BP123, 38521 Saint-Egrève Cedex, France
HCM SYSTREL, 34 Av. Joliot Curie, ZI Perigny, 17185 Perigny Cedex, France
Control and Test: Atmel Nantes, BP70602, 44306 Nantes Cedex 3, France

4.2 MICROCHIP ATMEL, FRANCE: ATC18RHA

NOTES:

1. LFoundry (LF) in Rousset ceased to supply ATC18RHA chips in December 2013
2. A second source of supply, UMC has been successfully added to the scope of Technology Flow qualification for this technology by Atmel.
3. New designs and fabrication after January 2014 make use of the UMC source.

4.2.1 Contact Information

Address	ESCC Chief Inspector
Microchip Atmel Nantes SAS Route de Gachet 44300 Nantes France	Ms V. Lepaludier Tel. +33 2 40 18 1633 FAX +33 2 40 18 1946 Valerie.Lepaludier@atmel.com

4.2.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
312B Rev 1	Aug. 2012	Integrated Circuits, Silicon, Monolithic, CMOS, Cell-Based Array, based on Type ATC18RHA

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/080

Atmel Process Identification Document PID 0030 (LF), PID 32 (UMC) , e2v PID DF 31S 100730 (assembly, common to both sources LF and UMC), HCM SYSTREL PID 11 (for columns attachment).

4.2.3 List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Atmel for use in conjunction with the ESCC Detail Specification No. 9202/080. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

ASIC Sheet	Component Type

In the case of ATC18RHA, standard components are also available. These are listed below with their full ESCC Detail Specification:

Detail Specification	Component Type
9512/004	Integrated Circuits, Silicon, 32-bit SPARC Processor, based on Type AT697F
9304/165	Integrated Circuits, Silicon, monolithic, CMOS digital, Field Programmable Gate Array, 280000 gates, based on type ATF280F

4.2.4 Technology Flow Abstract

See Notes under Para. 4.2

4.2.4.1 General Features

ATC18RHA standard cells family is designed with a 0.18µm radiation hard CMOS technology. This offering is based on 6 metal layers at 1.8V +/-0.15V for the core and 3.3V +/-0.3V for the periphery. This family features arrays with up to 7 Mgates and 544 pads. With its high speed performance, its low supply current and its radiation hard level, the ATC18RHA is suitable for digital applications working in radiation intensive environment.

(a) Basic Information

- CMOS technology AT58KRHA
- 40 to 70 kgates per mm² - Up to 6.5M gates
- Double supply operation
  - Periphery power supply 3.3V
  - Core power supply 1.8V
- Low supply current :
  Operating maximum value: 85nW/gate/MHz with a duty cycle at 20%
- I/O Interfaces:
  - Cold sparing
  - High speed LVDS (655 Mps) and LVPECL
  - PCI
- 544 pads (+ 8 pads power only)
- Embedded memories: Compiled and Synthesized
- EDAC library

– Radiation (LF and UMC):
  - No Single Event Latch-Up below a LET Threshold of 80 MeV/mg/cm² at ambient & high temperature
  - SEU hardened DFF's to 30 MeV/mg/cm2
  - Tested up to 300 KRad (Si), Radiation Level is 100 KRads (Si).

– Device Types – per individual custom ASIC sheets and ESCC Detail Specification 9202/080

(b) Component Types
This table presents the available couples (die, package) as defined in the Detail Specifications:

Die	Supply Voltage I/O / core	Max programmable I/O's	Case	Typical Routable gates
ATC18RHA_216	2.5V or 3.3V/1.8V	216	MQFP-F256	1M
ATC18RHA_216	2.5V or 3.3V/1.8V	216	MQFP-F196	1M
ATC18RHA_216	2.5V or 3.3V/1.8V	216	MQFP-F160	1M
AT697F	3.3V/1.8V		MQFP-F256	0.85M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	MQFP-T352	2.2 M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	MQFP-F256	2.2 M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	MQFP-F196	2.2 M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	MQFP-F160	2.2 M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	LGA-349	2.2 M
ATC18RHA_324	2.5V or 3.3V/1.8V	324	CCGA-349	2.2 M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	MQFP-T352	3.5 M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	MQFP-F256	3.5 M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	LGA-472	3.5 M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	LGA-349	3.5 M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	CCGA-472	3.5 M
ATC18RHA_404	2.5V or 3.3V/1.8V	404	CCGA-349	3.5 M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	MQFP-T352	5.5 M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	MQFP-F256	5.5 M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	LGA-625	5.5 M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	LGA-472	5.5 M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	LGA-349	5.5 M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CCGA-625	5.5 M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CCGA-472	5.5 M
ATC18RHA_504	2.5V or 3.3V/1.8V	504	CCGA-349	5.5 M
ATC18RHA_544	2.5V or 3.3V/1.8V	544	LGA-625	7 M
ATC18RHA_544	2.5V or 3.3V/1.8V	544	CCGA-625	7 M

4.2.4.2 Technology Flow Definition

The Technology Flow Definition domain covers the design, fabrication, assembly and testing of the ATC18RHA standard cells family.

4.2.4.2.1 Design

The design manual and the ASIC library data books cover design at the Atmel Nantes Design Centre.

- ATC18RHA Design manual ATD-DE-GR-R0212
- ATC18RHA TOS manual ATD-DE-GR-R0324
- ATC18RHA Buffers library databook ATD-TS-LR-R0252
- ATC18RHA Cells library databook ATD-TS-LR-R0251
- ATC18RHA Memory cells library databook ATD-TS-LR-R0254
- ATC18RHA specific library databook ATD-TS-LR-R0253

All ASIC designs will be performed by the customer at the customer site, with Atmel supported tools (front end).

4.2.4.2.2 Fabrication

The ATC58KRHA, processed in UMC Taiwan, is a 0.18µm CMOS, 6 metal, Ti, TiN and AlCu process.

4.2.4.2.3 Assembly

The assembly of ATC18RHA devices is performed at E2V, Grenoble, with the following capabilities:

Die attach Cyanate Ester (JM7000)
Wire bond Ultrasonic Wedge, 32µm Al
Lid sealing Brazed with Au/Sn alloy
Leads Au plated (MQFP and LGA)

Columns attachment is performed in SERMA HCM, La Rochelle, with the following capabilities:
Columns 85Pb15Sn with Cu ribbon

4.2.4.2.4 Control and Test

The control and test of ATC18RHA devices at Atmel Nantes. It includes Lot Acceptance, Test Flows and Test Procedures, Qualification Test and Reliability Monitoring, Screening and associated electrical tests and inspections.

4.2.4.2.5 TCVs and SEC

The die ATC18RHA_324 is used for both test vehicles. All details are described in the ATC18RHA test chip specification, reference ADF-DE-R0561-CUP.

V41 test vehicle

The V41 is a buffer test vehicle representative of the range of buffers available for performance testing in the MQFP 256 package. It contains standard IO33 buffers, specific IO33 buffers (LVDS, PCI), a PLL, a set of ring oscillators made of different library cells and a set of interconnect lines.

V40 test Vehicle – Technology SEC

The V40 SEC is developed for performance and radiation testing in the MQFP 256 package. It contains a set of memory blocks (compiled memories with and without EDACs and synthesized (on gates) memories made with standard and hardened latches), shift registers chains and a PLL.

4.2.4.2.6 Radiation Characteristics

The AT58KRHA family has been developed to fulfil the following characteristics in terms of radiation tolerance:

- No Single Event Latch-up below a LET Threshold of 80MeV/mg/cm^2 at high temperature
- Availability of SEU hardened flip-flops
- Total dose capability over 100Krad (Si)

4.2.4.3 Manufacturing sites

Design: Atmel Nantes, BP70602, 44306 Nantes Cedex 3, France
Wafer Fabrication: UMC Fab 8S, Hsin-Chu, Taiwan
Assembly: e2v Grenoble, BP123, 38521 Saint-Egrève Cedex, France
HCM SYSTREL, 34 Av. Joliot Curie, ZI Perigny, 17185 Perigny Cedex, France
Control and Test: Atmel Nantes, BP70602, 44306 Nantes Cedex 3, France

4.3 MICROCHIP ATMEL, FRANCE: ATMX150RHA

4.3.1 Contact Information

Address	ESCC Chief Inspector
Microchip Atmel Nantes SAS Route de Gachet 44300 Nantes France	Ms V. Lepaludier Tel. +33 2 40 18 1633 FAX +33 2 40 18 1946 Valerie.Lepaludier@atmel.com

4.3.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
342 rev1	Aug. 2016	Integrated Circuits, Silicon, Monolithic, CMOS, Cell-Based Array, based on Type ATMX150RHA – Ph1 Digital only 7 Mgates 5ML

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/083

Atmel Process Identification Document PID 37, e2v PID DF 31S 100730 (assembly), HCM SYSTREL PID 11 (for columns attachment).

4.3.3 List of Qualified Components

For each ASIC design an ASIC Sheet is produced by Atmel for use in conjunction with the ESCC Detail Specification No. 9202/083. Where the ASIC is not proprietary to the customer the ASIC sheet is published in ESCIES as a supporting document.

ASIC Sheet	Component Type

4.3.4 Technology Flow Abstract

4.3.4.1 General features

The ATMX150RHA ASIC family is designed with a 0.15µm Radiation-Hardened CMOS technology, 5 metal layers, with 1.8V +/-0.15V for the core and 2.5+/-0.25V or 3.3V +/-0.3V for the periphery supplies. This family arrays up to 7 Mgates and more than 500 pads.
With its high speed performance, its low supply current and its radiation hard level, the ATMX150RHA is suitable for digital applications working in radiation intensive environment.

(a) Basic information

CMOS technology AT77K9RHA

- 40 to 70 kgates per mm²
- Up to 7M gates
- Double supply operation:
    - Periphery power supply 2.5V & 3.3V
    - Core power supply 1.8V
- Operating maximum value of 8.8 nA/gate/MHz with a duty cycle at 20%
- I/O Interfaces:
    - Cold sparing
    - High speed LVDS (655 Mps) and LVPECL
    - PCI
- 544 pads (+ 8 pads power only)
- Compiled memory cells (ROM, SRAM, DPRAM, register files)
- Radiation:
    - No Single Event Latch-Up below an LET Threshold of 86 MeV/mg/cm² at high temperature.
    - SEU Hardened DFF's to 18 MeV/mg/ cm2
    - TID Radiation Capability of 100 kRads (Si).
- Device Types – per individual custom ASIC sheets and ESCC Detail Specification 9202/083

(b) Component Types

This table presents the available couples (die, package) as defined in the Detail Specifications:

Die	Supply Voltage I/O / core	Max programmable I/O's	Case	Typical Routable gates
ATMX150RHA_216	2.5V or 3.3V/1.8V	216	MQFP-F256	1M
ATMX150RHA_216	2.5V or 3.3V/1.8V	216	MQFP-F196	1M
ATMX150RHA_216	2.5V or 3.3V/1.8V	216	MQFP-F160	1M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	MQFP-T352	2.2 M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	MQFP-F256	2.2 M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	MQFP-F196	2.2 M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	MQFP-F160	2.2 M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	LGA-349	2.2 M
ATMX150RHA_324	2.5V or 3.3V/1.8V	324	CCGA-349	2.2 M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	MQFP-T352	3.5 M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	MQFP-F256	3.5 M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	LGA-472	3.5 M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	LGA-349	3.5 M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	CCGA-472	3.5 M
ATMX150RHA_404	2.5V or 3.3V/1.8V	404	CCGA-349	3.5 M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	MQFP-T352	5.5 M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	MQFP-F256	5.5 M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	LGA-625	5.5 M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	LGA-472	5.5 M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	LGA-349	5.5 M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CCGA-625	5.5 M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CCGA-472	5.5 M
ATMX150RHA_504	2.5V or 3.3V/1.8V	504	CCGA-349	5.5 M
ATMX150RHA_544	2.5V or 3.3V/1.8V	544	LGA-625	7 M
ATMX150RHA_544	2.5V or 3.3V/1.8V	544	CCGA-625	7 M

4.3.4.2 Technology Flow Definition

The Technology Flow covers the design, fabrication, assembly and testing of the ATMX150RHA standard cells ASIC family.

4.3.4.2.1 Design

The design manual and the ASIC library data books cover the design in the Atmel Nantes Design Centers:

ATMX150RHA design manual	2012_EC_054_ELE
ATMX150RHA TOS (Test Oriented Simulation) Manual	ATD-DE-GR-R0324
ATMX150RHA supply & ESD buffer databook	2012_EC_055_ELE
ATMX150RHA buffer 3.3V databook	2012_EC_051_ELE
ATMX150RHA buffer 2.5V databook	2012_EC_052_ELE
ATMX150RHA Cells library databook	2012_EC_050_ELE
ATMX150RHA memory cells library databook	2012_EC_053_ELE
ATMX150RHA power grid verification flow	2014_EC_131-ELE

All ASIC designs will be performed by customer at customer site, with Atmel supported tools (front end).

4.3.4.2.2 Fabrication

The AT77K9RHA, processed in UMC Taiwan, is a 0.15 µm CMOS, 5 metal, Ti, TiN and AlCu process.

4.3.4.2.3 Assembly

The assembly of ATMX150RHA devices is performed in e2v, Grenoble, with the following capabilities:

Die attach Cyanate Ester (JM7000)
Wire bond Ultrasonic Wedge, 32µm Al
Lid sealing Brazed with Au/Sn alloy
Leads Au plated (MQFP and LGA)

Columns attachment is performed in SERMA HCM, La Rochelle, with the following capabilities:

Columns 85Pb15Sn with Cu ribbon

4.3.4.2.4 Control & Test

The control and test of ATMX150RHA devices is performed in Atmel Nantes. It includes Lot Acceptance, Test Flows and Test Procedures, Qualification Test and Reliability Monitoring, Screening and associated electrical tests and inspections.

4.3.4.2.5 TCVs and SEC

The die ATMX150RHA_324 is used for both test vehicles. All details are described in the ATMX150RHA test chip specification, reference 2012_EC_024.

V55 test vehicle. The V55 is a buffer test vehicle representative of the range of buffers available for performance testing in the MQFP 256 package. It contains standard IO33 buffers, specific IO33 buffers (LVDS, PCI), a PLL, a set of ring oscillators made of different library cells and a set of interconnect lines

V54 test Vehicle V54 – Technology SEC. The V54 SEC is developed for performance and radiation testing in the MQFP 256 package. It contains a set of memory blocks (compiled memories with and without EDACs and synthesized (on gates) memories made with standard and hardened latches), shift registers chains and a PLL.

4.3.4.2.6 Radiation Characteristics

The AT77K9RHA technology has been developed to fulfil the following characteristics:

- Total dose capability over 100 kRads (Si).
- No Single Event Latchup below a LET threshold of 86 MeV/mg/cm2 at high temperature.
- Availability of SEU hardened cells.

4.3.4.3 Manufacturing sites

Design: Atmel Nantes, BP70602, 44306 Nantes Cedex 3, France
Wafer Fabrication: UMC Fab 8C, Hsin-Chu, Taiwan
Assembly: e2v Grenoble, BP123, 38521 Saint-Egrève Cedex, France
HCM SYSTREL, 34 Av. Joliot Curie, ZI Perigny, 17185 Perigny Cedex, France
Control and Test: Atmel Nantes, BP70602, 44306 Nantes Cedex 3, France

4.4 KONGSBERG NORSPACE, NORWAY

4.4.1 Contact Information

Address	ESCC Chief Inspector
Kongsberg Norspace AS Knutsrødveien 7 N-3189 Horten Norway	Mrs Cecilie Berg Tel: (+47) 3303 2700 Fax: (+47) 3303 2800 email: cecilie.berg@norspace.no

4.4.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
313B	Aug. 2011	SAW filters (transversal band pass/resonator/notch/low loss impedance element)

Applicable Documents

ESCC Generic Specification No. 3502; ESCC Detail Specification Nos. 3502/002

Norspace Process Identification Documents: