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# Radiation Testing of 2-D Imaging Detectors and ADCs

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# Theme: Star Tracker Applications

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- **12-bit ADCs: Analog Devices AD9223**  
**Linear Technology LTC1415**
  - ◆ Co-60 and heavy ion evaluation tested
- **ASCoSS Active Pixel Sensor (from IMEC)**
  - ◆ Co-60, 10 MeV proton and heavy ion evaluation tested
- **EEV CCDs: CCD02 (288 x 385 22  $\mu\text{m}$  x 22  $\mu\text{m}$  pixels)**  
**CCD47-20 (1024 x 1024 13  $\mu\text{m}$  x 13  $\mu\text{m}$  pixels)**
  - ◆ Investigation of displacement damage effects on charge transfer efficiency and star position measurements (also applicable to *laser communications* and *space science* missions)

# Irradiations

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- **Co-60: at ESTEC 21-24 September 1999 .**
  - ◆ **Dose rate 0.26 to 2.6 krad(Si)/hr.**
  - ◆ **6 x ASCoSS (2 UB) , 8 x each ADC type (2 UB)**

<b>Devices irradiated</b>	<b>Dose step krad(Si)</b>	<b>Exposure time hours</b>	<b>Dose rate krad(Si)/hour</b>	<b>Total accumulated dose on ASCoSS devices</b>	<b>Total accumulated dose on ADCs</b>
All ASCoSS	2.0	0.77	2.6	2.0	-
All	4.0	15.1	0.26	6.0	4.0
All, except ASCoSS #s 43, 54, 75	15.2	15.8	0.96	21.2	19.2
ADCs, except #s 6 and 7 (both types)	47.0	18.1	2.6	-	66.2

# Irradiations

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- **10 MeV protons : ASCoSS and CCD chips, unbiased, AEA Technology, Harwell. 7 December 1998**
- **Heavy ion:** at the Heavy Ion Facility (HIF) at Louvain-La-Neuve (Belgium) on 11 June 1999
  - $^{40}\text{Ar}^{8+}$  ions, (energy 150 MeV), 60° incidence **LET 28.2 MeV/mg/cm<sup>2</sup>**
  - $^{40}\text{Ar}^{8+}$  ions, (energy 150 MeV), 45° incidence **LET 19.9 MeV/mg/cm<sup>2</sup>**
  - $^{40}\text{Ar}^{8+}$  ions, (energy 150 MeV), normal incidence **LET 14.1 MeV/mg/cm<sup>2</sup>**
  - $^{20}\text{Ne}^{4+}$  ions, (energy 78 MeV), 60° incidence **LET 11.7 MeV/mg/cm<sup>2</sup>**

# AD9223 and LTC1415 12-bit ADCs

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## ■ **AD9223:**

- ◆ 3 MSPS, programmable on-chip (or external) reference
- ◆ pipelined architecture with output error correction logic
- ◆ low power:  $V_{dd}(an)$  26 mA (max)  $V_{dd}(dig)$  0.5 mA (max)
- ◆ used by Sira on the CHRIS instrument on ESA's PROBA mission
- ◆ 10 MSPS version (9220) previously tested by Turflinger et al\*  
at high dose rate (71 rad(Si) / s)
  - dependence on bias condition
  - failed at 35 krad due to DNL and voltage reference but recovered on annealing

\* 1996 IEEE Radiation Effects Data Workshop, pp 6-12

# AD9223 and LTC1415 12-bit ADCs

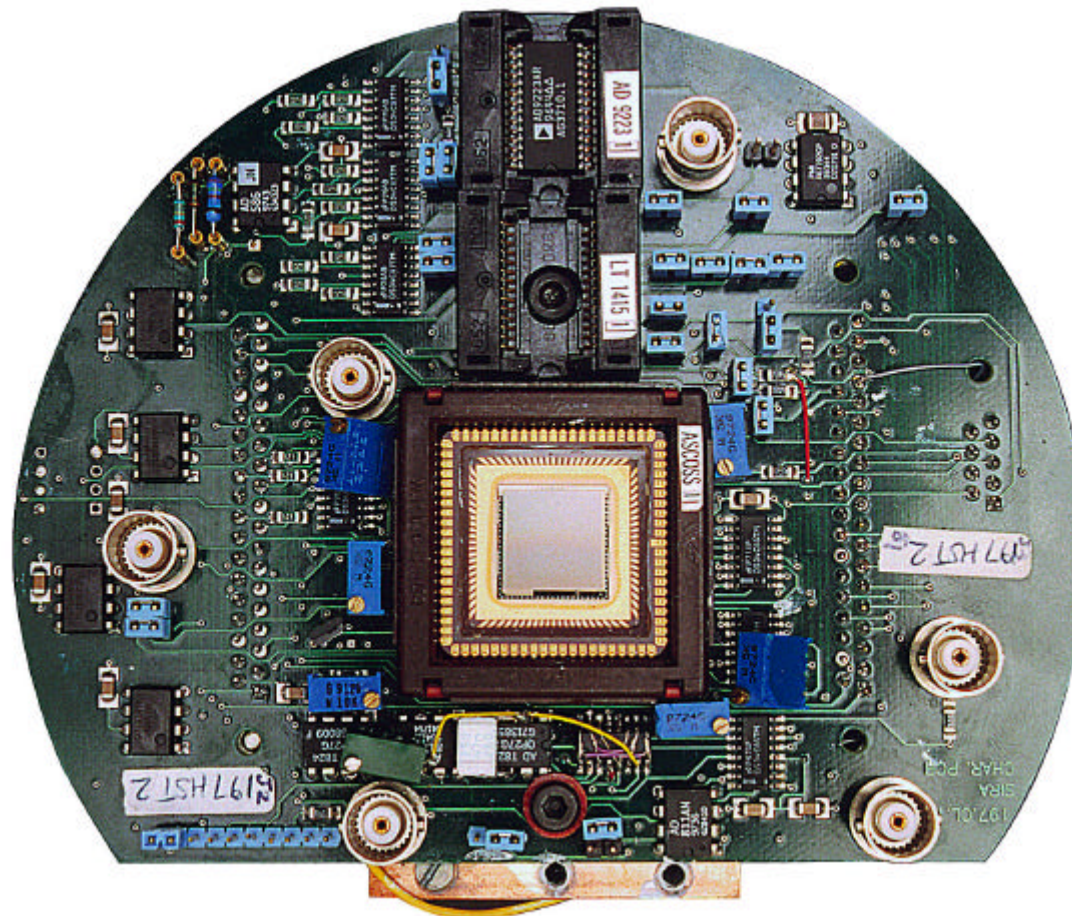
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## ■ LTC1415

- ◆ 1.25 MSPS, programmable on-chip (or external) reference
  - ◆ Low power: 20 mA (max) with 'nap' and 'sleep' modes
- 
- Devices were in plastic surface mount packages and were not burned in
  - Devices were de-lidded by ESTEC for SEL tests
  - Two PCBs were designed and manufactured
    - ◆ bias board for TID and SEL irradiations (all devices)
    - ◆ characterisation board (single devices)

# ADC & APS Characterisation Board

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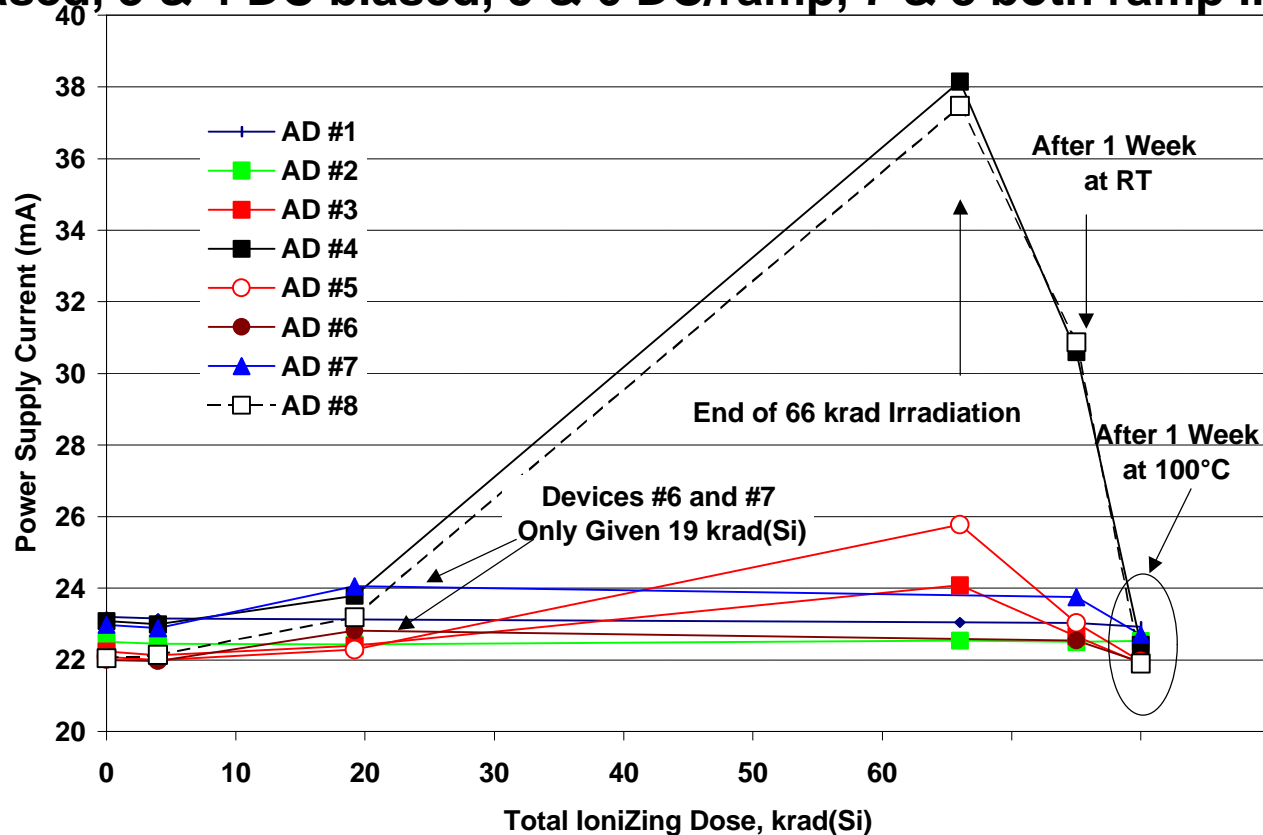
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**QCA Final Presentation Day**  
**26 January 2000**

**siraelectro-optics**

# Co-60 Tests, Power Supply Currents

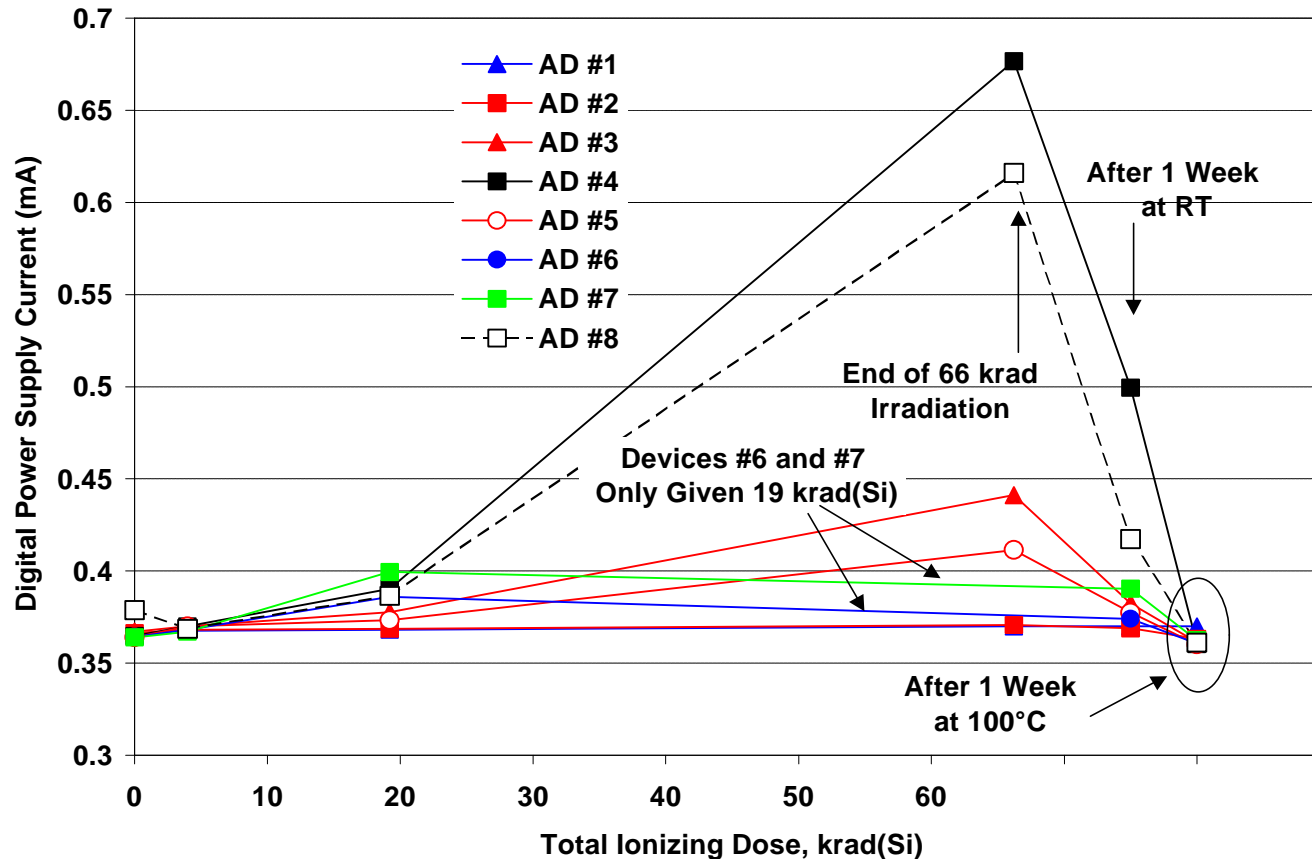
Analogue power supply current for the AD9223 (characterisation board)  
1 & 2 unbiased, 3 & 4 DC biased, 5 & 6 DC/ramp, 7 & 8 both ramp input





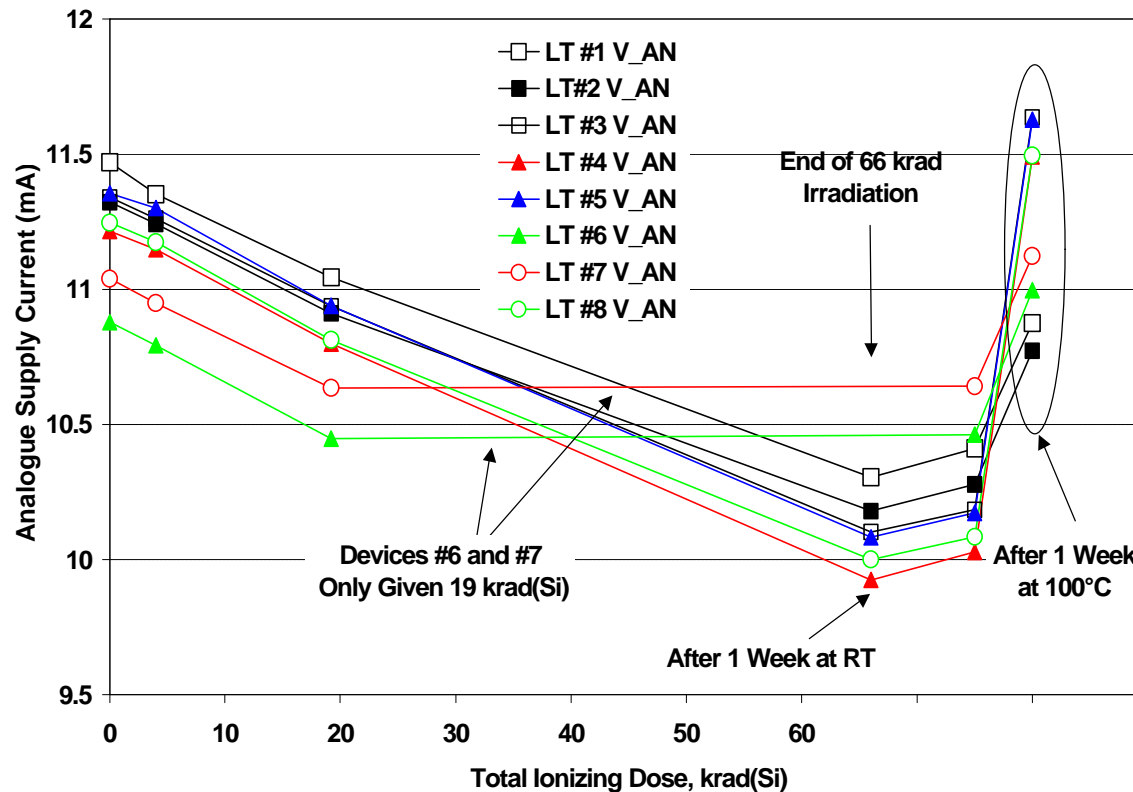
# Co-60 Tests, Power Supply Currents

Digital power supply current for the AD9223 (characterisation board)



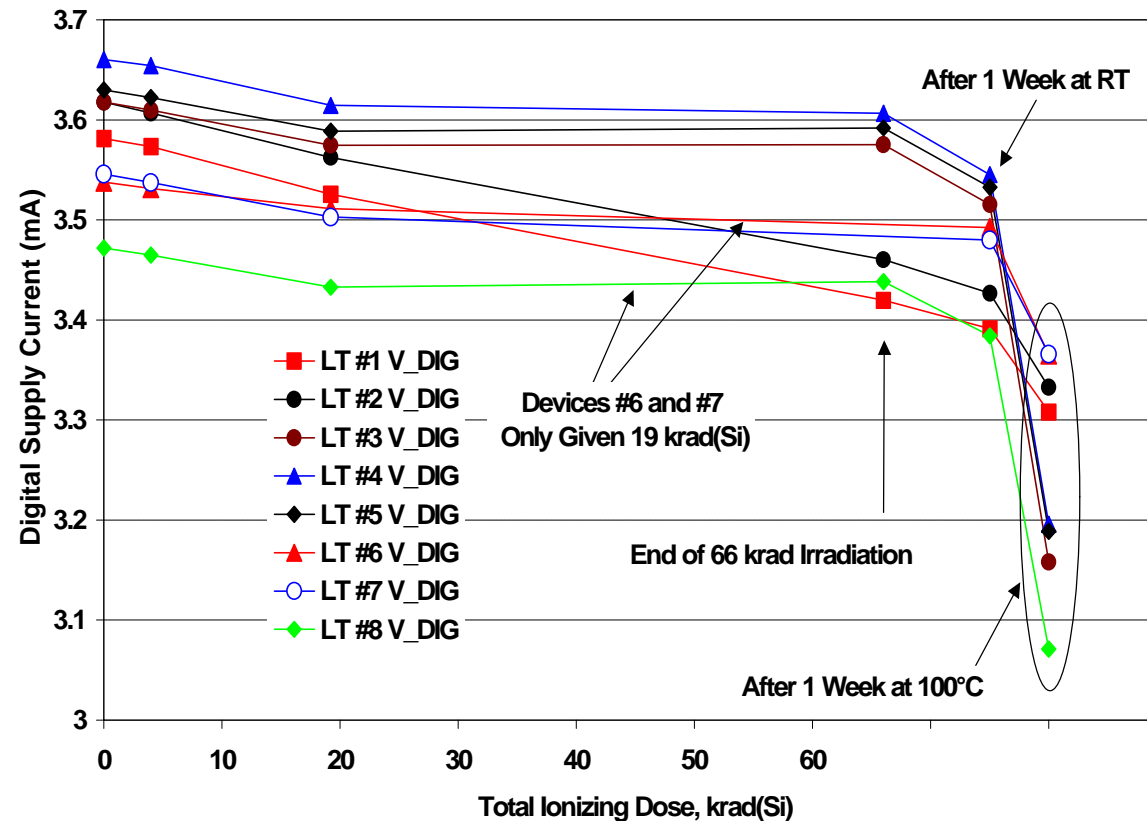
# Co-60 Tests, Power Supply Currents

Analogue power supply current for the LTC1415 (characterisation board)



# Co-60 Tests, Power Supply Currents

Digital power supply current for the LTC1415 (characterisation board)



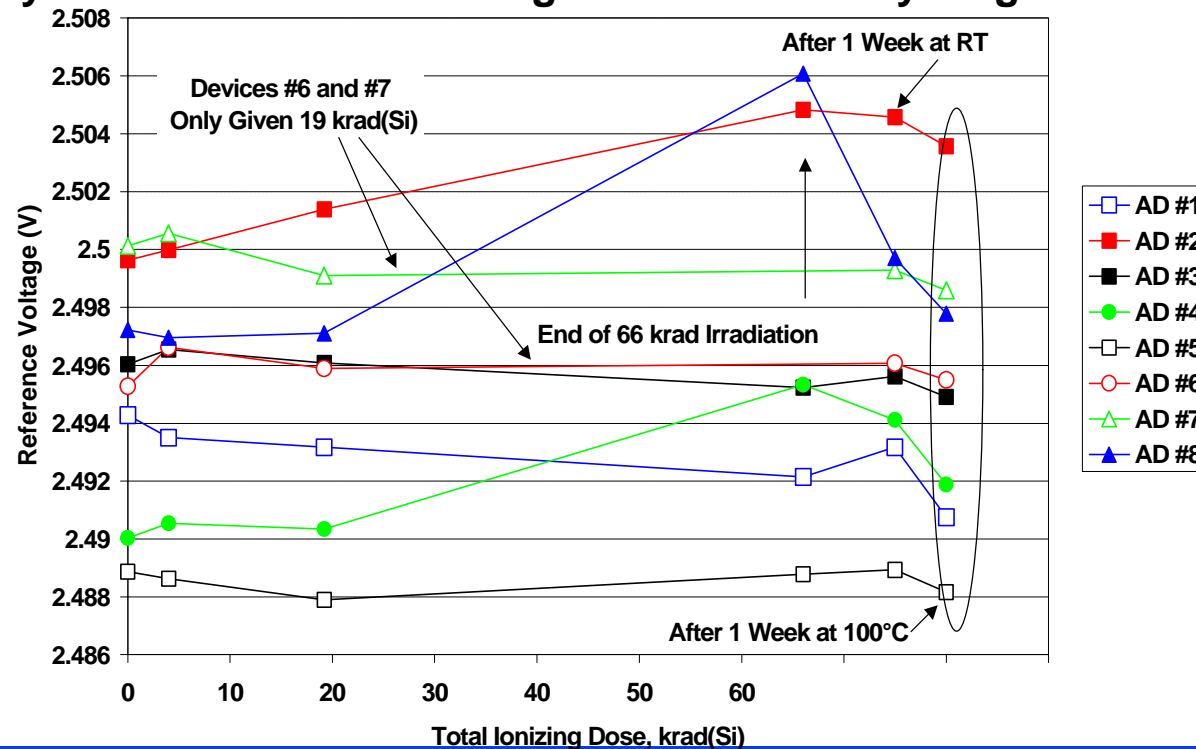
# Power Supply Currents: Conclusions

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- AD9223 #4 and #8 show large increases in current above ~10 krad (go out of specification), but these anneal out after a 100°C bake.
- Increase coincided with significant degradation in differential non-linearity. Both failed after 19 krad irradiation because of 'stuck bits'.
  - ◆ stuck bits were some of the most significant, so output data significantly corrupted.
  - ◆ Recovery of the supply current after the bake also coincided with return to normal DNL performance. Devices #4 and 8 also showed larger than average changes in VREF voltage.
- Little change in LTC1415 currents. DNL for unbiased devices (#1 and #2) degraded after 100°C bake - 'rebound' effects ?– but degradation not as severe as for the AD9223 (only least significant bits affected). #1 and #2 also showed largest increase in digital supply current.
- The low power modes for the LTC1415 ('sleep' and 'nap') remained functional for all the tests.

# Co-60 Tests: Voltage Reference

- critical for offset and gain accuracy
- changes were small and within specification ( $2.5 \pm 0.035$  V for AD9223 and  $2.5 \pm 0.020$  V for LTC1415)
- not necessary to use an external voltage reference at any stage



# ADCs, Co-60: DNL and INL

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## ■ AD9223:

- ◆ Apart from 'stuck' bits for devices #4 and #8 immediately after 66 krad(Si), no significant changes in DNL.

## ■ LTC1415:

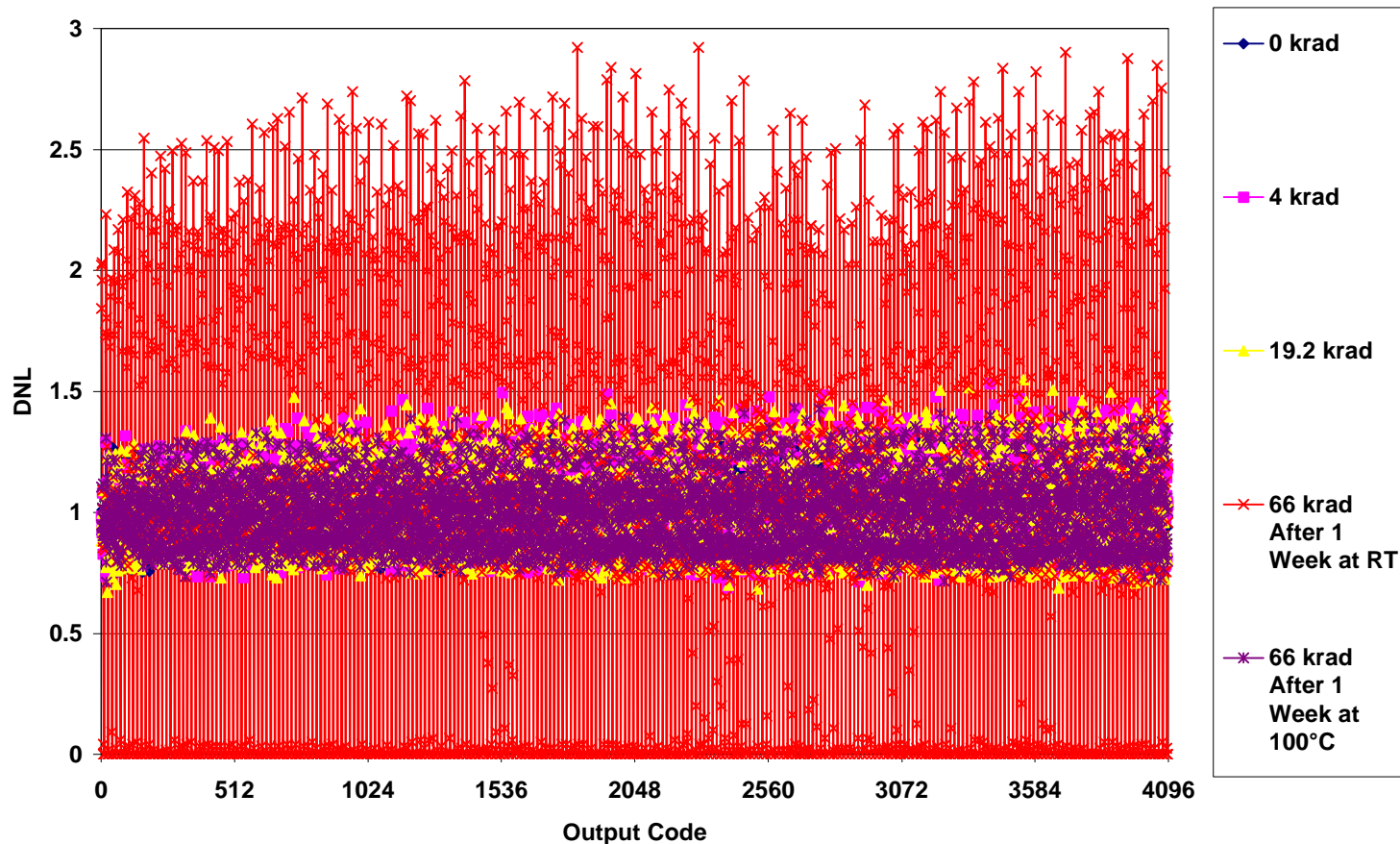
- ◆ no significant changes in DNL until after the 100 °C bake when #1 and #2 (un-biased during irradiation) showed increases in DNL – though the DNL for the LTC1415 was in general higher than for AD9223 and the changes in DNL were not dramatic.
- ◆ DNL varied with operating conditions and was better at some times than at others, nevertheless changes for devices #1 & #2 are probably significant.

## ■ No significant changes in INL for either device

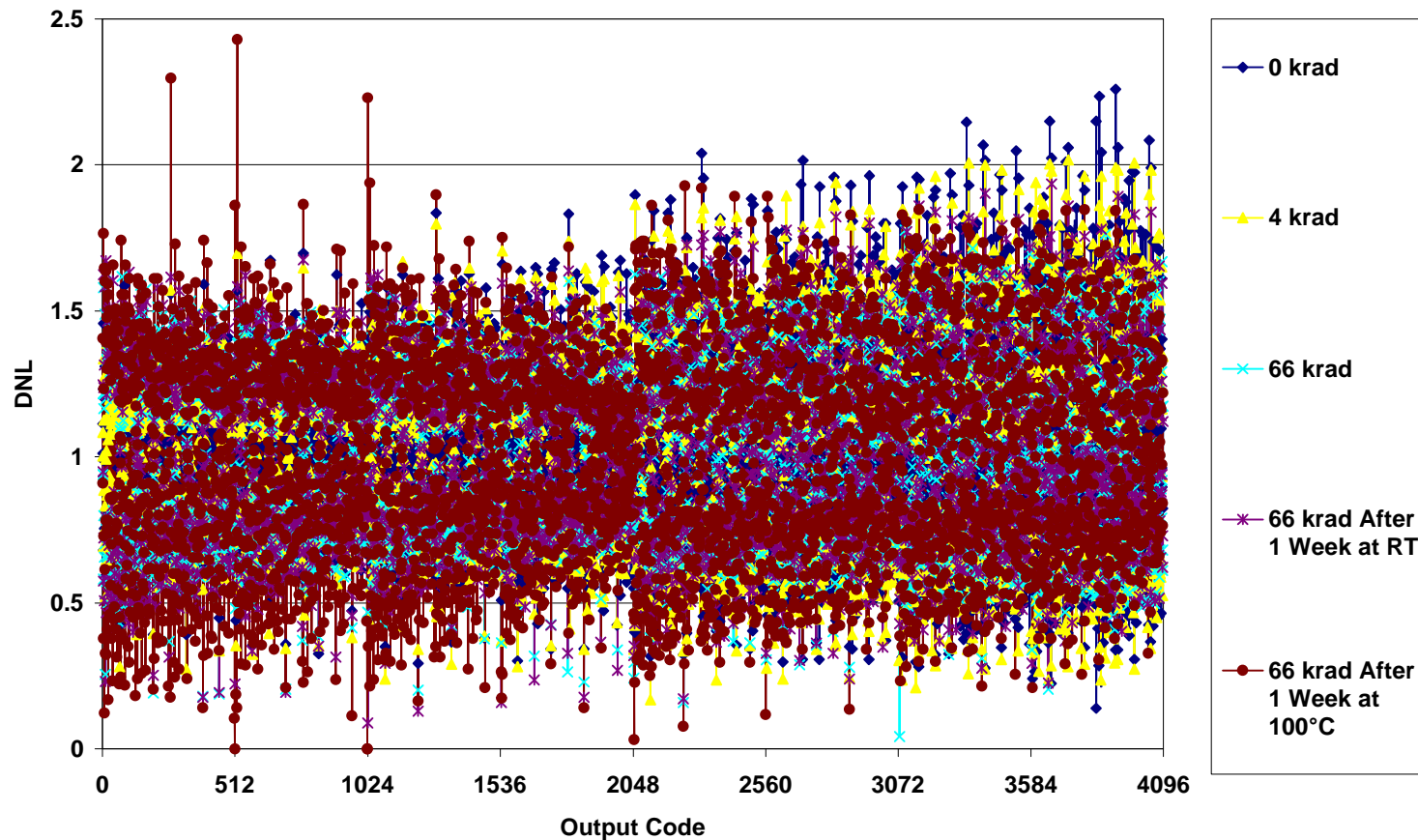
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# AD9223 DNL for #4 (Temporarily Failed)

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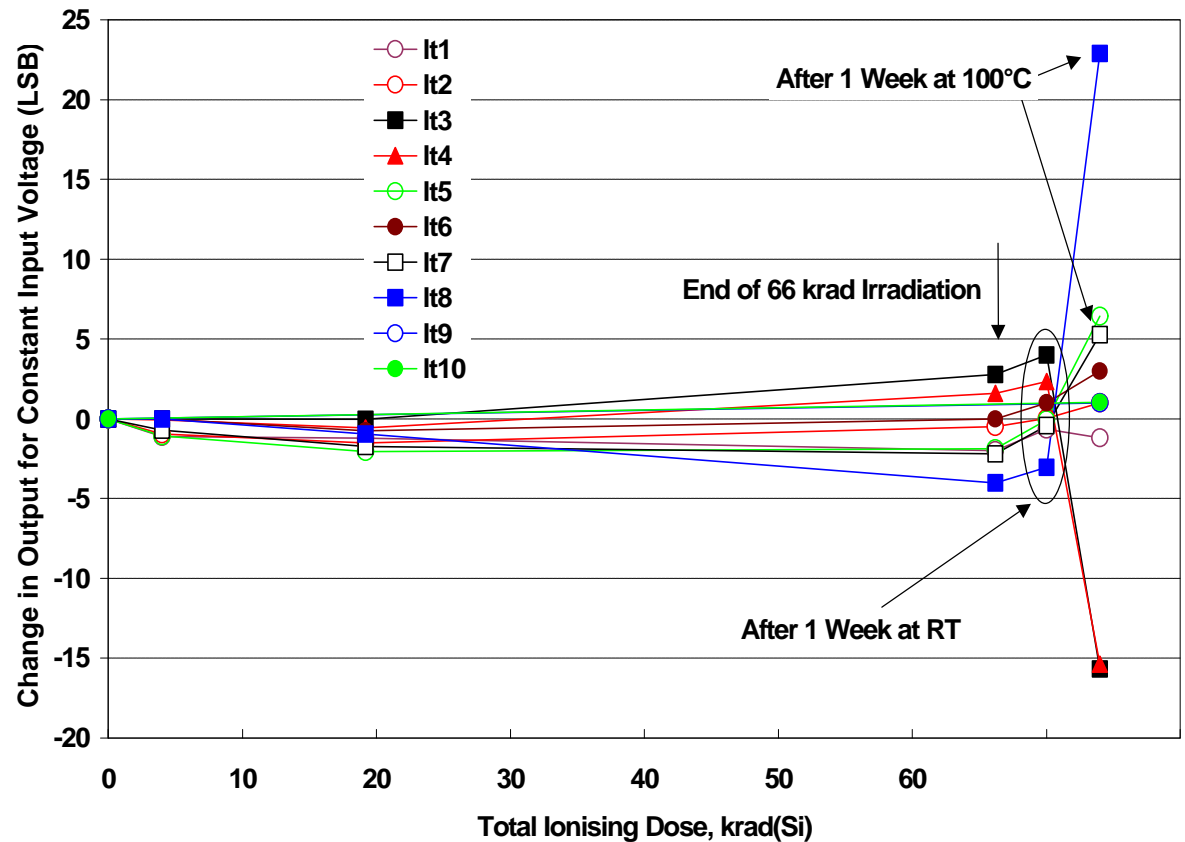
## LTC1415 DNL for #2





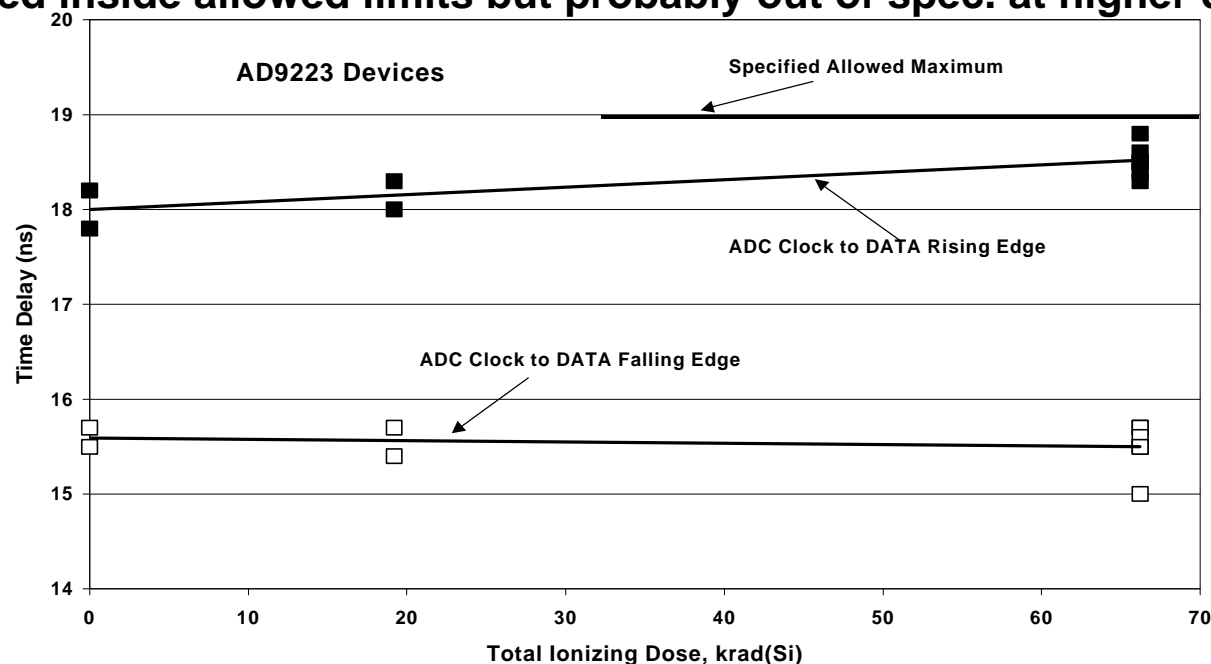
# Co-60 ADC Results, Offset

- LTC1415 #s 3, 4 and 8 showed shifts in offset after the 100C bake



# Co-60 ADC Results, Timings

- Delay time between clock and rising/falling edge of data is important.
  - ◆ remained inside allowed limits but probably out of spec. at higher doses.



- The LTC1415 BUSY clock can be used to latch data into an instrument. Data set up time ( 'data ready before busy' ) is important.
  - ◆ should be > 20 ns for correct operation, easily satisfied all devices

# Co-60 ADC/SEL Results

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- **Noise: no significant change**
- **Threshold voltages: no significant change**
- **Latch-up: LTC1415**
  - ◆ **No latch-up after maximum LET of 28 MeV/mg/cm<sup>2</sup> and fluence 5.3 x10<sup>6</sup>/cm<sup>2</sup>.**

# ADC Latch-up Tests

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- **Three de-lidded devices were tested, one from the current CHRIS flight batch A63155.1, date code 9702 (device #2) and two (devices # 1 and 3) from another batch (AG3710.1, date code 9644).**

$^{40}\text{Ar}^{8+}$  ions, (energy 150 MeV), normal incidence **LET 14.1 MeV/mg/cm<sup>2</sup>**

device #1

average cross section =  $4.5 \cdot 10^{-7} \text{ cm}^2$

device #2

average cross section =  $2.2 \cdot 10^{-6} \text{ cm}^2$

device #3

average cross section =  $3.5 \cdot 10^{-7} \text{ cm}^2$

$^{20}\text{Ne}^{4+}$  ions, (energy 78 MeV), 60° incidence **LET 5.85 x 2= 11.7 MeV/mg/cm<sup>2</sup>**

no latch-up seen after  $4.1 \cdot 10^6 \text{ ions/cm}^2$

- **threshold for latch-up is ~ 12 MeV/mg/cm<sup>2</sup>**
  - **Expect the saturation cross section is in the range  $2 \cdot 10^{-2}$  to  $2 \cdot 10^{-4} \text{ cm}^2$**
  - **SEL protection circuit implemented on CHRIS**
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# ADCs: Conclusions

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## ■ AD9223

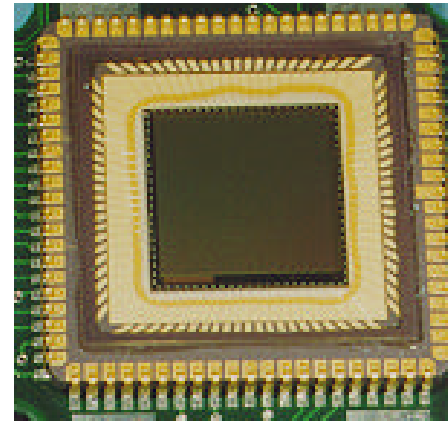
- ◆ Likely to fail at high dose rates after ~ 10 krad(Si): power supply current and 'stuck' bits
- ◆ Expected to be OK at low dose rates to > 66 krad(Si)
- ◆ Vulnerable to SEL

## ■ LTC1415

- ◆ Performance >66 krad(Si) marginal: some changes in DNL and offset after 100°C bake (rebound ?)
- ◆ No SEL after 28 MeV/mg/cm<sup>2</sup>

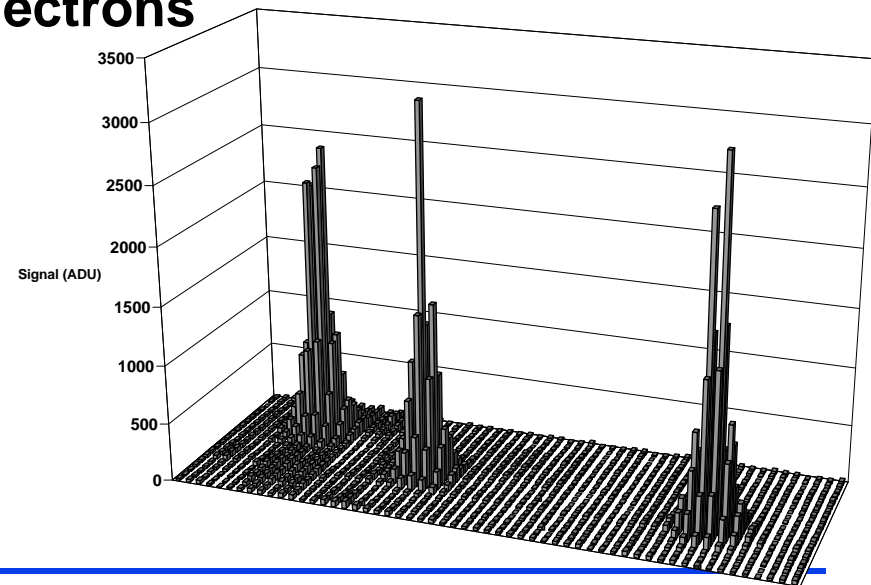
# ASCoSS APS

- Designed by IMEC for demonstrator star tracker for the ESTEC project 'Attitude Sensor Concepts for Small Satellites'.
- 512 x 512 25  $\mu\text{m}$  x 25  $\mu\text{m}$  pixels, 17  $\mu\text{m}$  epi thickness
- Photodiode detectors, CMOS readout High fill factor (~85%) but low MTF (in current version)
- Windowing and short integration time allowed (but reset fault)
- good noise and fixed pattern behaviour (~ 50 electrons) : rivals CCDs in star tracker applications
- On-chip '8-bit' ADC
- CVF ~ 8.5  $\mu\text{V}/\text{electron}$
- Full-well ~ 140,000 electrons



# ASCoSS APS: CVF Determination

- Could not use X-ray method: diode volume too small
- Could not use mean-variance method: some pick-up present
- IMEC design and off-chip gain leads to  
*45 electrons/ADU*
- 5.5 MeV alpha particle check gives 40 e/ADU assuming an average event size of  $1 \times 10^6$  electrons  
(events have to be in the range  $7 \times 10^5$  to  $1.5 \times 10^6$  el )



# ASCoSS APS: Dark Signal

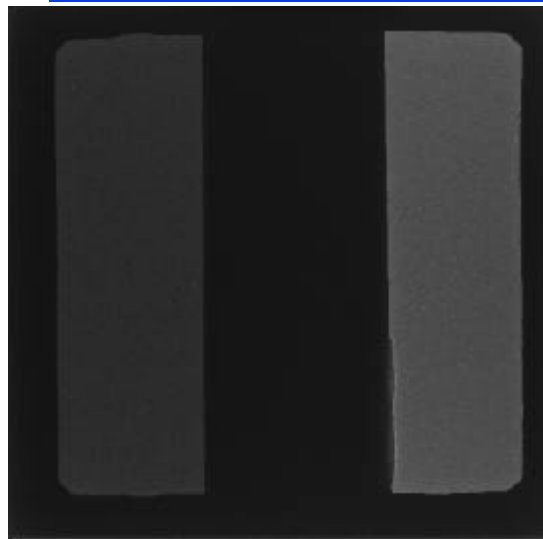
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- **Need to distinguish between thermal dark signal and fixed pattern noise (FPN)**
- **FPN approximately independent of temperature and integration time and ~ 5 ADU (230 es)**
  - need to subtract for accurate work
- **Proton irradiation gives dark current spikes**
  - localised to a pixel
  - tend to be smaller than for CCDs
  - vary as expected with temperature
  - random telegraph signal behaviour
- **Co-60 gives uniform dark signal increase**
  - varies as expected with temperature
  - large increase but anneals

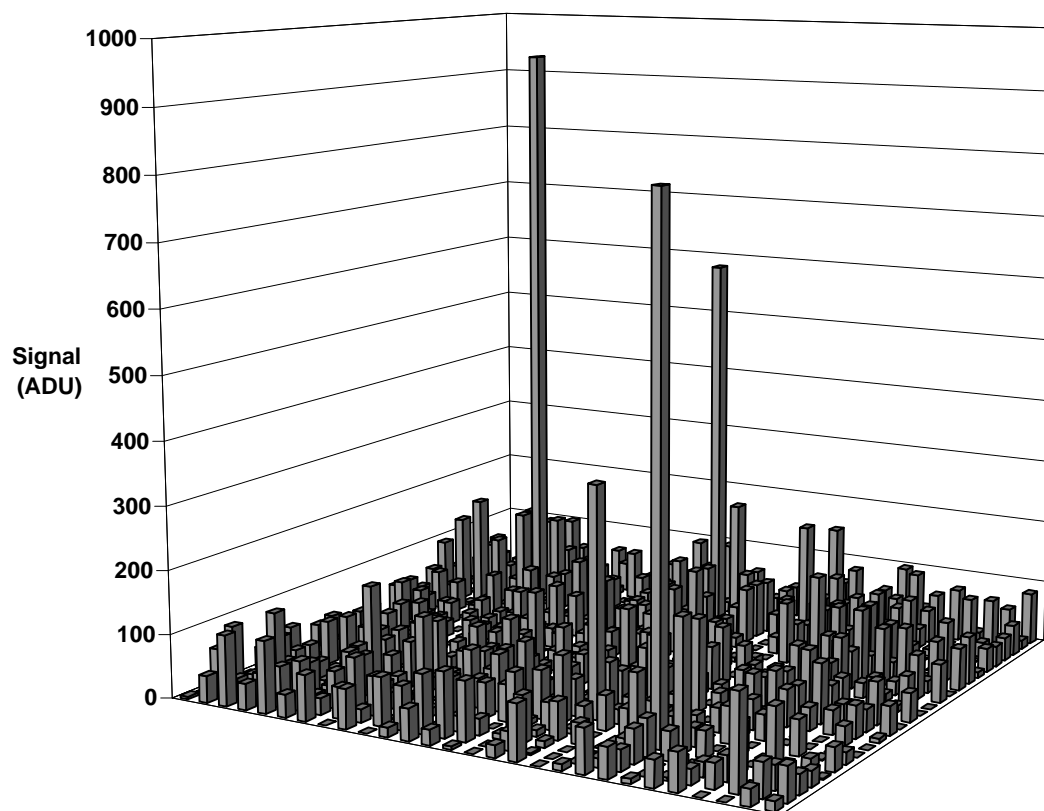


# ASCoSS APS: Dark Signal

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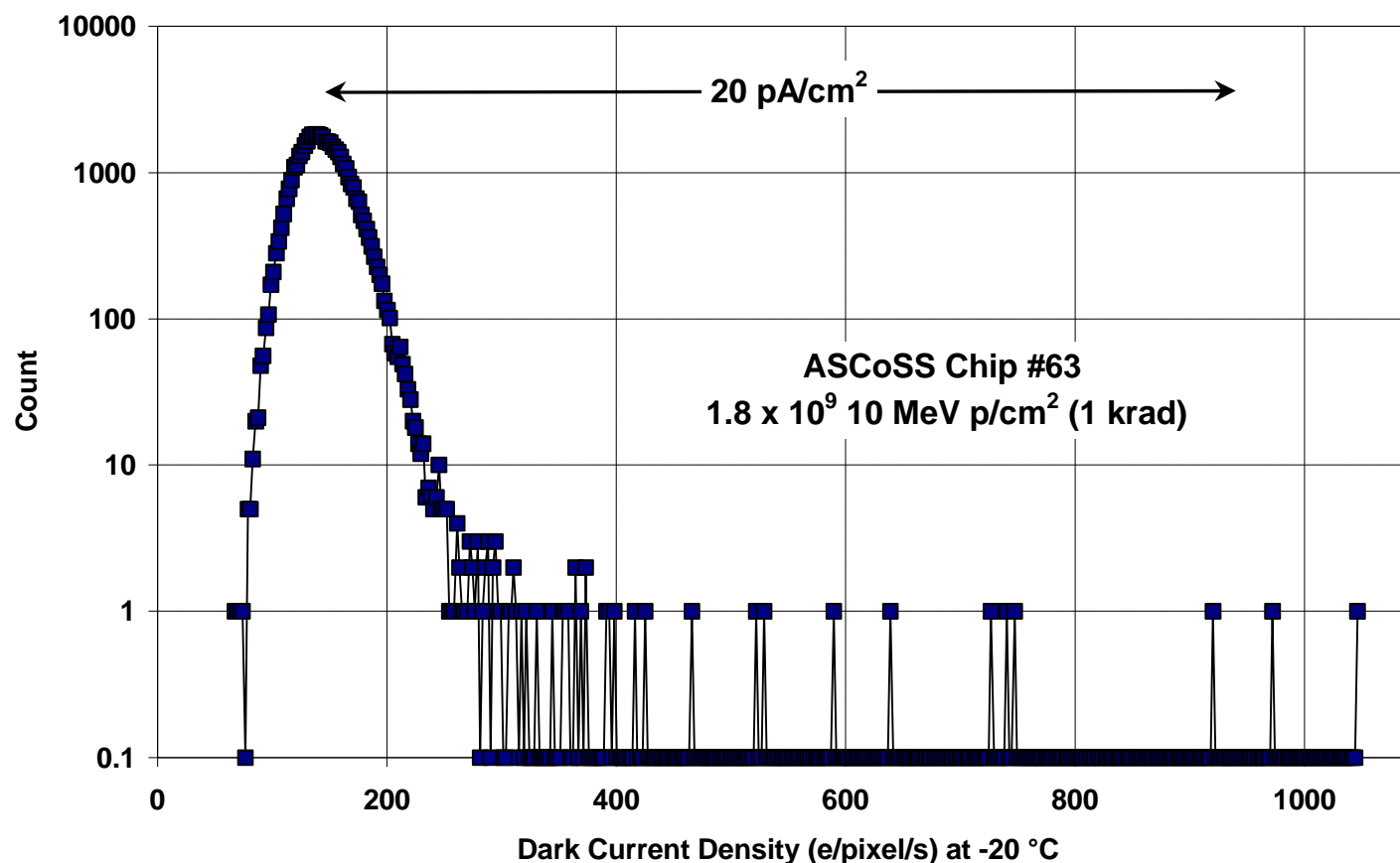


**10 MeV  
Proton  
Irradiation**



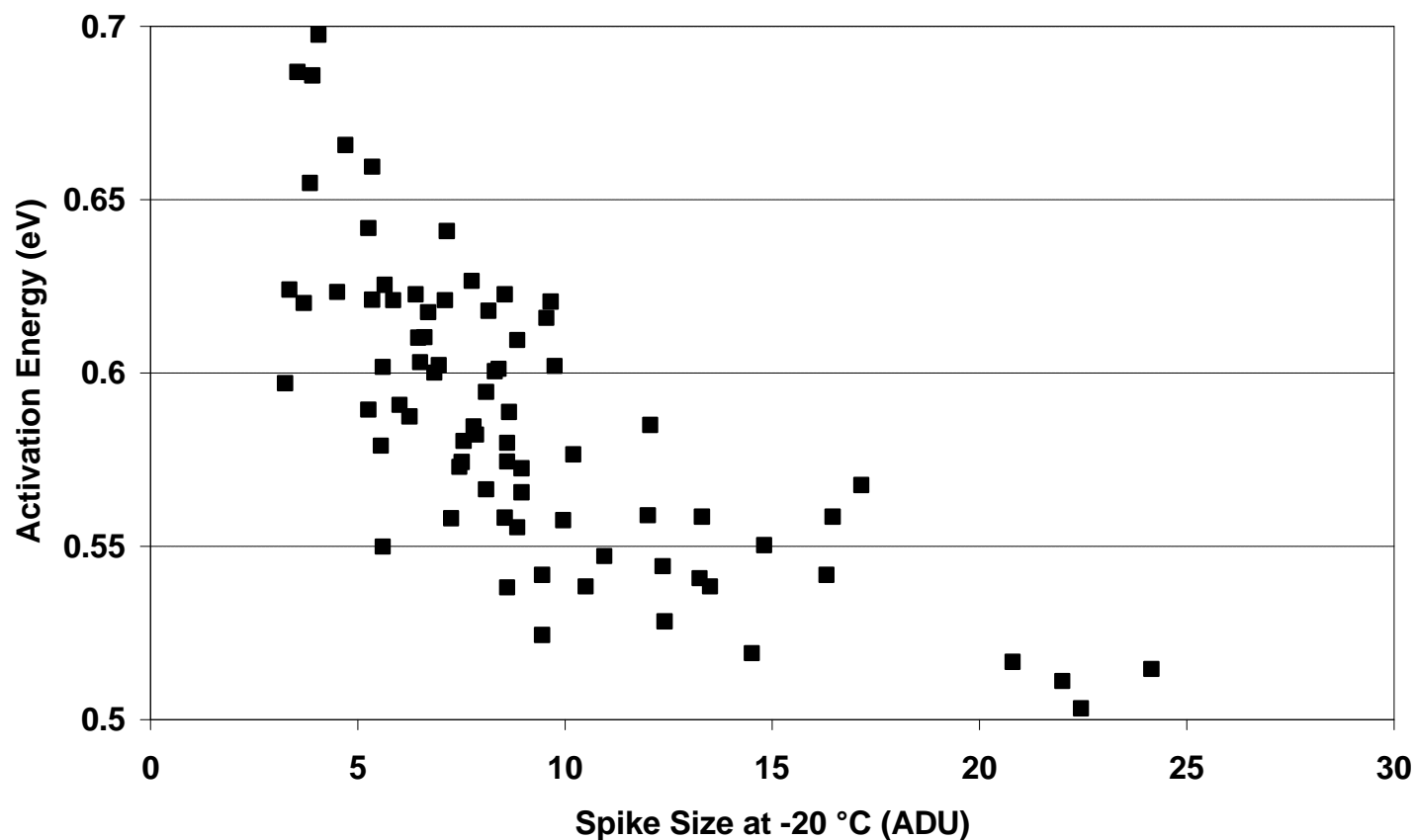
# ASCoSS APS: Dark Signal

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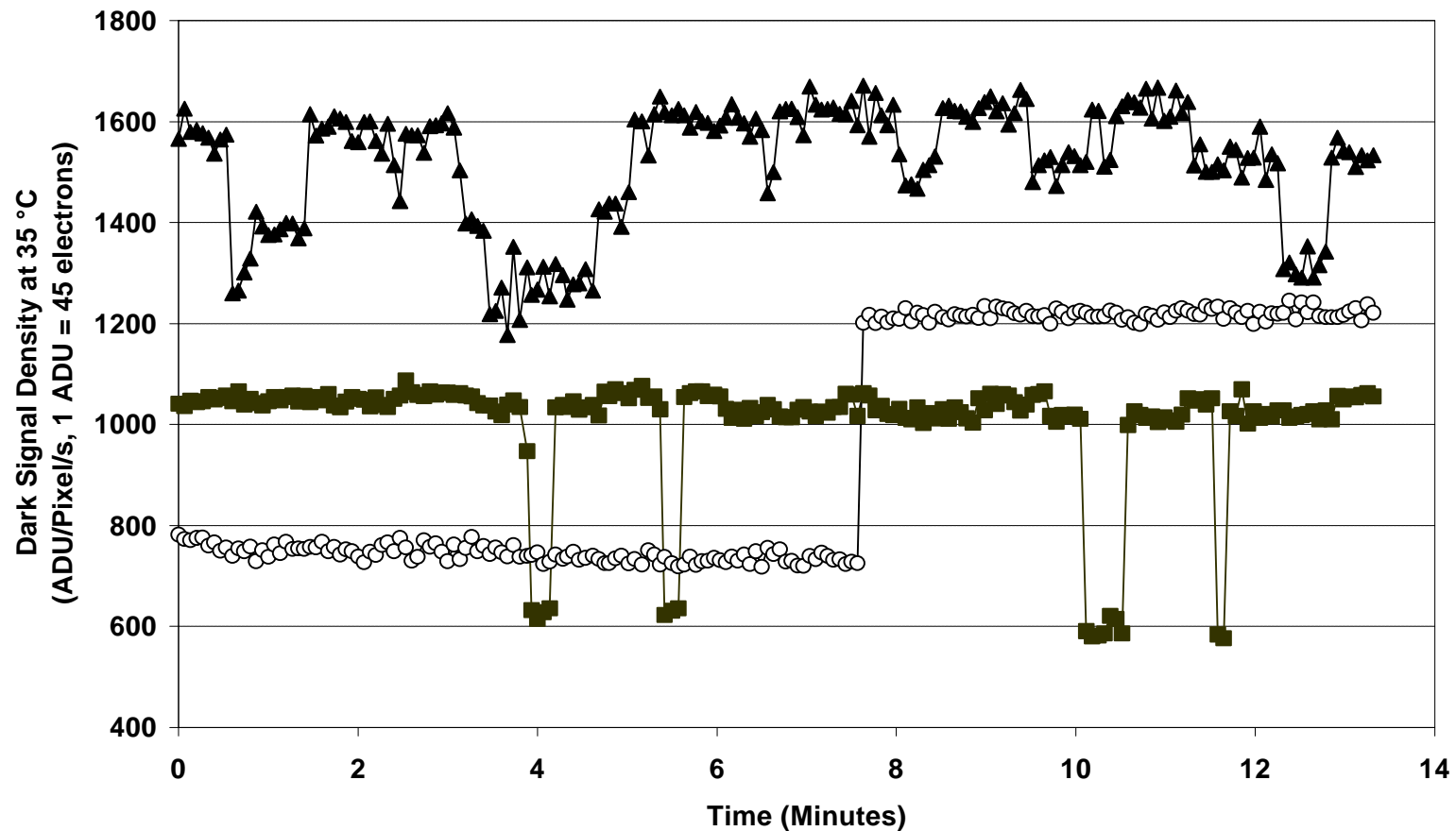


# ASCoSS APS: Dark Signal

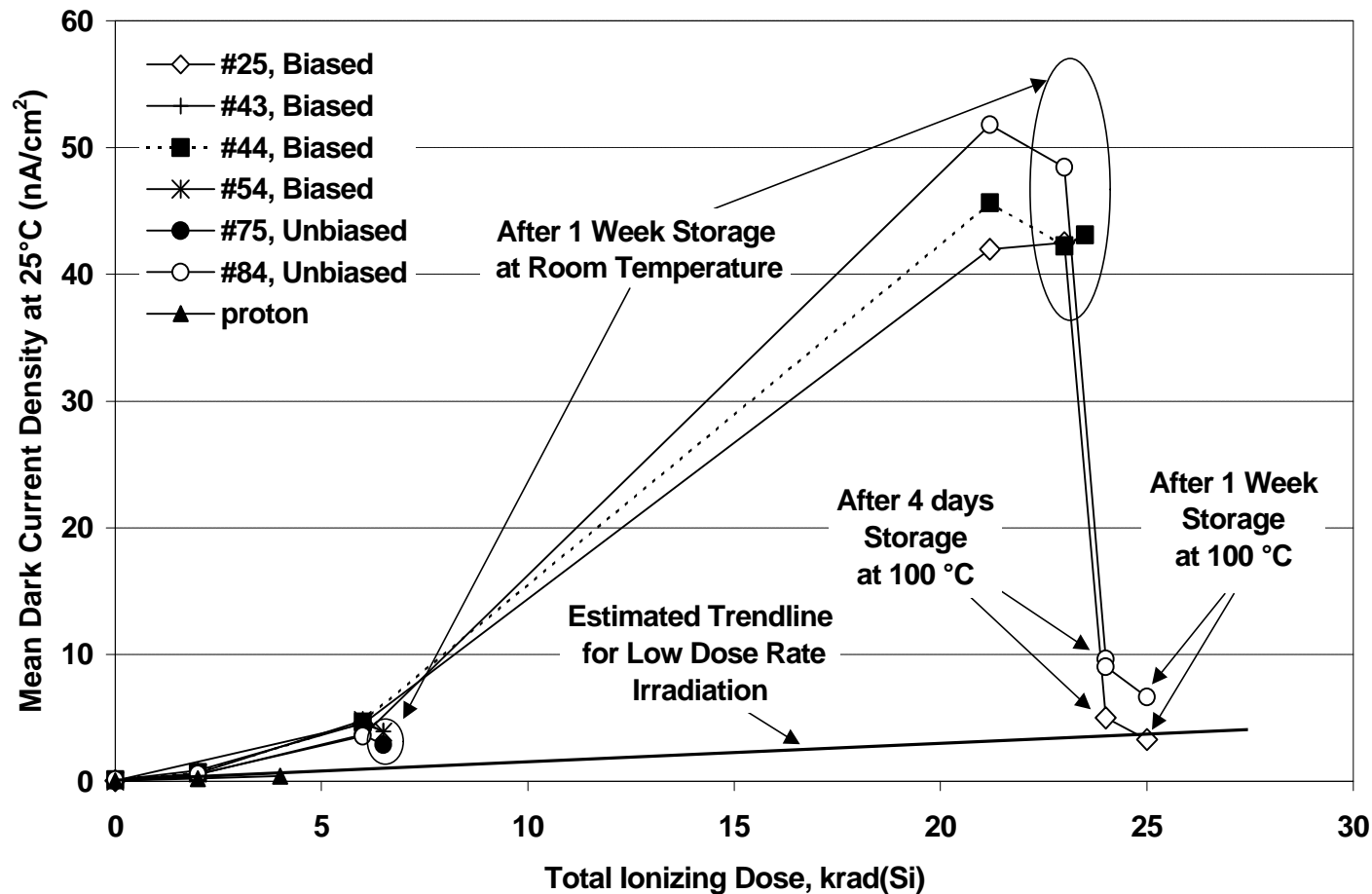
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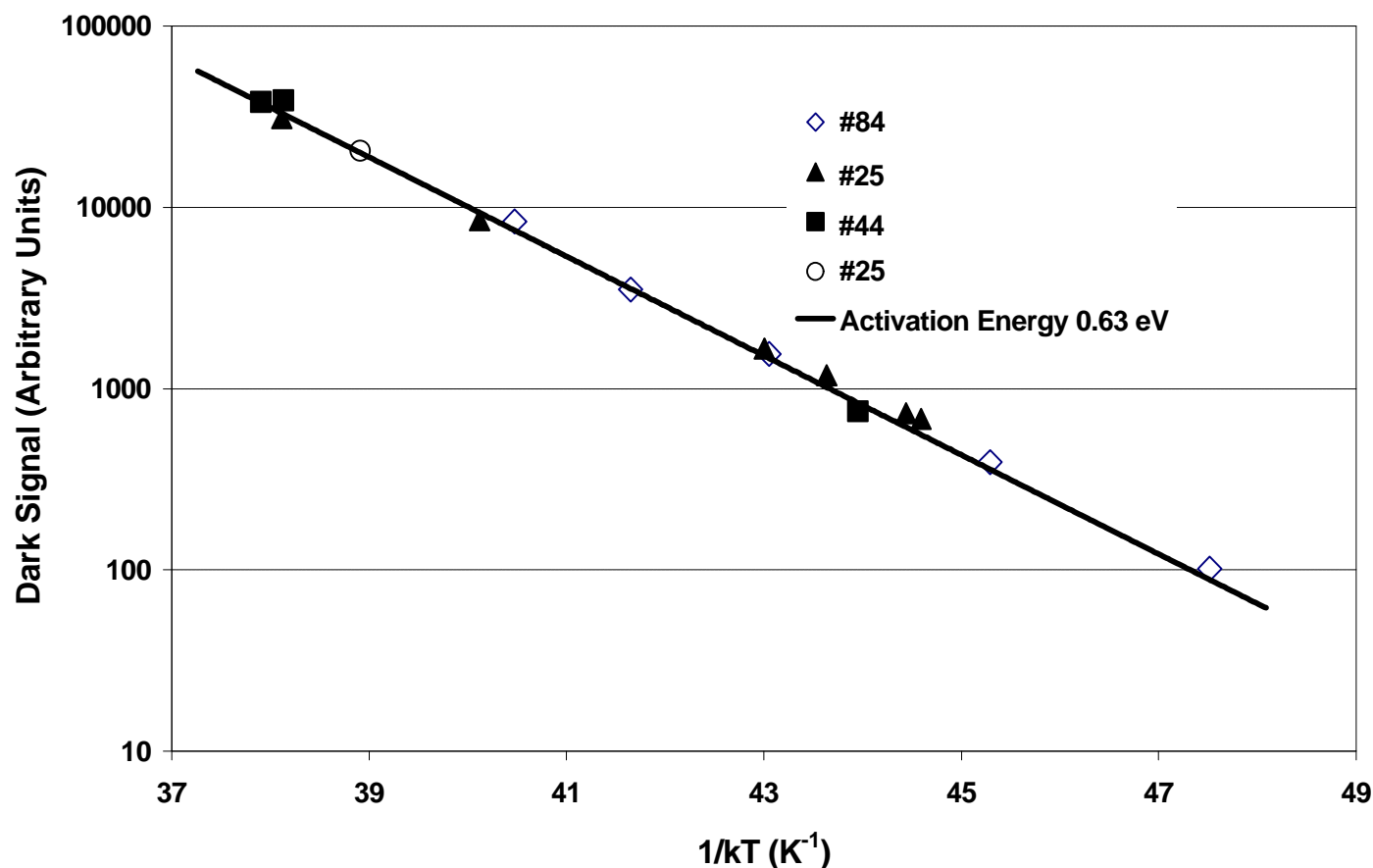
# ASCoSS APS: Dark Signal



# ASCoSS APS: Dark Signal



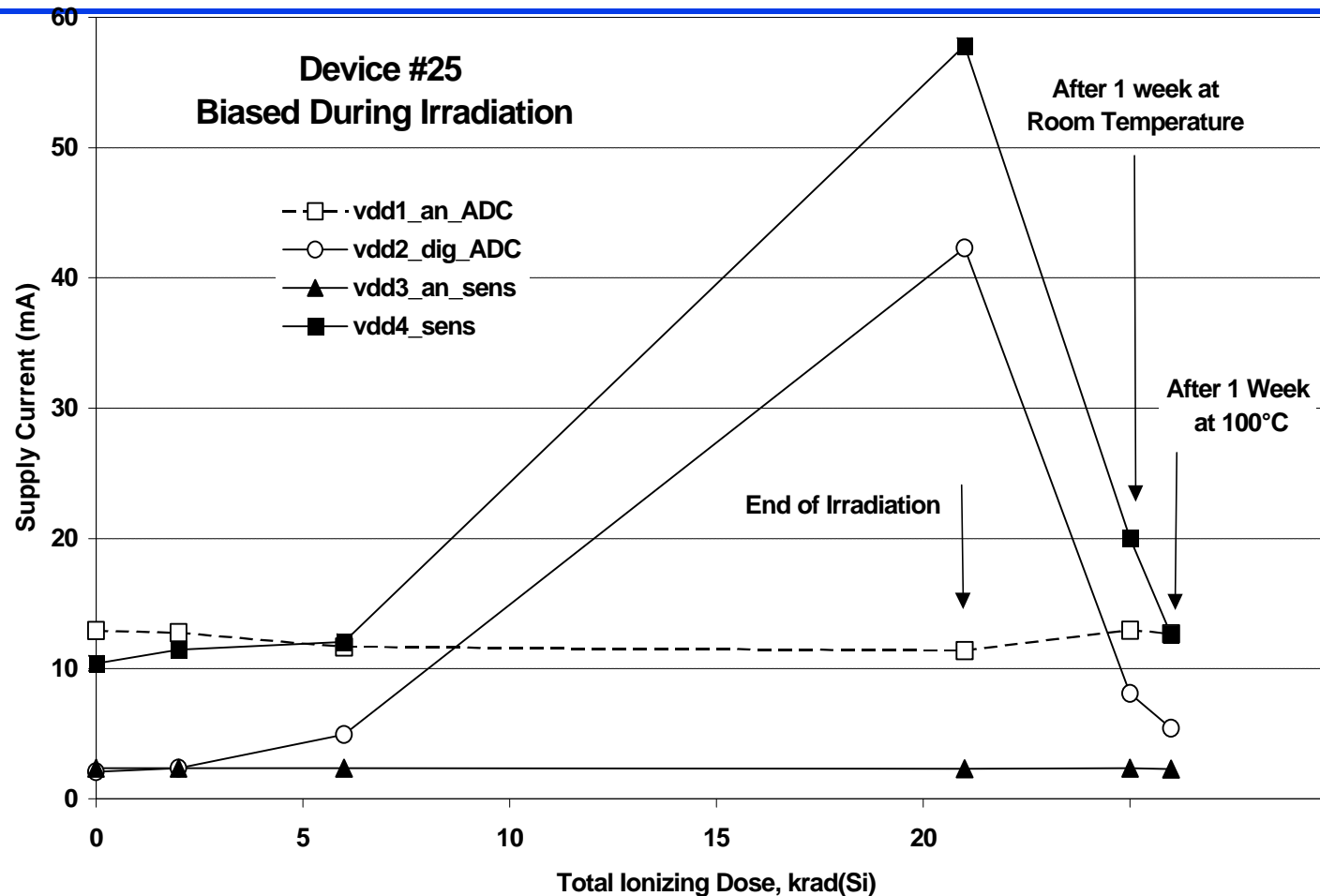
# ASCoSS APS: Dark Signal



# ASCoSS APS: Power Supply Currents

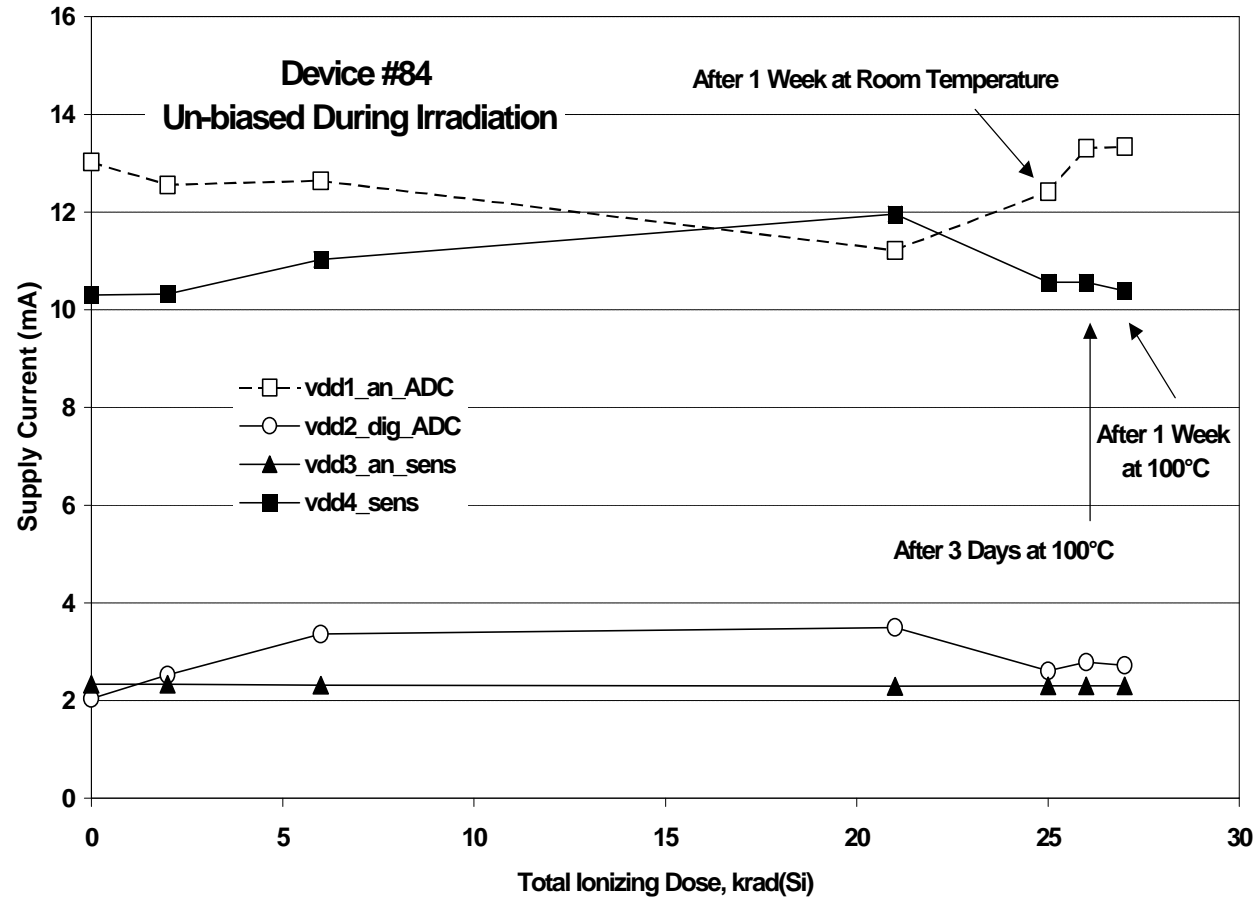
- Sharp increase in the Vdd1 (digital ADC) and Vdd4 (sensor) supplies after 6 krad(Si) for biased devices (but not the un-biased).
- After 21 krad the current limit to the board was nearly exceeded and significant heating of the devices occurred. Higher radiation doses without a current limit could potentially cause device damage: this may have happened with the earlier IMEC tests on IBIS 1 devices.
- There is significant post-irradiation annealing. However the annealing occurs at a somewhat variable rate: device #44 annealed with room temperature storage, whereas #25 needed a bake at 100°C.
- The other bias supplies were not greatly affected by the irradiation. There were some small changes in particular supplies but these annealed out. The ADC reference voltage remained unchanged.
- It is possible that parasitic leakage paths (e.g. in a field oxide) are being turned on just above 6 krad(Si). Annealing of flatband shift would result in a sharp return to normal current levels.

# ASCoSS APS: Power Supply Currents





# ASCoSS APS: Power Supply Currents



# ASCoSS APS: Other Co-60 data

## ■ Threshold Voltage Shift

- ◆ Thresholds for ADC CLOCK, ADC CLOCK\_XRD and ADC SYNC\_XRD were monitored. These supply the three different types of input gate structure used on the device. changes were small (of the order of 0.1 V or less after 21 krad(Si)).

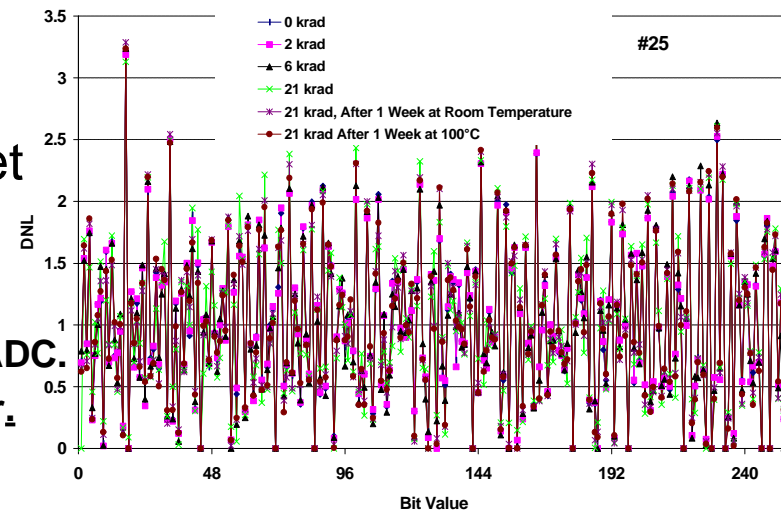
## ■ On-chip ADC Performance

- ◆ No change in DNL
  - (7-bit performance at start)
- ◆ small (few LSB) changes in offset
- ◆ shows SEL:

threshold  $\sim 19.9 \text{ MeV/mg/cm}^2$

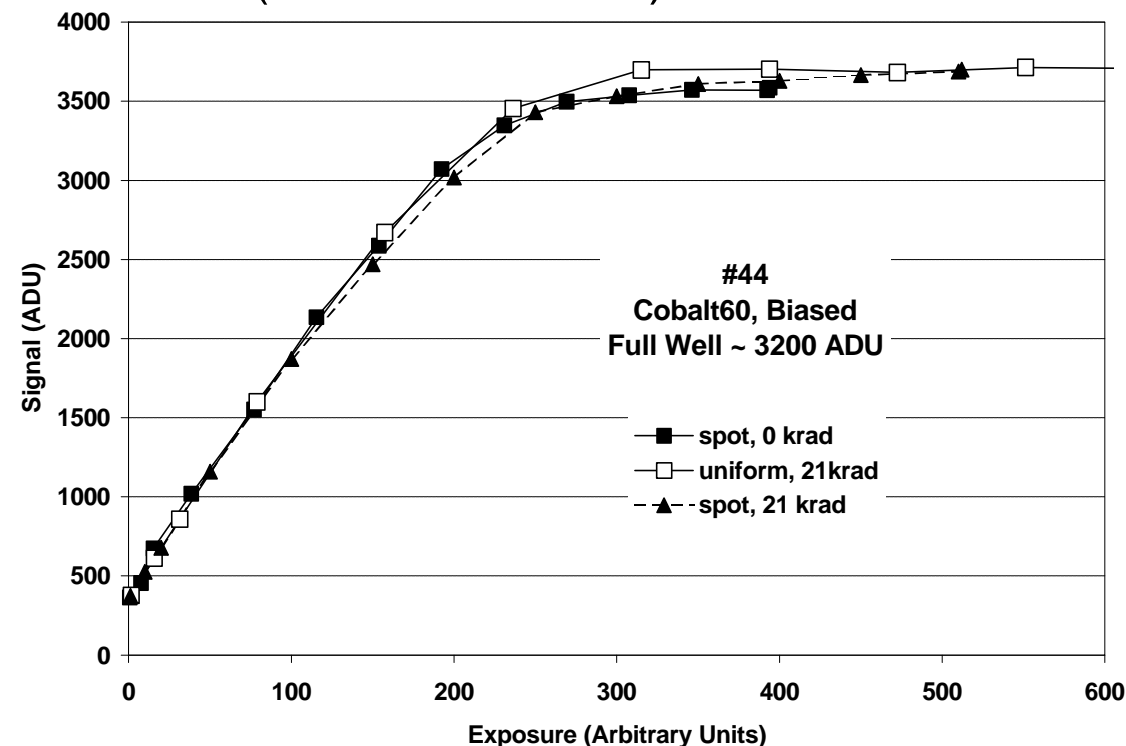
saturation cross section  $i > 2.2 \cdot 10^{-6} \text{ cm}^2$  for on-chip ADC.

Threshold  $> \text{LET } 28.2 \text{ MeV/mg/cm}^2$  rest of the sensor.

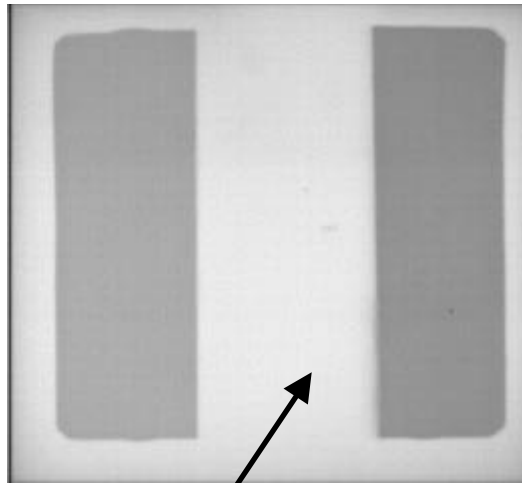


# Linearity and Full-well

- Slight 'roll-off' in linearity at high signal levels, particularly for spot illumination, but no significant change with radiation, full well capacity remaining at ~ 3200 ADU (14400 electrons)



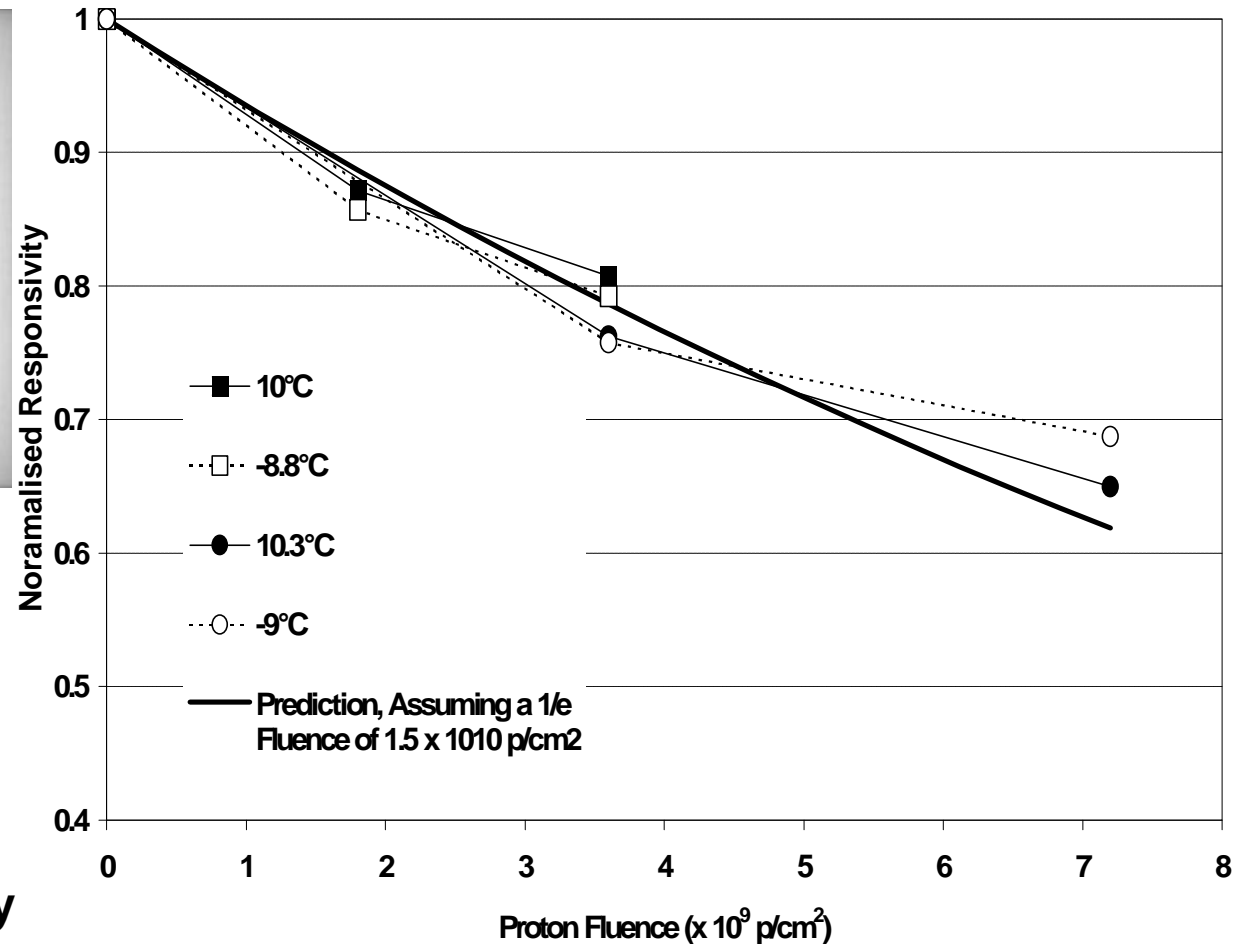
# ASCoSS APS: Responsivity



After Proton (also alpha) Irradiation.

No change in PRNU (~2%)

Co-60 showed no change in responsivity



# CCD Tests: Test Objects

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## ■ Two EEV CCD47-20 devices:

CCD47-20-2-231A (grade 2)

CCD47-20-5-231A (grade 5), both irradiated but only the grade 2 used

- ◆ frame transfer mode
- ◆ 1024 x 1024 image area pixels
- ◆ 13  $\mu\text{m}$  x 13 $\mu\text{m}$  pixels, no supplementary buried channel
- ◆ Advanced IMO (can only clock image and store registers forwards)
- ◆ no store shield
- ◆ non-antibloomed
- ◆ dump gate
- ◆ split readout register

# CCD Tests: Test Objects

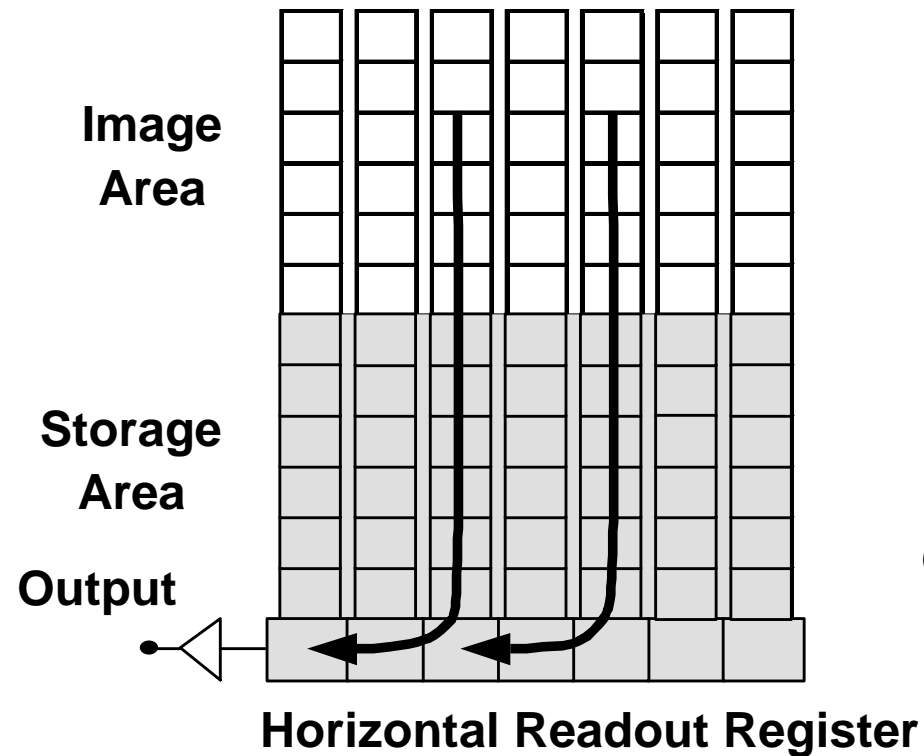
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- **Two EEV CCD02 devices:**
  - ◆ One IMO device, One AIMO device
  - ◆ frame transfer mode
  - ◆ 288 x 385 image area pixels
  - ◆ 22  $\mu\text{m}$  x 22  $\mu\text{m}$  pixels, no supplementary buried channel
  - ◆ With advanced IMO (can only clock image and store registers forwards)
  - ◆ no store shield
  - ◆ non-antibloomed
  - ◆ no dump gate

# CCD Architecture

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## *Frame Transfer CCD*



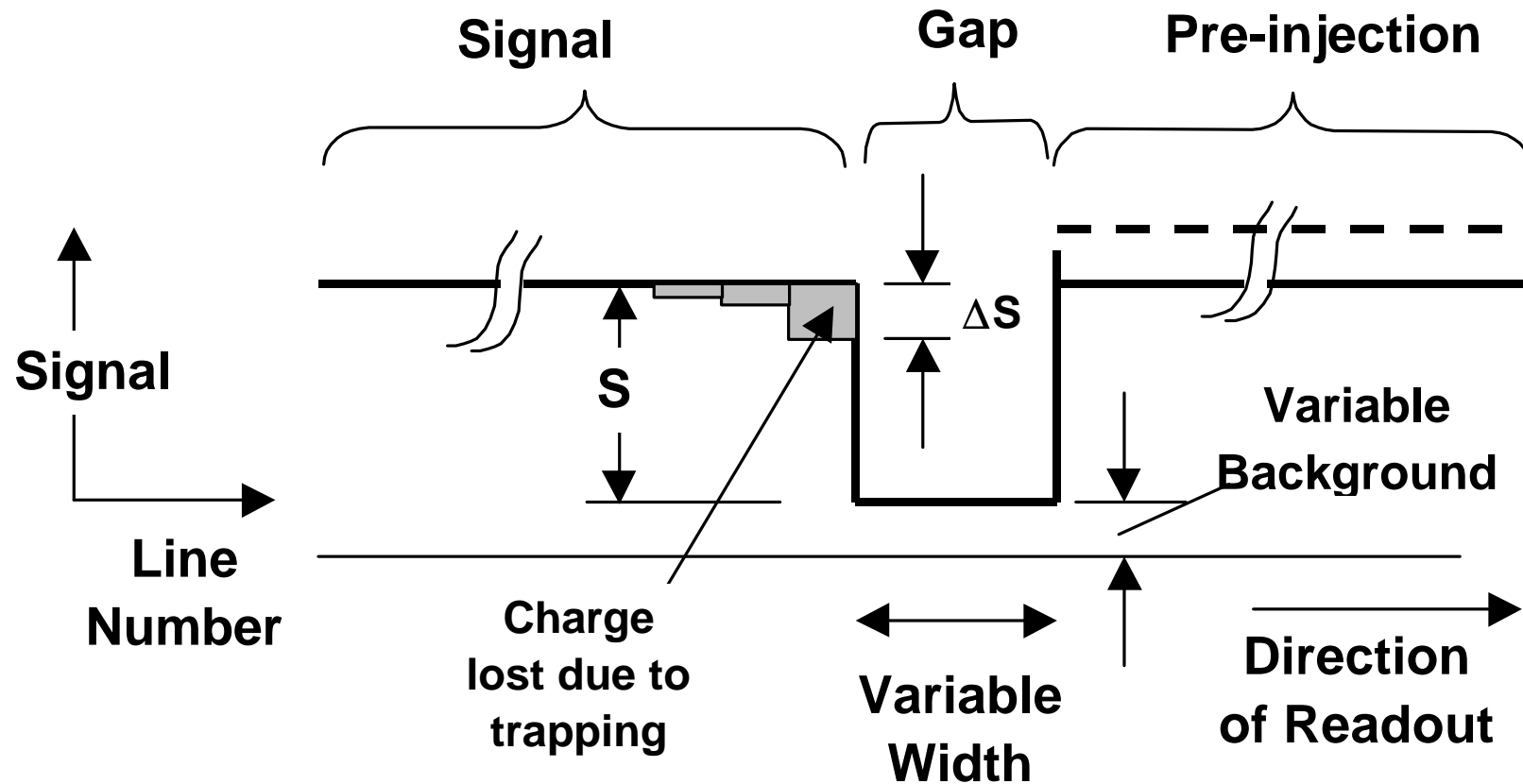
# Vertical CTI

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- Charge Transfer Efficiency = CTE =  
Fraction charge lost / No. of pixel transfers
- $CTI = 1 - CTE$
- Will measure 'worst case CTI' : all traps empty
- Worst case CTI depends on:
  - ◆ Signal Size
  - ◆ Background charge
  - ◆ dwell time in a pixel (I.e. line move time - so dependence of position in the image)
- Does NOT depend on temperature



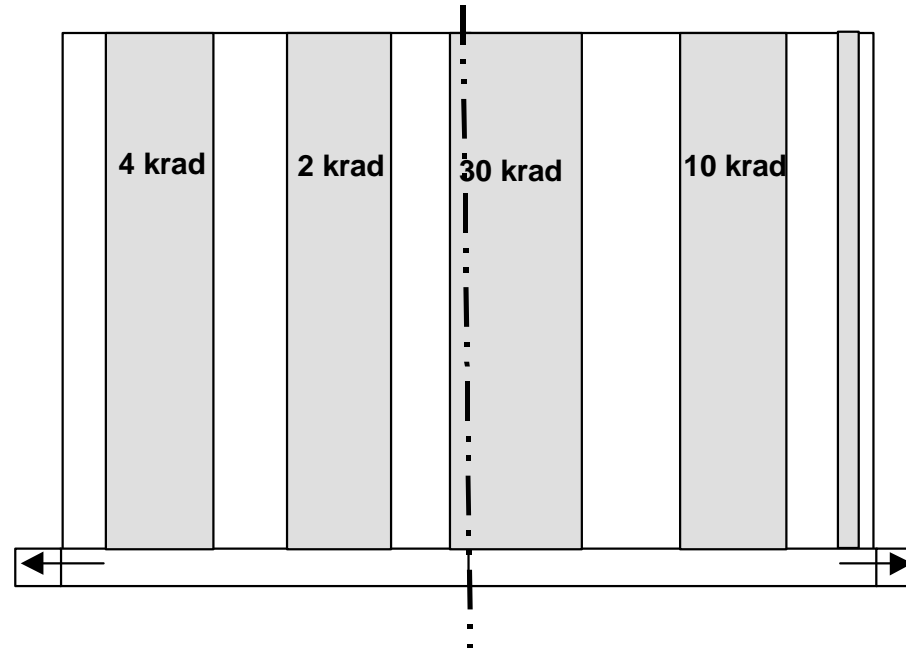
# CCD: CTI Measurements Using FPR



# Irradiations

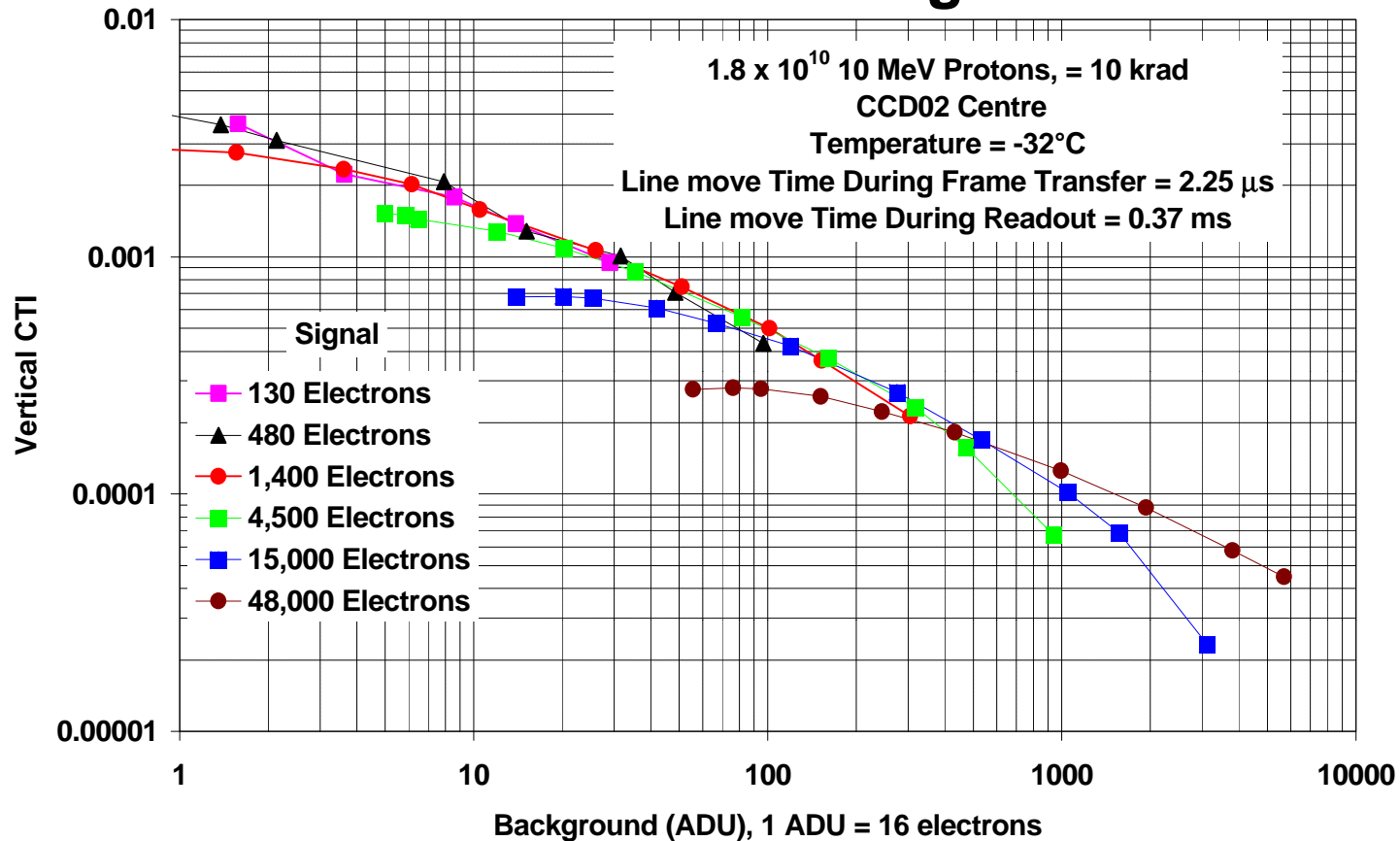
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- carried out on 7 December 1998
- Harwell Tandem Van de Graaff accelerator
- 10 MeV protons, normal incidence, unbiased, room temperature
- fluence regions:
- 1.5 mm Al masks

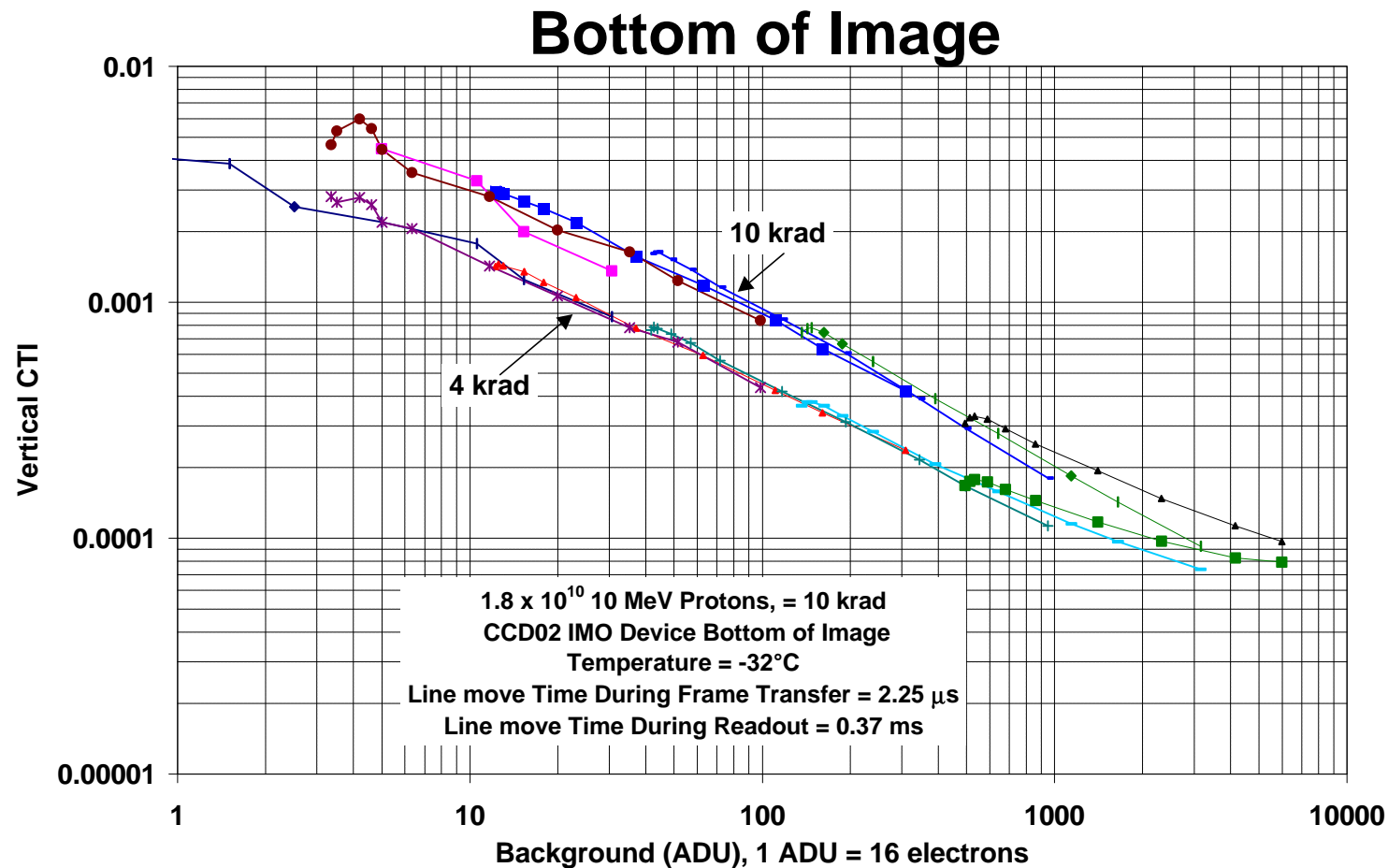


# FPR Results, CCD02

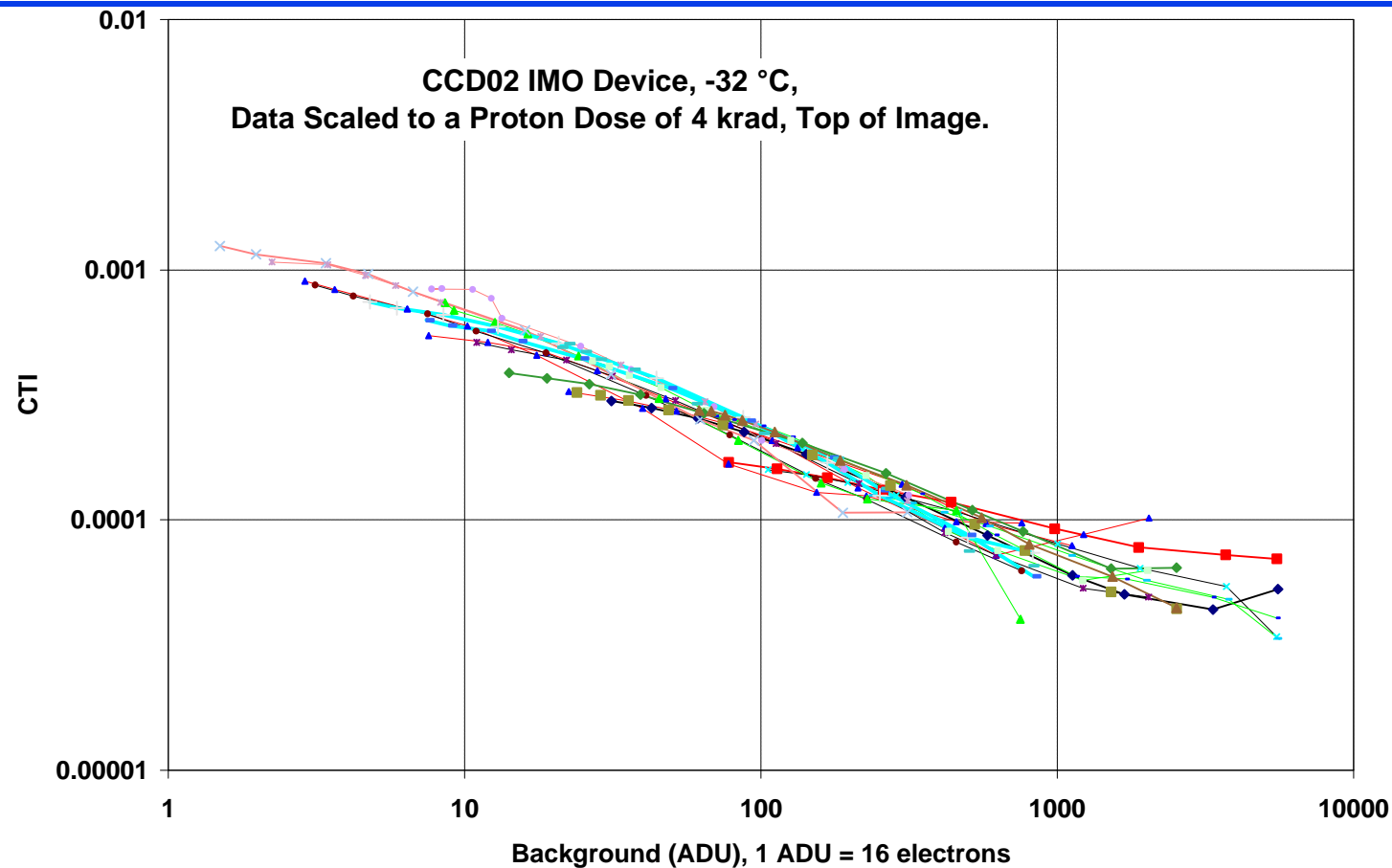
## Centre of Image



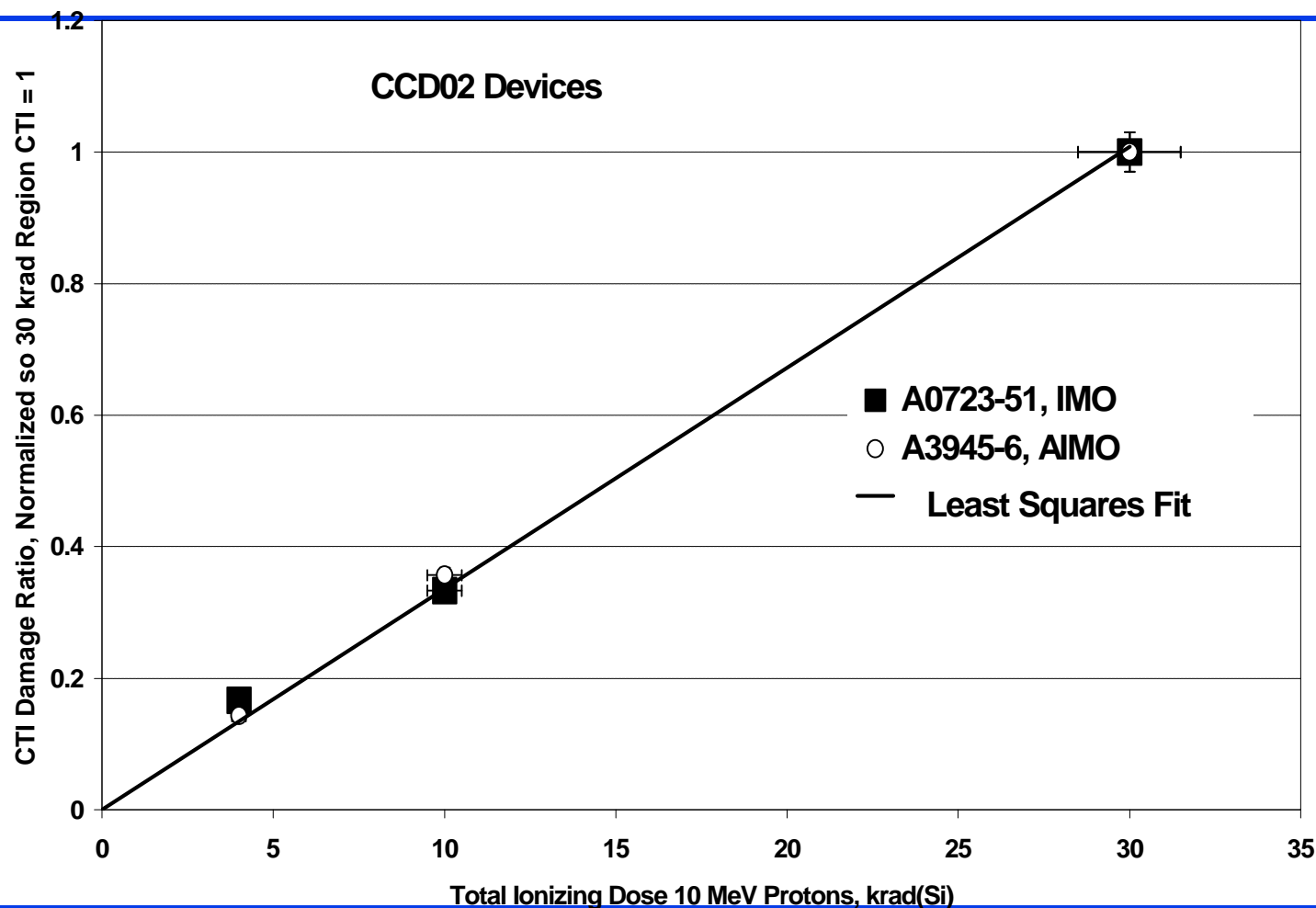
# FPR Results, CCD02



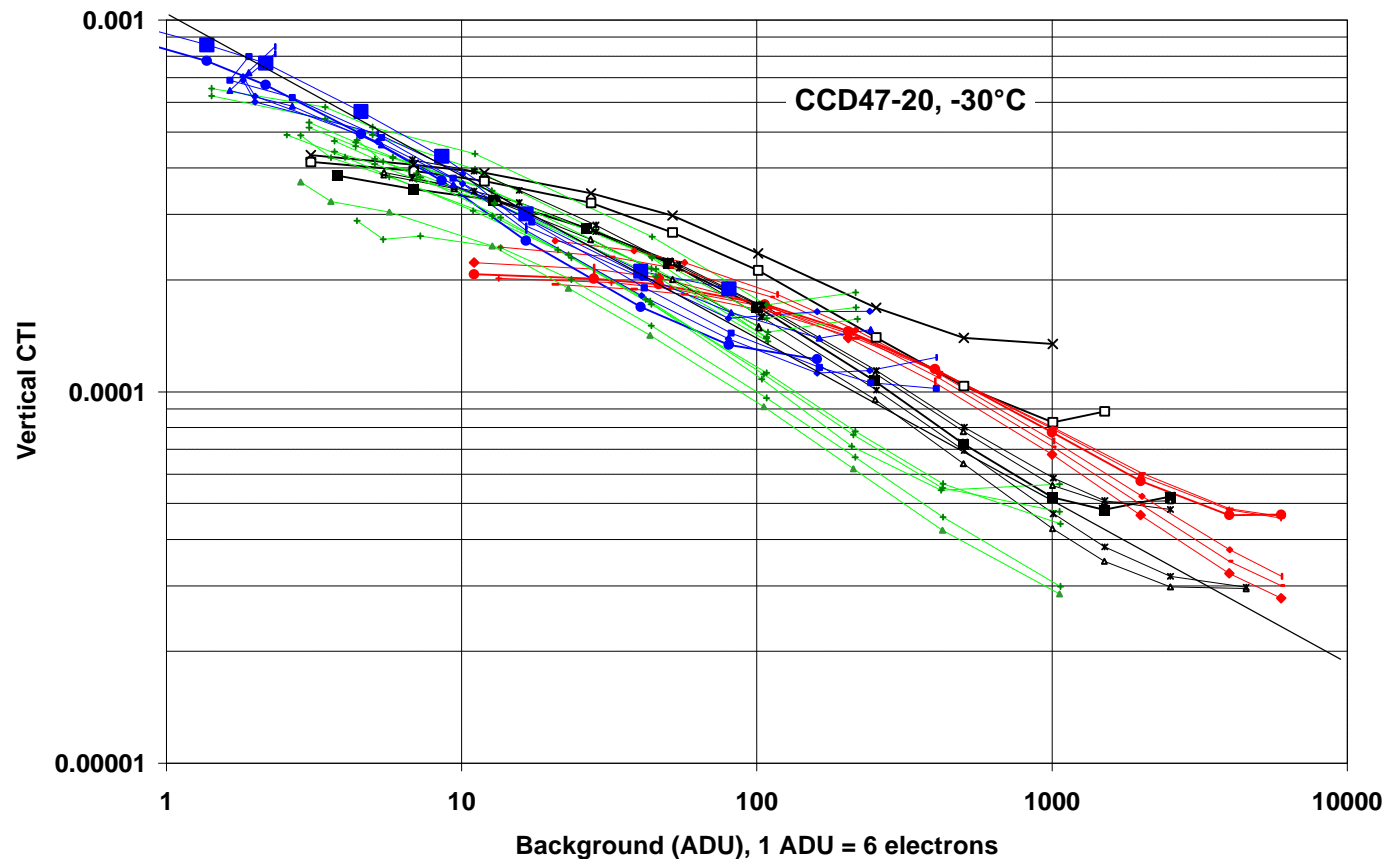
# FPR Results, CCD02



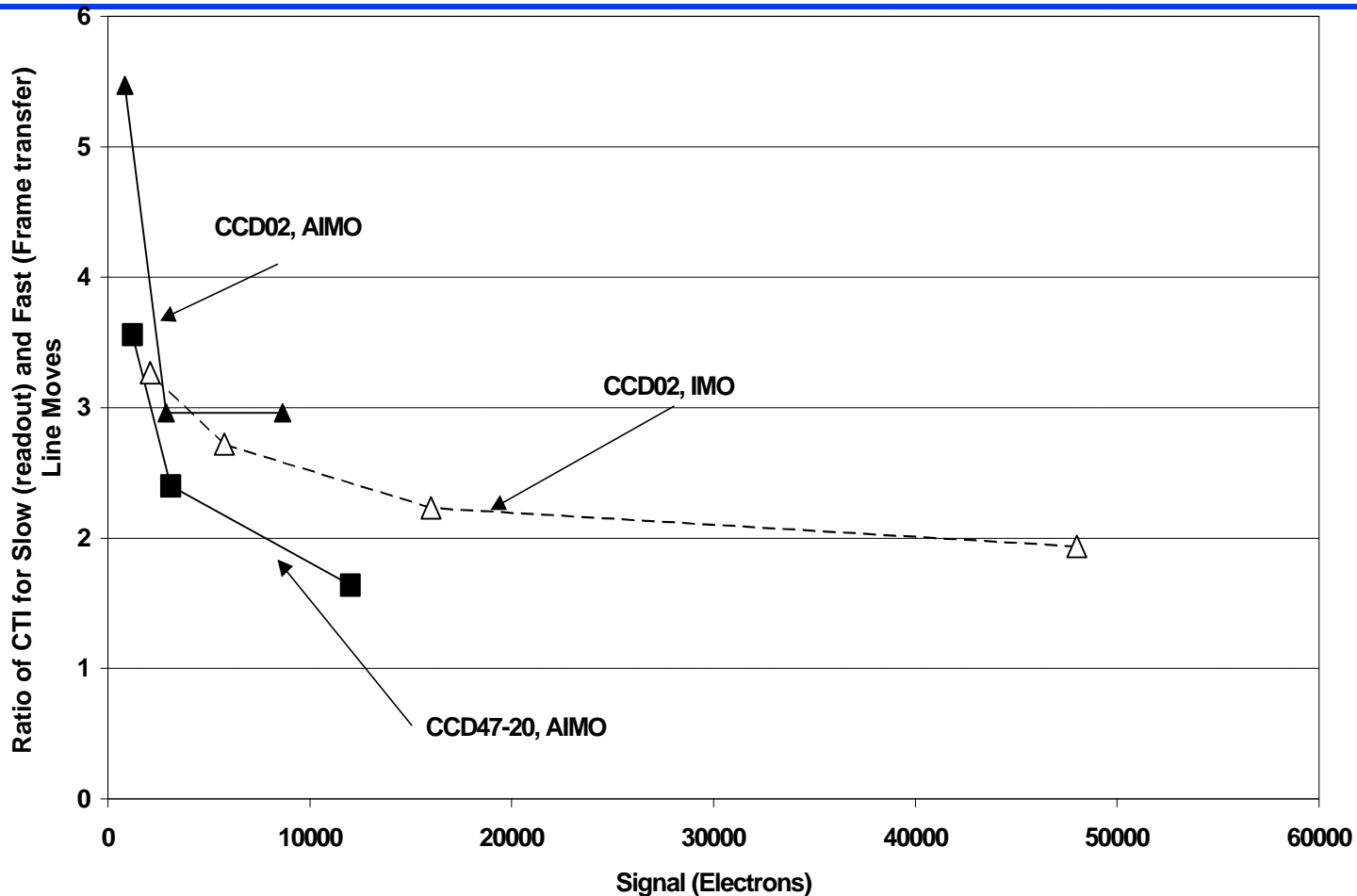
# FPR Results, CCD02



# FPR Results, CCD47-20



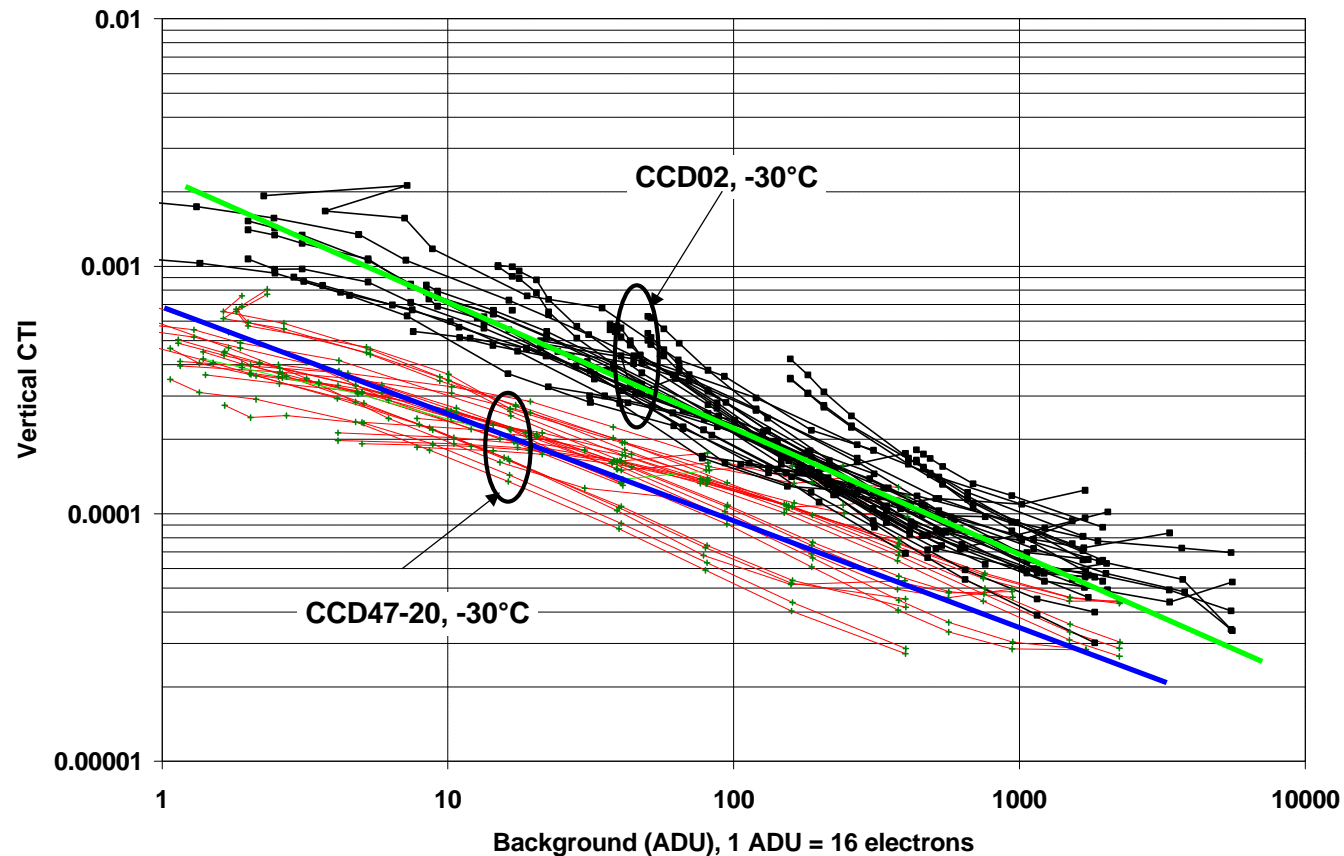
# FPR Results, CTI v. Dwell Time





# FPR Results: CCD02 & CCD47-20

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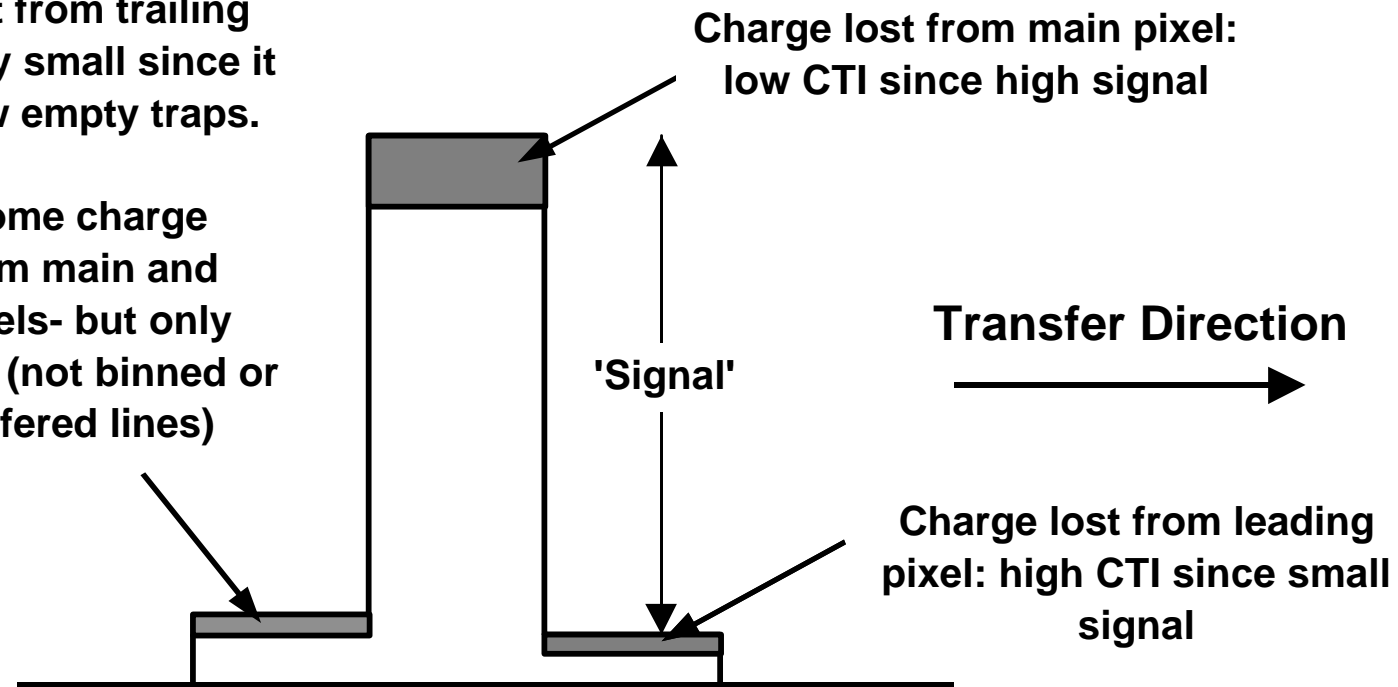


# Effect of CTI on Star Images

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Charge lost from trailing pixel is very small since it sees no few empty traps.

However some charge differed from main and leading pixels- but only for readout (not binned or frame transferred lines)



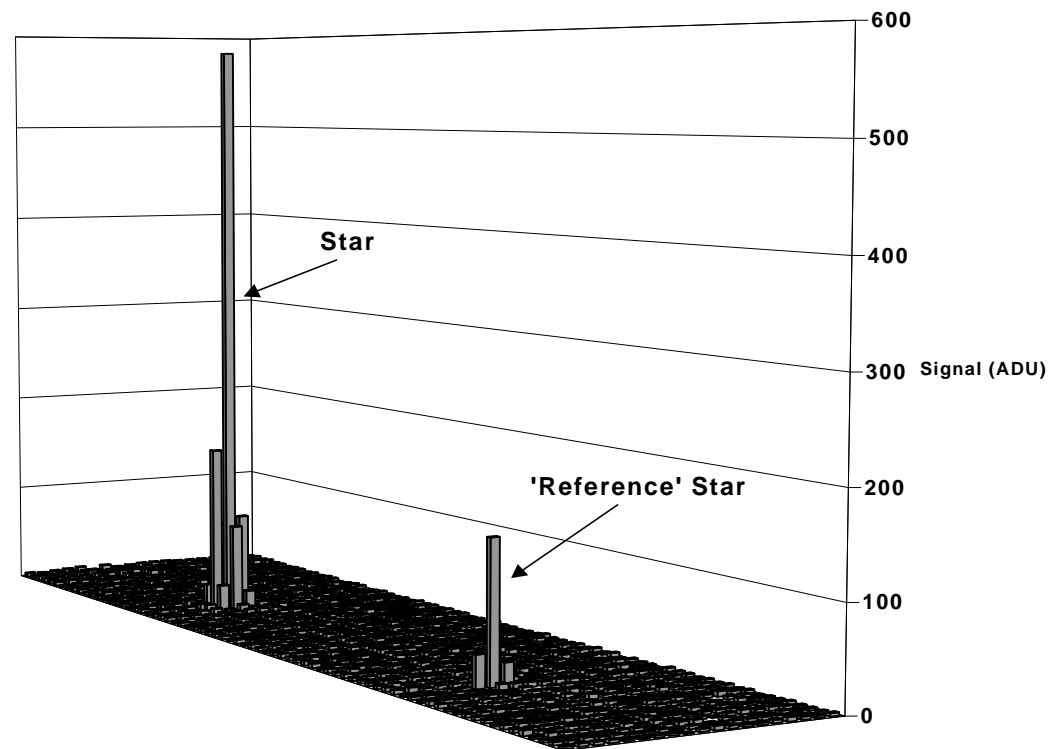
# Effects on Image: Prediction / Simulation

- **Can go from first principles (trap concentration and charge density model)**
  - good but time consuming
- **Sira C code model**
  - signal & background CTI dependence (empirical)
  - tracks emission & capture but effect of trap filling by preceding packets may not be entirely correct
  - can input real star and pixel profiles
- **Sira Excel<sup>TM</sup> model**
  - only slow line moves are important
  - constant (background dependent) CTI - no signal size dependence
  - Gaussian star profile (at present)
- **But why not measure errors directly ?**

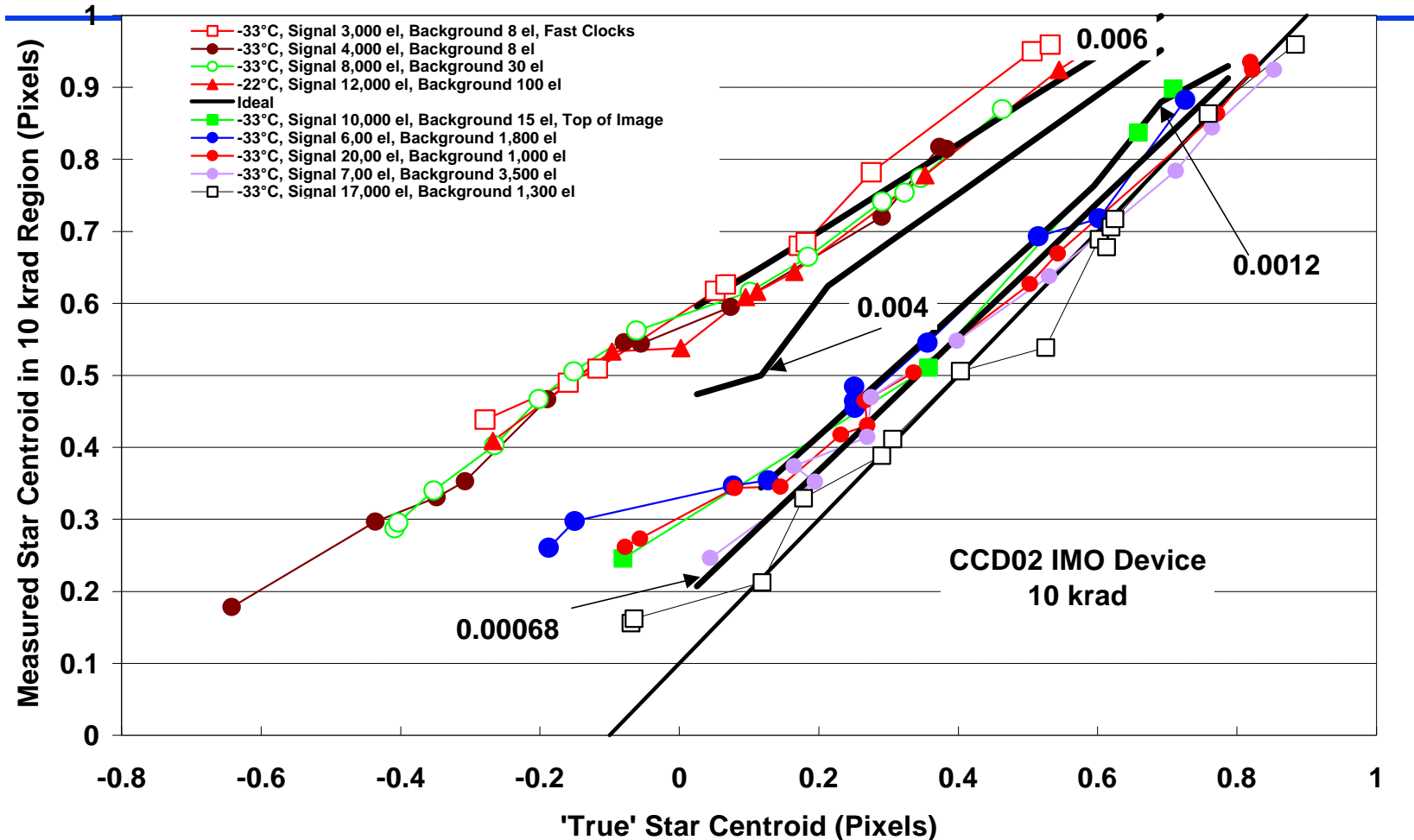
# Artificial Star Data

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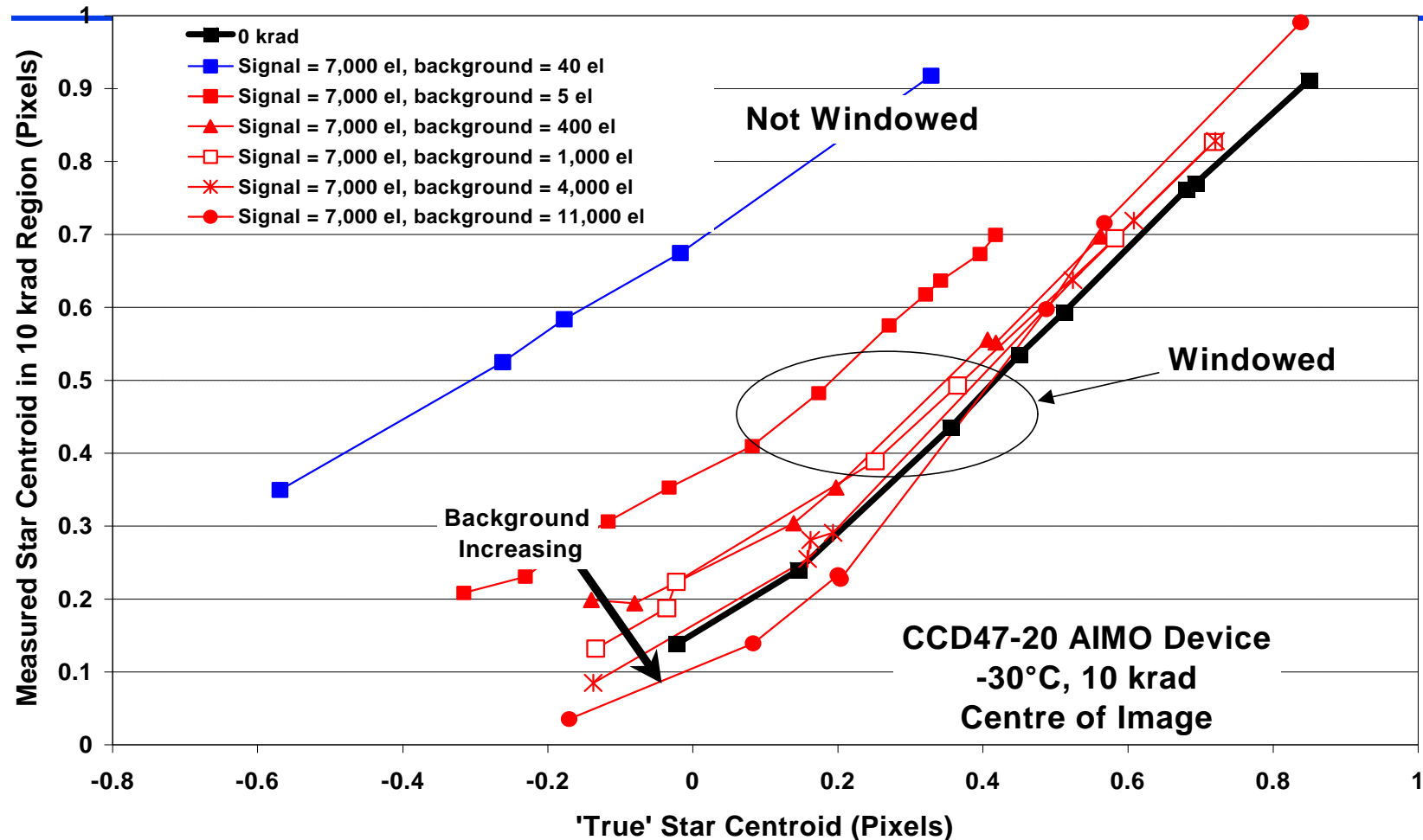
## Double Pinhole Illumination System



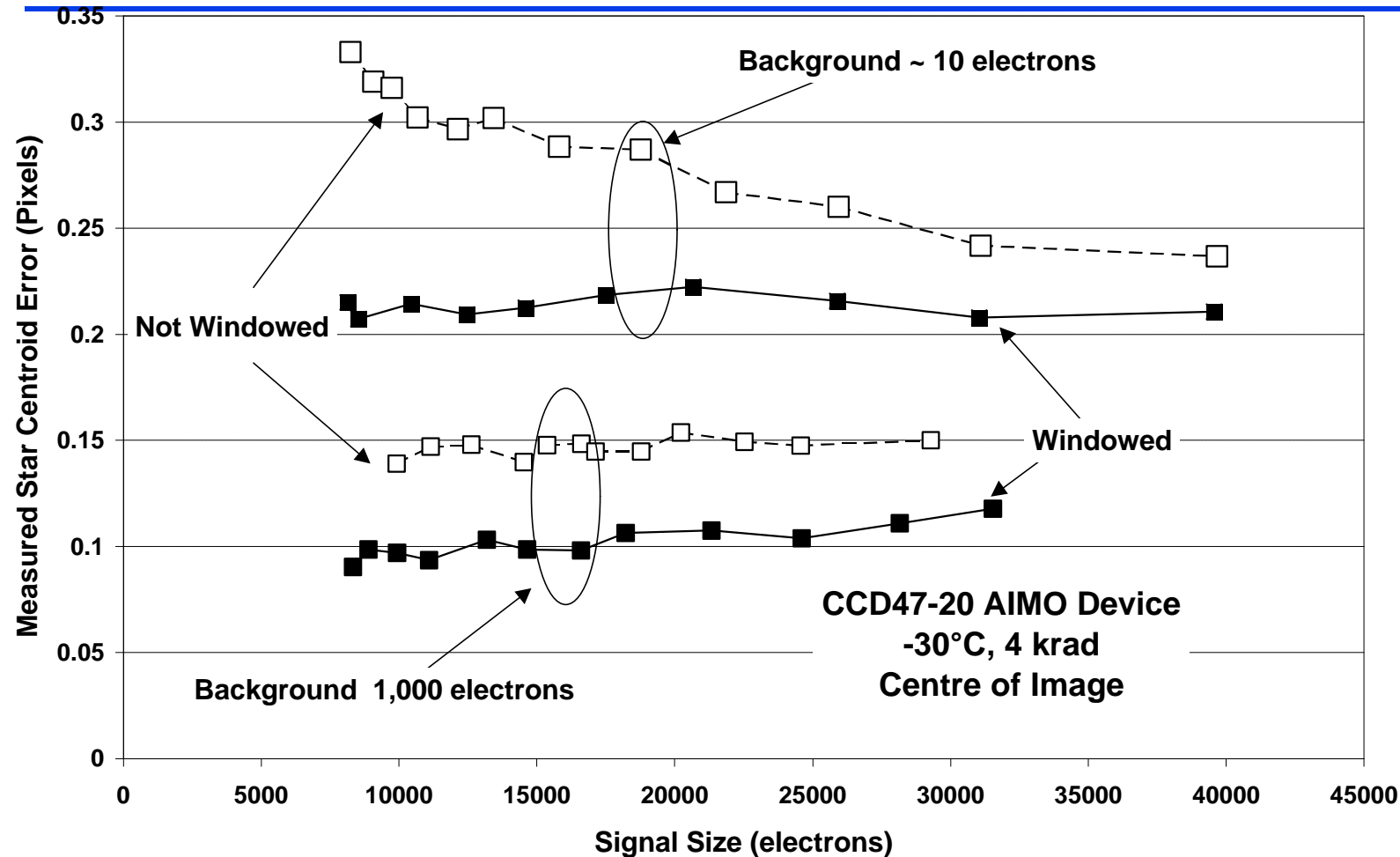
# Star Centroid Data: CCD02



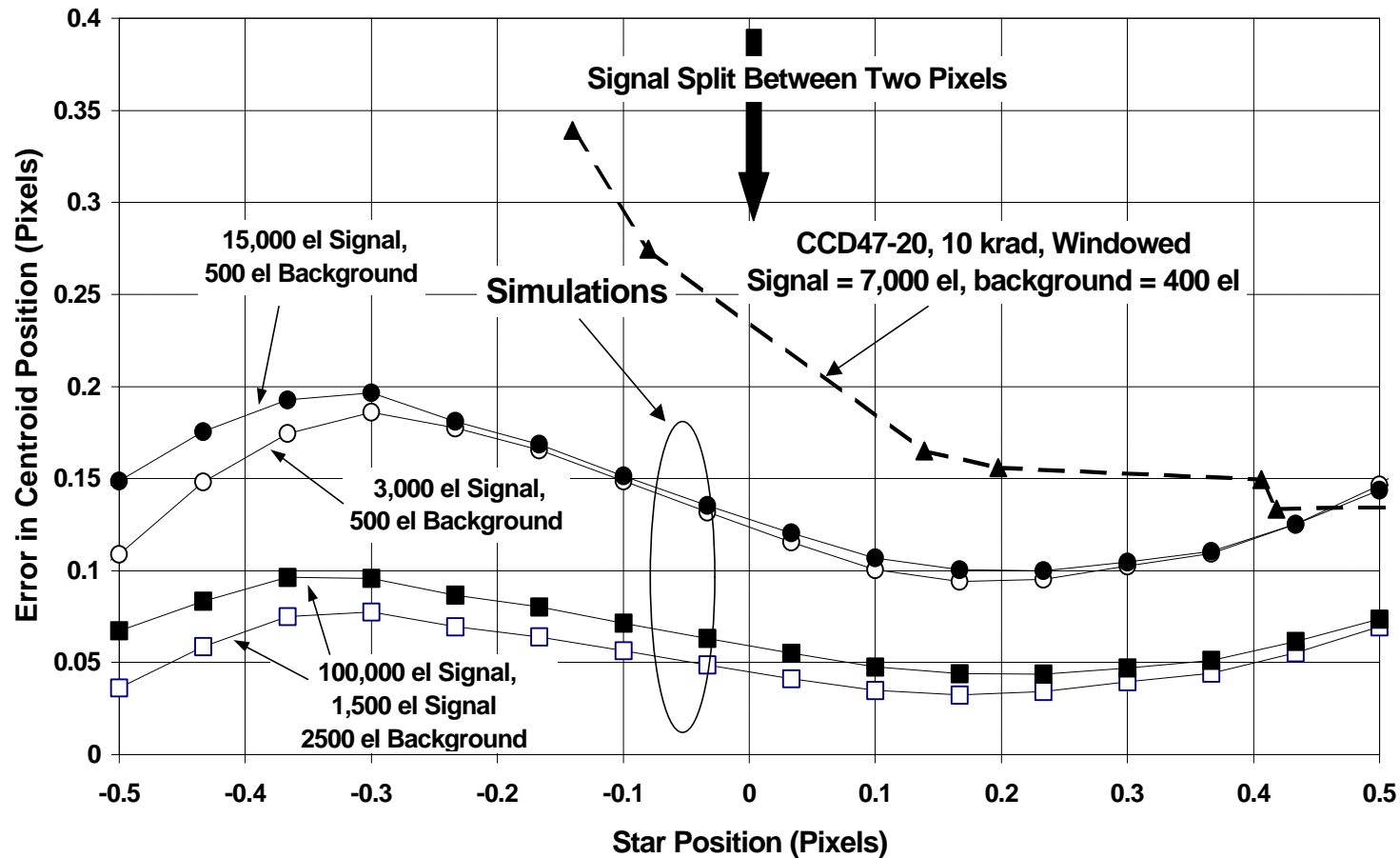
# Star Centroid Data: CCD47-20



# Star Centroid Data: CCD47-20



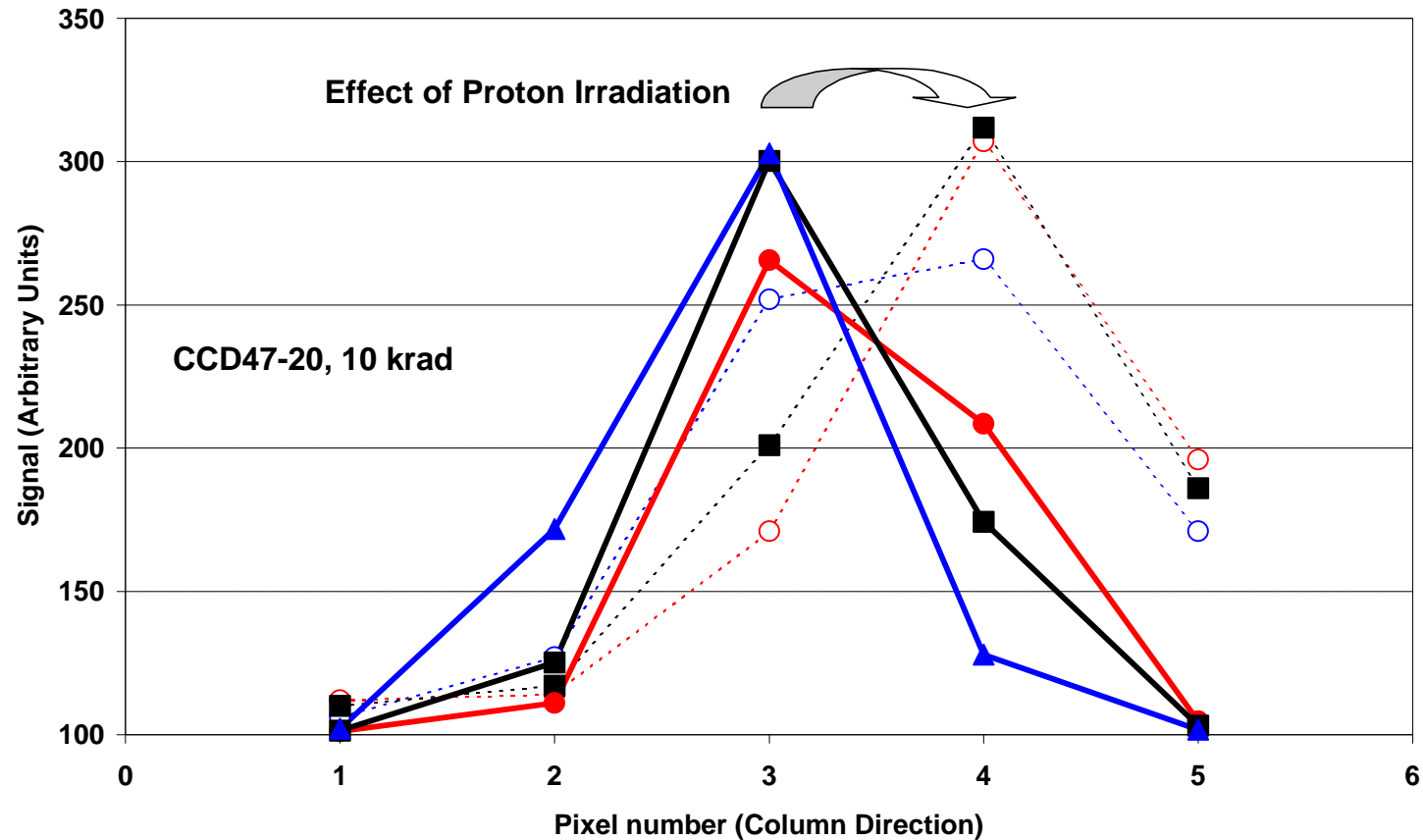
# C code Simulation





# Typical 'Star' Profiles

## Dotted Lines: After Irradiation



# Star Centroid Data: Conclusions

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- Large errors for low backgrounds, even for low irradiation levels.
- Background ('fat zero') has a large effect. To improve accuracy (better than changing star brightnesses or temperature) increase background level (to  $> 1000$  electrons/pixel for  $> 4$  krad(Si) environments).
- The centroid shifts do not change much with location within a pixel but worst when star on the boundary between pixels.
- For the same signal and background, the error tends to be worse as the temperature is increased (from  $-32^{\circ}\text{C}$  to  $-22^{\circ}\text{C}$ ). This is because the diffused charge is spread over fewer pixels at the higher temperature and tends to distort the star profile more.
- Increasing line move times did not have a large effect
- Centroid error at top of image (& for windowed readout) is significant ( $\sim 0.1$  pixels at low backgrounds: likely due to signal dependence of CTI for fast line moves, also contribution from emission from any fast traps).

# Overall Conclusions

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- **AD9223 and LTC1415 should be OK for most low dose mission if AD9223 SEL can be accepted**
- **ASCoSS radiation tolerance better than previously thought (dark current anneals, dark spikes not large) but unexplained responsivity change, ADC shows SEL**
  - new version will have a different pixel structure and new ADC
- **Displacement damage induced CTI in n-channel CCDs studied in detail using FPR method for first time**
- **Double aperture method for star centroid measurement has proved to be simple and reliable**
- **centroid errors can be large for individual stars - but overall error will be reduced by application of star tracker algorithms ('real-sky' testing is in progress)**

# Further Issues

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- **Continue tests on state-of-the art ADCs**
  - performance degradation for imaging systems most important
- **Test new version(s) of ASCoSS chip and test structures**
- **Test CTI for new CCDs (to understand dependences)**
- **Use double aperture for routine testing (establish a new figure of merit for imaging systems ?)**