STUDY OF RADIATION EFFECTS IN CRYOGENIC ELECTRONICS

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- **INTRODUCTION**

  Structure of the Project (ESTEC Contract No 11938/96/NL/LB)

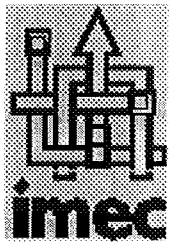
- **STUDY OF RADIATION EFFECTS IN CRYOGENIC ELECTRONICS**

  LITERATURE STUDY : Deliverable D1, Document No P35284-IM-RP-0003 (30 October 1997)

  "Literature Study on Radiation Effects in Cryogenic Electronics"

  EXPERIMENTAL

  - ⇒ **Device Fabrication**
  - ⇒ **Irradiation and Testing Conditions**



RESULTS

⇒ **Pre-Irradiation Characteristics at 4.2 K**

⇒ **Post-Irradiation Characteristics at 4.2 K**

⇒ **Conclusions from the Radiation Testing**

Deliverable D2, Document No P35284-IM-RP-0012, 25 February 1999

"Radiation Testing of Cryogenic Devices and Circuits"

☛ **GUIDELINES FOR CRYOGENIC ELECTRONICS DEVELOPMENT, DESIGN AND TESTING**

Deliverable D3, Document No P35284-IM-RP-0017, 23 September 1999

"Manual for Cryogenic Electronics in Space Applications"

☛ **GENERAL CONCLUSIONS AND OUTLOOK (PART II)**

Project Structure

ACTIVITY I

STUDY OF RADIATION EFFECTS IN CRYOGENIC ELECTRONICS

- ⇒ **Literature Overview (D1)**
- ⇒ **Radiation Testing of Parts Developed for ESA's FIRST Mission**
- ⇒ **Guidelines for the Development of Cryogenic Space Electronics**

☛ ACTIVITY II

STUDY OF RADIATION EFFECTS IN ADVANCED SEMICONDUCTOR MATERIALS AND DEVICES

⇒ **Literature Overview (D4)**

⇒ **Radiation Testing**

⇒ **Final Report**

Irradiation Effects on Cryogenic Electronics

- **Cryogenic Electronics**

  Performance Improvement

- **Space Applications**

  Low Power
  Availability Cooling Systems
  Irradiation Effects = f(orbit)

- **FIRST Mission**

⇒ **Cryogenic Read-out Electronics (4.2 K)**

AIM

STUDY OF THE IMPACT OF TOTAL DOSE AND PROTON IRRADIATION EFFECTS ON THE ELECTRICAL PERFORMANCE OF CRYOGENIC ELECTRONICS TO BE USED FOR THE FIRST MISSION

Device Processing

Submicron MOSFETs in a 0. 7 μm Technology

Gate Oxide Thickness : 16 nm

W = 10 μm (rectangular) & L=5 μm

Processing Splits :

- **Threshold Voltage Adjust Implant**
- **P-well**
- **Lowly Doped Drain (LDD) Architecture**

Irradiation Conditions

Cyclone facility (Louvain-La-Neuve, Belgium)

60 MeV Protons: Φ between $3x10^{10}$ and 10^{12} cm^{-2}

^{60}Co gamma irradiations (5 krad/hour) – 50 & 100 krad

Bias : V_{gs} = 5 V (n) and 0 V (p), other terminals grounded

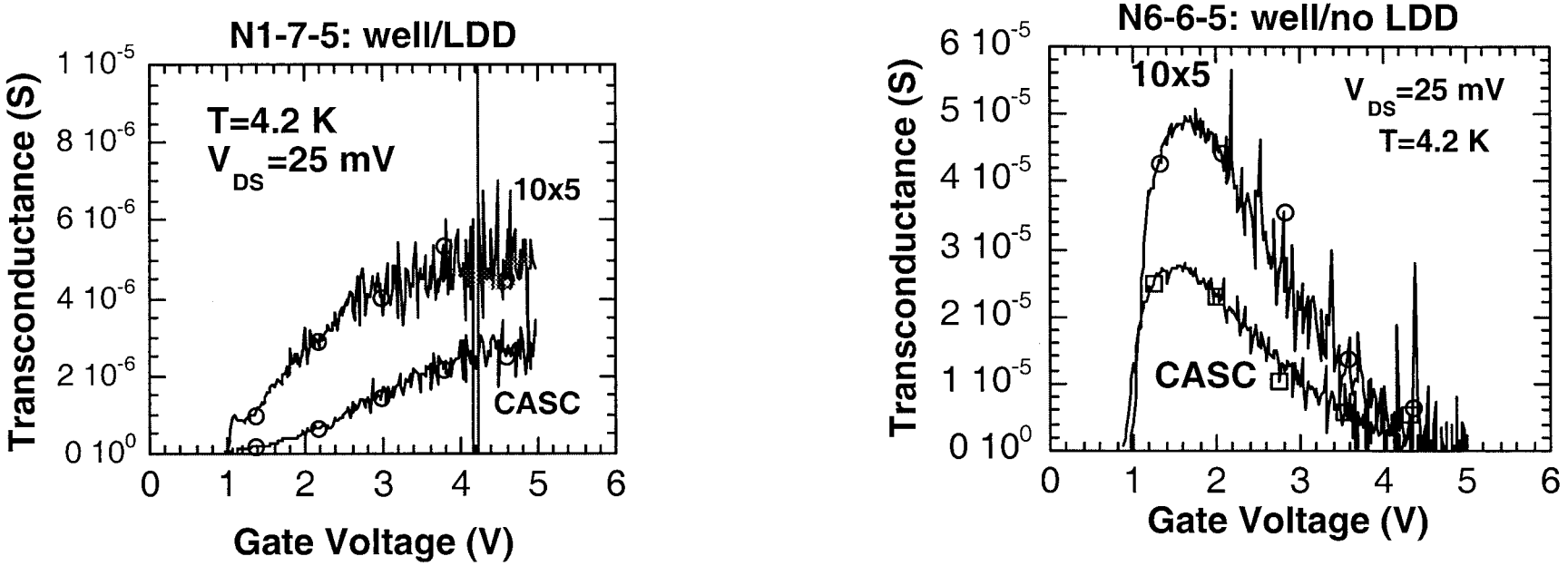
Testing Conditions

Linear Operation (small drain bias)

Saturation $\Rightarrow$ Kink Effect

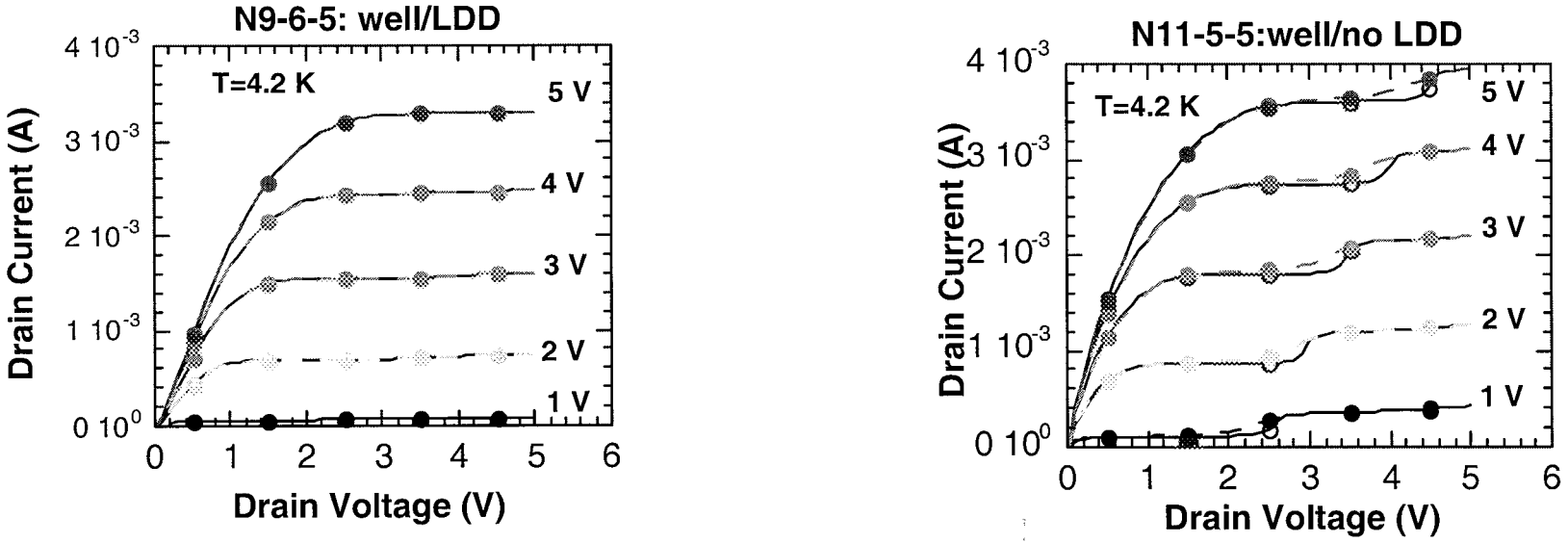
4.2 K Testing on Dual-In-Line Packages

Impact LDD on Transconductance g_m



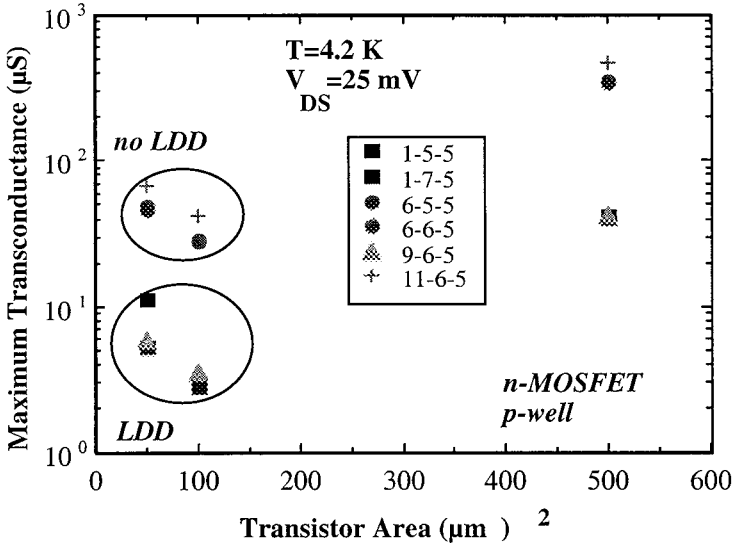
Transconductance at 4.2 K and V_{ds}=25 mV for different geometry n-MOSFETs with (left) and without (right) LDDs, before irradiation.

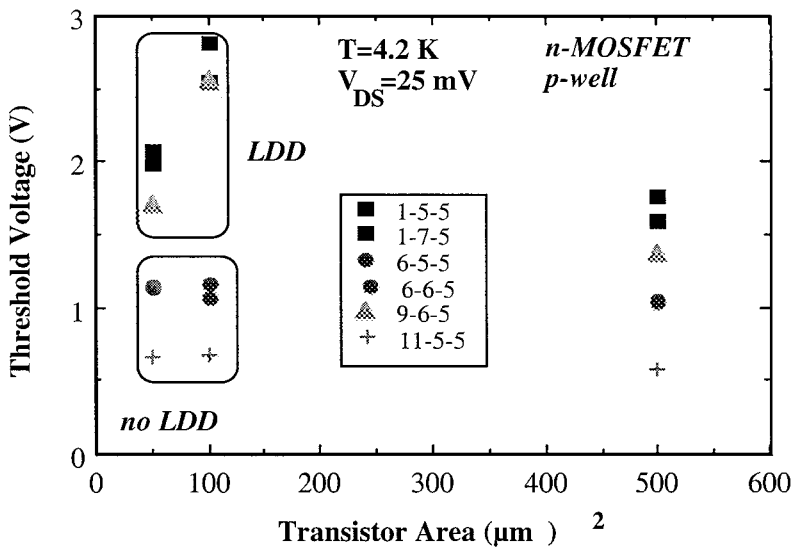
Impact LDD on Kink g_m



I_d – V_{ds} at 4.2 K and V_{ds}=25 mV for different geometry n-MOSFETs with (left) and without (right) LDDs, before irradiation.

Impact LDD on g_m and Threshold Voltage V_T





Transconductance and threshold voltage at 4.2 K for the different splits studied before irradiation.

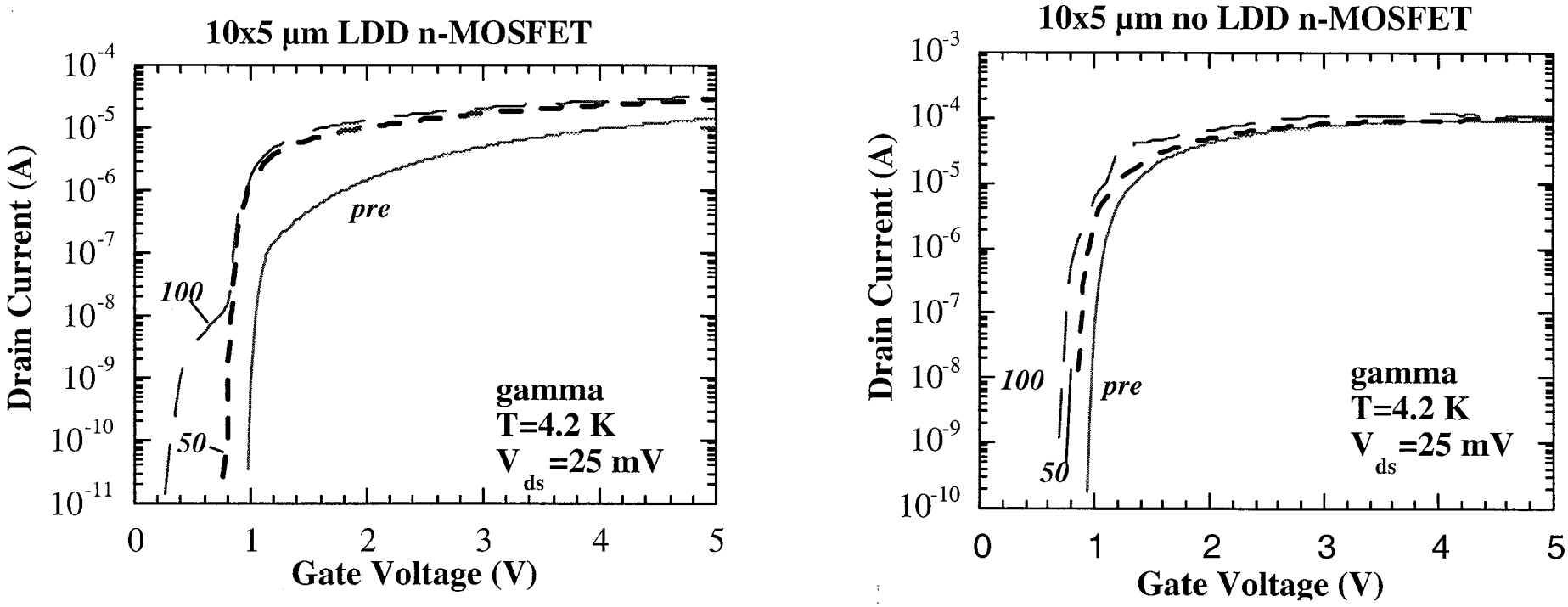
Conclusions

- **Splits with LDD show poor ohmic characteristics for low drain bias due to the high parasitic series resistance at 4.2 K.**

- **The LDD architecture is useful in reducing the drain current kink effect in saturation, for the n-channel devices.**

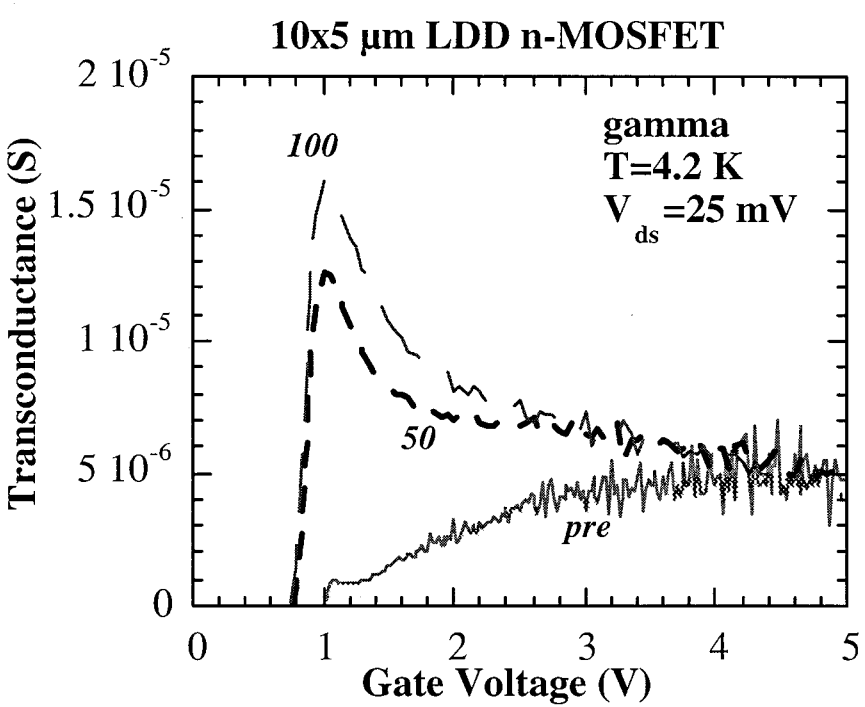
- **Overall, the standard 0.7 μm CMOS technology without LDDs yields the best cryogenic performance.**

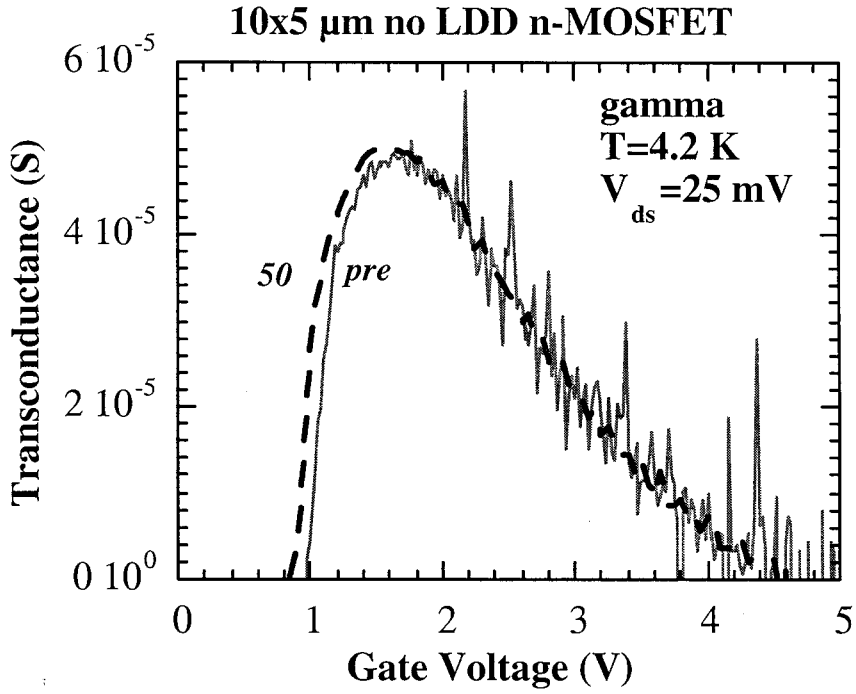
Linear Operation: I_d-V_{gs} n-MOSTs



Input curves at 4.2 K and V_{ds}=25 mV for a 10x5 µm n-MOSFET with (left) and without (right) LDDs, corresponding to unirradiated (pre) and irradiated samples (total dose).

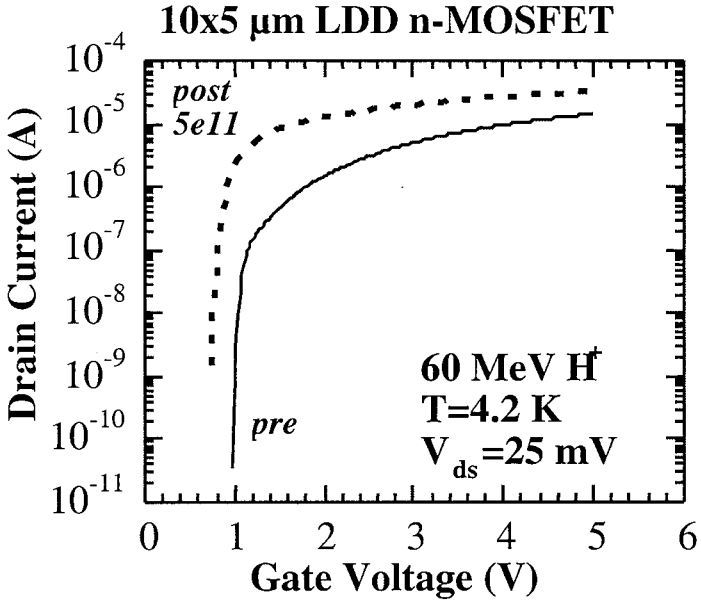
Linear Operation: Transconductance n-MOSTs

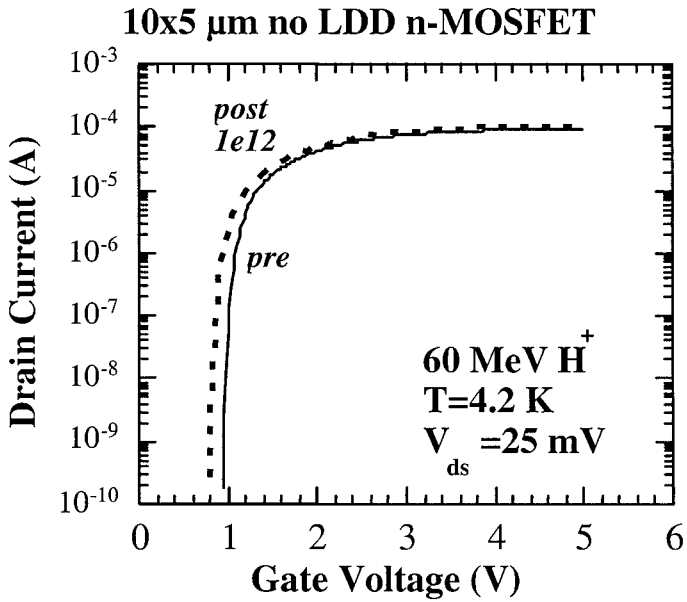




Transconductance at 4.2 K and V_{ds}=25 mV for a 10x5 µm n-MOSFET with (left) or without (right) LDDs, corresponding to unirradiated (pre) and irradiated samples (total dose).

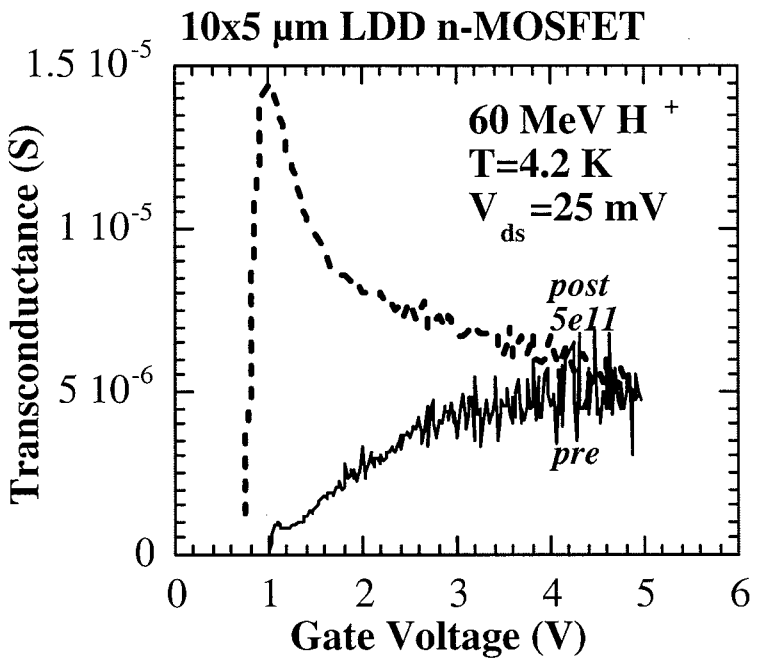
Linear Operation: I_d-V_{gs} n-MOSTs

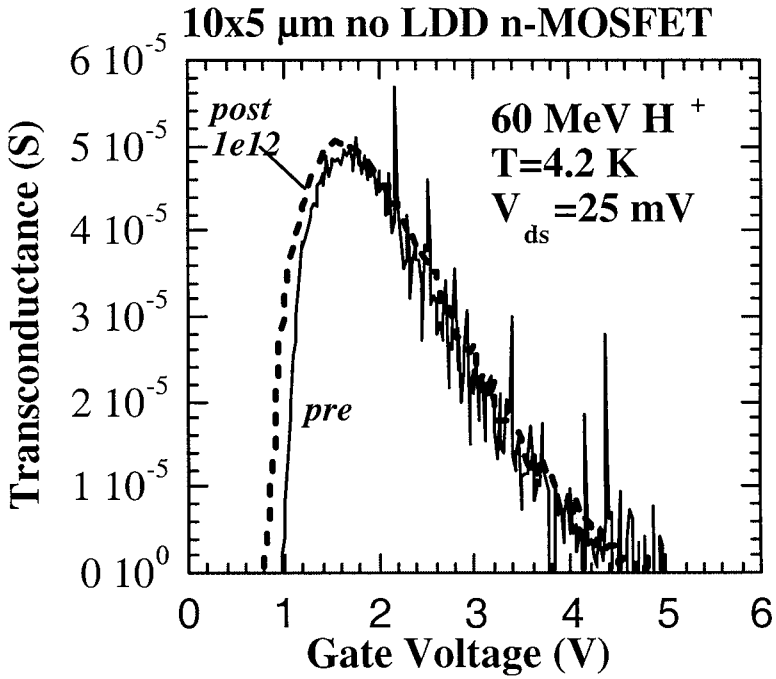




Input curves at 4.2 K and V_{ds}=25 mV for a 10x5 µm n-MOSFET with (left) or without (right) LDDs, corresponding to unirradiated (pre) and proton irradiated samples.

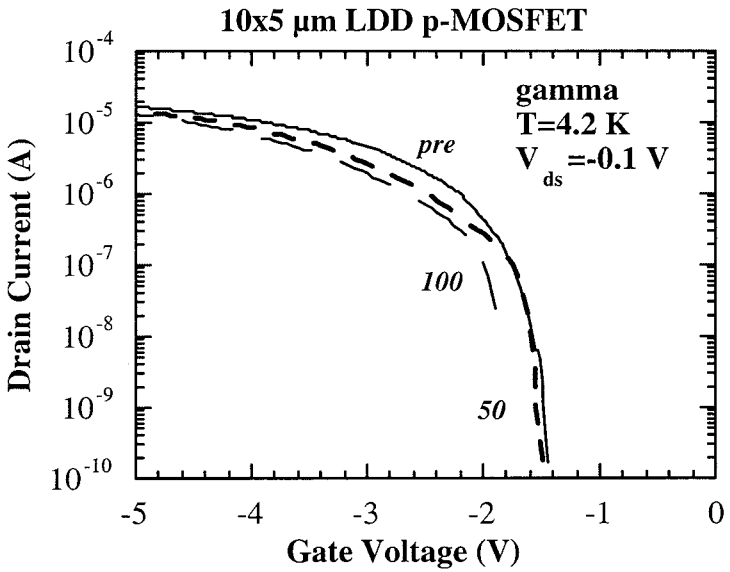
Linear Operation: Transconductance n-MOSTs

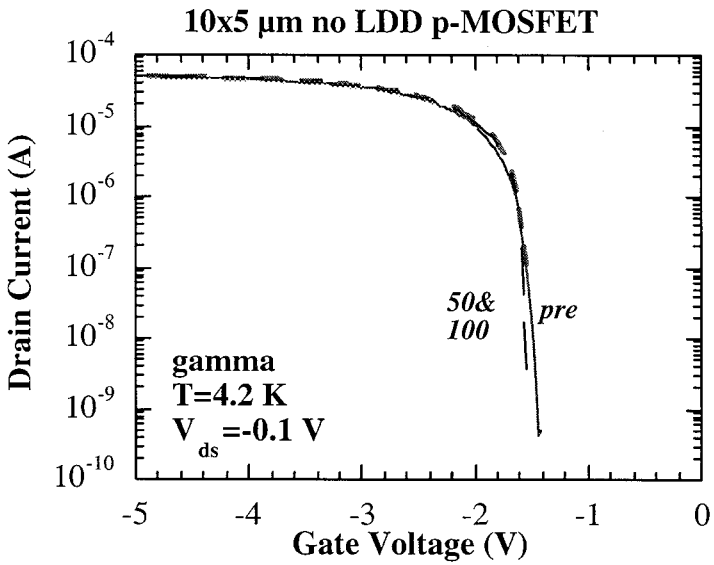




Transconductance at 4.2 K and V_{ds}=25 mV for a 10x5 µm n-MOSFET with (left) or without (right) LDDs, corresponding to unirradiated (pre) and proton irradiated samples

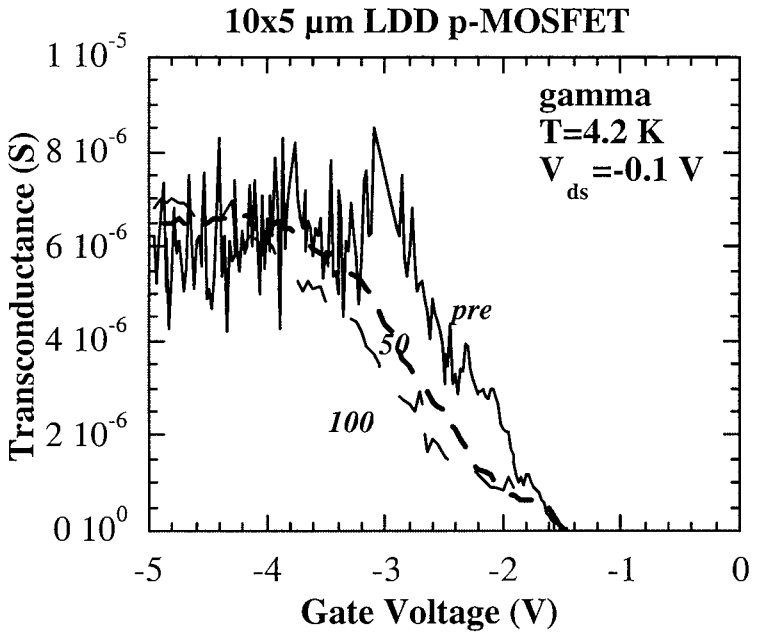
Linear Operation: I_d-V_{gs} p-MOSTs

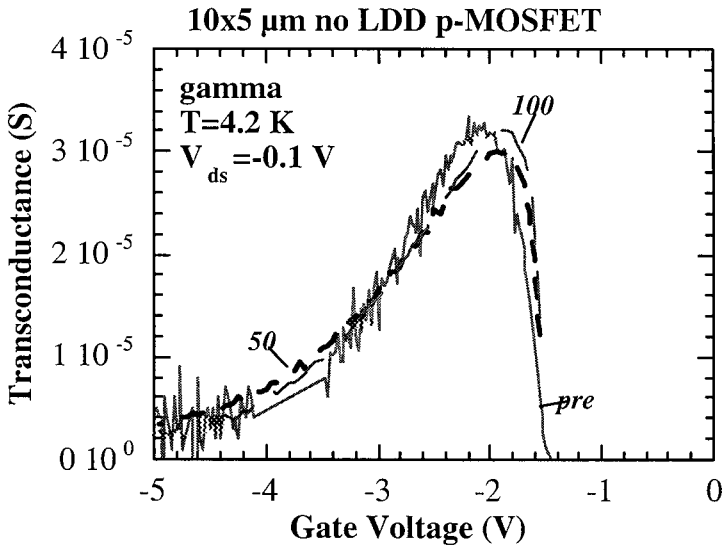




Input curves at 4.2 K and V_{ds}=-0.1 mV for a 10x5 µm p-MOSFET with (left) or without (right) LDDs, corresponding to unirradiated (pre) and irradiated samples (total dose).

Linear Operation: Transconductance p-MOSTs





Transconductance at 4.2 K and V_{ds}=-0.1 mV for a 10x5 µm p-MOSFET with (left) or without (right) LDDs, corresponding to unirradiated (pre) and irradiated samples (total dose).

Linear Operation : Summary

- **After irradiation the threshold voltage of the nMOSTs reduces slightly, while it increases in absolute value for the pMOSTs.**

  ⇒ Positive charge trapping in gate oxide

  ⇒ For non LDD devices a 6 to 20x lower influence

  ⇒ More complex behaviour for the pMOSTs

  ⇒ Rebound behaviour not well understood

Linear Operation : Summary

- **Quantitative Similar Behaviour for the Transconductance**

  ⇒ Slight increase nMOS and slight reduction pMOS

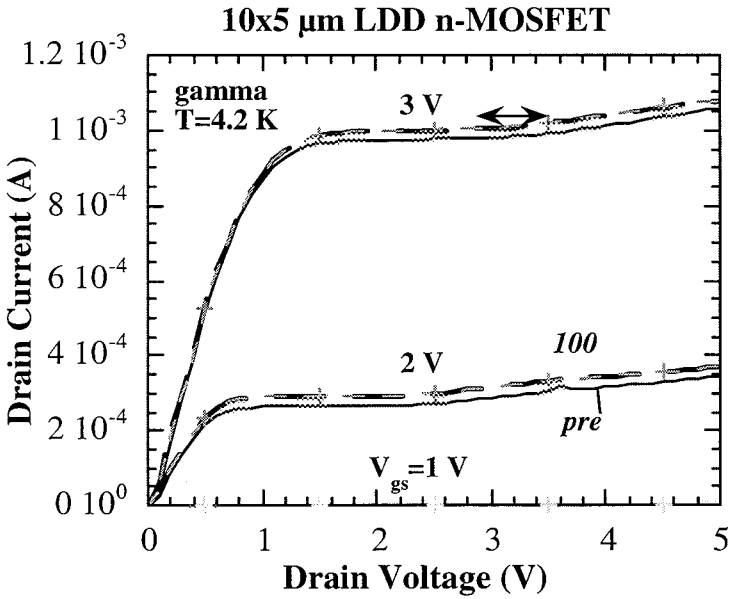
  ⇒ For proton irradiation of non-LDD Devices: Rebound

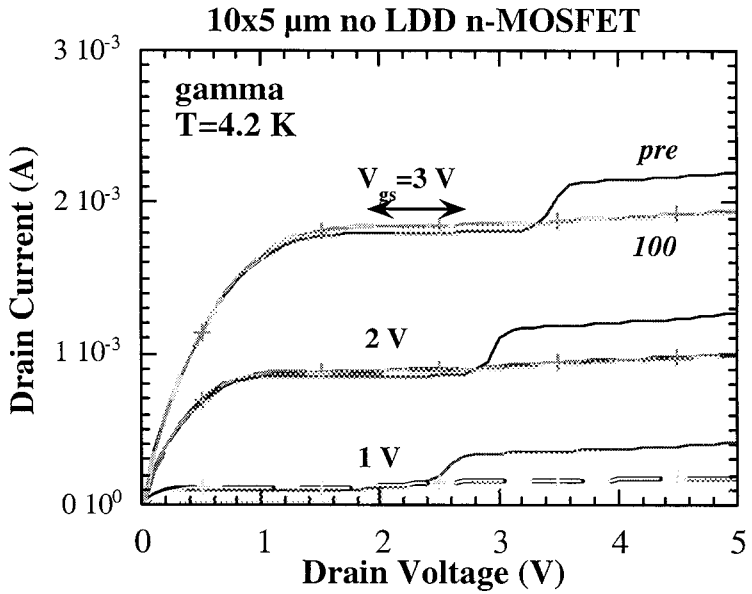
  ⇒ Typical behaviour before irradiation: Gate-Source overlap

  ⇒ After exposures of LDD transistor more regular behaviour

Non-LDD Devices are Preferred for LTE Operation, both before and after irradiation

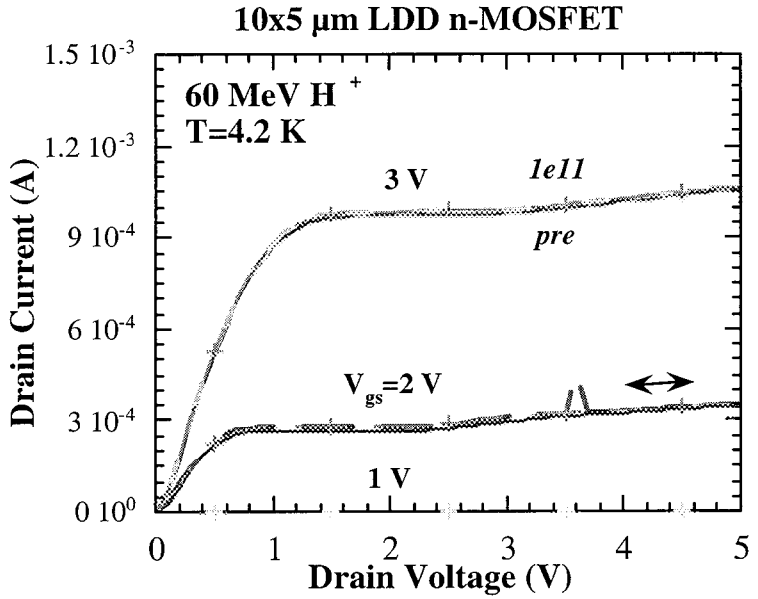
Saturation: I_d-V_{ds} n-MOSTs

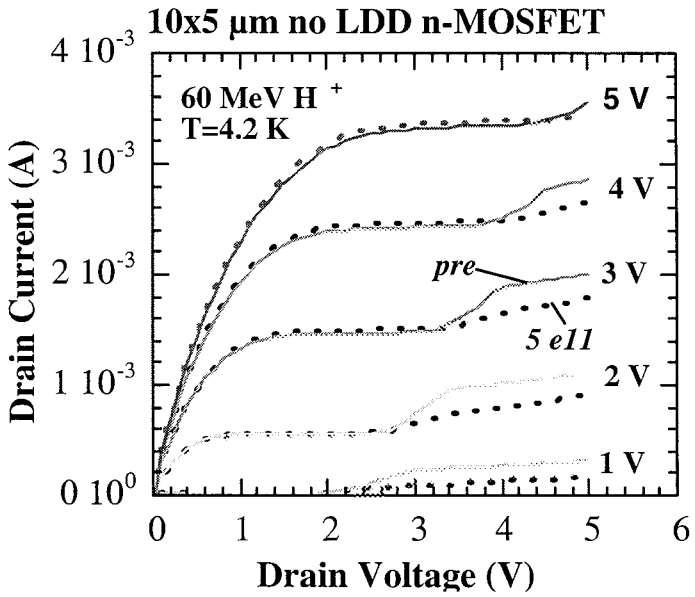




Output curves at 4.2 K and V_{gs}= 1,2 or 3 V for a 10x5 µm n-MOSFET with (left) and without (right) LDDs, corresponding to unirradiated (pre) and 100 krad(Si) (dashes: low-to-high; + high-to-low). No hysteresis is seen, as indicated by the arrow in the upper characteristic.

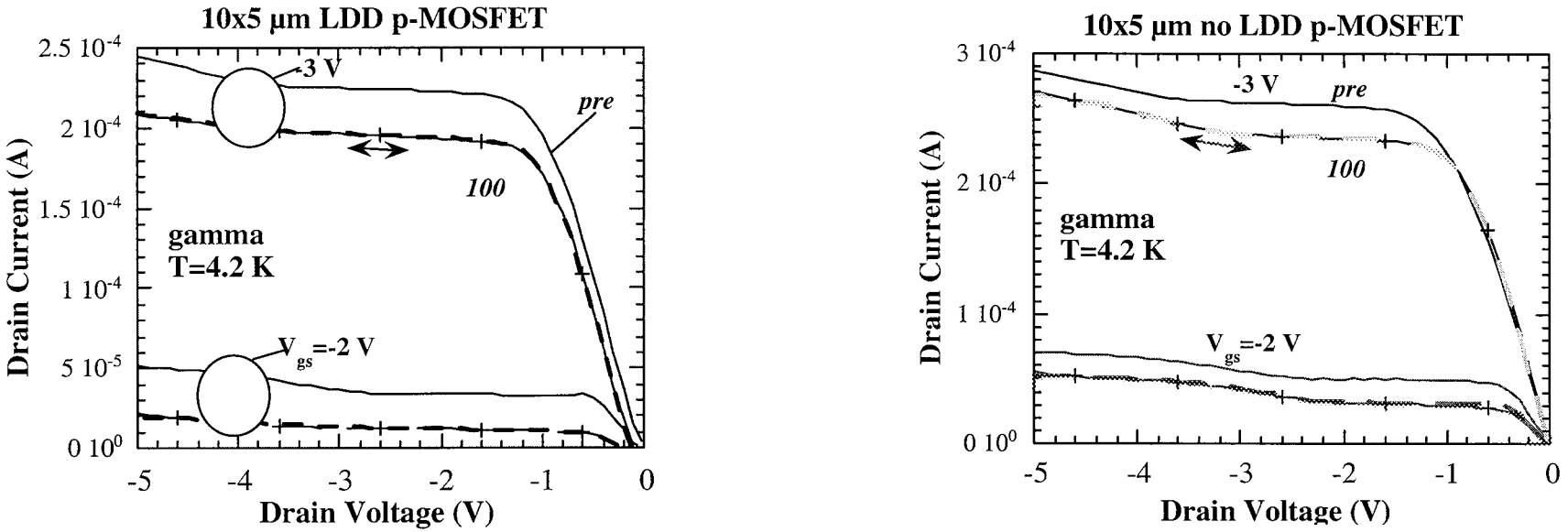
Saturation: I_d-V_{ds} n-MOSTs





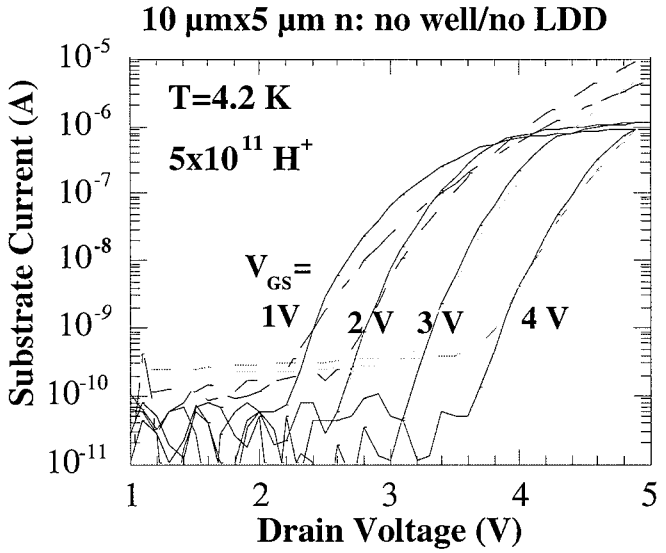
Output curves at 4.2 K and V_{gs}= 1,2 or 3 V for a 10x5 µm n-MOSFET with (left) and without (right) LDDs, corresponding to unirradiated (pre) and 60 MeV proton irradiated (dashes: low-to-high; + high-to-low). No hysteresis is seen, as indicated by the arrow in the upper characteristic.

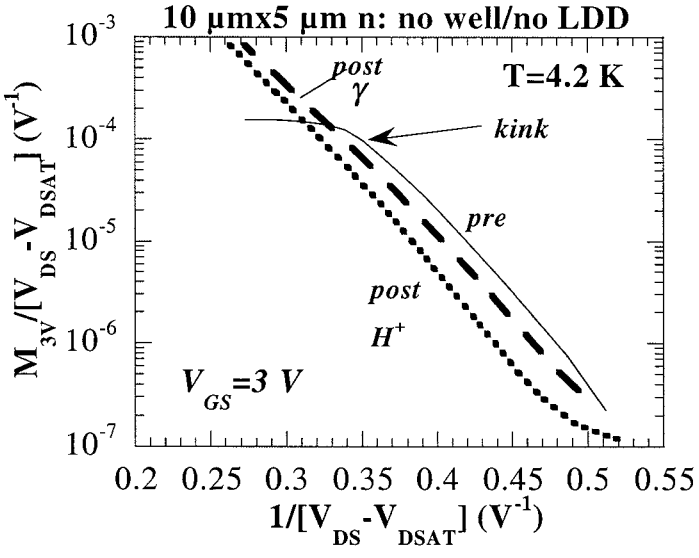
Saturation: I_d-V_{ds} p-MOSTs



Output curves at 4.2 K and V_{gs}= -2 or -3 V for a 10x5 µm p-MOSFET with (left) and without (right) LDDs, corresponding to unirradiated (pre) and 100 krad(Si) (dashes: low-to-high; + high-to-low). No hysteresis is seen, as indicated by the arrow in the upper characteristic.

Substrate Current and Multiplication Coefficient





Substrate current (left) and normalised multiplication coefficient (right) for an irradiated 10 µmx5 µm non-LDD n-MOSFET at 4.2 K.

- The used technology is sufficient radiation hard for the FIRST mission
- Better radiation tolerance for non-LDD Devices
- Some special low-temperature phenomena require further fundamental studies.

Guidelines for Cryogenic Electronics Development, Design and Testing

- From the literature search and the radiation testing, some simple rules of thumb can be formulated to optimise cryogenic operation on the one hand and radiation hardening on the other.

- In many cases, no LDD architectures are required to achieve good performance. It is, therefore, advised that for most analog or mixed applications, LDD-less technology is recommended.

- Hardening can be best achieved by design modifications like guard-rings. The kink effect can be suppressed by applying a cascode structure. This goes, of course, at the expense of the packing density.

- Radiation testing should preferably be performed at the operation temperature, to rule out annealing and 'ordering' effects. It can be stated, however, that as far as bulk displacement damage is concerned (i.e. following proton exposures), room temperature provides the worst-case scenario.

- Finally, the good news is that the radiation hardness increases upon further technology scaling

In spite of the downscaling trend, the introduction of alternative materials and advanced process modules raises again some concerns with respect to radiation hardening. Therefore, in Activity II, focus will be on:

- ⇒ The study of the impact of Shallow Trench Isolation (STI) on the radiation hardness of p-n diodes.
- ⇒ The impact of alternative gate dielectrics (NO,...)
- ⇒ The impact of scaling: components processed in a 0.18 μm CMOS technology

Accepted

"Proton Radiation Hardness of MOS Transistors at Cryogenic Temperatures"

E. Simoen, C. Claeys and A. Mohammadzadeh,

Presented at the General Scientific Meeting of the Belgian Physics Society, VUB, Brussels, May 20-21, 1999.

"Comparison of the Total-Dose and 60 MeV Proton-Irradiation Response of CMOS Transistors Operated at 4.2 K"

E. Simoen, C. Claeys and A. Mohammadzadeh,

Paper to be published in the Proc. of RADECS 1999, Abbaye de Fontevraud (France), Sept. 13-17, 1999.

"Impact of 60 MeV Proton Irradiation on the 4.2 K Characteristics of 0.7 μm CMOS Transistors"

E. Simoen, C. Claeys and A. Mohammadzadeh,

Presented at the Symposium on Low Temperature Electronics, The Electrochem. Society Fall Meeting, Honolulu, Hawaii, October 17-22, 1999.

Submitted

"Impact of ionising irradiation on the drain current kink of cryogenic n-MOSFETs at 4.2 K"

E. Simoen, C. Claeys and A. Mohammadzadeh,

Paper submitted to IEEE Electron Device Letters.

"Substrate Current and Kink Analysis of MOSFETs at Liquid Helium Temperatures"

E. Simoen, C. Claeys and A. Mohammadzadeh,

Paper submitted for presentation at the 4th European Workshop on Low Temperature Electronics WOLTE 4, ESA-ESTEC, Noordwijk, The Netherlands, 21-23 June, 2000.

"Guidelines for Cryogenic Spaceborn CMOS Testing and Optimisation"

C. Claeys, E. Simoen and A. Mohammadzadeh,

Paper submitted for presentation at the 4th European Workshop on Low Temperature Electronics WOLTE 4, ESA-ESTEC, Noordwijk, The Netherlands, 21-23 June, 2000.